An External Capacitor-less Low-Dropout Voltage Regulator using a Transconductance Amplifier

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***Abstract*—This paper presents an external capacitor-less NMOS low-dropout (LDO) voltage regulator integrated with a standard CSMC 0.6 μm BiCMOS technology. Over a $-55\,^{\circ}\mathrm{C}$ to $+125\,^{\circ}\mathrm{C}$ temperature range, the fabricated LDO provides a stable and considerable amount of 3 A output current over wide ranges of output capacitance $\mathrm{C_{OUT}}$ (from zero to hundreds of μF) and effective-series-resistance (ESR) (from tens of milliohms to several ohms). A low dropout voltage of 200 mV has been realised by accurate modelling. Operating with an input voltage ranging from 2.2 V to 5.5 V provides a scalable output voltage from 0.8 V to 3.6 V. When the load current jumps from 100 mA to 3 A within 3 μs, the output voltage overshoot remains as low as 50 mV without output capacitance, $\mathrm{C_{OUT}}$. The system bandwidth is about 2 MHz, and hardly changes with load altering to ensure system stability. To improve the load transient response and driving capacity of the NMOS power transistor, a buffer with high input impedance and low output impedance is applied between the transconductance amplifier and the NMOS power transistor. The total area of fabricated LDO voltage regulator chip including pads is 2.1 mm$\times$2.2 mm.**

***Index Terms*—Fast-Transient, Low-Dropout (LDO), Output-Capacitor-Free, Line/Load Regulation, Power Management**

I. Introduction

IN recent years, battery-powered electric and electronic devices such as energy-efficient cellular phones and other palm-size portable computer benefitted the rapid development of the semiconductor technology. Power management is necessary for a variety of analog and mixed-signal electronic devices for reducing the standby power and maximising the battery run-time [1], [2]. Low-dropout (LDO) regulators are one of the essential components in power management modules supporting widely distributed voltage domains, for noise-sensitive analog/RF circuits, and energy-efficient internet-of-things device applications [3]. Furthermore, as the final blocks in certain power suppliers, low undershoot and overshoot are always required.

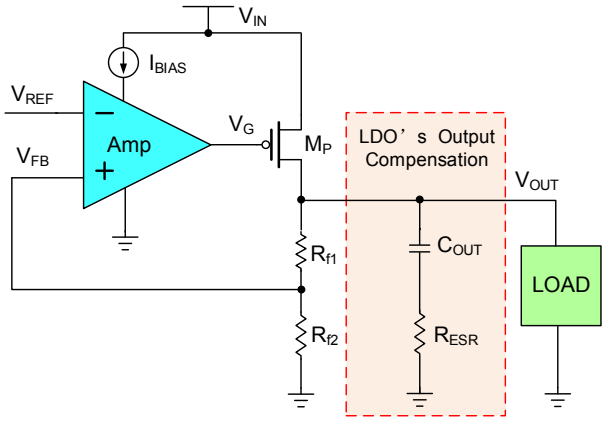

Fig. 1. Conventional topology of the analog-LDO.

Recently, the most adopted types of LDOs are the digital-LDO and the analog-LDO. The typical digital-LDO regulator in [4] uses an analog loop to set the output voltage. Digital-LDOs use a digital controller to minimise analog compensation. An analog-to-digital converter serves to switch on and off transistors making a digital-to-analog converter, which increases the circuit complexity and reduces efficiency [5]. The finite resolution introduces the quantisation noise.

Fig. 1 shows a typical analog-LDO regulator. It is a second-order system with a high gain error amplifier and an output PMOS transistor $\mathrm{M_P}$. Resistors $\mathrm{R_{f1}}$ and $\mathrm{R_{f2}}$ constituting a voltage divider that scales $\mathrm{V_{OUT}}$, compares it against the reference voltage $\mathrm{V_{REF}}$, and amplifies the error. When $\mathrm{V_{OUT}}$ deviates from the desired value, the error amplifier drives in feedback the power transistor and brings the output voltage to the proper value.

In general, the circuit uses an external large output capacitor $\mathrm{C_{OUT}}$ and its equivalent series resistance $\mathrm{R_{ESR}}$ to suppress the output voltage undershoot and overshoot of the LDO regulator under rapid and substantial load transient changes as the capacitor can supply instantaneous current required by the load transient. Nowadays, the development of man-

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ufacturing processes of electronic components makes the size and cost of ceramic capacitors significantly lower than before. Therefore, the use of ceramic capacitors is an optimal choice for today's LDO applications. However, because of the low ESR characteristics of ceramic capacitors, it is not easy to compensate for the secondary pole which always leads to the unstable phenomena [6]. Also, C_{OUT} affects the response time. This work proposes a solution for NMOS LDO where a load capacitance is not necessary for stability. The use of the NMOS power transistor also reduces the area compared to the PMOS power transistor scheme.

There are many proposed state-of-the-art LDO topologies , which feature capless [7], [8], fast transient [9]–[11], and so on. However, most of the researches do not consider ultra-large output currents, the package and a broad range of temperature operation. The LDO chip in this work is required to supply up to several amperes of load current at a very stable operation over a wide range of temperature. Additionally, the LDO must be simple enough for easy design verifications.

The LDO circuit target of this work must be able to provide a 3 A maximum output current with 200 mV of low dropout voltage. The transient response under abrupt changes of the large output current is an issue. The proposed solution uses a feedback network which senses transient changes in output voltage V_{OUT}. The bias current is able to react quickly to a change in the output voltage V_{OUT}, so that the LDO has stable operation and high phase margin (about 50 degrees in the worst case). This feature holds for wide ranges of output capacitance and ESR. For instance, when the load current jumps from 100 mA to 3 A within 3 μs, the output voltage overshoot remains as low as about 50 mV without output capacitance C_{OUT}. Also, the LDO can operate over a wide temperature range from $-55\,^{\circ}\mathrm{C}$ to $+125\,^{\circ}\mathrm{C}$.

The organisation of the paper is as follows: Section II and Section III describe the system overview, the circuit design and the main features of the LDO. Section IV discusses measurement results, and Section V concludes this paper.

II. System Overview

The system block diagram in this work is shown in Fig. 2. The V_{IN} terminal is an input of the LDO, input voltage range lies between 1.1 V and 5.5 V, the V_{OUT} terminal provides an adjustable output voltage for the load from 0.8 V to 3.6 V. Soft-Start (SS) provides a linear startup for the LDO chip and the monotonic soft-start is well-suited for powering a variety of different types of processors and specific integrated circuits. The user-programmable soft-start can effectively reduce the inrush current during startup, thus the reliability of the system can be enhanced. When the circuit is power on, a typical of 0.73 μA of current charges the capacitor C_{SS}, the initial voltage on the C_{SS} is 0, when the voltage on the C_{SS} reaches the 0.8 V of reference voltage, the control unit stops the charging, then the charge current becomes zero, the voltage of the C_{SS} keeps constant at 0.8 V of reference voltage. The bandgap voltage is typically 1.2 V. The EN terminal is an input which enables or shuts down the device, furthermore, the enable circuitry has hysteresis and de-glitching for use

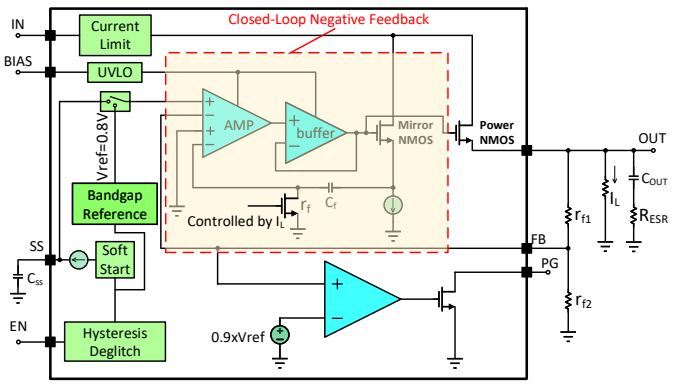

Fig. 2. The functional block diagram of the proposed LDO.

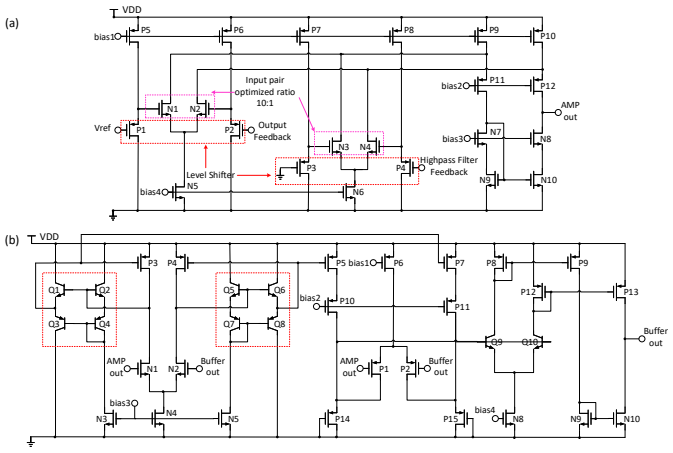

Fig. 3. (a) Schematic diagram of the error amplifier; (b) Schematic diagram of the buffer.

with relatively slow-ramping analog signals. The comparator makes a comparison between the reference and the fraction of the desired output voltage value, then the PG terminal provides an indication for the post-stage circuit to prevent the chip from attempting to operate on improper voltages. It is worth mentioning that this LDO is designed to have fast-transient response for large load current changes and also features thermal shutdown protection, under-voltage protection (UVLO) and over-current protection. The closed negative feedback loop (in red dashed box) which reacts to the current of load immediately includes: a dual-input transconductance error amplifier, a buffer, a mirror NMOS which keeps track of the current of the power transistor, and a high pass filter constituting by r_f and C_f, where r_f can be recognized variable resistor which is controlled by the current of the load.

III. Circuit Design Methodology

A. Error Amplifier and Buffer Design

a) Error Amplifier: As shown in Fig. 3 (a), the error amplifier has two pairs of NMOS differential input. One pair of differential input provides the main gain, and the other pair of differential input has smaller gain which provides a path for the feedback signals which will be superimposed on the main gain. In addition, since the reference voltage is

low, only 0.8 V, which is closer to the threshold voltage V_{th} of NMOS, the amplitude of the inputs is very small, then if PMOS transistors are used as the input differential pairs, the gate-source voltage V_{GS} will be too large, leads a very small g_m ($g_m = 2I_D/(V_{GS} - V_{TH})$) in case the tail current is predetermined, so that the width to length ratio will become much larger to achieve sufficient gain, at the same time, the parasitic gate capacitance becomes much larger and the loop response time becomes longer. Therefore, NMOS differential input pairs with level shifters are applied in this work. Firstly, since the feedback voltage is generally near the reference voltage, which is set to 0.8 V, so the level shifter is necessary to shift the input voltage range; accordingly, the transconductance g_m can be adjusted flexibly by controlling the input voltage. Both outputs of the two NMOS differential pairs are connected to a folded cascode output stage, their currents are summed together through the folded cascode output stage. Finally, the output signal $V_{Amp,out}$ is applied to the driver and a buffer for its proportional mirror transistor.

b) Buffer: Because the LDO uses NMOS as the power transistor, the voltage range applied to the gate of the power transistor is from 0.8 V to 5 V, then the buffer needs to work under this wide range, a two-stage buffer applied in this work is shown in Fig. 3 (b). The first stage is a complementary input stage, which is composed of a pair of PMOS and NMOS complementary differential pairs, which can respond to the wide input range required by the LDO. A fast transient design consisting of the bipolar transistors in the red dashed box (Q1, Q2, Q3, Q4 and Q5, Q6, Q7, Q8) can quickly charge and discharge the gate capacitors of P3, P4, P5, and P7, which is effective to improve the response speed. Bipolars Q9 and Q10 as the second stage input pair of buffer with small input capacitance will improve the output current capability and response time further, also the push-pull class AB output stage is used to enhance the output voltage swing and driving capability of load.

B. Loop Stability Considerations

In this work, the dual-input transconductance superimposed amplifier, buffer, as well as a high-pass filter constitute a closed-loop negative feedback, which has good stability and high phase margin (about 50 degrees in the worst case) over a wide range of output capacitor and its ESR (even without output capacitance).

In order to ensure the system stability, the high-pass filter feedback circuit and the transconductance ratio of the dual-input amplifier need to be carefully designed. As shown in Fig. 2, the high-pass filter feedback circuit comprises a current mirror NMOS whose current is scaled down of the NMOS power transistor (the ratio is about 1:40,000) and a first-order high-pass filter, the source of the mirror NMOS is connected to a current source, thus, the source voltage substantially follows the gate voltage without being affected by the output capacitance.

In Fig. 4, the green curve corresponds to the loop gain and phase without load, in this case, the loop gain and phase are 1 MHz and 80 degrees respectively, while the red curve corresponds to the loop gain and phase with 3 A full load current, the loop gain and phase are 200 kHz and 50 degrees. Through trial and error, the dual-input transconductance ratio of the error amplifier must satisfy at least $g_{m(N1,2)} : g_{m(N3,4)} = 10 : 1$, then the worst-case phase margin of 50 degrees can be satisfied. Under the extreme case, $g_{m(N1,2)} : g_{m(N3,4)} = 1 : 1$, the zero of the high-pass filter feedback circuit will almost counteract the second pole generated by the output capacitance, then the phase margin will become 90 degrees ($\pi/2$), this means that non-stability issues will never occur. However, in this case, the transient response speed of the LDO will worsen. In addition to the above issues, some performance requirements such as low noise and low offset also require the use of a smaller input transconductance $g_{m(N3,4)}$. Also, the larger input transconductance $g_{m(N3,4)}$ will increase the static current and chip area.

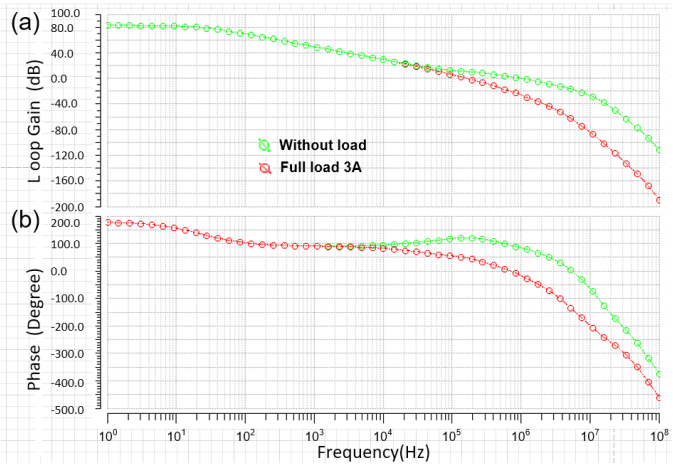

Fig. 4. Simulated response of the LDO.

In general, the LDO loop uses an innovative transconductance amplifier, a buffer and a high pass filtered feedback circuit that is unaffected by the load capacitance C_{OUT}. In fact, a zero is introduced to follow the second pole associated with the load capacitance C_{OUT} and provides a minimum of 50 degree phase margin with a wide range of load current I_L and output capacitance C_{OUT}. Moreover, the loop stability of the LDO is insensitive to the ESR of the out capacitance, which enables the NMOS LDO to achieve significant market advantages.

In addition, in order to achieve a dropout voltage of less than 200 mV at 3 A current even when packaged, bondwires are in parallel connection, as shown in Fig. 5(a), eight 1-mm gold wires form the R_{BOND}. In Fig. 5(a), L, D, and m respectively indicate the lead length, the bondwire diameter, and the number of bondwires in parallel connection respectively.

Fig. 5(a) shows the equivalent resistance of a ceramic package. R_{NMOS} is the on-resistance of the LDO, R_{BOND} is the equivalent resistance of the bond between the ceramic substrate and the leadframe, and R_{LEAD} is the equivalent resistance of the lead. Finally, the total resistance R_{total} from input to output is equal to 67.45 $m\Omega$.

IV. Measurement Results

The LDO is fabricated using a 0.6 μm CSMC BiCMOS process, and Fig. 5(b) shows the chip photo. The entire area

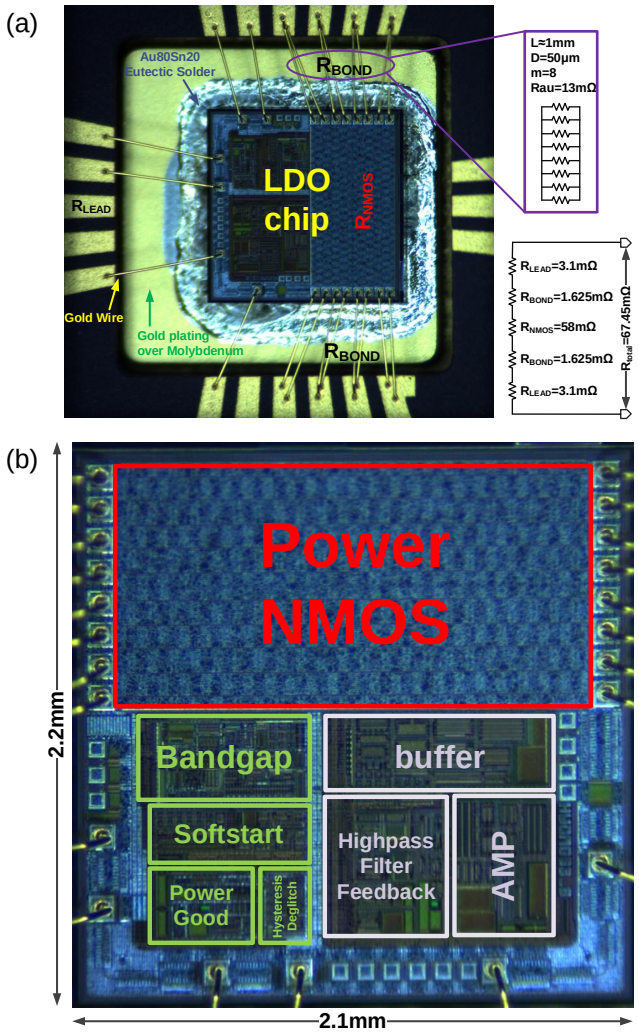

Fig. 5. The chip microphotograph: (a) The CLCC20 ceramic package and the equivalent resistance contribution of the package, and (b) detail of the chip area (with back-annotated layout).

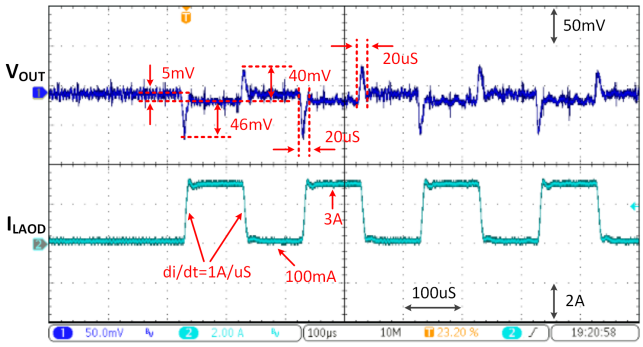

Fig. 6. Measured fast transient response of load current.

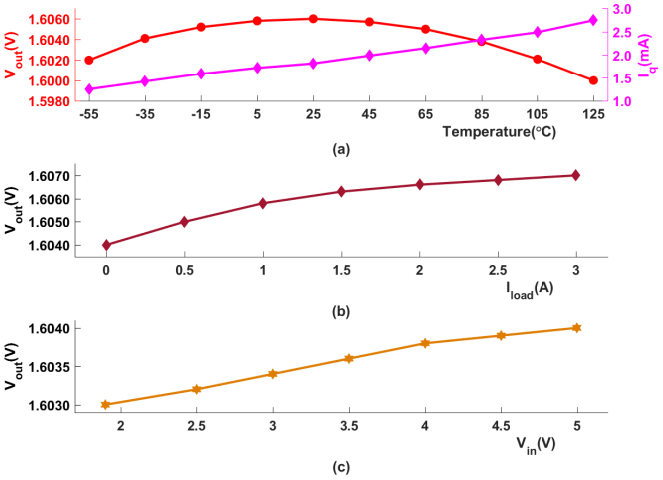

Fig. 7. (a) Quiescent current& Output voltage shifts versus Temperature; (b) Measured load regulation; (c) Measured line regulation.

of the chip including pads is 2.1 mm × 2.2 mm, and the core area without pads is 1.88 mm × 1.96 mm. The size of the power transistor is 896600 μm/0.6 μm to provide a high output current. The dropout voltage is approximately 200 mV.

The chip has a fast transient response with large load current variations. Fig. 6 shows the overshoot and undershoot are respectively about 40 mV and 51 mV without output capacitor, here, $V_{BIAS} = 5V$, $V_{OUT} = 1.6V$, and the settling time is approximately 20 μs.

The performance of the LDO keeps stable over the entire $-55\,^{\circ}C$ to $+125\,^{\circ}C$ range. As shown in Fig. 7(a), the variation of V_{out} over the full temperature range is less than 0.25 % and the quiescent current I_q varies from 1.25 mA to 2.74 mA over the full temperature range.

Fig. 7(b) shows the load regulation with load current varies from 50mA to 3A, the variance of V_{out} is 5 mV, and the LDO load regulation reaches 1.6 mV/A. Fig. 7(c) shows that when the load current is 50 mA, V_{in} changes from 1.9 V to 5 V, the variance of V_{out} is 1 mV, and the line regulation is 0.3 mV/V.

Table I summarises the measurement results of the fabricated LDO and comparison with state-of-the-art commercial products and academic research works. Among all the products, the proposed LDO has the fastest transient response, and can provide the maximum 3 A output current. Compared with similar product, this work has excellent line and load regulation. Although [14] has better line regulation, its maximum output current is only 0.8 A. Academic research works [6] can achieve low dropout voltage, but [6] does not provide the data of V_{OUT} when I_{OUT} is smaller than 30 mA. Also, all of these academic research works including [6], [15] and [7] do not consider the wide temperature operation and package. Finally, Figure of Merit (FOM) are compared by using [6]:

$$FOM = \frac{C_L \times \Delta V_{out} \times I_q}{I^2_{LOAD,max}} \quad (1)$$

The smaller the FOM, the better the transient response the LDO achieves. As shown in TableI, the proposed LDO obtains the smallest FOM factor among all of these commercial products, and in general, capless design can achieve excellent FOM.

V. Conclusion

An external capacitor-less NMOS low dropout linear regulator using a dual-input transconductance amplifier with CSMC 0.6 μm CMOS technology has been integrated. The measurement results show a maximum of 3 A output current

TABLE I
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART

	This work	[12]	[13]	[14]	[6]	[15]	[7]
Power Transistor	NMOS	NMOS	NMOS	NMOS	NMOS	PMOS	PMOS
Quiescent current (mA)	3	4	2	1	0.12	–	0.154
Output accuracy (%)	0.50%	1%	2%	1%	–	–	–
Output range	0.8 $\sim$ 3.6	0.8 $\sim$ 3.6	0.8 $\sim$ 3.6	1.22 $\sim$ 5.5	1	3.3	–
Maximum output current (A)	3	3	1.5	0.8	0.3	0.3	0.1
Operation temp. (°C)	$-55 \sim 125$	$-40 \sim 125$	$-40 \sim 125$	$-40 \sim 125$	27	27	27
Supply voltage (V)	2.2 $\sim$ 5.5	2.375 $\sim$ 5.25	2.7 $\sim$ 5.5	1.7 $\sim$ 5.5	1.05 $\sim$ 2.0	1.6 $\sim$ 1.8	1.4 $\sim$ 1.8
Technology(μm)	0.6	0.5	0.5	0.5	0.13	0.5	0.18
Dropout voltage (mV)	200mV @3A	195mV @3A	165mV @3A	200mV @0.4A	29.7mV @0.3A	–	200mV @0.1A
Load transient response(mV)	51mV @ΔIout=3A	50mV @ΔIout=3A	120mV @ΔIout=1.5A	200mV @ΔIout=0.4A	56mV @ΔIout=0.3A	–	97mV @ΔIout=0.3A
Load reg. (mV/A)	1.6 (worst) / 0.5 (typical)	0.48 (typical)	1.44 (typical)	8 (typical)	6 (typical)	33.4(typical)	10(typical)
Line reg. (mV/V)	0.3	0.8	0.48	0.16	5.5	1.66	10
Rising time (μS)	10 100mA $\sim$ 3A	10 100mA $\sim$ 3A	10 50mA $\sim$ 1.5A	2 10mA $\sim$ 0.4A	5 1mA $\sim$ 0.3A	1 0mA $\sim$ 0.1A	1 0mA $\sim$ 0.3A
FOM (fs)	5.1	6.65	292600	6.25	12440	2.1	150

and the low dropout voltage is about 200 mV. This fabricated LDO works stably under a wide range of output capacitance C_{OUT} and ESR, this non-sensitivity of loop stability to the ESR enables the NMOS LDO to achieve significant market advantages because most of the NMOS LDOs require an output capacitor to ensure circuit stability.

VI. Acknowledgments

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