Low off-state Leakage Currents in AlGaN/GaN High Electron Mobility Transistors By Employing A Highly Stressed SiN_x Surface Passivation Layer

S. J. Cho[a], X. Li[a], I. Guiney[b], K. Floros[a], D. Hemakumara[a], O. Ignatova[a], D. Moran[a] C. J. Humphreys[b], & I. G. Thayne [a]

[a] *School of Engineering, University of Glasgow, Glasgow G12 8LT UK*
[b] *Department of Materials Science & Metallurgy, University of Cambridge, Cambridge CB3 0FS UK*
Email: Sung-Jin.Cho@glasgow.ac.uk

Abstract

In this study, the impact of the stress in SiN_x surface passivation layers on off-state drain and gate leakage currents and off-state breakdown voltage in AlGaN/GaN High Electron Mobility Transistors (HEMTs) is assessed. The SiN_x films were deposited at room temperature by inductively coupled plasma chemical vapour deposition (ICP-CVD). Compared to unpassivated devices, the off-state drain and gate leakage currents of AlGaN/GaN HEMTs is increased by up to 2 orders of magnitude for a 200 nm thick SiN_x passivation layer with 309 MPa compressive stress. The use of a bilayer SiN_x passivation scheme comprising 70 nm SiN_x with 309 MPa compressive stress followed by 130 nm SiN_x with 880 MPa compressive stress resulted in off-state drain and gate leakage currents reduced by up to 1 order of magnitude when compared to unpassivated devices.

1. Introduction

The GaN based HEMT is a promising candidate for high power, high frequency and high temperature applications [1]. In these devices, SiN_x has been widely used for surface passivation between the transistor gate and drain and shown to be effective in mitigating current collapse and DC-to-RF dispersion due to the large density of surface states and trapped surface charge [2]. However, the use of SiN_x as a surface passivant can cause issues with increased off-state drain and gate leakage currents [3]. This is a critically sensitive issue for large area, high power transistors. In this work, a significant reduction in off-state drain and gate leakage currents in AlGaN/GaN HEMTs was observed by the use of a strain engineered bilayer SiN_x passivation scheme.

2. Experimental

AlGaN/GaN heterostructure epi-layers were grown on a silicon substrate by metal organic chemical vapor deposition. The layer structure comprised a 0.25 µm AlN nucleation layer; a 10^{18} cm^{-3} carbon doped buffer layer comprising a graded 4.6 µm AlGaN layer, followed by a 0.8 µm GaN layer; a 0.25 µm undoped GaN channel; a 1nm mobility enhancing AlN interlayer; a 27 nm AlGaN barrier and a 2nm GaN cap layer. Two samples of transistors were fabricated by first performing an electron beam evaporation of 30/180/40/100 nm Ti/Al/Ni/Au source and drain ohmic contacts which were annealed at 770 °C for 30 s in N_2, followed by a 600 nm etch of $SiCl_4$-based mesa isolation etch. The lateral mesa isolation leakage current was under 20 nA/mm. Then, 20/200 nm Ni/Au Schottky gate contacts 3 µm in length were deposited on the GaN surface. At this point, the "unpassivated" transistor characteristics were measured on both samples. Finally, a SiN_x passivation layer process split was implemented. The first sample, "Sample A", had a 200 nm thick SiN_x passivation layer deposited by ICP-CVD. This film was 309 MPa compressively strained (as measured when deposited on a silicon substrate) – the so called "normal" passivation in the following discussions. The second sample, "sample B", had a bilayer SiN_x passivation comprising 70 nm 309 MPa "normal" compressively strained SiN_x followed by a "highly" stressed 880 MPa 130 nm SiN_x film. The stress in the SiN_x films was controlled by varying the ICP power level in the CVD deposition tool.

3. Results and discussion

As shown in Figure 1(a) the sample with 200 nm "normal" stressed SiN_x passivation has significantly higher off-state drain and gate leakage currents, when compared to unpassivated devices. In comparison, as shown in Figure 1(b), the use of a 130 nm "highly" stressed SiN_x film on top of a 70 nm "normally" stressed passivation layer results in a 1 order of magnitude reduction in off-state drain and gate leakage currents, when compared to unpassivated devices. As shown in Figure 2, the off-state breakdown characteristics of the devices are similarly improved by using the bilayer passivation scheme. Table 1 summarised the key performance metrics obtained in this work. Bilayer stressed SiN_x layers can reduce gate and off-state leakage currents whereas also reduce transconductance. We need further studies of surface leakage currents and activation energies using Arrhenius plot to better understand the leakage mechanisms of each passivation scheme.

4. Conclusion

The impact of stress in SiN_x surface passivation layers on off-state drain and gate leakage currents and off-state breakdown voltage in AlGaN/GaN High Electron Mobility Transistors (HEMTs) is assessed. The use of a bilayer SiN_x passivation scheme comprising 70 nm SiN_x with 309 MPa compressive stress followed by 130 nm SiN_x with 880 MPa compressive stress resulted in off-state drain and gate leakage currents reduced by up to 1 order of magnitude when compared to unpassivated devices. This is a promising development for high voltage, large area and high current area GaN power transistors.

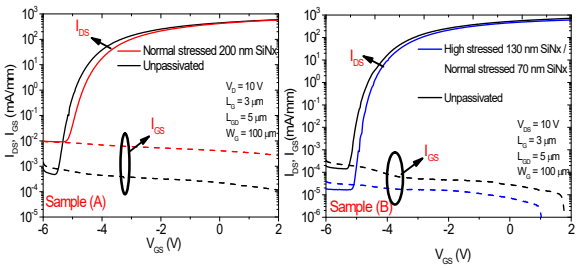

Fig.1. I_{DS}-V_{GS} and I_{GS}-V_{GS} characteristics for (a) 'normal' compressively stressed 200 nm SiN_x (b) the bilayer of 130 nm 'highly' compressive stressed SiN_x and 70 nm 'normal' compressive SiN_x surface passivation schemes.

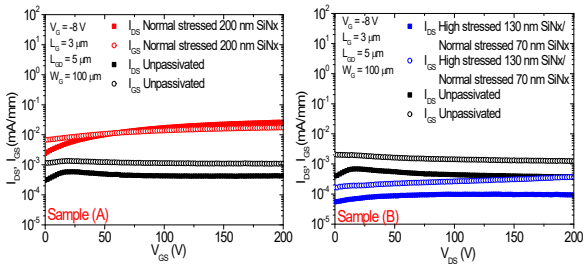

Fig.2. I_{DS}-V_{DS} and I_{GS}-V_{DS} off-state leakage current characteristics measured (a) 'normal' compressively stressed 200 nm SiN_x (b) 'highly' compressive stressed 130 nm SiN_x with 'normal' compressive 70 nm SiN_x surface passivation schemes.

Table.1. Summary of DC properties of different stressed SiN_x on AlGaN/GaN HEMTs.

	Sample (A)		Sample (B)	
	(1)	(2)	(3)	(4)
Off state leakage (μA/mm) @V_D=200 V, @V_G= −8 V	I_{DS} 0.42 I_{GS} 1.08	I_{DS} 26 I_{GS} 17	I_{DS} 0.36 I_{GS} 1.22	I_{DS} 0.09 I_{GS} 0.36
$I_{D\,max}$ (mA/mm) @ V_D= 10 V @ V_G= 2 V	541	593	707	632
$g_{m\,max}$ (mS/mm) @ V_D= 10 V	110	113	144	133
R_{ON} (Ω·mm)	4.21	3.82	4.46	4.81

(1) Unpassivated
(2) 'Normal' compressive stressed 200 nm SiN_x
(3) Unpassivated
(4) 'Normal' compressive stressed 70 nm SiN_x + 'highly' compressively stressed 130 nm SiN_x /

References

[1] U. K. Mishra, L. Shen, T. E. Kazior, and Y. F. Wu, Proc. IEEE 96,287 (2008).
[2] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, IEEE Electron Device Lett. 21, 268 (2000).
[3] Z. H. Liu, G. I. Ng, H. Zhou, S. Arulkumaran, and Y. K. T. Maung, Appl.Phys.Lett. 98, 113506 (2011).