High Mobility III-V MOSFETs For RF and Digital Applications

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Abstract

Developments over the last 15 years in the areas of materials and devices have finally delivered competitive III-V MOSFETs with high mobility channels. This paper briefly reviews the above developments, discusses properties of the GdGaO/Ga_2O_3 MOS systems, presents GaAs MOSFET DC and RF data, and concludes with an outlook for high indium content channel MOSFETs. GaAs based MOSFETs are potentially suitable for RF power amplification, switching, and front-end integration in mobile and wireless applications while MOSFETs with high indium content channels are of interest for future CMOS applications.

Introduction

Novel device architectures, high-κ gate dielectrics, metal gates, and high mobility channel materials will be required to continue CMOS device scaling according to Moore's Law and the International Technology Roadmap for Semiconductors (1). In the shorter term, high mobility GaAs MOSFET development will likely be more driven by RF applications. Developments over the last 15 years including the discovery of the device quality, MBE (molecular beam epitaxy) grown Ga_2O_3/GaAs interface in 1996 (2), the concept of bilayer dielectric stacks in 1995 (3), the proposal of heterostructure use to mitigate high band-edge interface-state density in 1997 (4), the realization of bilayer GdGaO/Ga_2O_3 dielectric stacks on GaAs in 1999 (5), the concept/fabrication of implant-free enhancement-mode high-mobility MOSFETs in 2000/2005 (6), (7), and the realization of low R_c Ohmic contacts in 2006 (8) have finally delivered competitive GaAs MOSFETs with effective channel mobilities exceeding 5,500 cm^2/Vs. Electron Hall mobilities of 12,000 cm^2/Vs have been measured in InP based MOSFET structures with $In_{0.75}Ga_{0.25}As$ channel layers (9). This paper discusses oxide/GaAs interface properties, presents GaAs MOSFET DC and RF data, and concludes with an outlook for high indium content channels for future CMOS applications.

Wafer Manufacturing

MOSFET wafers have been fabricated by MBE using an ultra-high vacuum (UHV) dual chamber configuration manufactured by DCA Instruments. Fig. 1 shows a dark field TEM micrograph of a typical GaAs MOSFET layer structure with an $In_{0.3}Ga_{0.7}As$ channel. Further fabrication details can be found in (10).

Results and Discussion

A. Oxide-GaAs Interface Properties

Electrical interface properties of Ga_2O_3 films and GdGaO/Ga_2O_3 dielectric stacks have been determined by a photoluminescence-intensity (PL-I) technique and by capacitance-voltage measurements. All investigated materials (Si, AlN, In_2O_3, SiO_x, MgO, Al_xO_y, Ti_xO_y, Ta_xO_y, Mo_xO_y, Zr_xO_y, Gd_2O_3, $LaAlO_3$, O, O_2) show essentially native oxide behavior on GaAs (group of high-interface defectivity films) except for Ga_2O_3 which provides a device quality interface (Fig. 2). Typical quasi-static and high-frequency (1 MHz) C-V curves of the dielectric stack deposited on a MOSFET-like epitaxial structure of Fig. 1 are shown in Fig. 3.

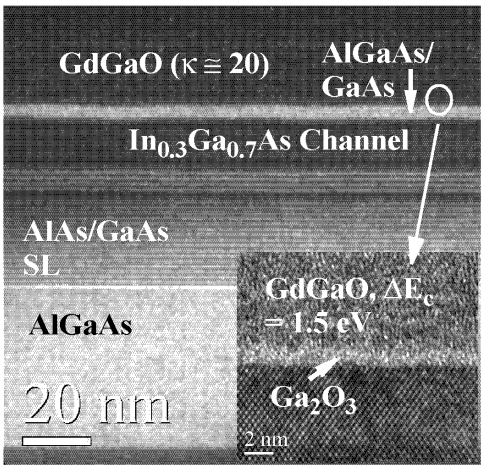

Fig. 1 Dark field TEM micrograph of a typical MOSFET structure with an InGaAs channel. The inset shows a high resolution TEM micrograph of the oxide/semiconductor interface.

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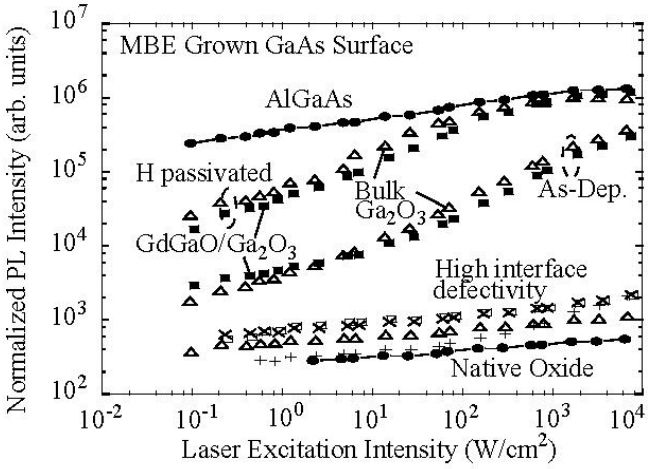

Fig. 2 Normalized GaAs photoluminescence (PL) intensity as a function of excitation intensity for AlGaAs (solid circles), bulk Ga_2O_3 (open triangles), $GdGaO/Ga_2O_3$ (solid squares), high interface defectivity films, and native oxide (solid circles) on GaAs. All materials are deposited on MBE grown surfaces under UHV conditions (except for native oxide).

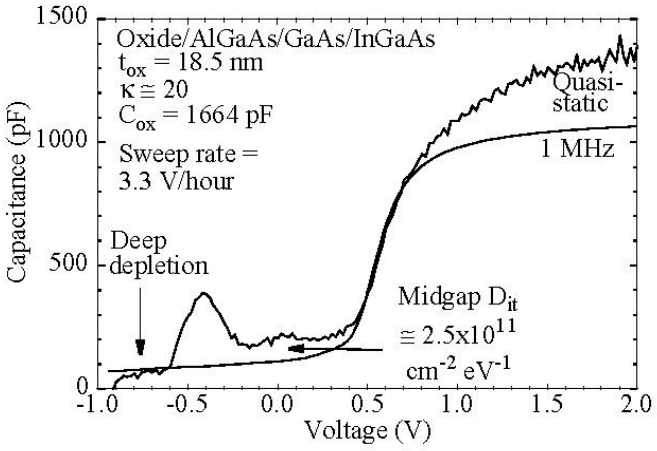

Fig. 3 Quasi-static and 1 MHz C-V curves of the GaAs based MOSFET structure shown in Fig. 1. The midgap interface state density for the dielectric stack with $\kappa = 20$ is determined to be $\cong 2.5x10^{11}$ cm^{-2} eV^{-1}.

B. GaAs MOSFET DC and RF Data

Enhancement-mode 1 µm n-channel GaAs MOSFETs with metal gate (Pt) and a 10 nm high-κ dielectric $GdGaO/Ga_2O_3$ ($\kappa \cong 20$) have been manufactured based on the implant-free device architecture proposed in (6). A two-level wrap-around gate design (where the gate encircles the drain) was used to simplify the device process flow, removing the need for isolation (see Fig. 4). With typical figures of merit including threshold voltage, V_t = +0.26 V, peak transconductance, $g_{m,max}$ = 477 mS/mm, on-resistance, R_{on} = 1.9 Ω mm, saturation drive current, $I_{D,sat}$ = 407 mA/mm, gate leakage current, I_g < 60 pA, output conductance, g_d = 11 mS/mm, and subthreshold swing, S = 100 mV/dec (Fig. 5, Fig. 6), our GaAs

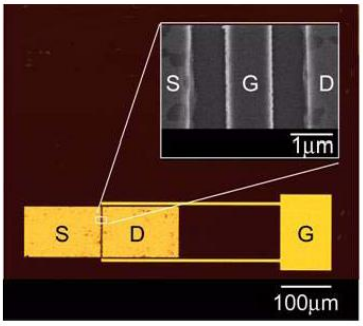

Fig. 4 Optical micrograph and SEM image of a 1 µm gate length GaAs MOSFET with wrap-around gate design. The source-drain distance is 2.7 µm.

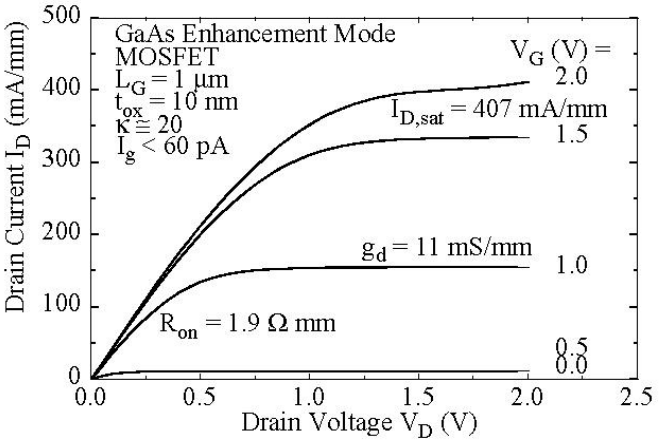

Fig. 5 Output characteristics of a 1 µm GaAs MOSFET.

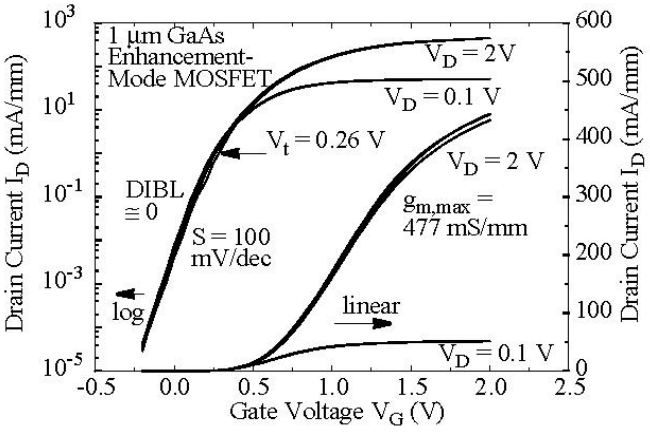

Fig. 6 Transfer characteristics of a 1 µm GaAs MOSFET. I_{on}/I_{off} ratio = $6.3x10^4$ (I_{off}, V_G = 0 V, V_D= 2 V) (I_{on}, V_G = 2 V, V_D = 2 V) and drain-induced barrier lowering, DIBL ≅ 0.

enhancement-mode MOSFETs perform as predicted by 2-dimensional device simulation. In contrast, GaAs enhancement-mode devices published by other groups over the last 40 years had typical g_m of less than 1 mS/mm with some recent marginal improvement into the 10-20 mS/mm range (11), (12). The peak effective channel electron mobility

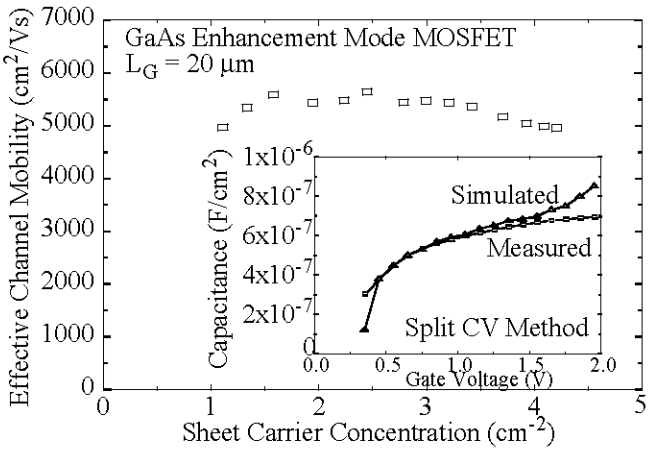

Fig. 7 Effective channel electron mobility as a function of sheet carrier density. The inset shows measured and simulated capacitance as a function of gate voltage.

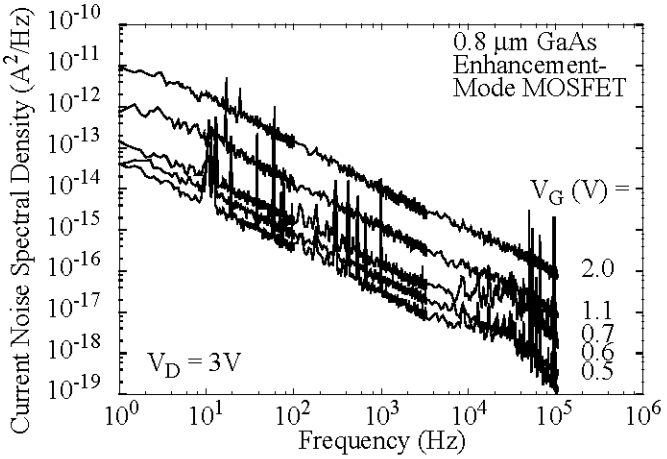

Fig. 9 Current noise spectral density vs. frequency with log-log scale with gate voltage bias point as a parameter for a 0.8 μm GaAs enhancement-mode MOSFET (W = 2x200 μm).

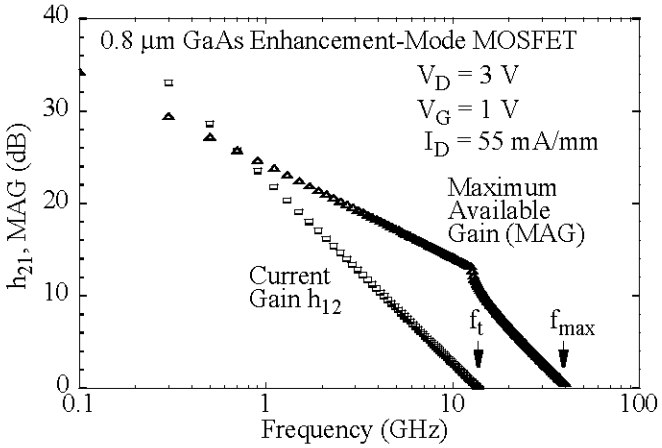

Fig. 8 Current gain h_{21} and maximum available gain MAG for a 0.8 μm GaAs enhancement-mode MOSFET (W = 2x100 μm). f_t and f_{max} are 13 and 42 GHz, respectively.

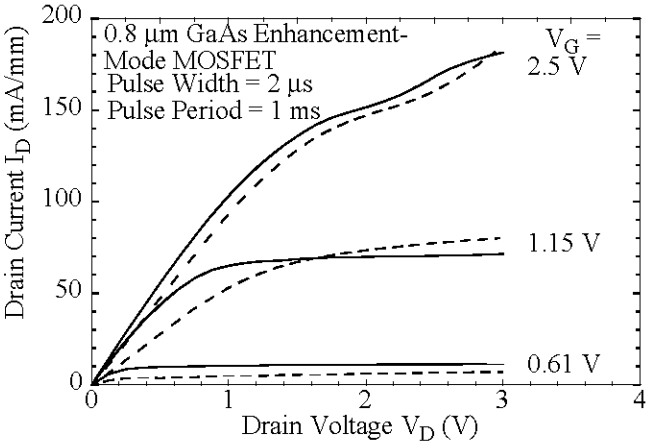

Fig. 10 DC (solid lines) and pulsed (dashed lines) I-V data of a 0.8 μm GaAs enhancement-mode MOSFET (W = 2x100 μm). The quiescent point for pulsed I-V is V_D = 3V and 10% $I_{D,sat}$ ($V_G \cong 0.6$ V).

is ≅ 5,500 cm^2/Vs (Fig. 7) as measured by an advanced split-CV method (13).

The gate and ohmic modules employed in the wrap-around gate design have been integrated into a flow for coplanar devices using oxygen implantation for device isolation. A first run has resulted in enhancement-mode devices ($V_t \cong +0.4$ V) with reduced DC performance of g_m = 135-160 mS/mm, R_{on} = 7-10 Ω mm, and $I_{D,sat}$ = 175 mA/mm. Small-signal parameters have been measured (Fig. 8) and average f_t and f_{max} of 13 GHz and 37 GHz (L_G = 1 μm), and of 14 GHz and 40 GHz (L_G = 0.8 μm), respectively, have been obtained (2x100, 2x200, 2x300 μm width). Preliminary on-wafer load-pull measurements at f = 900 MHz tuned for maximum power in class AB operation, provided P_{out} = 12.4 dBm with a corresponding gain of 11.3 dB and a power added efficiency of 45.6% (2x300 μm). Low frequency noise results are indicative of 1/f noise behavior with flicker noise typical of Si based MOSFETs (Fig. 9). Preliminary pulsed I-V measurements show small dispersion, with maximum dispersion occurring in the linear region at small V_D and in the threshold region (Fig. 10).

C. Towards CMOS

Preliminary lateral scaling data for 0.3 ≤ L_G ≤ 1 μm GaAs enhancement-mode MOSFETs with $In_{0.3}Ga_{0.7}As$ channels are shown in Fig. 11. To predict the performance of aggressively scaled III-V MOSFETs, we have used a finite element Monte-Carlo device simulator (14) verified against experimental data (sheet carrier density and mobility). As shown in Fig. 12, sub-20 nm gate length MOSFETs with $In_{0.3}Ga_{0.7}As$ channels could reach peak drive currents of around 1000 μA/μm at 0.8

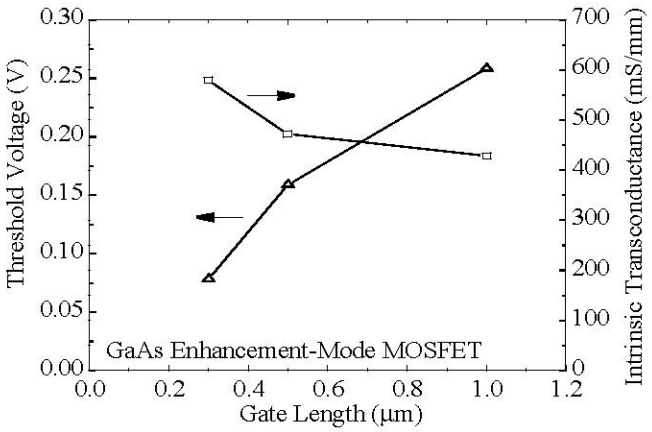

Fig. 11 Threshold voltage and intrinsic transconductance vs. gate length of 1, 0.5, and 0.3 μm GaAs MOSFET with an oxide thickness of 10 nm. The vertical layer structure was not scaled. Source-drain distance is 1.7 μm for L_G = 0.3 and 0.5 μm, and 2.7 μm for L_G = 1 μm.

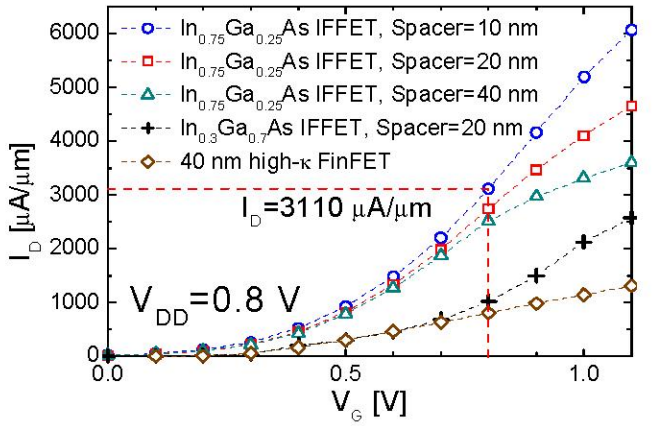

Fig. 12 Comparison of Monte-Carlo simulation of 15 nm III-V MOSFETs with different sidewall spacer sizes with a fabricated Si FINFET at V_D=0.8 V (supply voltage at the ITRS 22 nm node).

V supply voltages, outperforming the leading Si FINFET technologies (15). Moving to an $In_{0.75}Ga_{0.25}As$ channel potentially improves the drive current in excess of 2700 μA/μm (the current ITRS 22 nm technology generation target).

Summary

All investigated materials on GaAs were found to show essentially native oxide behavior except for Ga_2O_3 which provides a device quality interface. 1 μm GaAs enhancement-mode MOSFETs employing GdGaO/Ga_2O_3 dielectric stacks have been manufactured with V_t, $I_{D,sat}$, $g_{m,max}$, R_{on}, g_d, S, and I_g of 0.26 V, 407 mA/mm, 477 mS/mm, 1.9 Ω mm, 11 mS/mm, 100 mV/dec, and < 60 pA, respectively. An off-state breakdown voltage of 18 V was obtained for an oxide thickness of 18 nm. An effective channel mobility of ≅ 5,500 cm^2/Vs was measured using the split C-V method. A first coplanar process flow produced an average f_t and f_{max} of 13 GHz and 37 GHz (L_G = 1 μm), and of 14 GHz and 40 GHz (L_G = 0.8 μm).

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