

Converter Power Losses Computation by FPGA-based HIL Simulator

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Abstract—Converter losses play a crucial role in the process of power converter design. Especially semiconductor components and heat sink selection are strongly dependent on the total power converter losses and thus affect the power converter size and its price. The most popular techniques for determination of the losses are based on the computer simulation of the power converter. These kinds of simulations could be very time consuming, because on one side, the simulation needs very short step-time for differential equations calculation to model power converter switching. On the other side, the temperature dynamics of heat sink are commonly slow and depend on power cycles of converter. With the help of FPGA-based hardware in the loop (HIL), the simulation could run real-time and it is possible to test different scenarios, different modulation techniques and see their influences on converter losses. This approach can lead to reduction of losses to the state, when it is possible to reduce the size of converter. Furthermore, the HIL simulation could be used for testing and developing control algorithm in real time conditions. It also offers flexibility in the easy change of model parameters and monitoring values which are not or hardly obtainable in real machine. This paper presents the FPGA-based HIL simulator of induction motor drive with three phase voltage source inverter based on Semikron IGBT modules.

Index Terms—DSP builder; FPGA; conduction losses; switching losses; HIL testing

I. INTRODUCTION

Converter losses consist of two main parts. The first part is conduction losses which are influenced mainly by the choice of components. The second part are switching losses, which are influenced by switching frequency and current through component in time of switching [1]. This means, with the optimal switching pattern, it is possible to reduce switching losses. But it is also necessary to maintain current distortion, to avoid increased losses in the load of converter. Development and testing of techniques for converter losses reduction [2], [3] on real hardware takes huge amount of time and resources, because it is hard to measure power losses directly. In older techniques are the power losses measured as rise in temperature of components or heat sink. Problem with this approach is that temperature takes quite a long time to settle and results depend on accuracy of thermal model of converter. In addition conduction and switching losses are measured together and can not be separated.

Problems mentioned above can be solved by use of computer simulation, which can provide separated immediate values values of switching and conductive losses. Downside of simulation is impossibility to test real time control algorithm on end hardware and commonly slow computation of model. Computer simulation results heavily depend on accuracy of used model.

As optimal trade off can be used HIL simulation. It uses model similar to one used in computer simulation, so it provides separated immediate values of switching and conductive losses. Another advantage of this model is that it is driven in real time by the control algorithm loaded on end hardware.

II. HARDWARE AND HIL SIMULATOR

Hardware of HIL simulator is based on MLC interface [4], which was developed for control of multi-level converters and for development of complex control systems with FPGA-based hardware acceleration. In this case field programmable gate array (FPGA) is used to run real-time simulation of voltage source inverter with induction machine as load. This solution is great for development, because it allows easy change of converter and motor parameters. It is also possible to monitor values, which are not normally accessible from real machine. For example magnetic flux of machine or converter losses, which are the main concern of this paper. MLC interface allows use of various microcontroller units (MCU) and provides their connection to the FPGA, this leads to development and testing of control algorithm directly in C or C++ language. This makes transition from simulation to real application easier and quicker.

HIL simulation, which is the base for converter losses model, consists of voltage source inverter (VSI) and induction motor [5], [6]. Model is based on fixed-point arithmetic and individual parts of model are calculated with different accuracy, ranging from 16 to 20 bits. Inputs into this model are three phases of reference voltage, control signal, initial values of the model for the simulation start, parameters of converter and motor. Three phase reference voltage is used for pulse width modulation (PWM) control of the converter. It is not problem, that current HIL model works with constant switching frequency, because this model was

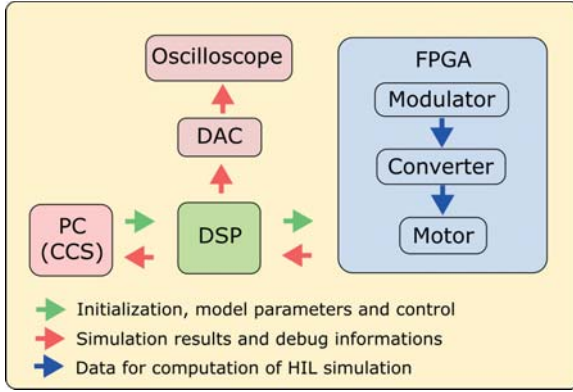


Fig. 1. Basic scheme of developed system

used just for development of losses model. Control signal is for model initialization/restart, PWM enable and results catch, which simulates analog to digital conversion of measured values. Initial values allows start of simulation from any state. Parameters of motor and converter are necessary for correct running of simulation. Parameters can be changed within the run of simulation. Inputs are loaded to the HIL simulation from digital signal processor (DSP) and they can be changed from computer through Code Composer Studio (CCS), integrated development environment (IDE).

III. MODEL OF CONVERTER LOSSES

As mentioned above presented model is based on previously developed model of induction motor with VSI. This paper focuses on upgrade of original model with the simulation of converter losses. As already mentioned HIL simulation is based on field programmable array (FPGA) chip. Code for this chip is automatically generated using Altera DSP builder advanced blockset for Matlab Simulink. To get results for the verification of model, parameters of converter components had to be chosen. The choice was semi-random and it was based on parameters of motor, already used in model, to get some reasonable results. Chosen parameters belong to Semikron IGBT module [7].

A. Conduction losses

For computation of conduction losses was used already developed model of voltage drop on semiconductor components. Voltage drop is determined by look up table (LUT) based on polarity and value of current. Losses are calculated with formula (1) for each phase separately and then summed (4) so the output is overall value of converter conductive losses.

$$P_{cond_i} = I_i dU_i \quad (1)$$

$$dU_{trans} = U_{trans} + IR_{trans} \quad (2)$$

$$dU_{diod} = U_{diod} + IR_{diod} \quad (3)$$

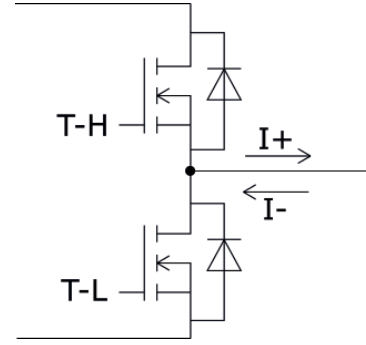


Fig. 2. Half bridge used for deduction of losses

$$P_{cond} = \sum_{i=1}^3 P_{cond_i} \quad (4)$$

To compute conductive losses, it is necessary to decide which component is active at given moment. This decision is made based on TABLE I. Current polarity and control signals, used in LUT, are shown in figure 2.

TABLE I
LUT FOR CONDUCTIVE LOSSES

T-H	T-L	Current	Loss
0	0	I+	$dU = dU_{diod}$
0	0	I-	$dU = dU_{diod}$
0	1	I+	$dU = dU_{diod}$
0	1	I-	$dU = dU_{trans}$
1	0	I+	$dU = dU_{trans}$
1	0	I-	$dU = dU_{diod}$

B. Switching losses

In computation of switching losses had to be taken different approach. Problem with switching losses is their concentration around the time of switching. For practical purposes is the calculation based on energy lost during the switching which is then used for calculation of mean power loss through switching period. Value of energy lost during switching process is based on polarity of current in time of rise/fall of transistor gate signal and value of current at given time. Figures in datasheet has shown there is almost linear dependence between energy lost during switching and current value, so it was possible to use equations (5).

$$E_{on} = k_{E_{on}} I \quad E_{off} = k_{E_{off}} I \quad E_{rr} = k_{E_{rr}} I \quad (5)$$

$$P_{switch} = f_{sw} \sum_{i=1}^4 Loss_i \quad (6)$$

Within switching period there are four times when switching, with non zero current, occurs. In these times of switching it is necessary to decide which kind of energy is lost. There are three possibilities, diode being turned off, transistor being turned off, or on. Decision is based on current polarity at the time of falling/rising edge of signal driving transistors. Energy lost during

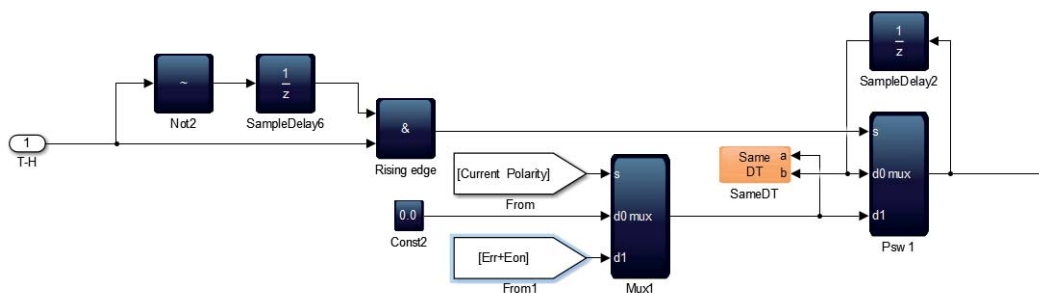


Fig. 3. T-H rising edge latch created by Altera DSP builder

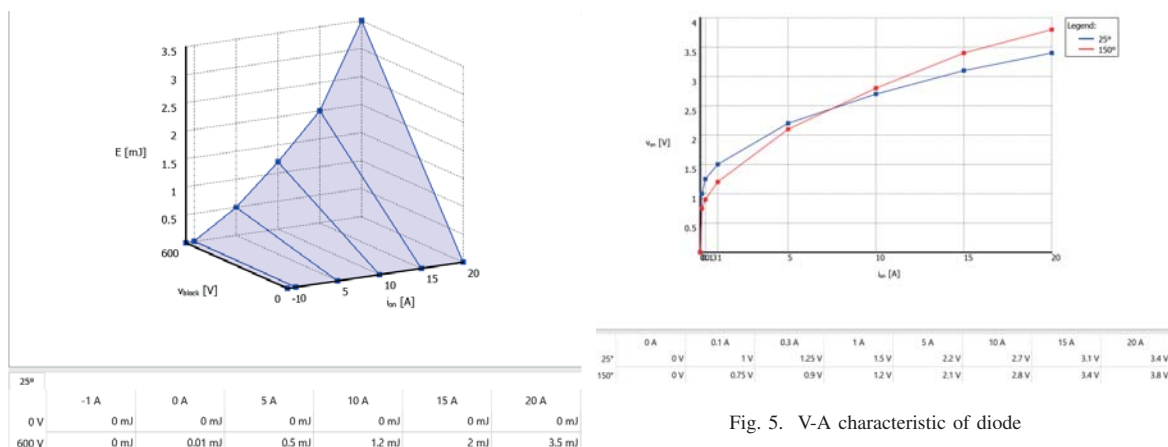


Fig. 4. Table for energy lost during switching on of transistor

switching period is used to calculate switching power loss for given phase (6). Total switching losses are equal to the sum of losses in individual phases.

In actual model this is calculated with use of four latches in each phase. Each latch reacts to its given event, rising/falling edge of control signal and updates itself to new appropriate value. Finished latch for rising edge of T-H signal made with the use of Altera DSP builder blockset is shown in figure 3.

 TABLE II
LUT FOR SWITCHING LOSSES

T-H	T-L	Current	Loss	i
↑	0	I+	$E_{on}+E_{rr}$	1
↑	0	I-	0	
↓	0	I+	E_{off}	2
↓	0	I-	0	
0	↑	I+	0	3
0	↑	I-	$E_{on}+E_{rr}$	
0	↓	I+	0	4
0	↓	I-	E_{off}	

C. Verification of model

To verify developed model was used simulation in Simulink blockset Plecs, which provides direct support for simulation of converter losses and thermal modeling. Outputs of converter model are similar to aforementioned techniques of calculation. Conduction losses are represented as power loss and switching

losses are represented as energy lost during switching. This also leads to need to convert lost energy into power. The conversion is made in manner similar to one used in HIL simulation, that means with the calculation of mean power loss during one switching period.

Parameters of used components are assigned to the Plecs model as table showing dependence of lost energy during switching on voltage and current shown in figure 4. It is also possible to include change of parameters for different temperatures. The conductive losses are computed based on V-A characteristic of components. For these characteristics, there is also possibility to include temperature dependency, as is shown in figure 5.

IV. RESULTS

There are two ways how to acquire results from HIL simulation. The first is to acquire results through CCS, used for compilation and debug of control algorithm loaded to MCU. HIL simulation is set to send results back to the MCU and from there results can be displayed in CCS. Other way is to use digital to analog converters (DAC) available in MLC interface and display outputs of DAC on oscilloscope. Advantage of the approach using DAC is possibility to show quick changes of simulation results in comparison to debug interface of CCS. Example of waveform displayed by oscilloscope is shown in figure 6. Shown results were obtained for the same model setting as results obtained by Plecs simulation in figure 7.

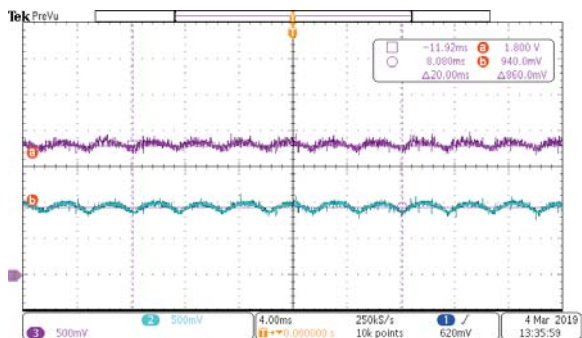


Fig. 6. Waveform of conduction losses (purple) and switching losses (blue) as result of HIL model (scale 20W/V)

Experiments show that model behaves in right way to the increase of current through converter and values of losses are similar to ones obtained by Plecs simulation. Measurement was executed by the change of load torque of the motor. In figure 8 are displayed results for Plecs and HIL simulation. Switching losses are almost identical for both simulations. In conduction losses is slight difference, this is caused by the use of more accurate V-A LUT table in Plecs model. Calculation of voltage drop in HIL model is far less sophisticated and uses simple linear regression.

V. CONCLUSIONS

This paper presents the FPGA-based HIL simulator of induction motor drive with three phase voltage source inverter based on Semikron IGBT modules. The HIL simulator of induction motor drive was used to real-time estimation of power converter losses. The comparison of results between computer simulation in Matlab Simulink with use of Plecs blockset and FPGA-based HIL simulator were used for HIL model verification. Experiment shows that results from Plecs environment and HIL simulation are similar. The errors are caused mainly by linear approximation of V-A characteristics used for modeling of conduction losses. Lesser influence has also linear approximation of turn on/off losses in HIL model and different calculation precision. FPGA-HIL model runs with fixed-point arithmetic and uses Euler method as solver. On the other hand, the Plecs model runs with floating point double precision arithmetic and uses Simulinks solver ODE45, but different solver can be used, only condition is variable time step, for Plecs blockset to work. Great advantage of FPGA-HIL simulation over Plecs is speed of calculation. For comparison: 1 second long simulation in Plecs takes 4 minutes on the common computer with intel i7 3GHz processor. The HIL simulation runs in real time, so simulation 1 second long takes 1 second to compute. That in this case means FPGA-HIL simulation is 240 times faster than computer simulation. This is going to have significant impact in the future, when the power losses calculation will be extended by heat transfer model for temperatures calculations. because implementation of

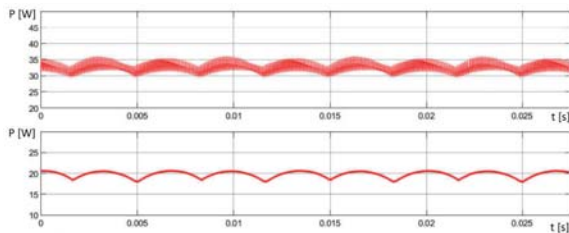


Fig. 7. Waveform of conduction losses (upper) and switching losses (lower) as result of Plecs model

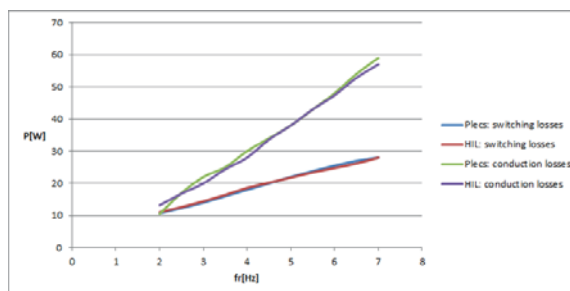


Fig. 8. Comparison of results for different values of rotor frequency

thermal model will lead to longer time constants of the simulation.

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