

CCII+ Based Novel Waveform Generator with Grounded Resistor/Capacitor for Tuning

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Abstract – This paper presents a new topology for waveform-generation using two current conveyors, and a grounded capacitor or a resistor for tuning. It uses current-conveyors in place of voltage op-amps to offer better linearity, bandwidth, slew rate and thermal stability. Measured results obtained using commercially available devices AD844AN and passive components show excellent linearity and tunability for both grounded resistor and capacitor topologies over the range of interest. Component sensitivity and temperature-sensitivity from -150°C to $+150^{\circ}\text{C}$ are studied. A comparison with existing candidate-designs shows superiority of the proposed design on all aspects. Grounded-connection of tuning components makes digital control easy.

Keywords- CCII+; Schmitt trigger; linearity; slew rate; tunability; digital control

I. INTRODUCTION

Triangular and square waveform generators are useful circuits with application in industrial electronics, sweep generation [1], mathematical function circuits and implementation of membership functions in analog and mixed-signal neuro-fuzzy systems [2], and also for testing and related measurements of analog-to-digital converters [1]-[4]. Although traditionally voltage-mode operational amplifiers (OA) as active element, connected in positive feedback as in Schmitt trigger had been used to design these circuits [5]-[6], it has been seen that current feedback operational amplifiers (CFOA) [7], operational transconductance amplifiers (OTA) [2] and current conveyors (CCII) [8] can also be connected in identical manner to generate square and triangular waveforms with capacitors suitably placed in the topology to have the required integration for triangular waveforms. In fact current mode devices offer better linearity over a wider frequency range with improved slew rate to attract designers to take renewed interest in current mode circuits.

A three-OTA based design [2] that has recently been reported is one of the topologies for current mode waveform generation. The design uses the OTAs as switching elements and controls the frequency by dc bias current. However, the design of [2] suffers from requirement of a complex tuning process where the 3-bias currents need to be simultaneously varied to get the full frequency-range. Further, most current-mode circuits using OTAs also have dependence on thermal

voltage V_T [2], [6], although less significant than their voltage-mode counter parts [9].

However non-linear circuits using current mode devices were not reported until about a decade ago when a Schmitt trigger using a single current conveyor was first reported by Cataldo et al [10]. This opened up a new era in terms design and industrial application of current mode devices operating in non-linear mode. Single-CFOA based relaxation oscillators soon came-up [4], [7]. But once again due to capacitor saturation, the waveforms produced by these single CFOA based configurations were highly distorted for most industrial applications. Moreover the linear operation range of these were limited to ~ 71.0 kHz which is another drawback. As such although application of current mode devices for linear operation continued to be observed [11], and even wideband waveform generators or oscillators using alternative technologies continued to be reported, very few original topologies came-up with current mode devices operating in non-linear mode [12]-[15].

Pal et al [1] have added a second active device (basically another CCII) for a new current-mode Schmitt trigger topology which overcomes the capacitor saturation problem of [4], [7] to report better linearity, frequency range and has very little distortion as can be seen from the elaborate comparative study included in [1] vis-a-vis OTA, CFOA and voltage mode waveform generators already reported or known to exist. However in [1] the use of floating capacitor is an undesired feature particularly for tunability and for Application Specific Integrated Circuits (ASIC)-implementation where high valued integrated capacitors are not recommended. In this paper therefore another new topology with two CCII is presented that uses grounded capacitor and resistor, each of which can be used for tuning. Further the new topology generates square and triangular waveforms with even better linearity and wider bandwidth compared to [2], [4], [7], [1] and produces less distorted wave shapes compared to [4], [7] and thus has the potential to be a better building block for use in electronics industry for cited applications. The grounded tuning components are advantageous because they offer easy digital tuning by switching-in a component of desired value with the help of a digital code or word.

The remaining Sections of the paper are organized as follows. The CCII(+) fundamentals, the proposed design and the analysis are presented in Section II.

Simulation and component sensitivity issues are presented in Section III and Section IV, respectively. Measured results based on AD844AN [16], the commercially available CCII(+), and a comparison of related performance indices with other contemporary designs are included in Section V. The current conveyor non-idealities are dealt-with in Section VI and finally the conclusion is included in Section VII.

II. PROPOSED DESIGN AND ANALYSIS

A. CCII+ Fundamentals

The symbol of a CCII is shown in Fig. 1. The terminal characteristics are defined by the following hybrid matrix for the signals at the three ports [8]:

$$\begin{bmatrix} i_Y \\ V_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ i_X \\ V_Z \end{bmatrix} \quad (1)$$

The \pm sign in (1) indicates whether the conveyor is formulated as a non-inverting or inverting circuit, represented by CCII+ or CCII-, respectively. By convention, positive is taken to mean both i_X and i_Z are either flowing simultaneously in (Fig.1) or away.

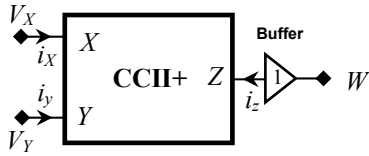


Figure 1. CCII+ model with buffer

However, for commercially available current conveyors such as the AD844AN [16] an additional voltage buffer is internally attached to node Z with its output terminated at a low impedance port W as shown in Fig. 1.

B. Proposed Design and Analysis

The proposed waveform generator is presented in Fig. 2. Initially let us assume that the voltage at node W of CCII+(1) is at the positive peak of the square wave V_s . As such the voltage at Z_1 is also at V_s and the current I_{z1} ($= V_s/R_1$) is going out. For ideal CCII(+) $I_{x1}=I_{z1}$ and therefore I_{x1} flows out of the node X_1 as shown in the Fig. 2.

From the node equations of ideal CCII(+) we also get that the node voltage at X_2 is at V_s and $I_{x2} = V_s/R$ is going out. We can therefore conclude that the node current going out of I_{z2} is V_s/R . Therefore at this point of time the capacitor C is getting charged by the combined current $I_{z2}+I_{x1}$. We can thus write the charging equation for C as

$$C \frac{dV_T}{dt} = \frac{V_s}{R} + i_{x1} \quad (2)$$

where V_T is the voltage charging the capacitor linearly to give rise to a triangular waveform.

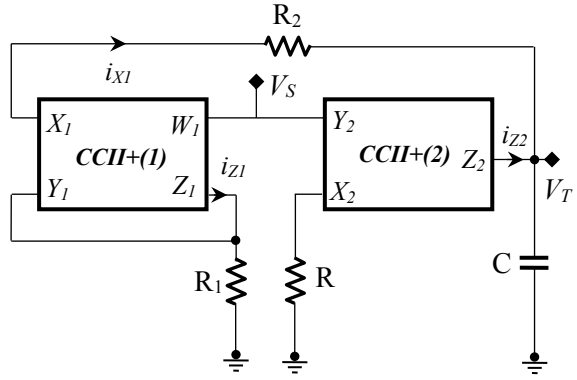


Figure 2. Proposed waveform generator using CCII+

Again i_{x1} which is i_{z1} can be written as

$$i_{x1} = \frac{V_s - V_T}{R_2} \quad (3)$$

Substituting i_{z1} for i_{x1} and combining (2) and (3) to eliminate V_s we can write

$$V_T \frac{R_1}{R(R_1 - R_2)} + V_T \frac{1}{R_1 - R_2} = C \frac{dV_T}{dt} \quad (4)$$

Now this process continues and the capacitor gets charged to V_T until the node voltage Z_2 is high enough to force a current in the opposite direction in the branch i_{x1} . When that happens, the current direction of i_{x1} , i_{z1} , i_{x2} and i_{z2} changes and the node voltage at Y_1 drops from V_s to $-V_s$ and the reverse transition with the capacitor-voltage discharging through i_{z1} and i_{x1} starts. The governing equation as can be seen easily, however, remains the same for the discharging path as well and thus (4) holds.

Solving (4) we can get the expression for time period of the waveform generator which can be written as $T=1/f$. where f is expressed as

$$f = \frac{R_1}{2\pi R(R_1 - R_2)C} + \frac{1}{2\pi(R_1 - R_2)C} \quad (5)$$

Obviously the condition for the waveform generation is a positive feedback with a loop gain greater than unity which in this case leads to the condition

$$R_1 \gg R_2 \quad (6)$$

Further by selecting $R \ll R_2$, we can simplify (4) to arrive at a more compact equation which is expressed for the time period T as

$$T \cong 2\pi RC \left(1 - \frac{R_2}{R_1} \right) \quad (7)$$

However, R_2 cannot be increased indefinitely to make it larger than R . Because apart from the fulfilment of the condition (6), the drop $i_{x1} \cdot R_2$ has a direct relation on the peak of the triangular waveform and the higher the value of R_2 , the smaller will be the level of the peak from the supply-rail. From (7) it can be further seen that both the grounded components R and C can be independently varied for tuning the waveform-generator.

III. SIMULATION RESULTS

Next we tried to verify the validity of our analysis with the supporting simulation results. For this purpose the SPICE level 1 model of MOS transistors with $V_{tn} \cong 0.5V$ and $V_{tp} \cong -0.6V$ were used. The CCII(+) design was imported from [17] which is reproduced here in Fig. 3 for its CMOS version. The complete design of Fig. 2 needs two such CCII(+) blocks presented in Fig. 3 apart from the passive components and the buffer, which in this case is an operational amplifier connected in unity-gain topology. The MOS level complete circuit is not presented here for brevity but the device dimensions used for simulation are included in Table-I. The capacitor C_c inside the CCII(+) block has been chosen to be 5.1 pF and a bias current of 100 μA has been set for observing the simulation.

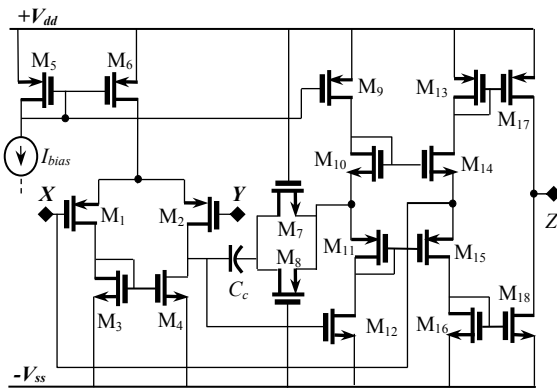


Figure 3. CMOS CCII(+) block used for simulation

TABLE I. ASPECT RATIOS

Symbol	M_1, M_2	M_3, M_4	M_5, M_6	M_7	M_8	M_9
W/L (μm)	120/7	50/10	150/10	7.5/15	7.5/5	150/10
Symbol	M_{10}, M_{14}	M_{16}, M_{18}	M_{13}, M_{17}	M_{11}	M_{12}	M_{15}
W/L (μm)	135/5	200/10	365/10	287.5/5	95/10	402.5/5

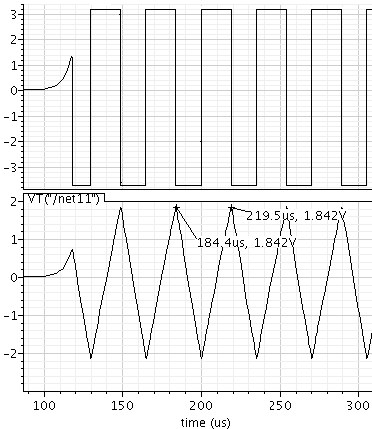


Figure 4. Typical simulation profile of square and triangular waveforms (for $R_1 = 70$ k Ω , $R_2 = 30$ k Ω , $R = 2$ k Ω and $C = 5$ nF)

The circuit was first simulated for generation of triangular and square waveforms from DC to 400 kHz. The configuration exhibited smooth variation over the entire range with very little distortion. A test waveform is presented in Fig. 4. The tunability for the grounded capacitor C was next tested for the configuration and once again the theoretical plots derived from (9) and simulated plots matched as can be seen from Fig. 5. Similar tunability was observed for variation of another grounded component, R_1 , for the entire range (DC to 400 kHz) and once again the theoretical and simulated responses matched closely as can be seen from Fig. 6. Next the circuit was tested for temperature stability over the range from $-150^\circ C$ to $+150^\circ C$ and for both square and triangular waveforms the simulation profile produced less than 0.02% variation.

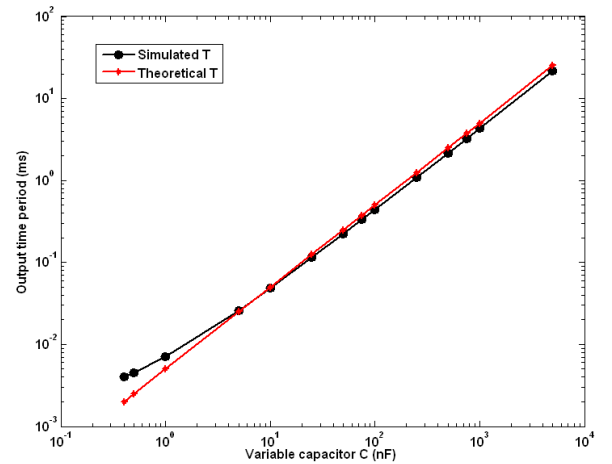


Figure 5. Time period versus C (for $R_1 = 50$ k Ω , $R_2 = 30$ k Ω , $R = 2$ k Ω , C is variable)

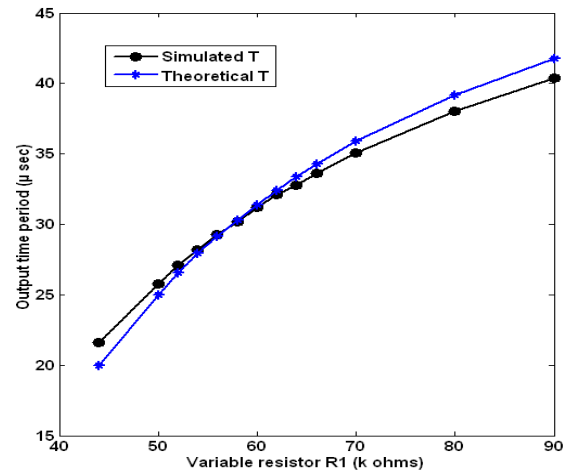


Figure 6. Time period versus R_1 ($R_2 = 30$ k Ω , $R = 2$ k Ω , $C = 5$ nF and R_1 is variable)

IV. MEASURED RESULTS

To verify and benchmark the theoretical design, AD844AN was next adopted to construct the proposed circuit. For the sake of comparison in terms of linearity, bandwidth and power consumption with existing configurations such as [4] and [7], we had built the proposed circuit. The configuration produced

square and triangular waveforms over the linear range of DC to 400 kHz. The tunability of the configuration was tested for both C and R₁ and the stability of the amplitude over the linear-range for the square wave was also verified. As the graphs obtained from the measured results closely replicated the already presented simulated ones, they are not included here to avoid repetition and for brevity.

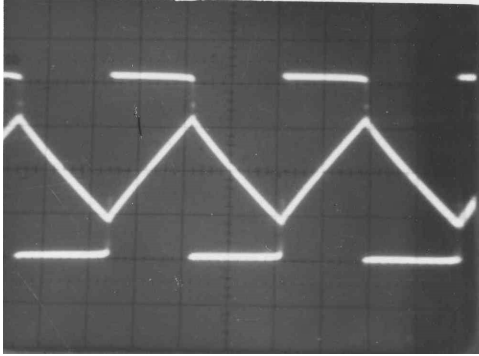


Figure 7. Observed output at VT (triangular wave) and VS (square-wave) from the circuit as in Fig.3 (built with AD844AN with for R₁ = 100 kΩ, R₂ = 20 kΩ, R = 22 kΩ, and C = 4.7 nF); Scale: X-axis 0.2 m Sec/Div and Y-axis 5 Volts/Div.

From a comparative experimental study it was further established that the proposed circuit outscored the competitive OTA [2] and CFOA [4] based designs in linearity and power consumption, and the conventional voltage OA-based design in terms of bandwidth, linearity and component count. The proposed design also outperformed a previous design proposed by these authors which is included in [1]. Although the voltage mode design reports lower power dissipation, but the linearity and bandwidth for these designs are unacceptably low. Moreover it requires nearly double the number of passive components as compared to the proposed design. Similarly, although the OTA based design reports higher bandwidth, its linearity is very poor and power dissipation is very high. Moreover control of the OTA-based configuration and tuning of the frequency [2] involves the complexity where the 3-bias currents need to be simultaneously varied to get the full frequency-range. Likewise although the CFOA-based configuration [4] uses only one active element as compared to the proposed design which uses two, the former reports very low linearity and bandwidth both, and has slightly higher power consumption as compared to the proposed design. Thus from the comparison presented in Table-II, the proposed configuration is observed to have the best overall performance taking all aspects into consideration. A square and triangular waveform viewed typically on the oscilloscope screen is presented in Fig. 7.

TABLE II. COMPARATIVE PERFORMANCE ANALYSIS

Candidate Designs	Power Consumption	Band-Width	Linear-range (linearity =5% or less)	No. of Elements (P: Passive, A: Active)
Proposed Design (Using AD844)	300 mW	400kHz Z	400 kHz	Total 6 (4-P, 2-A)
Ref [2] OTA (Using LM13600)	>750 mW	900 kHz	20 kHz	Total 6 (3-P, 3-A)
Ref [5] (Using LM 741)	102 mW	100kHz Z	50 kHz	Total 9 (7-P, 2-A)
Ref [4] (Using AD844)	348 mW	100kHz Z	85 kHz	Total 5 (4-P, 1-A)
Ref [1] (Using AD844)	384 mW	225kHz Z	225 kHz	Total 6 (4-P, 2-A)

V. CONCLUSIONS

A new topology for waveform generator using two CCII(+) and four passive elements with grounded tuning resistor and capacitor is presented. The simulation results included exhibit excellent matching with the theoretical results obtained from analysis. The topology is next realized using AD844AN, the commercially available form of CCII(+) and the measured results once again show close matching with the simulated and theoretical estimations on every account.

The proposed topology also has its genesis (like that reported by Abuelma'atti et al [4],) in current mode Schmitt trigger first used by Cataldo et al [10], but overall it improves upon all candidate topologies (including [4] that was built using voltage-mode devices,) in terms of band with, linearity and DC power dissipation. An appropriate comparison establishes its superior substitute on overall performance index. Tunability by grounded passive components is an attractive feature as it provides an easy digital control [18] by programmable switched capacitor/resistor array and makes the circuit suitable for ASIC-implementation. The component-sensitivity and temperature sensitivity (not included here)is small which also makes the topology a candidate for integration. The topology assumes special significance in view of recently renewed-interest observed in CCII(+) based non-linear designs [1], [11].

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