FPGA-Based Resonant-Frequency-Tracking Power Amplifier for Ultrasonic Transducer

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***Abstract* – An FPGA-based class-D power amplifier is designed for driving an ultrasonic transducer. The amplifier is capable of automatically detecting and tracking the transducer's resonant frequency, driving the transducer right at its resonance for maximizing vibration efficiency. The design focuses on devising resonant frequency tracking and optimal modulation algorithms that are suitable for FPGA implementation.**

Keywords- class-D power amplifier, ultrasonic transducer, resonant frequency tracking

I. INTRODUCTION

Ultrasonic transducers, devices that convert electrical energy to ultrasonic vibrations, find their way into a wide spectrum of applications, including ultrasonic spray coating [1], ultrasonic assisted machining [2], ultrasonic cleaning [3], ultrasonic welding [4], and many more. Ultrasonic transducers are commonly designed to have high Q-factors in order to achieve high efficiency. However, high Q-factor means a narrow bandwidth; a slight deviation from the resonant frequency may quench the oscillation and cause a serious drop in transducer efficiency. To make the matter worse, the transducer's resonant frequency may vary with temperature and load [5]. This motivates the design of a resonant frequency tracking power amplifier that is capable of detecting and tracking the resonance of an ultrasonic transducer and automatically drive the transducer right at its resonance. There are three main categories of control methods for automatic resonant frequency tracking: relay feedback self-oscillation [5], extremum seeking [6], and phase locked loop (PLL) [7]. This work focuses on the PLL method and devises a PLL resonant frequency tracking algorithm that is suitable for FPGA implementation. For better power efficiency, an FPGA-based class-D power amplifier is designed. Also an algorithm for generating optimal one-pulse PWM is presented.

II. FPGA-BASED POWER AMPLIFIER DESIGN

Figure 1 shows the FPGA-based design of a resonant-frequency-tracking class-D power amplifier [8]. An FPGA is programmed to generate switching commands for an H-bridge of NMOS power transistors to produce a three-level switching waveform. Digital isolators isolate the low-voltage control and sensing circuits from the high-voltage

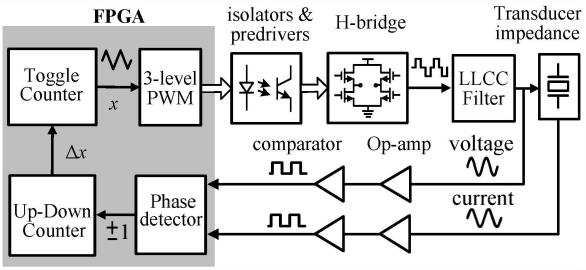

Fig. 1. Schematic diagram of the FPGA-based resonant-frequency-tracking power amplifier.

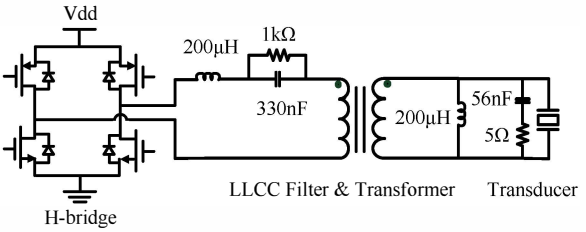

Fig. 2. Power stage of the designed class-D amplifier.

power stage. Pre-driver ICs drive both the low-side and high-side NMOS transistors. Figure 2 shows the detailed power stage. A bandpass LLCC filter [9] removes high-frequency noise from the chopped waveform to recover a nearly sinusoidal waveform for driving the transducer. The resonant frequencies of series and parallel LCs in the LLCC filter of Fig. 2 determine the filter's cutoff frequencies, 11 kHz and 80 kHz in this case. Additional 1 kΩ and 5 Ω resistors are used to attenuate the LC resonances. A 1:1 transformer is for isolation and filtering. Following the sensing amplifiers, two comparators convert the transducer's driving voltage and current waveforms into the square ones. By the comparison of the phases of the voltage and current, the FPGA tunes the driving frequency, performs pulse-width modulation (PWM), and generates the associated switching commands for the transistors. The FPGA algorithms for resonant frequency tracking and PWM are detailed in the following sections.

III. PLL RESONANT FREQUENCY TRACKING ALGORITHM

The phase locked loop (PLL) method [7] is employed for resonant frequency tracking. The PLL

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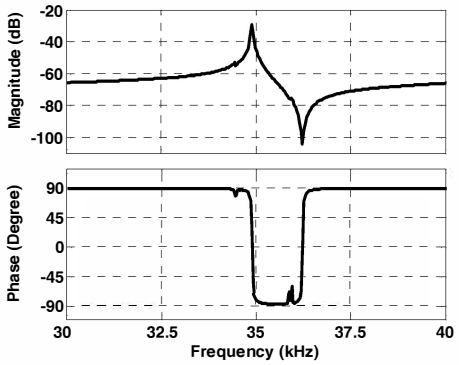

Fig. 3. Admittance measurement of a 35kHz transducer.

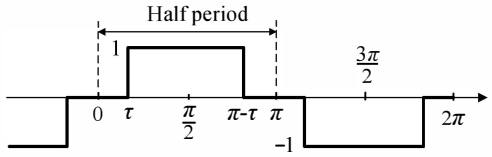

Fig. 4. One-pulse PWM with the period normalized to 2π.

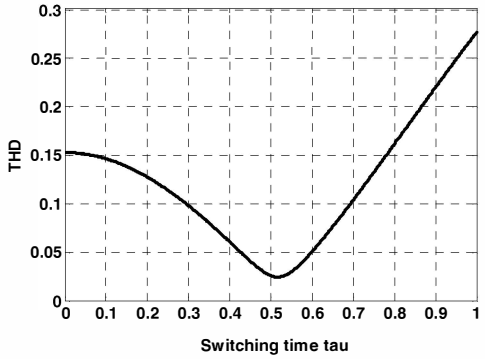

Fig. 5. THD of transducer's driving waveform vs. switching time τ.

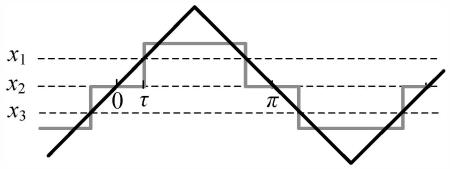

Fig. 6. Optimal one-pulse PWM generated by comparing the triangle wave x with the prescribed values x_1, x_2, and x_3.

method works because that, for a high Q-factor transducer, its resonance occurs when the driving voltage and current are in phase. Strictly speaking, the zero-phase frequency is slightly higher than the theoretical resonant frequency, but the frequency discrepancy is negligible for a high Q-factor transducer. Consequently, so long as the amplifier keeps tuning the driving frequency to make the driving voltage and current in phase, frequency locking at resonance is guaranteed.

The admittance vs. frequency graph of a 35 kHz transducer in Fig. 3 suggests a simple tuning rule: Initially set the driving frequency near the nominal resonant frequency of a transducer (i.e., 35 kHz in this case). Measure the driving voltage and current, and compare their phases. Increase (decrease) the driving frequency a little bit at each sampling time when the current leads (lags) the voltage. Repetition of this process at each sampling time leads to frequency locking near the resonance. The discrepancy between the driving frequency and the real resonant frequency depends on the frequency tuning resolution.

The block diagram in the FPGA block of Fig. 1 illustrates how the PLL algorithm works. A toggle counter counts up or down with an increment or decrement Δx. The mode of counting, up or down, toggles when the counter overflows or underflows. So the toggle counter, which plays a role similar to a voltage-controlled oscillator in a conventional PLL, can be used to generate a triangle wave x with its frequency controlled by the value of Δx. The triangle wave frequency will be the driving frequency. The value of Δx is constantly adjusted by an up-down counter. When the current leads the voltage, the phase detector gives an output of +1. In this case, the up-down counter adds Δx by one, thereby causing a slight increase in the triangle wave frequency. When the current lags the voltage, the phase detector gives –1, resulting in the subtraction of 1 from Δx and a slight decrease in the triangle wave frequency.

IV. Optimal One-Pulse PWM

Without loss of generality, assume the frequency of the desired driving sinewave is normalized to 1 (i.e., the period is 2π), and the driving waveform is represented by the one-pulse PWM as shown in Fig. 4. The one-pulse PWM [8] contains only one pulse in every half period, and due to its odd, quarter-wave symmetry, the switching time τ is the only chosen parameter. The design objective is to select τ to minimize the total harmonic distortion (THD) of the filtered driving waveform to the transducer.

The Fourier series of the one-pulse PWM signal in Fig. 4 is

$$f(t) = \sum_{n=1,3,5,\cdots} a_n \sin(nt) \tag{1}$$

where

$$a_n = \frac{4}{n\pi}\cos(n\tau) \tag{2}$$

Since the amplitude of the PWM is normalized to 1, the modulation index m is related to the switching time τ by the following Formula.

$$m = a_1 = \frac{4}{\pi}\cos(\tau) \tag{3}$$

Assume that under the same frequency normalization, the frequency response function of the LLCC filter of Fig. 2 is assumed to be $G(\omega)$. Then, to every one-pulse PWM of different switching time τ there corresponds a filtered driving waveform, the THD of which is estimated as follows.

$$\mathrm{THD} = \frac{\sqrt{a_3^2 \,|G(3)|^2 + a_5^2 \,|G(5)|^2 + a_7^2 \,|G(7)|^2 + \cdots}}{a_1 \,|G(1)|} \tag{4}$$

Figure 5 shows a graph of THD vs. switching time τ. When $\tau = 0$, the 3-level PWM reduces to a simple two-level square wave with the THD of 15.3%. The THD reaches its minimum value 2.43% at $\tau = 0.517$, which corresponds to a modulation index of 1.107. Figure 6 shows that once the optimal switching time τ is determined, we can find the corresponding switching points x_1, x_2, and x_3 for the triangle wave x generated by the toggle counter. The optimal one-pulse PWM waveform can thus be easily determined by comparing the triangle wave x with the prescribed switching points x_1, x_2, and x_3.

V. Experimental Results

The above mentioned optimal one-pulse PWM and PLL resonant frequency tracking algorithms are implemented on an FPGA, Altera EP4CE6E22C8N. The shunt-resistor method is used for current sensing. A 5 Ω shunt resistor is connected in series with the transducer and the voltage across it is measured. The supply voltage Vdd for the power transistors in Fig. 2 is generated by a single-ended primary inductance converter (SEPIC) [10].

Figure 7 displayed the measured waveform for the resonant frequency tracking amplifier when driving a 35 kHz transducer. The PWM switching voltage and the filtered voltage are shown on the oscilloscope with ten times reduction. To achieve 8W driving power, the supplied voltage Vdd is adjusted to 52 V. It shows that the class-D amplifier generates the desired three-level chopped waveform. The resonant frequency tracking algorithm works very well; the driving voltage and current are always kept aligned in time to maximize the driving power. It can be seen from the scope graph that the driving frequency is locked at 34.97 kHz at the moment of measurement.

VI. Conclusion

An FPGA-based power amplifier is designed for driving ultrasonic transducers in the ultrasonic spray coating application. The targeted driving frequencies are from 20 kHz to 80 kHz.

Two main design objectives are considered. First, to maximize transducer efficiency, a resonant frequency tracking algorithm is devised so that the amplifier can automatically tune the driving frequency and drive the transducer right at resonance. Second, to improve the driving efficiency, a class-D amplifier structure is used for the design. An optimal one-pulse PWM algorithm is devised to minimize the harmonic distortion seen from the transducer. Both the resonant frequency tracking and PWM algorithms are implemented on an FPGA. The class-D amplifier together with the FPGA-based control circuit greatly enhances both driving efficiency and transducer efficiency.

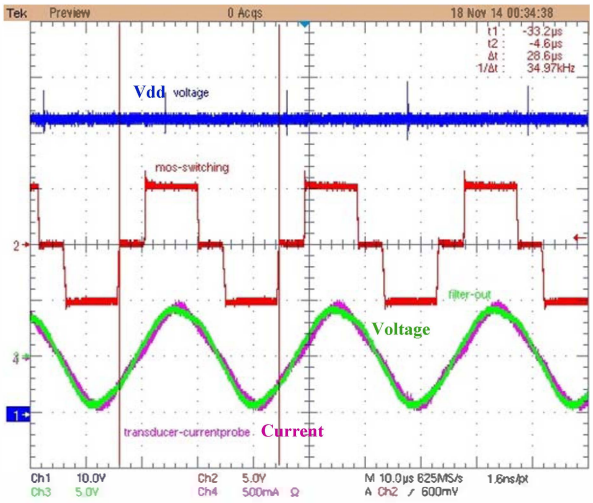

Fig. 7. Measured waveforms for the amplifier.

Acknowledgment

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