Testing nonlinear analog circuits by supply current variation and supply voltage monitoring

Andrzej Kuczyński

Faculty of Electrical, Electronic, Computer and Control Engineering, Lodz University of Technology, Żeromskiego 116, Łódź, Poland, e-mail: andrzej.kuczynski@p.lodz.pl

Abstract **In this paper a method for testing nonlinear analog circuits by supply current variation and supply voltage monitoring is presented.**

Keywords **Analog circuits, fault detection, discrete wavelet transform, feedforward neural network, testing.**

I. Introduction

Detection and localization of analog electrical circuits faults is still an important part of modern modeling and designing process. Procedures based on monitoring the supply current (IDD tests), when the supply voltage changes, are often used for analog circuits fault detection and localization [1]. The aim of this paper is to present the method for testing nonlinear analog circuits by supply current variation and supply voltage monitoring (proposed name – VDD test).

II. Test description

To measure the transient supply voltage we need to set the tested circuit into an unsteady state. For this purpose at a zero, the supply current value fell from a I_{max} to a I_{min} during the time T like linear function. I_{max} and I_{min}-values should be determined experimentally, so as not to damage the system under study. The voltage changes are illustrated in the Fig. 1. In order to exposure changes of

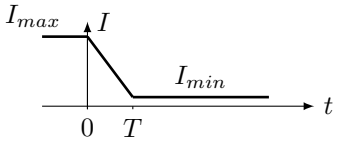

Fig. 1. Time-varying supply current

features of the device resulting from damages, test signals will be divided into elements by means of bank of filters formed with the use of discrete wavelet transform [1], [2].

III. Example

The circuit, shown in the figure 2, was chosen as an example. The figure shows the power supply of the circuit

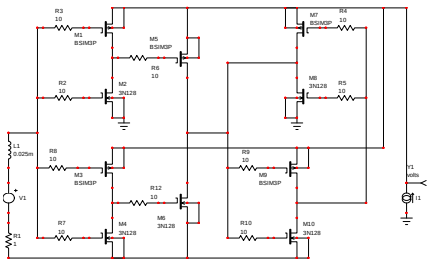

Fig. 2. The test circuit

in the VDD test.

In the damaged circuit, short circuit of transistor M4 was assumed. The Fig. 3 shows the change of the test signal from the damaged (solid line) and undamaged circuit (dashed line) when the IDD test is used. As can be seen the differences are too small to identify damage.

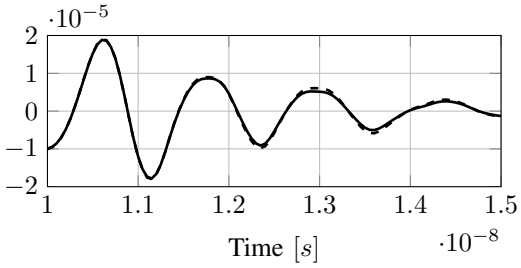

Fig. 3. 4th level detail of the supply current (IDD test)

When we apply the test VDD the signals allow the identification of the fault.

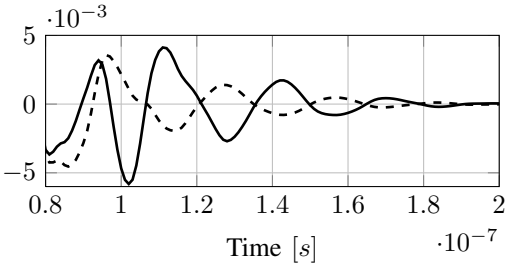

Fig. 4. 4th level detail of the supply voltage (VDD test)

IV. Acknowledgements

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