Multiple soft fault diagnosis of analog circuits using restart homotopy method

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Extended abstract

Abstract—**This paper offers a method for multiple soft fault diagnosis of nonlinear circuits containing bipolar and MOS transistors. The method enables us to locate faulty elements and evaluate their parameters, using a nonlinear algebraic type test equation which may possess several solutions. To find the solutions the homotopy concept is applied and a homotopy differential equation written. Next the terminal value problem is formulated and solved using the restart approach. A numerical example illustrates the proposed approach.**

Keywords—analog circuits, fault diagnosis, multiple soft fault, restart homotopy

This paper offers a method for multiple soft fault diagnosis of nonlinear circuits containing bipolar and MOS transistors.

Fault diagnosis of analog circuits is an important and still open problem for design validation of electronic devices [1]-[5]. If a faulty parameter is drifted from its tolerance range, but do not leads to some topological changes, the fault is said to be soft or parametric. The methods for soft fault diagnosis exploit simulation after test (SAT) approach, where circuit simulations take place after any testing. The test equation can be linearized if the parameters are slightly drifted from their tolerance ranges. If the parameter deviations are large the original nonlinear equation must be taken into account and solved using a dedicated method.

In this paper we consider multiple soft fault diagnosis of nonlinear DC circuits containing bipolar or MOS transistors characterized by the Gummel-Poon or the Shichman-Hodges model, respectively. Let n parameters $x_1, \ldots, x_n$ such as resistances, β forward factors of bipolar transistors, intrinsic transconductance parameter K_p and channel width/length (W/L) of MOS transistors be considered as possible faulty. We wish to locate these parameters and evaluate their actual values. For this purpose a diagnostic test is arranged, which leads to a set of nonlinear algebraic type equations. The set of nonlinear equations may actually possess multiple solutions. It means that several sets of the parameters $\{x_1, \ldots, x_n\}$ may meet the diagnostic test. Hence, a method which is capable of finding multiple solutions has

to be applied. The mentioned above problem has been solved in [4] using the homotopy approach and a sophisticated and difficult for implementation method for solving the algebraic homotopy equation. This paper offers a simpler method based on creation of homotopy differential equation and solving the terminal value problem, using the concept known in mathematics under the name restart approach [6].

SKETCH OF THE ALGORITHM

1. Perform the diagnostic test as in references [4], [5].
2. Formulate the homotopy equation

$$h(x, \lambda) = f(x) - u^{(0)} - \lambda(u - u^{(0)}) = 0, \qquad (1)$$

where $x = [x_1 \cdots x_n]^{\mathrm{T}}$ is a vector of the circuit parameters, $u^{(0)}$ is a vector of the output voltages for the nominal values of the parameters, λ is the homotopy parameter, u is a vector of the measured output voltages during the diagnostic test, $f(x) = [f_1(x) \cdots f_n(x)]^{\mathrm{T}}$ where $f_i(x)$, $i = 1, \ldots, n$, means a nonlinear function expressing i-th output voltage in terms of x. Function $f(x)$ in equation (1) is not given in explicit analytical form.

3. Formulate the homotopy differential equation on the basis of (1) and solve it using the restart homotopy approach [6]. As a result the homotopy path is traced and any intersection point of this path with the plane $\lambda = 1$ gives a vector of the parameters which satisfies the test. At any step of the procedure the DC analysis and the sensitivity analysis of the circuit are carried out for the actual values of the parameters.

The proposed method was implemented in DELPHI and tested using several circuits containing bipolar and MOS transistors. The calculations were executed on a computer with the processor Intel Core 2 Duo E6400, 3GB RAM. To illustrate effectiveness of the algorithm we consider a numerical example
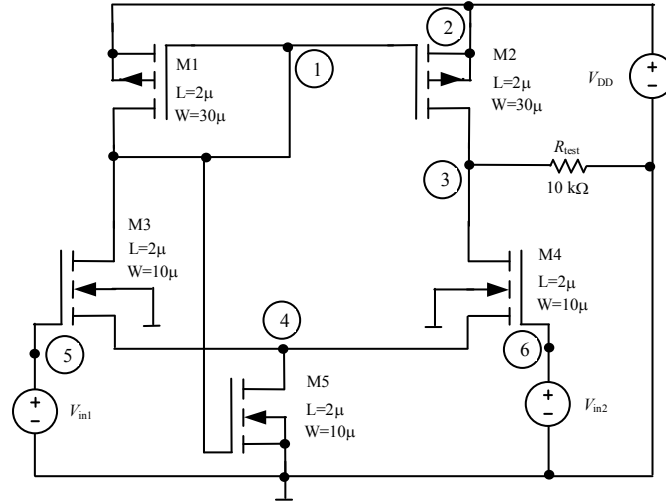
Fig. 1. Differential amplifier

Numerical example

Let us consider the differential amplifier shown in Fig. 1. To perform diagnostic test we connect the load resistance $R_{test} = 10\text{k}\Omega$. The channel width and length of all the transistors are indicated in Fig.1. The MOS transistors are characterized by the Shichman-Hodges model built up in Level 1 of SPICE. The nominal parameters of the MOS transistors are as follows: $\gamma = 0.6\,\text{V}^{0.5}$, $I_S = 10^{-14}\,\text{A}$, $K_p = 40\,\mu\text{A}/\text{V}^2$, $\varphi = 0.6\,\text{V}$, $R_D = R_S = 10\,\Omega$, $V_{to} = -0.90\,\text{V}$, $V_T = 25.86\text{mV}$, $R_{ds} = 1\cdot10^{12}\,\Omega$ for all PMOS, and $\gamma = 0.5\,\text{V}^{0.5}$, $I_S = 10^{-14}\,\text{A}$, $K_p = 120\,\mu\text{A}/\text{V}^2$, $\varphi = 0.6\,\text{V}$, $R_D = R_S = 10\,\Omega$, $V_{to} = 0.80\,\text{V}$, $V_T = 25.86\text{mV}$, $R_{ds} = 1\cdot10^{12}\,\Omega$ for all NMOS.

To perform the diagnostic test we choose the measurement nodes 1 and 3 and apply three sets of the voltages V_{in1}, V_{in2}, V_{DD}:

$$\{V_{in1} = 1.5, V_{in2} = 2.5, V_{DD} = 5.0\},$$

$$\{V_{in1} = 1.5, V_{in2} = 2.0, V_{DD} = 4.0\},$$

$$\{V_{in1} = 2.3, V_{in2} = 2.5, V_{DD} = 5.0\},$$

all in volts. We choose five of the measured voltages.

Case 1

At first we consider the intrinsic transconductance parameters K_p as possible faulty. The faults can be caused by deviation of the gate oxide thickness t_{ox} or the carrier mobility U_0. Let us consider the following values of K_p: $K_{PM1} = 37.0$, $K_{PM2} = 37.0$, $K_{PM3} = 123.0$, $K_{PM4} = 123.0$, $K_{PM5} = 170.0$, all in $\mu\text{A}/\text{V}^2$. The proposed method gives two sets of the parameters K_p, which meet the test, as follows:

$$\{36.93, 36.97, 122.90, 123.03, 170.38\}$$

and

$$\{195.85, 37.24, 651.46, 124.50, 608.69\}.$$

The first set contains the parameters very close to the actual ones, whereas the second is virtual. The time consumed by the method is 0.59 s.

Case 2

We consider the deviations of the channel width/length (W/L) as possible faulty: –4.54% for PMOS and –12% for NMOS transistors. Thus, the actual values of W/L of the transistors are:

$$\{14.32, \ 14.32, \ 4.400, \ 4.400, \ 4.400\}.$$

The proposed method gives one set of the parameters (W/L) which meets the test, as follows:

$$\{14.31, \ 14.31, \ 4.39, \ 4.39, \ 4.39\}.$$

The are very close to the actual values of the parameters. The time consumed by the method is 2.36s.

Numerical experiments including 30 cases show that the method never loses the correct solutions, leading either to only the correct solution (24 cases) or the correct solution and one virtual solution (6 cases).

REFERENCES

[1] G. Fedi, R. Giomi, A. Luchetta, S. Manetti, M.C. Piccirilli, "On the application of symbolic techniques to the multiple fault location in low testability analog circuits", *IEEE Trans. Cir. Syst. II.*, vol. 45 pp. 1383-1388, 1998.

[2] D. Gizopoulos (Ed.), Advances in electronic testing, Challanges and methodologies, Springer, 2006.

[3] M. Tadeusiewicz, S. Hałgas, M. Korzybski, "An algorithm for soft-fault diagnosis of linear and nonlinear circuits", *IEEE Trans. Cir. Syst. I.*, vol. 49, pp. 1648-1653, 2002.

[4] M. Tadeusiewicz, S. Hałgas, "Multiple soft fault diagnosis of nonlionear circuits using the continuation method", *Journal of Electronic Testing: Theory and Applications*, 28, pp. 487-493, 2012.

[5] M. Tadeusiewicz, S. Hałgas, "Global and local parametric diagnosis of analog short-channel CMOS circuits using homotopy-simplicial algorithm", *International Journal of Circuit Theory and Applications,* Published online in Wiley Online Library (wileyonlinelibrary.com), DOI: 10.1002/cta.1904, 2013.

[6] W.I. Zangwill, C.B. Garcia, Pathways to solutions, fixed points, and equilibria, Prentice-Hall, Inc., 1981.