Ročník 2013 electroscope Číslo V

Waffle MOS channel aspect ratio calculation with Schwarz-Christoffel transformation

P. Vacula [1,2], M. Husák, M.[1]
[1] Department of Microelectronics, Faculty of Electrical Engineering,Czech technical university in Prague , Technická 2, Prague 6, 16627, Czech Republic,
[2]STMicroelectronics s.r.o., Pobrezni 620/3, Prague
E-mail : vaculpat@fel.cvut.cz, husak@fel.cvut.cz

Abstract:
The main goal of this work is to describe alternative way of effective channel width to length (*W/L*) ratio calculation for Waffle MOS structure. Due to non-conventional gate geometry of the Waffle MOS transistor compare to the fingers structure, the channel *W/L* ratio calculation is not trivial and conformal mapping can be used. In terms of mapping the Schwarz-Christoffel (SC) Transformation is proposed. The optimal element shape of the Waffle MOS is proposed, to be easy solved by SC conformal mapping. Because result of the conformal mapping for the Waffle MOS element is rectangle shape in transformed domain, the solving of the effective channel *W/L* ratio of the element is become very easy because it is aspect ratio of rectangle in transformed domain.

INTRODUCTION OF WAFFLE MOS STRUCTURE

There are many reasons why this old approach Waffle MOS structure Fig. 1 should be in scope of interest even for actual processes and designs. Compare to classical fingers MOS structure the Waffle MOS is known due to 40 % lower resistance R_{on} [1]. Another not negligible advantages of this structure is lower source and drain capacitance [6]. And it was described that Waffle MOS structure in terms of under die stress induced by packaging are much better than fingers MOS structures [2].

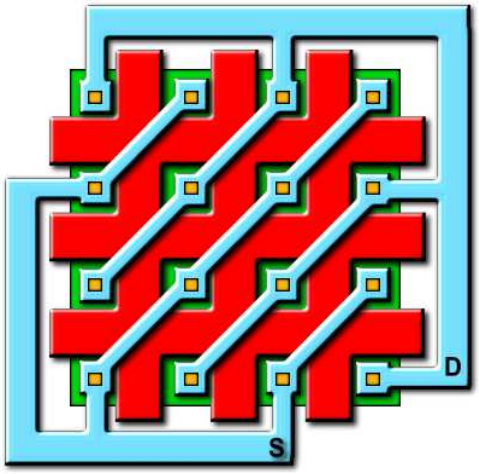

Fig. 1: Waffle MOS structure, active area (green), polysilicon gate electrode (red), contacts (yellow), metallic interconnection (blue),source electrode (S) , drain electrode (D) .

All of this is obtained without any process change. Because there is no need for extra cost due to additional process step we can implement Waffle MOS structure in almost all CMOS processes. All what is needed is just to change the pattern shape of the polysilicon gate electrode mainly. In addition there is need to change the contact and interconnection metallization for electrode source (S) and drain (D) also. In some processes diagonal metal interconnection routed at 45 degree should be problematic. In such cases alternative routing should be apply (Fig. 2) [9].

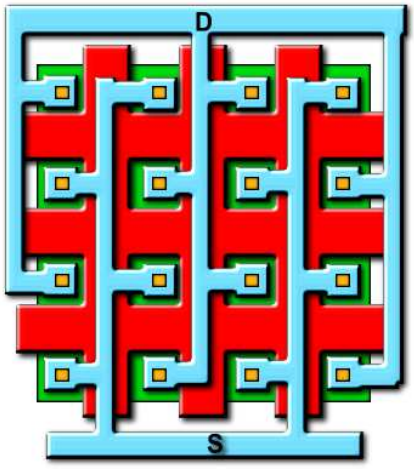

Fig. 2: Waffle MOS structure, with orthogonal metal interconnection routing.

As was mention in [1] several different layout schemes that are useful for implementing low resistance switches with MOS transistors was discussed and characterized. A comparison of the area required for implementing a switch with a standard alternating gate finger MOS (Fig. 3) approach was made with physical layouts using

waffle structures and serpentine structures. When designing low-resistance MOS switches, significant reduction in area was achievable by using Waffle structures. A reduction in area of over 40% was demonstrated for a typical process [1].
Base on [8] today's integrated DC-DC converters require low-voltage power devices with low on-resistance R_{on} and low gate charge Q_G to provide good power conversion efficiency. Since the conduction and switching losses are dependent on the on-resistance R_{on} and total gate charge Q_G, it is necessary to minimize both parasitic resistance and capacitance.

According to [2] common centroid geometries (or point symmetric) are recommended for optimum matching. However, these structures become increasingly complex for more than two transistors, with severe penalties in area. The interdigitated waffle (Fig. 2) and the quad (common centroid) transistor layout structures show no systematic mismatch, and the matching follows the well established linear relationship with the inverse of the transistor channel area. Under induced die stress due to packaging, the waffle and the quad (common centroid) is better because the finger style transistor pair shows a significant systematic mismatch, which is a function of its position in the die. The finger style transistor pair and the interdigitated finger structure show a mismatch up to 5 times higher than the value predicted by only considering random fluctuation of the channel area.

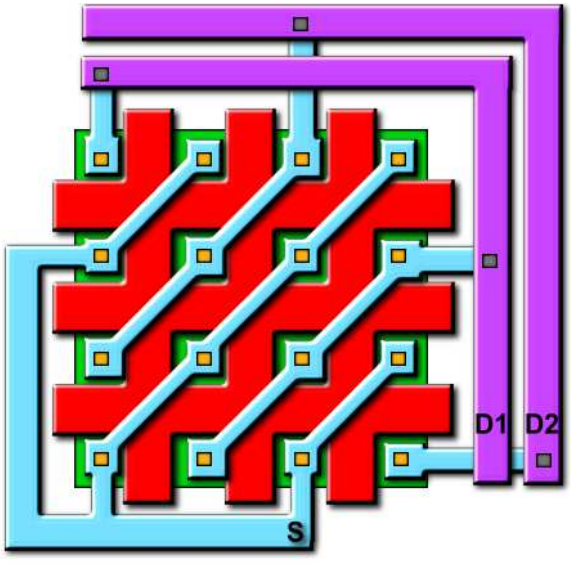

Fig. 3: Interdigitated Waffle MOS structure, active area (green), polysilicon gate electrode (red), contacts (yellow), first metallic interconnection (blue), second metallic interconnection (purple),source electrode (S) , first drain electrode (D1), second drain electrode (D2) .

On first look the interdigitated waffle and the quad (common centroid) transistor layout looks that they are almost same in terms of matching. But the interdigitated waffle has one main advantage. Because on same area we can reach smaller resistance compare to standard finger structure, on same area we can match transistors with larger effective channel width. Or alternatively we can match transistors with same effective channel width on smaller area.

In practice designer generally preferred to use finger structure as much as possible instead of Waffle structure. The main reason for that is that rectangular geometry of standard finger structure is convenient for layout, transistors should have sufficient density, are easy to reshape and for this device precise model have been developed [3]. To bypass one of this disadvantages the precise model of the Waffle MOS structure is requested.

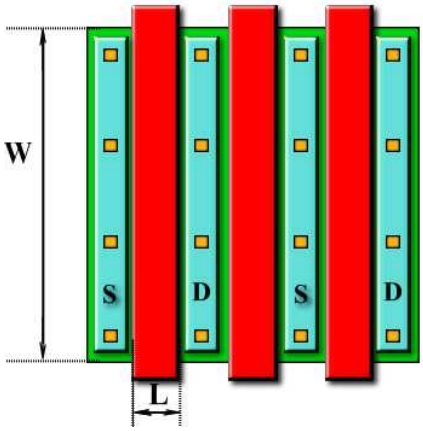

Fig. 4: MOSFET with rectangular shape of gate electrode with length of the channel *L* and width of the channel *W*, active area (green), polysilicon gate electrode (red), contacts (yellow), metallic interconnection (blue),source electrode (S) , drain electrode (D) .

Let's consider simple DC electrical model of the MOSFET (Fig. 4) with rectangular shape of gate electrode with length of the channel *L* and width of the channel *W* in saturation region without considering channel length parameter

$$I_D = \frac{\mu C_{OX}}{2}\frac{W}{L}(V_{GS} - V_T)^2 \qquad (1)$$

where I_D ,V_{GS} and V_T are drain current, gate to source voltage and threshold voltage. The μ is a charge-carrier effective mobility and C_{OX} is a gate oxide capacitance per unit area. The only one model parameter which depends on gate or channel shape geometry is width to length (*W/L*) ratio. For non-rectangular gate geometry the effective *W/L* ratio parameter should be considered.

$$I_D = \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)_{EF}(V_{GS} - V_T)^2 . \qquad (2)$$

The $(W/L)_{EF}$ represent effective *W/L* ratio of gate geometry. As we can see the precision of this parameter should have significant influence on total precision of electrical model of Waffle MOS structure. Due to this reason for precise model of the Waffle MOS structure the precise effective channel *W/L* ratio calculation is needed.

DESCRIPTION OF THE PROBLEM

When we look on Waffle MOS structure (Fig. 5) we should recognize and define two different types of channel areas.

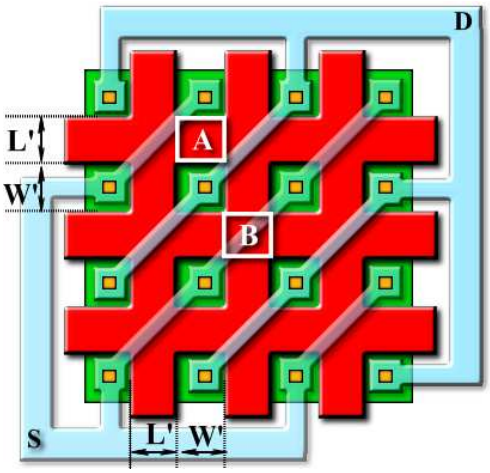

Fig. 5: Waffle MOS structure with defined areas of interest *A*, *B* and main dimension *W'* and *L'*.

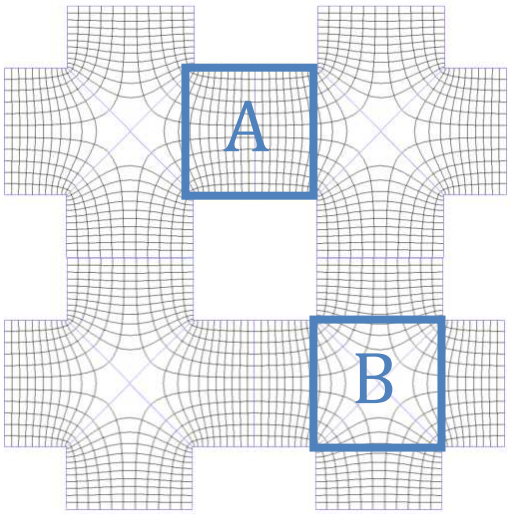

Fig. 6: Macro element with orthogonal mesh after SC transformation with defined areas of interest *A*, *B*.

The first area *A* type represent all channel areas where Source (S) and Drain (D) electrodes are located on two opposite sides of rectangle *A*. Those regions are with almost homogenous current distribution in channel area. And due to this effective *W/L* ratio for rectangle *A* is directly aspect ratio of rectangle *A*

$$\left(\frac{W}{L}\right)_A = \frac{W'}{L'} \qquad (3)$$

where *W'* is a width dimension and *L'* is length dimension of Waffle MOS.

The second area *B* type represent all channel areas where source (S) and drain (D) electrodes are located diagonally and due to this there is no homogenous current distribution. For such cases effective *W/L* ratio calculation is not trivial and conformal mapping can be used (Fig. 6).

SCHWARZ-CHRISTOFFEL TRANSFORMATION

The Schwarz-Christoffel (SC) approach to Laplace-related calculations on polygons has the virtue that unlike methods based on integral equations, finite differences, finite elements, or the superposition of particular solutions, it preserves the property inherent in the problem of having only a finite number of parameters. In particular it automatically obtains the correct singularities at corners. Because of this, the Schwarz-Christoffel method can achieve very high accuracy without much penalty in execution time. For low accuracy, other methods may be better. Its chief drawback is that it generalizes poorly to related problems involving more complicated differential equations (e.g. variable coefficients or nonzero right hand side) or geometries (e.g. curved boundaries or multiple connectivity) [4]. To fix this drawback method based on breaking the domain up into simple subpolygons is highly effective.

OPTIMAL ELEMENT SHAPE FOR SC TRANSFORMATION

Due to constraints that are related to SC transformation the choice of optimal element shape is very important. There are many shapes which should be considered as element pattern, as we can see on Fig. 7. But not all of them are simple enough to be easily solved by SC transformation. As was mention before one of the drawback of SC transformation is that it is not optimal for conformal mapping when polygon contains multiple connectivity on boundary. Due to this reason elements *F* and *G* are not well shaped. The optimal element shape *E* (Fig. 8) of the Waffle MOS is proposed, to be easily solved by SC conformal mapping.

Base on expectation that *W/L* ratio of area *B* type is independent on *W'* dimension and *L'* dimension we can scale element *E* freely as needed to simplify later calculation. Due to this in our case we

will scale element *E* to have *W'* dimension equal to *L'* dimension as follows

$$W' = L'. \qquad (4)$$

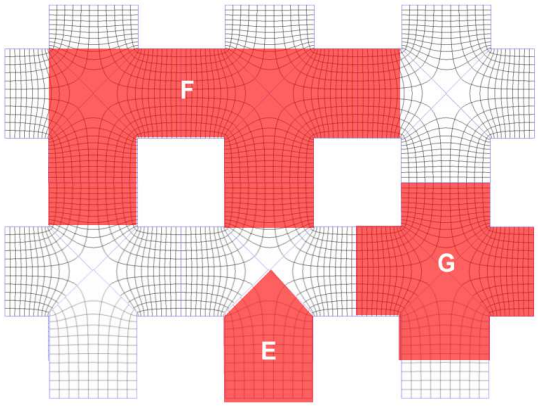

Fig. 7: Proposed elements *F*, *G* and *E* in Waffle MOS pattern.

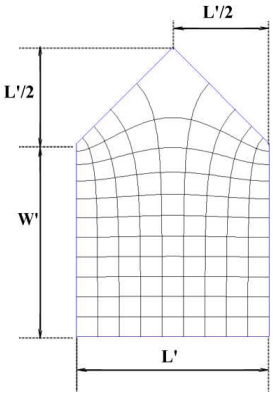

Fig. 8: Proposed element E with defined dimensions and containing conformal mapping mash.

SC TRANSFORMATION WITH ELEMENT *E*

The one way how to perform effective channel *W/L* ratio calculation is to constructing a conformal mapping onto a new domain where the problem is trivial. In our case that new domain should be a rectangle [4]. Base on Riemann mapping theorem we know that for any polygon exist mapping to open unit disk. The mapping from unit disk to any polygon is called Schwarz-Christoffel transformations [5]. The mapping *h* from W_1 plane to W_2 plane should be done as composition of two independent SC mapping as shown in Fig. 9. First is inverse SC mapping f^{-1} from element polygon *E* to the unit disk *P*. And second mapping is SC mapping *g* from unit disk *P* to rectangular polygon *Q* [4]

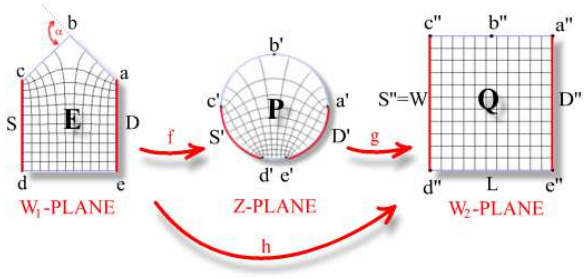

Fig. 9: Conformal map of a elementar polygon onto an equivalent rectangle.

$$f^{-1}(z) = K + C\int_0^z \prod_{k=1}^{5} (1 - w/z_k)^{-\beta_k}\, dw \qquad (5)$$

where *K* , *C* and z_k are unknown complex constants and $|z_k|=1$. The exponents β_k are associated with angles at k-th corners points in plane W_1 and

$$\beta_k = 1 - \frac{\alpha_k}{\pi} \qquad (6)$$

where α_k are exterior angels for points $z_k = \{a, b, c, d, e\}$ in plane W_1 and where $\beta_1 = \beta_3 = 3/4$, $\beta_2 = \beta_4 = \beta_5 = 1/2$.

The mapping *g* from unit disk *P* to rectangular polygon *Q* is

$$g(z) = \int_0^z [t(w)]^{-1/2}\, dw \qquad (7)$$

where

$$t(w) = (w - a')(w - c')(w - d')(w - e'). \qquad (8)$$

The constant *K*, *C* in equation (7) was skipped there because they have only influence on position and scale of the polygon and *W/L* ratio is invariant for them. To get effective *W/L* ratio of *Q* it is need to calculate just three points

$$\left(\frac{W}{L}\right)_Q = \frac{|g(e') - g(a')|}{|g(c') - g(a')|}. \qquad (9)$$

As was mention before the SC transformation is just mathematical construction allowing a conformal mapping of polygon *E* to polygon *Q* where problem is trivial. Due to this the *W/L* ratio of polygon *Q* is same as unknown effective *W/L* ratio of polygon *E*

$$\left(\frac{W}{L}\right)_E = \left(\frac{W}{L}\right)_Q. \qquad (10)$$

MATLAB CALCULATION

For solving of all above described nonlinear system of equations (5), (6), (7), (8), (9) the Matlab software with dedicated Schwarz-Christoffel Toolbox was used.

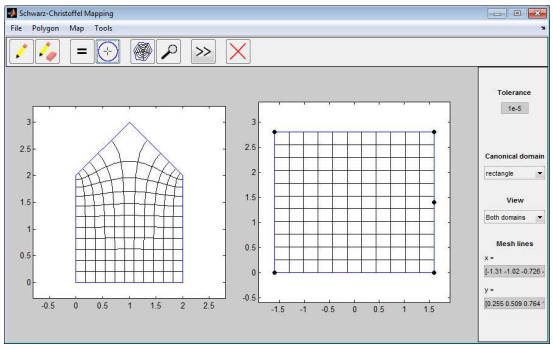

Fig. 10: Graphical User Interface of SC toolbox in Matlab environment.

The result for effective *W/L* ratio of region *E* is as follows

$$\left(\frac{W}{L}\right)_E = 1.1396783\,. \qquad (11)$$

After composition of four element *E* we should get macro-element as shown in Fig. 11. This macro-element contains four times area *A* type on the periphery and one area *B* type located in the center.

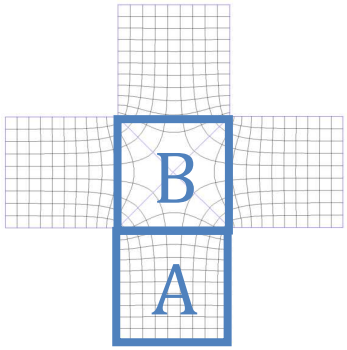

Fig. 11: Macro element with orthogonal mesh after SC transformation with area type *A* and *B*.

EFECTIVE W/L OF THE ELEMENT B

To have effective *W/L* ratio of element *B* it is needed to have effective *W/L* ratio for region *A* first. In the Fig. 11 we can see that element *A* is not exactly homogenous and contain some small no homogeneity close to the common boundary with element *B* type. To do not lose the high precision of *W/L* ratio reached for element *E*, all no homogeneity of region *A* will be shifted and calculated in already nonhomogeneous element *B* type. It means that we will consider element *A* type as fully homogenous. In our case where width dimension *W'* is equal to length dimension *L'* effective ratio is

$$\left(\frac{W}{L}\right)_A = \frac{W'}{L'} = \frac{|a-e|}{|e-d|} = \frac{L'}{L'} = 1\,. \qquad (12)$$

The effective *W/L* ratio for triangular subarea is

$$\left(\frac{W}{L}\right)_T = \left(\frac{W}{L}\right)_E - \left(\frac{W}{L}\right)_A = 0.1396783\,. \qquad (13)$$

The effective *W/L* ratio of element *B* is done as composition of *W/L* ratio of four triangular subareas

$$\left(\frac{W}{L}\right)_B = 4\cdot\left(\frac{W}{L}\right)_T = 0.55871 \pm 10^{-5}\,. \qquad (14)$$

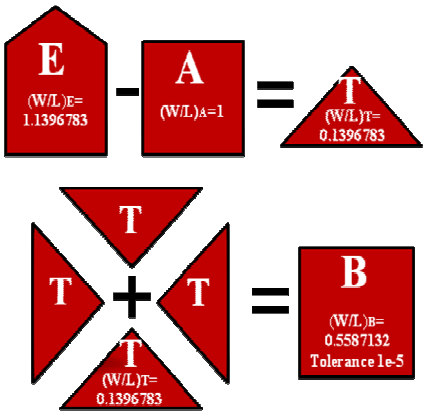

Fig. 12: The effective *W/L* of the element *E* is used to get unknown effective *W/L* of the element *B*.

Total Waffle MOS *W/L* ratio can be simply describe as the sum of *W/L* ratio of all elements type A and *W/L* ratio of all elements type *B*

$$\left(\frac{W}{L}\right)_{\text{WAFFLE}} = \sum_{i=1}^{N_A}\left(\frac{W}{L}\right)_{Ai} + \sum_{j=1}^{N_B}\left(\frac{W}{L}\right)_{Bj} \qquad (15)$$

where N_A is total quantity of element *A* type and N_B is total quantity of element *B* type. Described equation (15) even if is simple is not optimal in term of time needed for calculation. For big Waffle MOS structure there will be so many elements *A* and *B* to be summed. Due to this reason for more effective calculation new optimized equation will be needed. By knowing number of rows and columns of gate fingers we can calculate the total Waffle MOS *W/L* ratio as follows

$$\left(\frac{W}{L}\right)_{\text{WAFFLE}} = N_A\frac{W'}{L'} + N_B(0.55871) \qquad (16)$$

where total quantity of elements *A* type N_A is

$$N_A = N_R \cdot (N_C + 1) + N_C \cdot (N_R + 1) \ . \quad (17)$$

And finally the total quantity of element *B* type N_B is as follows

$$N_B = N_R \cdot N_C \quad (18)$$

where N_R is number of rows of gate fingers and N_C represent number of columns of gate fingers.

By knowing total effective *W/L* ratio of gate electrode of Waffle we can finally describe the simple DC electrical model of the Waffle MOS transistor as follows

$$I_{DWAFFLE} = \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)_{WAFFLE}(V_{GS} - V_T)^2 \quad (19)$$

where $I_{DWAFFLE}$ is drain current for whole Waffle MOS. The V_{GS} and V_T are, gate to source voltage and threshold voltage. The μ is a charge-carrier effective mobility and C_{OX} is a gate oxide capacitance per unit area.

After insertion of (16) to equation (19) we obtain

$$I_{DWAFFLE} = \frac{\mu C_{OX}}{2} \cdot \left(N_A \frac{W'}{L'} + N_B(0.55871)\right)(V_{GS} - V_T)^2 \quad (20)$$

CONCLUSION

For Waffle MOS transistor which is well known mainly due to lower Ron resistance the more precise model was proposed. This result was reached by more precise calculation of effective *W/L* ratio of gate channel region of Waffle MOS transistor. The total *W/L* channel ratio of the whole Waffle MOS is done as the sum of *W/L* ratio of all elements type A and *W/L* ratio of all elements type *B*.

The effective *W/L* channel ratio of the element *A* is directly aspect ratio of rectangle *A*. The effective *W/L* channel ratio of the element type *B* in Waffle MOS is 0.55871 with tolerance 10-5. It is much precise value than 0.55 described by Saqib [1].

The alternative solution to calculate the total *W/L* channel ratio of whole Waffle MOS from knowing quantity of rows and columns of gate fingers was proposed.

For further investigation the finite elements method in TCAD should be used to have additional more precise comparative result of effective *W/L* channel ratio of the element *B*.

ACKNOWLEDGMENTS

This work is part of the CTU SGS grant No. SGS11/156/OHK3/3T/13, (RISMiNO).

REFERENCES

[1] Saqib Q. Malik, Randall L. Geiger, Minimization of Area in Low-Resistance MOS Switches, Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium. 2000, pp. 1392 - 1395.

[2] J. Bastos, M. Steyaert, B. Graindourze, W. Sansen, Matching of MOS Transistors with Different Layout Styles, IEEE International Conference on Digital Object Identifier, 1996 ,pp. 17-18.

[3] P. Grignoux and R. L. Geiger, Modeling of MOS transistors with nonrectangular-gate geometries, IEEE Trans. on Electron Devices, Vol 29,August 1982, pp.1261-1269.Name, A, Name, L. at al. Diagnostics of insulation. Place, Publisher, 1984, 256 p.

[4] Lloyd N. Trefethen, Analysis and design of polygonal resistors by conformal mapping. Massachusetts Institute of Technology, Cambridge, Vol. 35, September 1984.

[5] Koepf W., Schwarz-Christoffel mapping: Symbolic computation of mapping function for symmetric polygonal domains, Fachbereich Mathematic, Freie Universitat Berlin, Vol. 13

[6] Maloberti F.; Layout of Analog CMOS Integrated Circuit,

[7] P.Vacula, V. Michal, M. Thomas, M. Husák, Waffle MOS channel W/L calculation with Schwarz-Christoffel transformation ,,STEricsson, Department of Microelectronics, Faculty of Electrical Engineering, IMAPS June 2013 .

[8] A. Yoo, M. Chang, O. Trescases, W. Tung Ng, High Performance Low-Voltage Power MOSFETs with Hybrid Waffle Layout Structure in a 0.25µm Standard CMOS Process, Material Science and Engineering, University of Toronto, 184 College Street, Toronto, ON, Canada, Electrical and Computer Engineering, University of Toronto, 10 King's College Road, Toronto, ON, Canada

[9] S. Madhyastha.; Design of circuit breakers for large area CMOS VLSI circuits, Department of Electrical Engineering McGill University, September 1989