

## PROPERTIES OF 3D LTCC STRUCTURE INTERCONNECTIONS

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### Abstract:

This paper describes design, construction and some recent tests of 3D stacked lead-free soldered structures based on Low Temperature Co-fired Ceramic substrates (LTCC). These structures have a great potential to create compact structure combining multiple different modules in one package. Internal connections used in these 3D structures have an important role, because they not only provide electrical and signal connection, but they also present mechanical attachment between connected substrates. Goal of this work is to develop, simulate and evaluate new structures based on interesting “zero shrink” Heraeus HL2000 LTCC substrates, where dimples help to reduce thermo-mechanical stress and pads modified with copper to reduce problems with leaching.

### INTRODUCTION

Three dimensional structures present way to find better ways to implement more and more complicated systems in smaller, compact and complex packages. This needs to be achieved because miniaturization and densification of electronic interconnections are the inevitable future of packaging and also the whole microelectronic world.

This project is linked to previous research of soldered 3D structures containing “dimpled LTCC substrates”, which was in its early stage presented on MSMF6 [2], ISSE and EMPC [3] international conferences. Main goal of this work is to develop methods for design and implementation of lead-free soldered stacked 3D packages based mainly on interesting “zero-shrink” Heraeus HL2000 HeraLock Low Temperature Co-fired Ceramic substrates.

HL2000 LTCC substrate provides many construction options because of its unique parameters. The “zero-shrink” means that these substrates have almost zero shrinkage in x and y axes during firing process. Material shrinks only in z axis (thickness of material is reduced) by about 30%. This means much easier structure design and also manufacturing process when compared to other known LTCC materials reducing their dimensions in all axes significantly and mostly with different ratio in different axes. The main advantage speaking for of LTCC material is of course the possibility of machining raw ceramic material into desired shape before firing. Even low power pulse YAG trimming LASER can be used for precise cutting and drilling with this material, which is incomparably easier than machining of alumina substrate usually used for thick film structures. On the other hand there are also few disadvantages. For example the thickness of one tape is only 100um and one layer after firing is extremely fragile. Because of this usually at least three or four layers must be laminated and fired together to improve mechanical

parameters and to ensure satisfactory sturdiness of one final substrate.

Another issue is the lack of wide variety of thick-film co-fireable pastes for these substrates. Heraeus provide only the basic selection of conductive pastes and internal via fills. For example there is only compatible paste that can be used to create solderable contact pads. It's the TC0306 silver-based conductor paste. But the problem is that significant leaching occurs during soldering and repeated reflow almost completely removes contact pads. Other standard co-fireable silver-based pastes like for example from ESL range are incompatible and their behavior during firing is unpredictable. Also other big issue is that there is currently no dedicated resistive paste available for this substrate too. Fortunately, workaround is possible there. The final structure surface can be modified by the use of one layer of different Heraeus/Kerafol shrinkable LTCC CT800 green tape, which can carry compatible resistive co-fireable pastes. Other way is to incorporate SMT resistors in surface cavities and solder them in final structure.

Mentioned issues bring some difficulties when 3D structures are created, however there are design methods available to reduce leaching problem and also help to reduce thermo-mechanical stress in soldered HL2000 LTCC structure. Particularly substrate dimples and contact pads modified with copper layers, which are described in this article.

### EXPERIMENT SETUP – SUBSTRATES

As first step the test substrates layout were designed. The test pattern is inspired by standardized BGA test dummy packages. It uses doubled daisy-chain circuit with 64 soldering pads interconnected by wires. Each pad has 0.6 mm in diameter and pitch (center-to-center distance) is 2.54 mm (two times the standard

1.27 mm). Wiring is 0.3 mm wide. Base substrate circuit also provides connections for electrical tests. Design of test substrate is shown on figure 1.

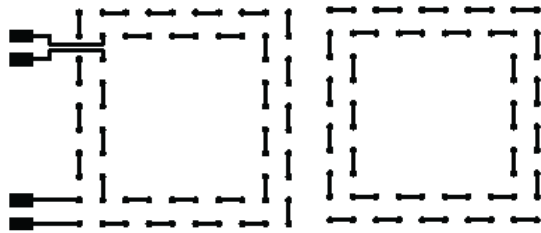


Fig. 1: Design of test substrate showing base part (left) and first stage (right)

Each substrate consists of three or four HL2000 substrates laminated together. At least two layers of tape are used as a base body which supports the screen-printed TC0306 conductive solderable Ag paste. For screen printing the 350 mesh screen is used. Then another layer, which contains 64 laser-drilled holes with diameter of 0.7 mm, covers the entire structure from above. Precise alignment is needed during this operation. When substrate structure is assembled, the lamination process follows.

Substrates are placed in tempered hydraulic axial press and laminated together. Planar steel press template with alignment pins supporting substrates during process is used, because as temperature increases, LTCC material becomes to be quite soft. Process parameters are: pressure 1500 psi and temperature 70°C for 10 minutes. Heated layers pressed together form one compact layer. The second figure shows an example of assembled substrates during lamination process.

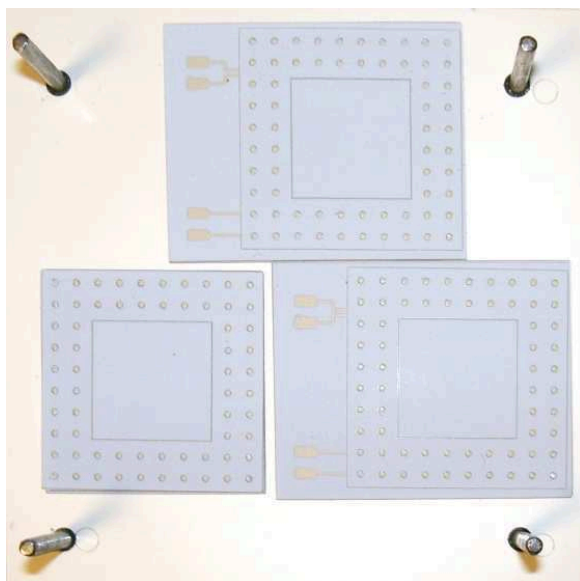


Fig. 2: Laminated substrates before firing

On this picture there are two base substrates and one “package” device displayed. Sheets of white anti-adhesive plastic are used to separate LTCC from metal.

After lamination process, substrates are fired in box furnace with 12 hours profile peaking at 865°C after long pre-heating part. Cooling is also important and usually takes about two hours.

## SOLDERING PADS MODIFIED BY COPPER

When substrate is fired it has to pass initial inspection, where substrate flatness and pad surfaces are examined. If substrate meets expectations then the modification of soldering pads begin. There are two possible setups. First one creates only a sub 1 μm thin Cu cover layer over Ag pad, which enhances wettability, solderability and slightly reduces leaching issues. The second setup creates thicker Cu layer which has 20 μm. This adds improvement in thermo-mechanical stability to results achieved by first setup. Thin copper cover is created using physical vapor deposition process, where cleaned substrate is coupled with 100um Cu alloy foil stencil, which leaves openings with 0.8 mm diameter for contact pads. Substrates with stencils are then covered by 0.5 μm of very clean copper coating. OSP film is then recommended to protect pads from humidity and dust causing fast corrosion. After process the substrates are ready for soldering.

Thicker copper cover utilizes galvanic principle to enhance thickness of final copper layer. At first the whole substrate has to be perfectly cleaned and without any grease or dust particles. During PVD process the substrate is covered by thin Cu layer, which must provide enough electrical conductivity needed in next steps. Measured corner to corner resistivity has to be less than 1 Ohm.

When substrate surface is covered by copper, application of solid photo resistive film follows. Entire surface is covered by photoresist and only small windows corresponding to dimples with pads are opened by photo-development process.

In next step the galvanic process using copper sulfate with sulfuric acid is performed. Five minutes and 0.4 A current are both needed to create layer 20 μm thick. At the end the photoresist is stripped down and desired pattern is revealed.

## SOLDERING EXPERIMENTS

Three types of solder balls were used during soldering process. The main batch was soldered using Senju lead-free SAC305 (96.5% Sn, 3% Ag and 0.5% Cu) type with 0.76 mm in diameter. Alternatively two types of solid-core balls were tested as they are able to provide and hold uniform gap between connected substrates. The first were the 0.76 mm Sekisui SOL balls with divinylbenzene core covered with thin Cu layer and lead-free solder alloy. The second type balls

were 0.64 mm Senju Sparkle Ball C with 0.56 mm copper core covered by lead-free solder alloy. Balls were placed between two stencil-printed 100µm thick layers of SAC3-XF3 Cobar solder paste (SAC305). Structures were then assembled together with the use of FRITSCHE Mikro-placer rework station, where both upper and lower patterns can easily be matched to have the same orientation. Position of each pad on upper surface covered with solder paste then exactly matches position of lower pad, where solder ball is sitting on printed layer of solder paste.

Whole structures assembled together were then reflowed in vapor-phase laboratory oven Asscon Quicky 300, where in Galden-240 vapors uniform temperature across soldered structure and almost inert atmosphere with reduced oxygen content are present. This helps to minimize solder oxidation during reflow process and ensures optimal heat transfer.

## RESULTS OF SOLDERING EXPERIMENTS

Several test groups of soldered structures were completed during experimental part and research still continues with many modifications.

Soldered structures were inspected by various methods. The daisy chain pattern provides the easiest way to check if structure is conductive. Then a close optical inspection using BGA test station Ersascope was performed utilizing its unique ability to look under package and to check internal solder joints. The Ersascope detailed view of one of soldered joints can be seen on figure 3.

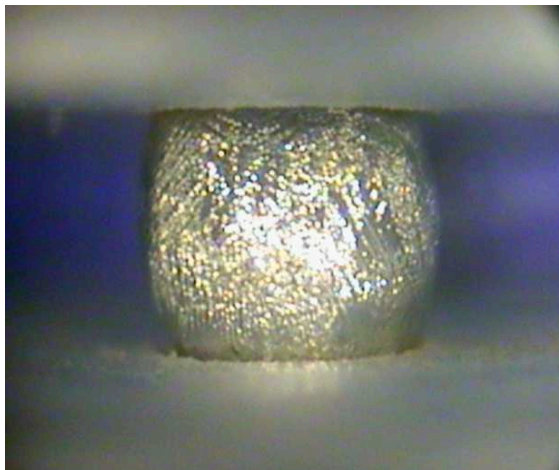


Fig. 3: Close-up detail of solder joint created between two dimpled LTCC substrates

To check internal structure of solder joints closely many cross sections of several soldered structures were made. On figure 4 there is a clearly visible solder joint between two dimpled substrates. Also conductive layers of Ag co-fireable paste are visible in LTCC structure.

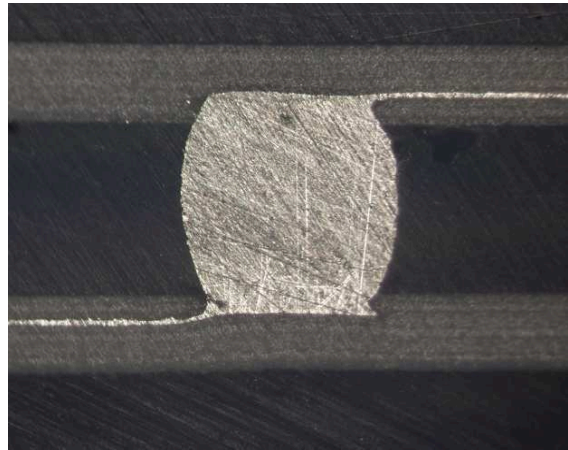


Fig. 4: Detail of microsection of solder joint between two dimpled LTCC substrates

It can be seen, that the solder completely filled both cavities, wetting was good thanks to thin Cu film and there are also serious no voids or cracks.

As it was mentioned before, solid core balls were also tested in recent experiments.

Next micro section depicted on figure 5 shows the Sekisui SOL spheres. The plastic core covered by copper layer is perfectly visible inside solder joint. Also the daisy-chain structure of connected substrates is well visible in LTCC layer structure. Solder joints created with these solid core balls show well-defined joint height, but it is obvious, that these balls tend to float in molten alloy which results in partly exposed copper skin of spheres in some joints.



Fig. 5: Micro sections of solder joints with Sekisui SOL balls

The second type of solid-core balls used was the Senju Sparkle Balls with copper core. These balls also exhibited some floating in molten solder alloy, but their core was not completely exposed on any soldered joint. The micro section on figure 6 shows mentioned behavior. Notable is the small difference in ball core size in joint between Cu and plastic. This is caused because both solid-core solder balls are quite hard to acquire in smaller amount for testing purposes in required diameter.

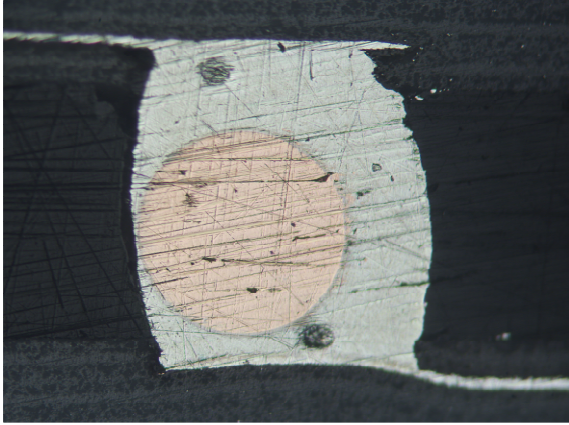


Fig. 6: Micro sections of solder joints with copper-cored Senju Sparkle Ball C

## ESTIMATION OF RELIABILITY

To estimate thermo-mechanical stress and reliability of interconnections, several processes are used. Structures are tested in thermal chamber, which in connection with micro sections helps to detect cracks and areas damaged by stress. This is especially important for outer interconnections, where substrates from materials other than LTCC are connected. Figure 7 shows detail of crack taken by scanning electron microscope. Cracks like this can be easily found in joint between solder ball (upper part of image) and silver pad when ceramic package board without dimples is connected to another board with different coefficient of thermal expansion.

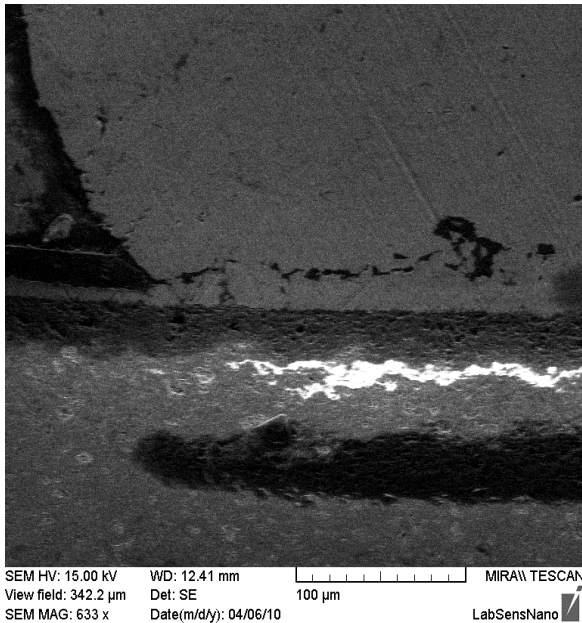


Fig. 7: SEM image of crack in solder joint between solder ball and ceramic substrate

Different coefficients of thermal expansion induce a lot of unwanted stress, when whole soldered structure

is tested in thermal chamber, where temperature cycles between  $-20^{\circ}\text{C}$  and  $+100^{\circ}\text{C}$  in 45 minutes. Thermal cycling tests of course take several months to cover relevant cycle-count, so we decided to speed-up the initial evaluations of reliability using powerful ANSYS simulation software. For comparison figure 8 shows standard ball shaped solder joint created without dimple on plain silver pad printed on ceramic substrate.

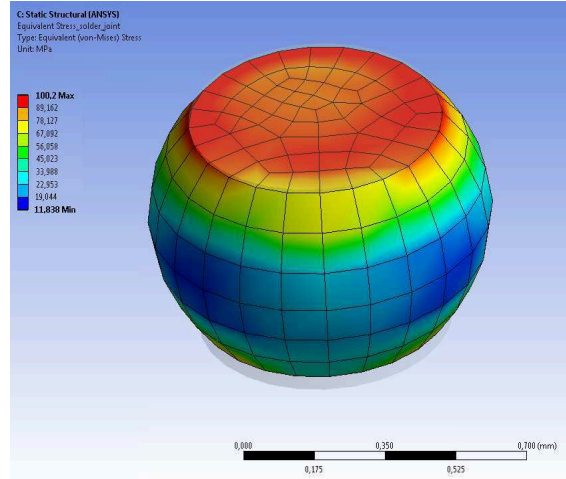


Fig. 8: Thermo-mechanical stress in standard ball shaped solder joints

On the other hand figure 9 shows solder joint created with dimpled structure in LTCC. The difference in thermo-mechanical stress is quite obvious. The dimple acts here like small stress buffer and also lengthens the solder joint area affected by stress forces.

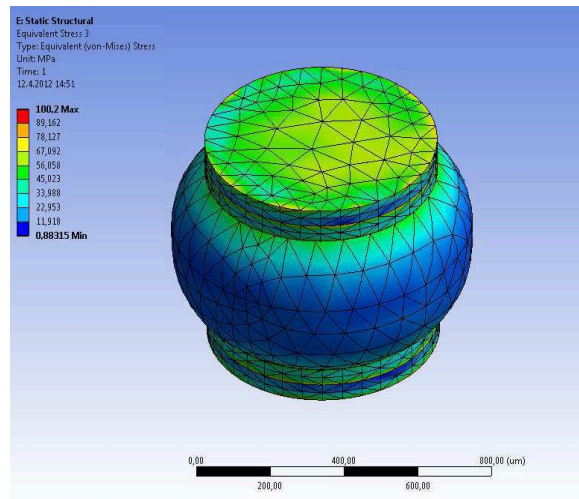


Fig. 9: Thermo-mechanical stress in dimpled structure solder joints

## CONCLUSION

Research of mentioned structures still continues and already shows the possibility of building 3D stacked and interconnected package multi-substrate structures using quite new and not widely used Heraeus HL2000 LTCC substrates. In simulations and early tests the dimpled structures show that they can help to reduce thermo-mechanical stress problems. This means, that these interconnections should be also able to connect final ceramic packages not only to other ceramic substrates, but also to organic (FR-4) or plastic (polyimide) substrates. An example scheme of dimpled structure combined with FR-4 substrate can be found on following figure 10.

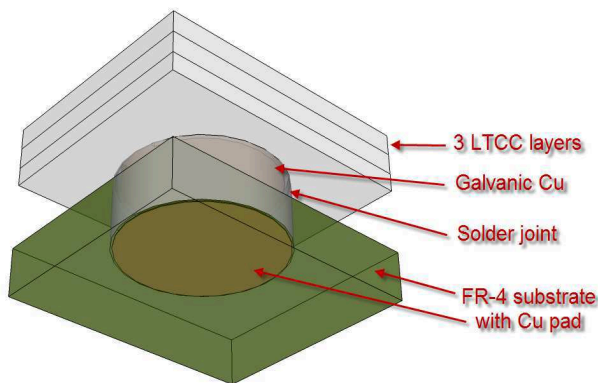


Fig. 10: 3D model of dimpled structure combined with organic FR-4 printed circuit board

These 3D stacked structures can combine the ceramic's advantages of thermal, insulating and mechanical properties with other substrates in one compact interconnected package.

Pads modified by copper thin layer show improved wetting. Created solder joints are more stable, as dangerous leaching on silver pads during reflow is significantly reduced.

Still there are many tests waiting to be performed. Plan contains tests of different solder alloys, alternative co-fireable materials, combinations of other LTCC substrates and extended thermal cycling tests with detailed evaluation. Intermetallic structures created in mentioned interconnections will also be interesting theme for further research.

## ACKNOWLEDGMENTS

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## REFERENCES

- [1] Kangasvieri, T.: Surface-mountable LTCC-SIP module approach for reliable RF and millimetre-wave packaging, University of Oulu, Tampere, Finland, 2008, ISBN 978-951-42-8921-7
- [2] Nicák, M., Švecová, O., Šandera, J., Pulec J., Szendiuch, I.: Reliability and Simulation of Lead-Free Solder Joint Behavior in 3D Packaging Structure, Key Engineering Materials Vol. 465, 2011, Switzerland: Trans Tech Publications, 2011. s. 491-494, ISSN 1013-9826
- [3] Nicák, M.; Šandera, J.: 3D LTCC and Flexible Structure Interconnections Based on Galvanized Layers. In Proceedings of 18th European microelectronics packaging conference EMPC 2011. Brighton, UK: IMAPS - Europe, 2011. s. 358-361. ISBN: 978-0-9568086-0- 8.
- [4] Lautzenhiser, F., Amaya, E.: HeraLock™ 2000 Self-constrained LTCC Tape, p. 43-49, Proceedings of the 2002 International Conference on Advanced Packaging and Systems (ICAPS), Reno, Nevada, March 12-13, 2002
- [5] Lautzenhiser, F., Amaya, E., Barnwell, P., Wood, J.: Microwave module design with HeraLock™ HL2000 LTCC, Proceedings of IMAPS 2002, Denver, USA, ISBN 0-930815-66-1