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Asymmetrical Nine-level Inverter Topology with Reduce Power Semicondutor Devices

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Abstract

In this paper a new single-phase multilevel inverter topology is presented. Proposed topology is capable of producing nine-level output voltage with reduce device counts. It can be achieved by arranging available switches and dc sources in a fashion such that the maximum combination of addition and subtraction of the input dc sources can be obtained. To verify the viability of the proposed topology, the circuit model is developed and simulated in Matlab-Simulink software. Experimental testing results of the proposed nine-level inverter topology, developed in the laboratory, are presented. A low frequency switching strategy is employed in this work. The results show that the proposed topology is capable to produce a nine-level output voltage, capable in handling inductive load and yields acceptable harmonic distortion content.

Keywords*: multilevel inverter, reduced components, topology, polarity changer*

1. Introduction

Power conversion is the key technology in a modern power set-up of generation, distribution, transmission and utilization of electric power [1-2]. Unlike several decades ago, the electrical power can be generated and harvested from diverse sources, namely fuel cells, photovoltaic, tidal, Microbiology activities, batteries, wind, ultra-capacitor and its [3]. These sources of energy produce unregulated power which may not suitable for industrial and home appliances. Hence, efficient power converter i.e. rectifier, dc-dc converter and inverter is required to form and regulate the power. The conversion is done by means of controlling the switching of the power semiconductor of the converters. For sources that produce dc power i.e. photovoltaic, batteries, ultra-capacitors and fuel cells, an inverter is required to convert it into ac power.

Full-bridge inverter is a common inverter topology used in the industries. It is used in diverse application such as uninterruptable power supplies (UPS), active power filter (APF), smart grid and etc. The popularity is due to its simple layout and flexibility in control [4]. For high power applications, however, the topology is no longer suitable due to the reliability issue [5]. The voltage stress across the power semiconductors is high. Moreover, the current draw by this converter is highly distorted. Since most of the inverter is pulse width modulation (PWM) based switching, the *dv/dt* can be very high which translated to high electromagnetic interference [6].

In order to alleviate this problem, multilevel inverter (MLI) is proposed. The first topology of MLI has been proposed and patented in 1975 by Baker and Banister [7]. It is a string of full-bridge inverters that connected in cascaded fashion. The concept of MLI is to produce high voltage required by the load, but at the same time reduced the voltage stress across the power switches [8-11]. The output is the staircase waveform of a sinusoidal voltage waveform synthesized from the dc source of each full bridge inverters [12-14].

It is known that higher level of output voltage will provide cleaner sinusoidal waveform. Hence, the design of the filter can be less burden. For MLI, the number of levels is related to the number of power switches used [15-17]. If the number of levels is increased, the number of power switches will also be increased. For example, in cascaded MLI, if the required number of levels is N= 5, then the number of switches can be calculated as 2 (N -1) = 8. Therefore, if the required number of levels is N = 9, then the number of power switches is 2 (N – 1) = 16. The

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increment is in exponential pattern. The same case goes to other conventional MLI namely the Neutral Point Clamp (NPC) [18] and Flying Capacitor (FC) MLI [19].

The exponential increment in the number of power switches and component count to obtain the higher number of levels is the down side of the conventional MLI. Progress on developing a new MLI topology with high number of levels, but reduced number of component count is active and is still carried out [20-29]. Referring to the previous researchers, the MLI topologies with reduced number of component count can be categorized under two, namely the topologies with H-bridge or without H-bridge. Commonly H- Bridge is used to solely to function as polarity change. Their merits and downside has been thoroughly discussed in [15].

In this paper a new MLI topology is proposed that is capable to produce nine-level output voltage with reduce component counts. The idea is to arrange available switches and dc sources in a fashion such that the maximum combination of addition and subtraction of the input dc sources can achieve. To verify the design, the circuit is developed via Matlab simulation tool. Simulation results are recorded to analyze the performance of the circuit. This paper is organized in different sections. In Section 2, circuit configuration of the proposed topology and switching pulses pattern is discussed. Then its operation in different modes is explained. Section 3 deals with the comparative study of the proposed topology with other existing topologies. Circuit parameters and results are discussed in section 4 followed by a conclusion.

2. The Proposed Multilevel Inverter

2.1. Circuit Description

Figure 1 shows the schematic circuit topology of the proposed nine levels asymmetrical multilevel inverter. It consists of two parts i.e. Level generator and polarity changer (H- Bridge). The level generator produces different output levels by connecting available dc sources through switches in different arrangements. The polarity changer converts the output of the level generator into alternating voltage. Proposed topology requires nine switches and two asymmetrical dc sources, defined as V1 and V2. Switches S1 − S5 are for level generator circuit and four switches i.e. Sa1, Sa2, Sb1 and Sb2 for H-Bridge.

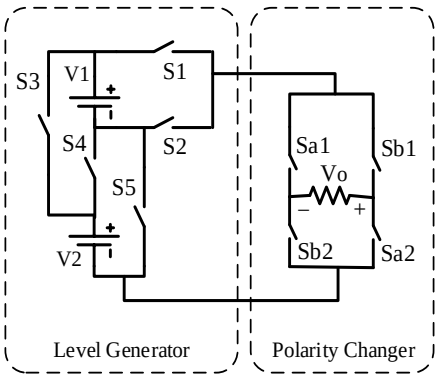


Figure 1. Proposed nine-level inverter circuit topology

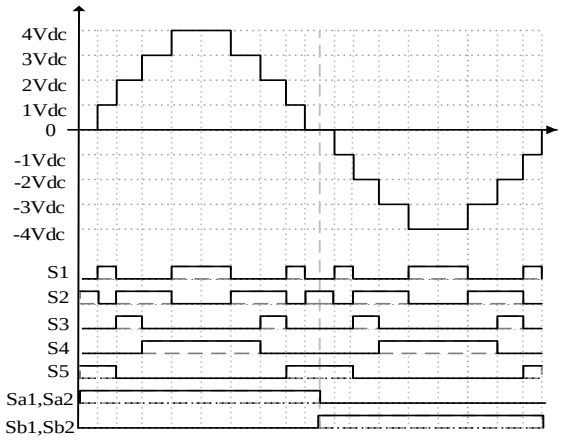


Figure 2. Switching pulses pattern for one complete cycle of the proposed nine-level inverter

Asymmetrical dc sources are independent of each other and are in ratio of V1:V2 = 1:3. In order to prevent the short circuit of the sources, simultaneous conduction of the switches (S1, S2), (S3, S4), (S4, S5), (Sa1, Sb1), (Sa2, Sb2) must be avoided. This can be done by proper switching of the switches. Figure 2 shows the switching pulses for one complete cycle. All the switches operate at low frequency. The conduction period is short for all switches except the polarity changer switches. Hence, it envisages that the power losses in the circuit are reduced significantly.

2.2. Modes of Operation

Figure 3 shows different modes of operation in the positive half cycle of the proposed topology. The path follows by the current for different modes is indicated with the thicker line. For one complete cycle, the circuit will be operated in nine different modes i.e. four for positive half cycle, four for negative half cycle and one mode for zero level. In this way, each mode is responsible for generating one output voltage level. Switching states of the switches, the magnitude of the output voltage in per unit and path followed by the current in each mode is tabulated in Table 1. Modes I(a)-IV(a), positive cycle modes, produces positive output levels and Modes I(b)-IV(d), negative cycle modes, produces negative output levels. It is evident from the table that switching sequence of the switches S1−S5 is same in both the half cycle. Whereas the switches (Sa1, Sa2) and (Sb1, Sb2) conducts only during positive half and negative half cycle respectively.

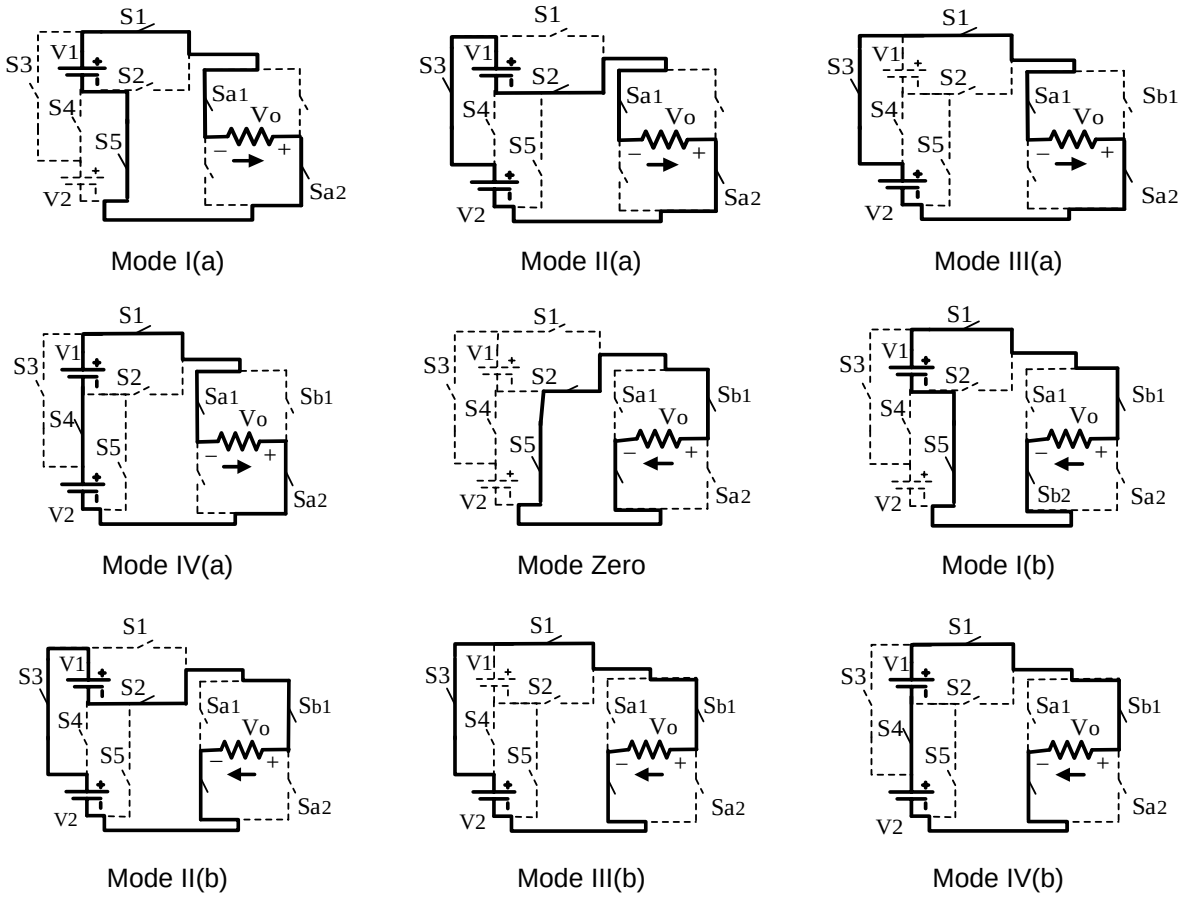


Figure 3. Different Switching state of the proposed nine-level inverter topology during positive half cycle

Table 1. Modes of Operation: Switching sequence, current path and output voltage

Modes	Switching Sequence (ON Switches) *Level Generator*	*Polarity Changer*	Current Path	Output Volt. (per unit)
I (a)	S1, S5	Sa1, Sa2	S5–V1–S1–Sa1–Sa2	1V
II (a)	S2, S3	Sa1, Sa2	V2–S3–V1–S2–Sa1–Sa2	2V
III (a)	S2, S4	Sa1, Sa2	V2–S4–S2– Sa1–Sa2	3V
IV (a)	S1, S4	Sa1, Sa2	V2–S4–V1–S1–Sa1–Sa2	4V
Zero	S2, S5	Sa1, Sa2	Sa1–Voutput –Sa2	0
Zero	S2, S5	Sb1, Sb2	Sb1–Voutput –Sb2	0
I (b)	S1, S5	Sb1, Sb2	S5–V1–S1–Sb1–Sb2	-1V
II (b)	S2, S3	Sb1, Sb2	V2–S3–V1–S2–Sb1–Sb2	-2V
III (b)	S2, S4	Sb1, Sb2	V2–S4–S2– Sb1–Sb2	-3V
IV (b)	S1, S4	Sb1, Sb2	V2–S4–V1–S1–Sb1–Sb2	-4V

3. Comparison with Other Topologies

Comparative study, based on the number of switches, diodes, dc links and total component count, of the proposed topology with other existing topologies for nine-level output is carried out and the results are tabulated in Table 2. The other compared topologies includes: conventional cascaded H-bridge (CHB), Neutral Point Capacitor (NPC), Fly-Capacitor (FC), asymmetrical CHB and the topologies presented in [17] and [28].

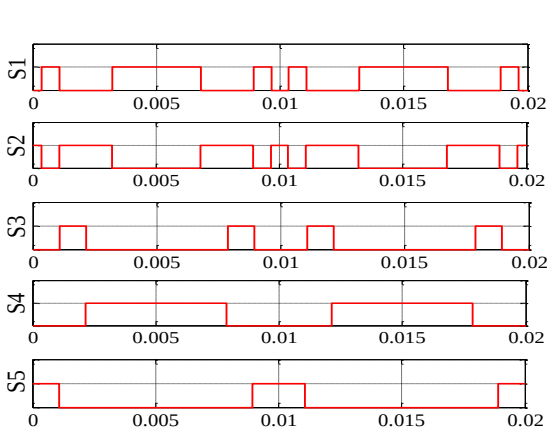
In [17], an asymmetrical multilevel inverter is proposed with reduce device count. For nine level output, it utilizes 12 switches including two bidirectional switches (counted as four switches) and 2 dc sources, which are lesser in than required by other conventional CHB, NPC and FC inverters. However, asymmetrical CHB inverter with tertiary source combination requires only two dc sources and eight switches with auxiliary diodes. In [28], a new asymmetrical inverter topology is with reduce device count is presented. Proposed nine level inverter also requires two dc sources, but number of auxiliary diodes reduces to four as the remaining switches are unidirectional. Number of components require by the proposed topology is 15 which is a lowest number than other comparable topologies. As the number of device count increases reliability decreases and the cost, losses as well as complexity in the circuit increases. Therefore, the proposed inverter depicts better performance than other topologies.

Table 2. Comparison of conventional and some existing asymmetrical inverter topology

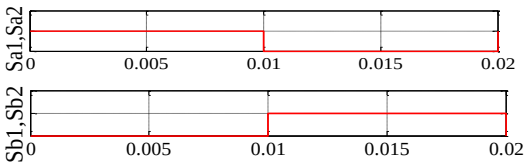
			CHB				
No. of	NPC	FC	*Urinary*	*Tertiary*	[17]	[28]	Proposed
Switches	16	16	16	8	12	10	9
Diodes	9	16	16	8	12	10	4
DC Links	4	7	4	2	4	2	2
Total	29	42	36	18	28	22	15

4. Results and Analysis

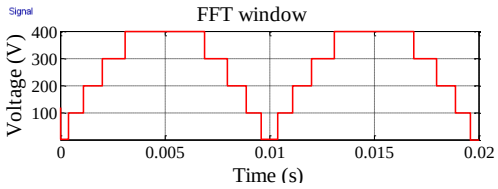
To verify the performance of the proposed topology, simulation model based on Figure 1 is developed in Matlab-Simulink software. Circuit is simulated at a fundamental frequency of 50Hz. In order to obtain a ternary source arrangement with maximum output of 400V, the value of the DC sources are taken as V_1 =100V and V_2=300V. The inverter is operated in open loop mode and different load conditions (R and RL load) are assumed. Fundamental frequency switching control modulation scheme has been used [1]. In this scheme of modulation, the reference signal is a sinusoidal voltage waveform which is compared with the available dc levels. Level close to reference is chosen. As this is a low switching frequency method [29]. This method leads to lower switching losses.



(a) Switching Pulses for level-generator switches



(b) Switching Pulses for polarity changer switches

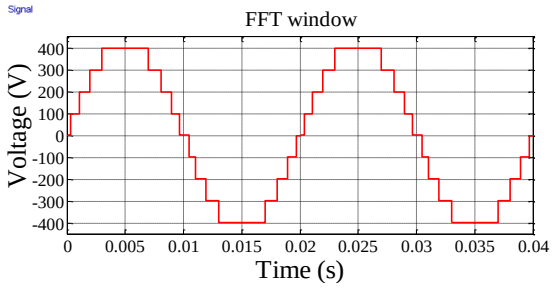


(c) Level generator output voltage waveform.

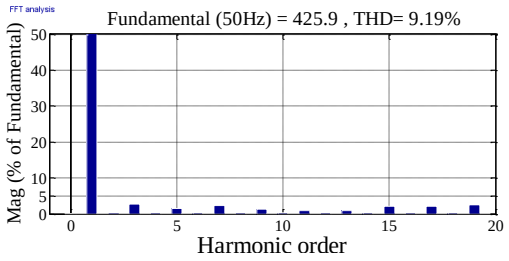
Figure 4. Simulation results for proposed nine level inverter topology

Figure 4 shows the switching pulses given to different switches of the proposed inverter. It is clear from the figure that the switches are operated according to Table 1, thus avoid short circuiting of the sources.

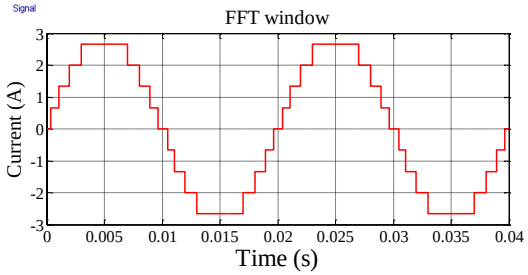
Output voltage and current waveform of the inverter and their corresponding harmonic spectrum for resistive (R) load of 150ohm (Power Factor: P.F=1) is shown in Figure 5. Simulation results for resistive-inductive (R-L) load at P.F=0.9 is presented in Figure 6.



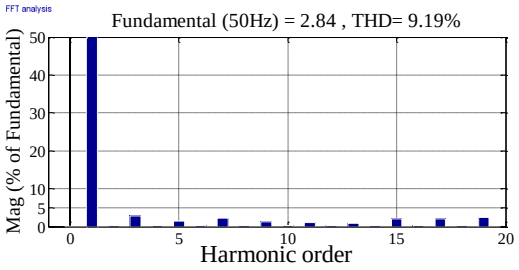
(a) Output voltage waveform



(b) Voltage Output Harmonic spectrum

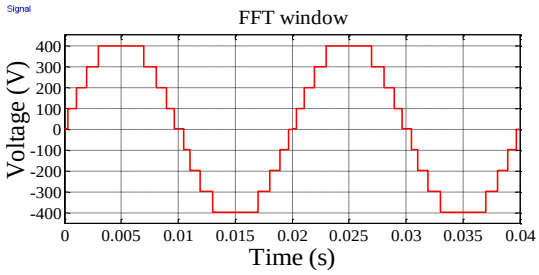


(c) Load current waveform

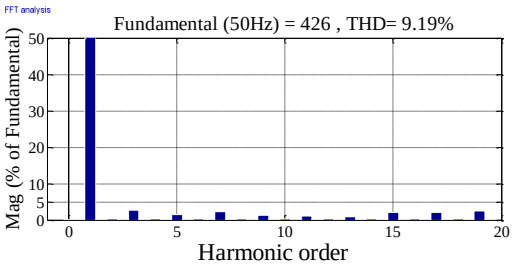


(d) Load Current Harmonic spectrum

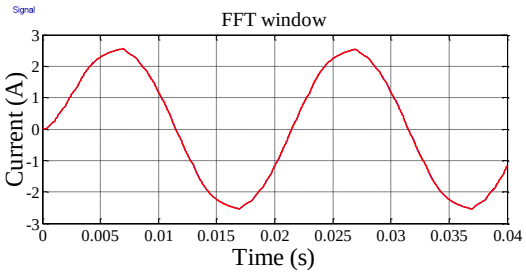
Figure 5. Simulation Output results at 50Hz fundamental frequency for R = 150ohm



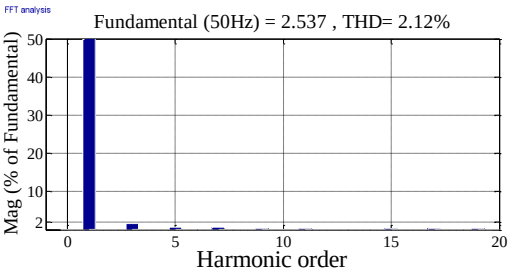
(a) Output voltage waveform



(b) Voltage Output Harmonic spectrum



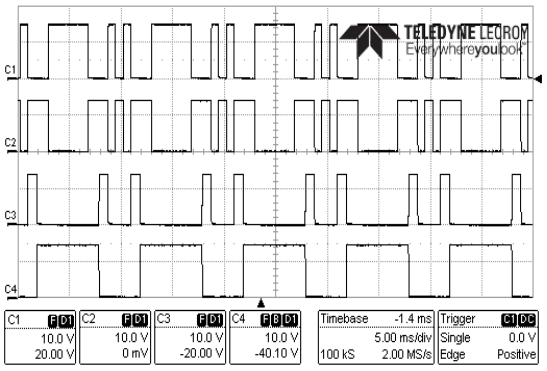
(c) Load current waveform



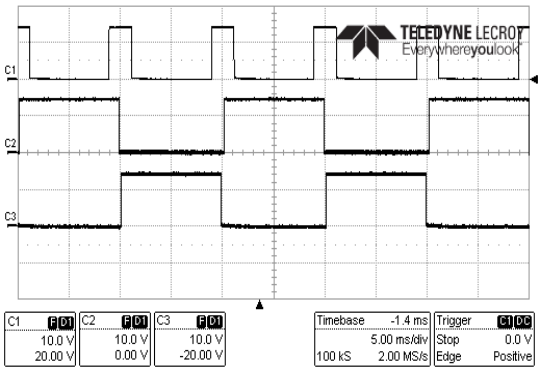
(d) Load Current Harmonic spectrum

Figure 6. Simulation Output results at 50Hz fundamental frequency for R = 150ohm, L= 240, P.F = 0.9

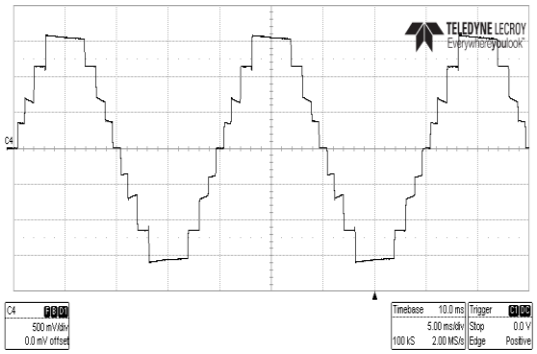
The voltage waveform shows that the proposed topology is able to generate nine level output (four positive, four negative and one zero) with almost uniform step size. Output current waveform with R-L load, shown in Figure 6(c), justify the operation of the proposed topology. The output voltage without using filter has Total harmonic distortion (THD) of 9.19% and the magnitude of each individual harmonic is less than 5%, satisfying the condition of IEEE-519 Std. (i.e. max harmonic for each order is 5%). Whereas THD in load current is 2.12% with R-L load (P.F=0.9).



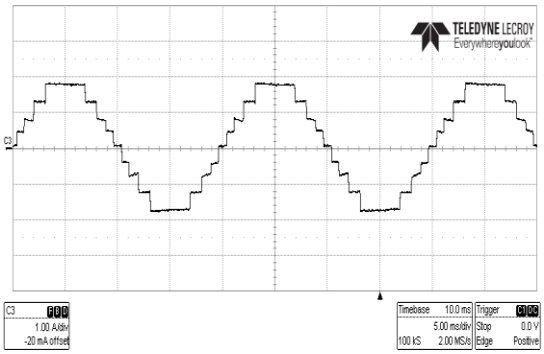
(a) Driver circuit output to the switches S1, S2, S3 and S4



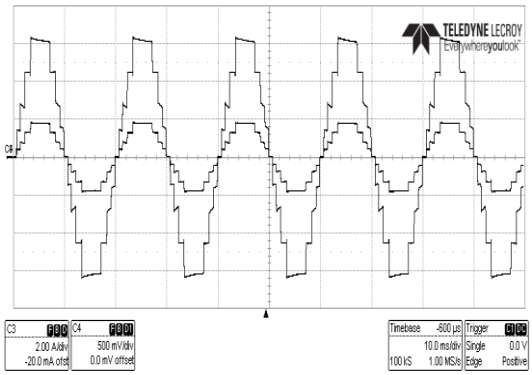
(b) Driver circuit output to the switches S5, Sa1 and Sb1



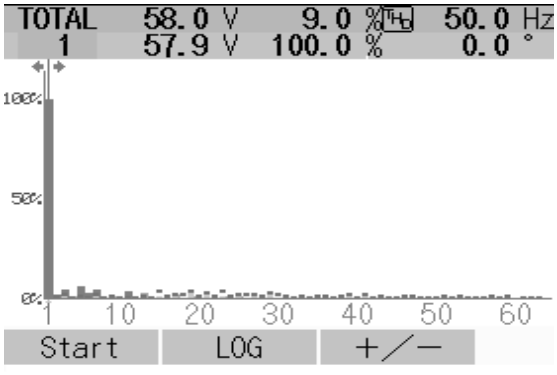
(c) Output Voltage waveform of the proposed nine level inverter



(d) Output current waveform of the proposed nine level inverter



(e) Output voltage and current waveform of the proposed nine level inverter



(f) FFT spectrum for one complete cycle of the output voltage

Figure 7. Experimental results of the propose nine-level inverter

In order to verify the simulation result and to analyse the performance of the proposed topology in generating desired output voltages, single phase 9 level inverter prototypes has been implemented and tested in laboratory. IGBTs model IRGP35B60PDPBF has been used as switches. DC sources V1= 20V and V2 = 60 are used in order to get voltage step size of 20V each. For driving IGBTs, switching pulses were generated using digital signal controller (DspTM320F2812). These pulses are applied between gate and emitter of IGBTs through driver circuits. Output voltage waveforms were measured by Teledyne LeCory WAVESURFUR-3034 digital storage oscilloscope using potential probe (voltage ratio 1/50) and THD has been recorded using power quality analyser KEW-6310 manufactured by Kyoritsu Electrical Instruments.

Figure 7(a) and 7(b) shows the output pulses from the driver circuit give to the switches. Output voltage and current waveform of the proposed 9-level inverter at unity power factor for a frequency of 50Hz is shown in Figure 7(c) and Figure 7(d) respectively. FFT spectrum for one cycle of experimental waveform is illustrated in Figure 7(f), indicating the THD of 9% for 9-level inverter.

5. Conclusion

In this paper a new single-phase multilevel inverter topology is presented. Proposed topology is capable of producing nine-level output voltage with reduce device counts. It can be used in medium and high power application with unequal dc sources. Different modes of operation are discussed in detail. On the bases of device counts, the proposed topology is compared with conventional as well as other asymmetrical nine-level inverter topologies presented in literature. Comparative study shows that, for nine level output, the proposed topology requires lesser component counts then the conventional and other topologies. Proposed circuit is modeled in Matlab/Simulink environment. Detailed Simulation analysis is carried out and validated experimentally. Experimental prototype of the proposed nine-level inverter is developed and tested in the laboratory. Results obtained show that topology works properly. As the THD obtained in the output voltage without filtering is 8.95% in simulation and 9.0% in experimental testing whereas the each harmonic order is < 5%, satisfies harmonic Standard (IEEE-519).

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