Voltage Balance and Control in a Multi-Level Unified Power Flow Controller

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***Abstract*—The neutral-point-clamped multilevel converter is an attractive implementation of the unified power flow controller because it facilitates back to back operation, high voltage operation (without direct series connection of devices) and low distortion (without the use of multi-pulse transformers). A UPFC using three converters is proposed. Two phase-shifted converters are required to provide a full range of voltage control of the series connection while ensuring low distortion and a balanced DC link. A single shunt converter is used. A commutation angle solution that balances the voltages of the multiple DC link capacitors is analyzed in terms of the active power balance at each node. Control of shunt reactive power requires a variable DC link voltage. Control schemes for both shunt and series converters are developed and verified in terms of voltage balancing and power flow control on a micro-scale experimental system using 5-level converters.**

***Index Terms*—FACTS, multi-level converter, power flow control, unified power flow control.**

I. Introduction

THE UNIFIED Power Flow Controller, UPFC, is a FACTS device able to provide, simultaneously, both series and shunt compensation to a transmission line [1]. Implementation of such a device relies on providing high-performance, high-power power converters in a cost-effective way. The limitations of present semiconductor devices (insufficient voltage rating and high conduction and switching losses) make the implementation of such converters difficult. In particular, several semiconductors must be placed in series to meet the voltage requirement and the switching frequency must be kept very low to limit power loss. Therefore, viable converter topologies for FACTS devices are radically different to those commonly used in low power applications such as motor drives.

A small number of experimental FACTS devices have entered service including STATCOMs [2], [3] (with rating of approximately 100 MVAr) and a UPFC [4] (with a total rating of 320 MVA). These devices use multi-pulse converters that exploit the principle of harmonic neutralization between phase-shifted waveforms to provide harmonic mitigation.

Recently, multi-level converters of various topologies have emerged as an alternative way of implementing low-distortion and high-power voltage source inverters [5]–[7]. In general, these converters synthesize the output voltage from a number of available DC voltage supplies held on storage capacitors. The complex phase shifting transformers of the multi-pulse converter are not needed and, in principle, the series connection of devices can be avoided.

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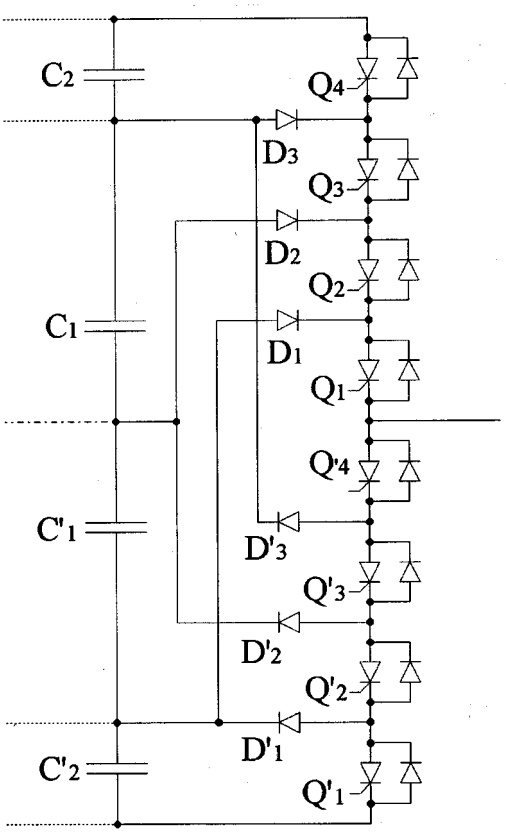

Fig. 1. One phase of a 5-level NPC converter.

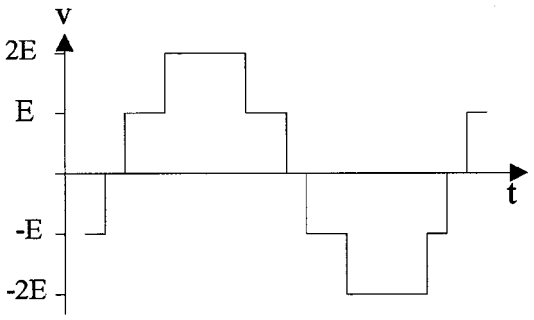

Fig. 2. Phase voltage of a 5-level converter.

The neutral point clamped, NPC, inverter is a 3-level inverter [5] that can be extended to a higher number of levels as shown in Fig. 1 [6], [7]. Fig. 2 shows the phase voltage waveform available from the 5-level converter of Fig. 1. All inverters of this class are referred to here as NPC. Additional levels enable higher AC voltages to be achieved for a given device voltage

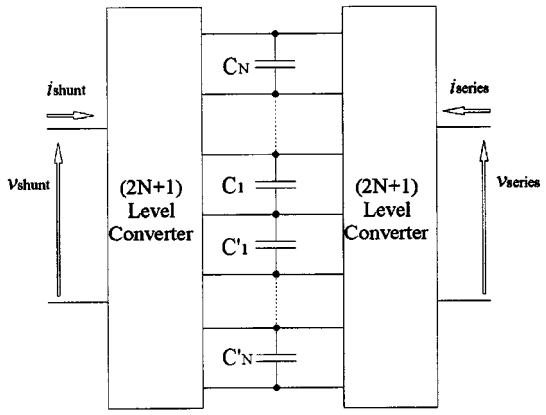

Fig. 3. A UPFC using NPC multi-level converters.

rating and each pair of extra levels provides one more commutation angle that can be set. The objectives that can be met by setting the commutation angles are the control (or maximization) of the AC fundamental voltage, the elimination of certain harmonic voltages and the control of capacitor charge transfer. Generally, the number of levels will be inadequate to meet all the desired objectives.

A difficulty arises with numbers of levels beyond three in that the capacitors near the center of the chain carry the AC-side current for a greater proportion of the time than the outer capacitors. For all conditions except voltage and current in quadrature, the inner-most capacitors experience a larger charge transfer than the outer capacitors. Corrective action must be taken to ensure that the capacitor charge transfers are balanced if real power processing is required. One balancing method is to employ auxiliary converters to exchange charge between inner and outer capacitors. In PWM inverters several techniques exist that are not available with line frequency switching.

In the case of the back-to-back converter arrangement of NPC converters, the charge transfer of one converter could be balanced by the charge transfer of the other [7]. Back-to-back converters have been used for phase shifters [8], back-to-back inertias [7], [9], [10] and UPFCs [11]. Auxiliary converters may still be of value in back-to-back connection because they can be of relatively low rating provided the back-to-back connection is exploited to provide most, if not all, of the balancing effort [9], [10].

This paper describes a back-to-back multi-level converter implementation of a UPFC which achieves independent control of the shunt and series voltage magnitudes, maintains capacitor voltage balance and maintains transmission quality harmonic distortion. The control system required for this UPFC is then examined.

II. DC-Link Voltage Balance in Back-to-Back Connections

In the UPFC of Fig. 3, the DC component of the current flowing through each capacitor is the sum of the series and shunt converter contributions. An analysis of the DC current in terms of the switching functions, the voltages and the active power

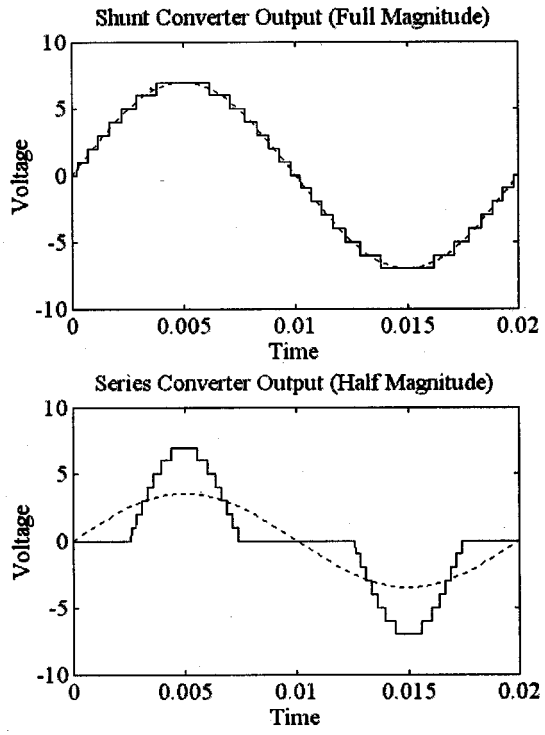

Fig. 4. Shunt and series converter voltages for $|V_{ser}| = 0.5|V_{sh}|$. (The dotted line waveform corresponds to the fundamental component.)

flows of the series and shunt converters yields (1) for the DC link currents of the ith capacitor

$$I_{C_i,\mathrm{DC}} = \frac{\sqrt{2}}{\pi}\left[\frac{P_{sh}}{|V_{sh}|}\cos\left(\alpha_{\mathrm{shunt}_i}\right) + \frac{P_{ser}}{|V_{ser}|}\cos\left(\alpha_{\mathrm{series}_i}\right)\right]. \tag{1}$$

Assuming power balance between the shunt and series converter (i.e., $P_{\mathrm{shunt}} = -P_{\mathrm{series}}$) and setting all the capacitor currents to zero, the condition for achieving the voltage balance in the DC link can be written as (2)

$$\cos\left(\alpha_{\mathrm{series}_i}\right) = \frac{|V_{ser}|}{|V_{sh}|}\cos\left(\alpha_{\mathrm{shunt}_i}\right). \tag{2}$$

Equation (2) establishes that the control angles of the shunt and series converter are not independent of each other. Nevertheless, the commutation angles (α_i), and hence the magnitude of the converter voltages, are not required to be equal. In principle, this enables independent control of the series and shunt converter voltages.

The selection of the control angles on the basis of harmonic elimination in the shunt converter whilst controlling the voltage in the series converter using (2) will not lead to harmonic elimination in the series converter. Fig. 4 shows the phase voltage waveforms of 15-level shunt and series converters. The commutation angles of the shunt converter were chosen to maximize the fundamental component and to eliminate harmonics up to the 23rd. The angles of the series converter were obtained from (2) after setting $|V_{\mathrm{series}}| = 0.5|V_{\mathrm{shunt}}|$. It is evident that the series voltage is far from sinusoidal and that an alternative method of series voltage control is required.

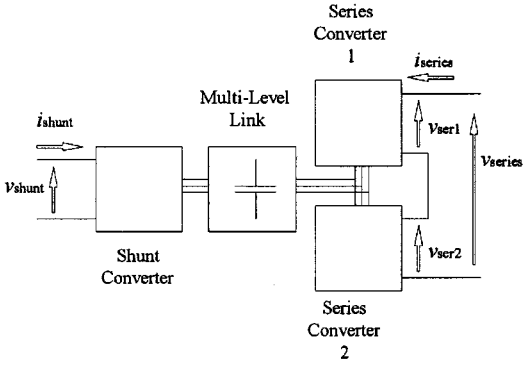

Fig. 5. A UPFC composed of one shunt NPC converter and two series NPC converters.

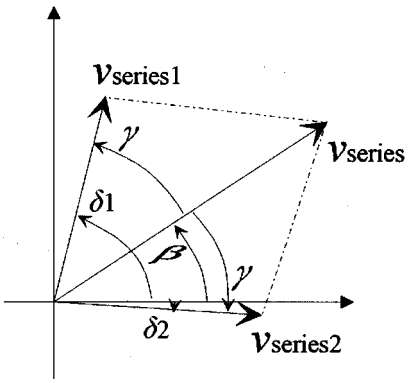

Fig. 6. Phasor diagram showing control of the series injected voltage through phase difference.

III. Proposed UPFC Topology Using NPC Multi-Level Converters

Two converters of fixed voltage magnitude can be phase-shifted such that the voltage appearing between them is of controlled magnitude. The two converters can operate from the same DC-link using an open-delta series transformer. Fig. 5 shows a UPFC circuit topology comprising one converter for the shunt element and two for the series element. The two series converters would each process half the total VA exchanged through the series connection.

A. Control of the Series Converter Voltage

Fig. 6 illustrates the phasor diagram of two series converter voltages, V_{series1} and V_{series2} (assumed to be of the same magnitude) at phase angles of δ_1 and δ_2 with respect to the system reference. The voltage of each converter is dependent on the voltage of each level, E and the number of positive levels, N (there being $2N+1$ levels in total). The voltages also depend on the depth of modulation, M of the converters which is in turn dependent on the control angle, α_i solution found through harmonic elimination. The angle difference $2\gamma = \delta_1 - \delta_2$ is set to control the magnitude of the resultant voltage vector, V_{series} as expressed in (3). The angle of V_{series}, $\beta = (1/2)(\delta_1 + \delta_2)$ is set using (4)

$$\cos(\gamma) = \frac{|V_{\text{series}}|}{2|V_{\text{series1}}|} = \frac{|V_{\text{series}}|}{2\sqrt{2}MNE} \tag{3}$$

$$\delta_1 = \beta + \gamma$$
$$\delta_2 = \beta - \gamma. \tag{4}$$

B. DC-Link Voltage Balance

By extension of (1) to three converters, the DC component of the capacitor current can be expressed as:

$$I_{C_i,\text{DC}} = \frac{\sqrt{2}}{\pi}\left[\frac{P_{\text{shunt}}}{|V_{\text{shunt}}|}\cos(\alpha_{\text{shunt}_i}) + \frac{P_{\text{series1}}}{|V_{\text{series1}}|}\cos(\alpha_{\text{series1}_i}) + \frac{P_{\text{series2}}}{|V_{\text{series2}}|}\cos(\alpha_{\text{series2}_i})\right]. \tag{5}$$

Assuming that the amplitude of the series converter voltages are related to each other according to:

$$|V_{\text{series1}}| = k|V_{\text{series2}}| \tag{6}$$

and that this is achieved by choosing the control angles so that

$$\cos(\alpha_{\text{series1}_i}) = k\cos(\alpha_{\text{series2}_i}) \tag{7}$$

the capacitor current will be given by (8)

$$I_{C_i,\text{DC}} = \frac{\sqrt{2}}{\pi}\left[\frac{P_{\text{shunt}}}{|V_{\text{shunt}}|}\cos(\alpha_{\text{shunt}_i}) + \frac{P_{\text{series}}}{|V_{\text{series1}}|}\cos(\alpha_{\text{series1}_i})\right]. \tag{8}$$

Noting that $P_{\text{series}} = P_{\text{series1}} + P_{\text{series2}}$ and using the power balance in (8), the condition for voltage balance will be given by:

$$\cos(\alpha_{\text{series1}_i}) = \frac{|V_{\text{series1}}|}{|V_{\text{shunt}}|}\cos(\alpha_{\text{shunt}_i}). \tag{9}$$

The latter is similar to the condition for the two converters, however, (7) should also be satisfied. Thus the conditions for achieving DC voltage balance in this configuration (three converters) can be summarized as follows:

$$\cos(\alpha_{\text{series1}_i}) = k_{\text{series1}}\cos(\alpha_{\text{shunt}_i})$$
$$\cos(\alpha_{\text{series2}_i}) = k_{\text{series2}}\cos(\alpha_{\text{shunt}_i}) \tag{10}$$

where k_{series1} and k_{series2} are the ratios between the series converter voltages, 1 and 2, respectively, and the shunt converter.

Although the voltages of the three converters are not required to be equal, this may be the only case where (10) and harmonic elimination in both the shunt and series converter can be simultaneously satisfied.

In establishing the conditions to achieve voltage balance for both the two-converter and three-converter cases, it has been assumed that each converter draws a symmetrical set of three-phase sinusoidal currents. Pre-existing harmonic voltages in the AC system and imperfections in the converters adversely affect the balance of the capacitor voltages. It is expected that the power flow imbalance will be small when compared with the inherent imbalance of a single converter but, nevertheless, the power imbalance leads to DC voltage imbalance and therefore a compensation mechanism is required. The voltage imbalance could be overcome by making small adjustments to the switching pattern of the converters (with a consequent small increase in distortion) or by using auxiliary converters. An auxiliary converter may be a practical solution since it requires only a small fraction of the VA rating of the UPFC. These methods can also compensate voltage imbalance due to transient disturbances in the power flow of the converters.

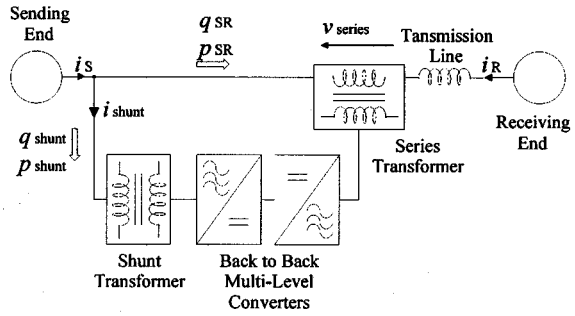

Fig. 7. Simplified single-line diagram of the test system. (Parameters: shunt interface impedance $0.058 + j0.85$ p.u.; line impedance $0.01 + j0.1$ p.u.)

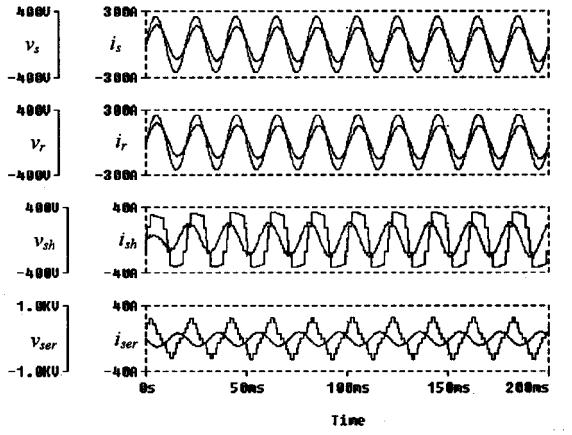

Fig. 8. Voltage and current waveforms in the UPFC and transmission system for $|V_{ser}| = 0.0707$ (p.u.) and $\alpha = 45°$. (In each subplot, the trace with the smaller relative amplitude corresponds to the current.)

C. Verification of Voltage Balancing

Fig. 7 shows a simplified single-line diagram of the system that will be experimentally investigated. The UPFC is located in a transmission line that connects two ideal generators (sending and receiving ends). The power flow from sending end to receiving end as measured at the UPFC connection point, is denoted $p_{sr} + jq_{sr}$. The test UPFC was formed from 5-level converters.

Initial verification was through a Pspice simulation. The series element UPFC was set to inject 70.7% of its maximum voltage at an angle of 45°. The excess capability of the shunt converter was used to inject reactive power into the line. Fig. 8 shows the voltage and current waveforms at the sending-end, receiving-end, shunt converter and series converter. Fig. 9 shows the voltages across the capacitors in the DC link. From this figure it can be seen that all voltages remain well balanced even during the start-up transient of the simulation. In steady-state approximately 2.5 kW of average power is injected by the series converter and, therefore, a matching power is demanded by the shunt converter. These results demonstrate the ability of the proposed circuit topology to transfer active power through the DC link without destabilizing the capacitor voltages. They also verify the effectiveness of the basic control strategies for voltage control and DC voltage balance.

In order to confirm the operation of the proposed UPFC a low power prototype consisting of three 5-level NPC converters

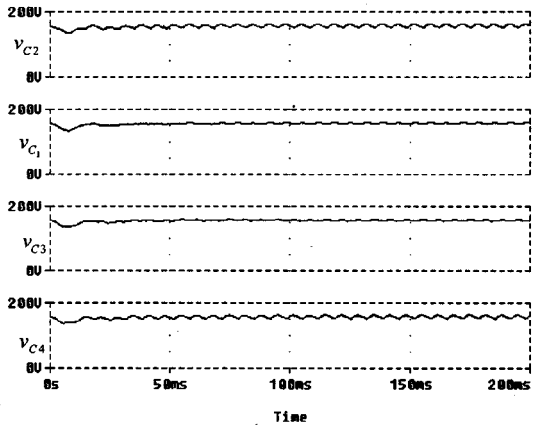

Fig. 9. Capacitor voltage waveforms.

was built and tested on a scaled model transmission line. The converters used a fixed switching pattern and each was rated at 2 kVA and 105 V.

Initial experiments with the shunt converter operating as a STATCOM showed that the DC voltages became unbalanced. The voltage difference between the inner and outer capacitors increased with the converter current. It was found that this imbalance was a result of pre-existing voltage harmonics in the mains. Measured THD in the mains was approximately 3% of which 2.8% was 5th harmonic. Simulations confirmed that pre-existing harmonic distortion in the mains could cause DC voltage imbalance. For simplicity, DC voltage imbalance was overcome by using small VA rating bi-directional choppers. Even when operating the shunt converter at its maximum of 14 A RMS (90° lagging) the compensation current required was only 125 mA.

IV. Control of Multi-Level UPFC

The most versatile role of the UPFC is to regulate the active and reactive power flow in the transmission line. Feedback of these quantities is used to control the series injected voltage [1]. The steady-state real power exchanged between the line and the series converter must be balanced by a real power exchanged between the shunt converter and the line. A small difference can be introduced between the real powers shunt and series converters in order to change the DC link capacitor voltages. The reactive power exchanged between the shunt converter and line can be independently set for VAr compensation objectives.

The UPFC implemented with three multi-level converters has restrictions that follow from the choice of commutation angles and these must be addressed in any control strategy. The angles can be chosen so as to set the fundamental component of the shunt converter voltage to a specified value (assuming a constant DC link voltage) and to eliminate low order harmonics. The series injected voltage is then set according to Fig. 6.

Alternatively, the commutation angles can be fixed and the overall DC link voltage can be varied to set the shunt voltage magnitude. This can release one more commutation angle for the purpose of harmonic elimination. Again the series converter voltage is controlled according to Fig. 6. Because the shunt voltage magnitude will always be in a narrow range close to the

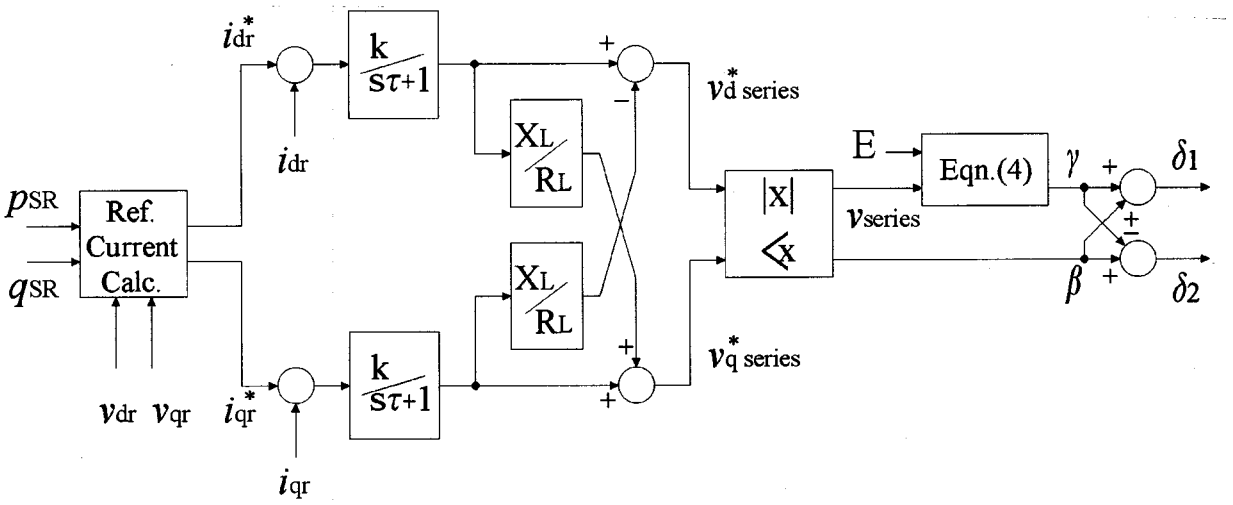

Fig. 10. Series converter control schematic with static de-coupling.

line voltage, the DC link voltage will be always sufficient for series injection purposes.

The overall power control strategy can be accomplished using steady state power flow concepts [1] or by using the concept of the instantaneous power and a d–q representation of voltages and currents [12], [13]. The latter enables fast, and an almost independent, control of the line active and reactive power flows to be implemented. For this case, the series voltage is controlled so as to regulate the d- and q-axis current flowing through the line and thereby the active and reactive power in the line. The de-coupling between the p- and q-control loops is provided by de-coupling the internal d- and q-axis currents loops.

In general, the provision of perfect de-coupling between d- and q-axis current, hence p and q, control loops is difficult because it requires system parameters to be accurately known. In addition, system performance deteriorates due to delays in the control actions of the converters and in the measurement system. More robust control strategies have been proposed in [12] and [13].

A control strategy that provides only static de-coupling is considered here and is sufficient to demonstrate the abilities of the power converters. The strategy is similar to the cross-coupled controller in [12] but it also includes direct terms in the controller. Fig. 10 shows a block diagram of the control system that regulates the voltage of the series converter. The d- and q-axis current controllers consist of proportional controllers followed by first-order, low-pass filters. These filters are introduced in order to impose a reduced rate of change in the series voltage demand. The angle difference, 2γ between the two series converters is found from the required series voltage magnitude using (3). This calculation also depends on the magnitude of the DC-link voltages, E, which together with the control angles of each level determines voltage of each individual converter.

The shunt converter can be controlled in terms of the d- and q-axis currents required to exchange the specified active and reactive power. Concurrent control of shunt active and reactive power flows ($p_{\rm shunt}$ and $q_{\rm shunt}$) requires a VSI with the capability to control both voltage magnitude and phase angle. In the scheme considered here the commutation angles are fixed and only the phase displacement, $\delta_{\rm shunt}$, is freely variable.

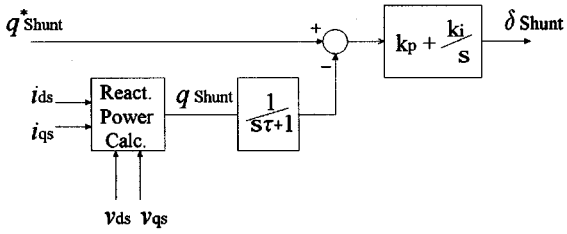

Fig. 11. Shunt converter control schematic.

The chosen shunt reactive control loop, Fig. 11, is similar to that of a STATCOM that uses a VSI with a fixed switching pattern. In such a STATCOM, the reactive power depends on the voltage difference between the line and the converter and thereby depends on the DC voltage. This voltage is regulated by charging, or discharging, the DC-link capacitors until the desired reactive power has been reached. This is achieved by exchanging a small amount of real power between the capacitors and the line. In the UPFC case, the series converter also exchanges real power with the line and so the controller in Fig. 11 is required to compensate for this also.

The reactive power is calculated using the line voltage and the shunt converter current. A low pass filter may be required to filter out the ripple caused by harmonic currents. A PI controller makes the necessary adjustments of the phase angle δ_{sh} to maintain a specified reactive power flow exchange with the line and in doing so also compensates any disturbance in the DC voltage due to the active power of the series converter. The balance of the active power between the series converter and the shunt converter is maintained despite the DC link voltage not being regulated. To reduce the coupling between the series and shunt converters, a pre-compensation loop based on the feed-forward of the active power demanded by the series converter may be used.

The DC link voltage varies within acceptable limits for the series converter to operate since only a small voltage deviation

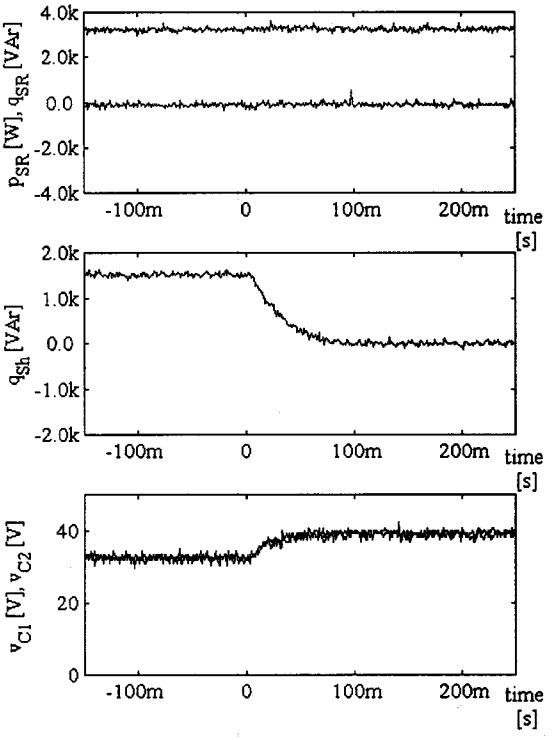

Fig. 12. Response to a step change in the shunt reactive power reference from 1.5 kVAr to 0.

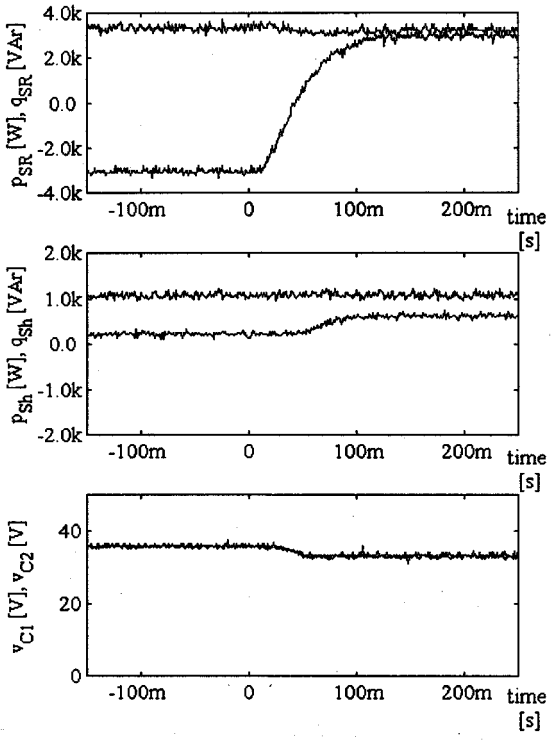

Fig. 13. Response to reversal of the reactive power reference from −3.0 kVAr to 3 kVAr.

(typically ±20% with respect to the nominal DC voltage) is required to supply or absorb the nominal reactive power.

V. Verification of UPFC Control Strategy and Variable DC-Link Voltage

The dynamic performance of the UPFC was tested using the experimental system described in Section IV. Tests involved sudden changes in the reference inputs of the control system such as changes in the line active and reactive power flows and in the shunt reactive power. Waveforms were captured with a digital storage oscilloscope and the data exported to a PC for plotting.

Fig. 12 shows the response of the system to a step change in the shunt reactive power reference from 1.5 kVAr to zero. The references for the active and reactive power in the line were held constant at 3 kW and 0 kVA, respectively. The first graph shows that the control loops for the line power provide an adequate rejection of disturbances arising from the shunt reactive power control loop. The second graph shows that the shunt reactive power falls over 0.1 s to achieve its new steady-state value. The third graph shows the voltages across the capacitors C_1 and C_2. It can be seen that the DC-link voltage, and by this means the shunt converter voltage, is increased by the controller in order to reduce the reactive power absorbed by the shunt converter. Further, the capacitor voltages are seen to stay in balance during the transient.

The response of the system to step changes in the active and reactive power references for the line are shown in Figs. 13 and 14. During these tests the shunt reactive power was held constant at 1.0 kVAr. Fig. 13 shows the response to a reversal of the

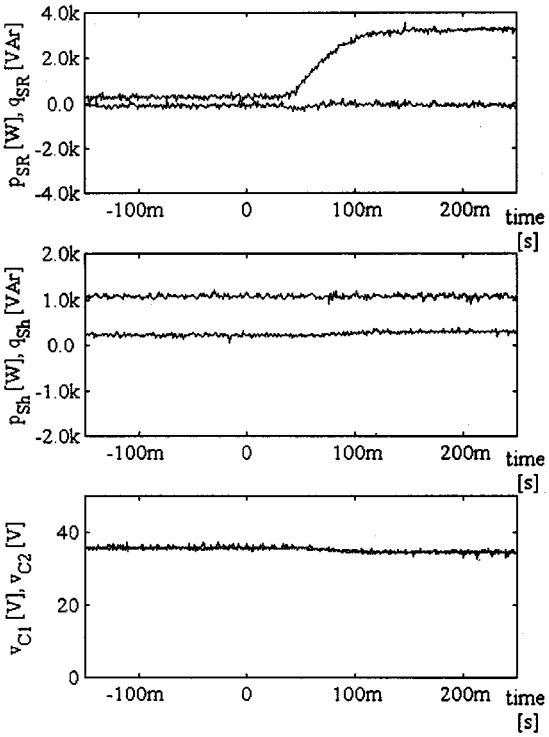

Fig. 14. Response to a step change in the active power reference from 0 to 3 kW.

line reactive power. (The line active power reference was held constant at 3 kW.) As can be seen from this figure, there is little interaction between the active and reactive power of the line. In

addition, the shunt reactive power remains constant and capacitor voltages maintain balance. For the operating point chosen here, the increase in the line reactive power requires an increase of the active power injected by the series converter and hence an increase in the real power supplied by the shunt converter. This is, therefore, a useful test of the dynamics of the DC voltage balance when transferring active power through the DC-link. DC voltages decrease as the link supplies real power to the series converter. After a short delay, the shunt active power increases to match the increase the active power requirement of the series converter. The capacitor voltages reach a new steady-state condition a little lower than the pre-disturbance values.

Fig. 14 shows the response to a step change in the line active power reference from zero to 3 kW. The line reactive power reference was set to zero. From this figure, it can be seen that there is only a slight disturbance in the line reactive power during the increase of the line active power. For this condition, unlike that of Fig. 13, the DC voltages remain almost constant. There is only a small increase in the active power demanded by the shunt converter from the line. This is required to supply the increase in the conduction losses of the series converter (the line current is very small before the transient but large enough to cause significant power loss in the experimental converters in the new condition).

These results confirm the operation of the DC voltage balancing mechanism for the multi-level converters and confirm the provision of adequate de-coupling between the various control loops. Time response in all cases is about 3–4 cycles which is adequate for transmission systems.

VI. Conclusion

A proposal has been made for a UPFC based on multi-level converter using a high number of levels (higher than three) and featuring balanced DC link voltages and fully controllable injected series voltage. The UPFC uses three neutral-point-clamped multi-level converters operating at the line switching frequency. Thus, low distortion is achieved without high switching frequency (or phase shift transformers) and high DC link voltages can be employed without the voltage sharing problems of long series strings of devices. The basic operation of the UPFC and suitable control strategies were confirmed through experimental tests of a micro-scale system.

The DC voltage balance in a back-to-back configuration was analyzed. It was found that the DC link voltage balance could be maintained by setting commutation angles, for steady state operation, accordingly to a relation between the converter voltages. However, this yields high harmonic distortion when controlling the voltage of the series converter. Therefore, it constrains the range of voltage control of the series converter in a UPFC based on two converters. This problem was overcome by dividing the series converter into two half-power rated converters and controlling the output voltage through the phase displacement between them.

A suitable control structure was developed that allowed the DC-link voltage to vary and the commutation angles to remain fixed. A d- and q-axis control scheme with correction for static coupling was found suitable for the series converter. Control of the shunt converter reactive power through voltage phase angle, and indirectly the DC link voltage, was found to also give adequate regulation of the DC-link voltage for proper operation of the series converter. These properties were confirmed in a micro scale experimental system.

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