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Trigger performance of the ALICE Silicon Pixel Detector

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Summary. — The ALICE Silicon Pixel Detector (SPD) forms the two innermost layers of the ALICE Inner Tracking System (ITS). The unique feature of the SPD among the vertex detectors of LHC experiments is the prompt trigger capability, called Fast-OR, which allows it to contribute to the experimental first level (L0) trigger decision. The SPD has been participating in data taking since the first proton-proton collisions providing the trigger for minimum bias event selection. A first evaluation of Fast-OR efficiency is presented.

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1. – Introduction

The ALICE Silicon Pixel Detector (SPD) forms the two innermost layers of the ALICE Inner Tracking System [1]. It consists of two cylindrical layers of hybrid silicon pixel detectors placed at radii of 3.9 cm and 7.6 cm. The basic detecting element is the ladder which consists of a sensor matrix bump bonded to five readout chips. The chip matrix contains 256×32 pixels measuring 50 μm ($r\varphi$-plane) by 425 μm (beam direction z). Every pixel provides a binary information if it has been fired or not. The SPD contains 1200 readout chips and about 10^7 readout channels in total. A unique feature of the SPD among the vertex detectors of LHC experiments is the prompt trigger capability which allows it to contribute to the first level (L0) trigger decision of the experiment. The SPD provides 1200 digital signals, called Fast-OR (FO) [2], synchronous to the 10 MHz internal clock. FO signals are promptly transmitted on the presence of at least one pixel hit in one of the readout chips. The Pixel Trigger system extracts the FO signals and processes them according to predefined algorithms to improve background rejection and event selection in proton-proton and heavy-ion interactions. The results are delivered to the ALICE Central Trigger Processor (CTP) within a maximum latency of 835 ns.

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2. – First results on Fast-OR trigger performance

The SPD has been providing a minimum bias event selection trigger signal in the central rapidity region since the early commissioning phase of LHC. The SPD trigger has been used during proton-proton collision data taking at $\sqrt{s} = 900\,\text{GeV}$ [3, 4], $\sqrt{s} = 2.36\,\text{TeV}$ [4] and $\sqrt{s} = 7\,\text{TeV}$. The Minimum Bias algorithm required the activation of at least one FO signal in the SPD, *i.e.* the presence of at least one hit in the detector. The SPD trigger input is combined in logic OR with the trigger signal of the high rapidity trigger detector (V0). The synchronization of the 10 MHz SPD clock with respect to the 40 MHz LHC clock has an important role for the response of the FO. The collision event can actually occur in four different time positions relatively to the SPD clock. A bunch counter (BC) time stamp is associated to each event recorded, indicating the position of the interaction with the resolution of the LHC bunch spacing (25 ns). The phase relationship of a given recorded collision with respect to the 100 ns SPD clock duration can be determined from the event BC stamp. The four possible phase relationships correspond to the value of the BC stamp module 4 (BCmod4). Events with all 4 possible relative phases (BCmod4 $= 0, 1, 2, 3$) are present in the runs considered in this study. The data sample is composed of about 100 k p-p events at $\sqrt{s} = 900\,\text{GeV}$ and 30 k events at $\sqrt{s} = 2.36\,\text{TeV}$. The method to measure the FO signal efficiency consists in looking, event by event, at the chips with at least one fired pixel and checking if the corresponding FO bit is active. The chip is considered FO inefficient in case FO bit in the datastream is not active. The V0 trigger is required in each event in order to unbias the measurement. The efficiency has been evaluated for the 904 chips included in the trigger mask splitting the events sample according to the four BCmod4 values. Events with BCmod4 equal to 0, 2 and 3 have similar efficiency distributions with the bulk of the chips with efficiency greater than 99%. The events with BCmod4 equal to 1 show a general efficiency loss with a corresponding mean value of 80%. This study shows that the alignment of the SPD clock with respect to the LHC clock is not well optimized yet. The non-perfect alignment appears in some interaction events with a particular relative phase with respect to the SPD, indicated by BCmod4 = 1. The results obtained give rise to a fine tuning of the alignment of the SPD clock with respect to the LHC clock and the method adopted to carry out this study will be used as monitoring tool.

REFERENCES

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