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Recent developments of a monolithic silicon pixel detector on moderate resistivity substrates

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Summary. — This paper is focused on the recent submission of a novel monolithic pixel detector developed in standard 90 nm CMOS deep sub-micron technology on wafers with moderate resistivity. This option, offered by some silicon foundries, allows to implement monolithic sensors for particle tracking that combine the low power consumption and material budget offered by monolithic active pixel sensors (MAPS) with the speed and radiation hardness characterizing hybrid pixel detectors. Seven ASICs have been submitted in March 2010 containing transistor test structures, a large diode, breakdown test structures and four pixel matrices produced both on standard substrates and on higher resistivity wafers.

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1. – Project description

The main challenges for an upgrade of a vertex detector at the Large Hadron Collider LHC are: spatial resolution, timing precision, radiation hardness, reduced thickness (material budget), low power consumption, mass production at low cost and reliable production yield. A monolithic detector integrating detector and readout in one piece of silicon would offer a number of advantages for such vertex detector upgrade. Such detectors have been under study for a long time, but they were either developed in non-standard technologies with production or cost issues, or exhibited a readout not compatible with LHC upgrades.

The LePIX project was started as a cooperative research effort involving at present CERN, INFN, IReS in Strasbourg, Imperial College and C4i-MIND. The aim is to

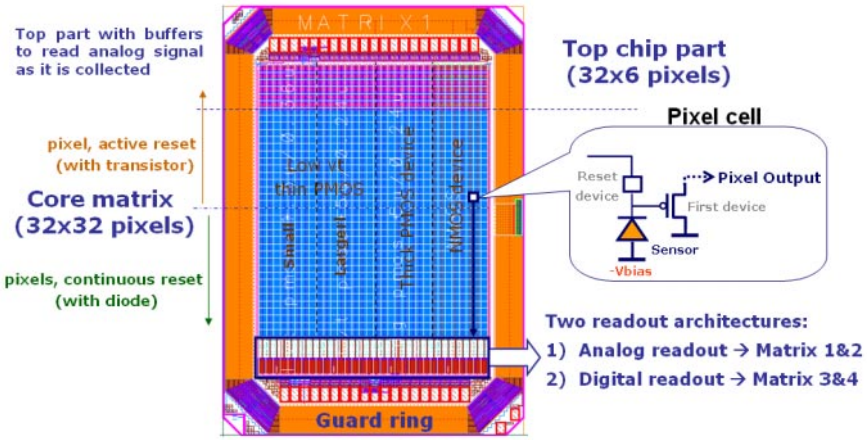

Fig. 1. – Pixel matrix chip architecture.

develop monolithic sensors integrating the readout and detecting elements in the same piece of silicon using standard deep sub-micron CMOS processes on a moderately doped p-type substrate ($\sim 100\,\Omega$·cm). A uniform and adequate thickness of the depletion region between 10 and 40 μm is obtained by applying a reverse bias of up to 100 V. The charge is collected by drift rather than by diffusion as it is the case for the MAPS. The high electrical field decreases the charge collection time and reduces the effect of charge trapping and therefore increases the charge collection efficiency. Since charge traps are often generated by radiation, collection by drift is expected to enhance the radiation tolerance.

The high metal density of 90 nm CMOS allows to connect every pixel in the matrix to the periphery by means of an individual metal line. This solution makes the information of the fired pixels promptly available at the periphery. As shown in fig. 1, only the input transistor is housed in the pixel cell, the rest of the analog and digital readout chain is located at the chip periphery. The absence of the clock distribution over the matrix reduces the power consumption and the risk of interference with the clock [1].

2. – Matrix architectures

The first layouts have been sent to the foundry in March 2010. They contain four pixel matrices ASICs of size 2.5 mm × 2 mm each produced both on standard low-resistivity and moderate-resistivity wafers. The matrices contain different pixel cell options and readout architectures. The readout architecture is sufficient to study the device, but will need to be modified to satisfy the upgrade requirements at the LHC. Each matrix is formed by a core part of the 32×32 pixel cells of $50 \times 50\,\mu\text{m}^2$ and an upper part of 6 rows where the analog pixel output can be connected directly to the top pads by analog buffers. A special guard ring structure about 200 μm wide (see fig. 1) has been introduced to allow a large reverse bias applied to the substrate.

Two different charge reset mechanisms have been implemented in each matrix. The upper $6 + 16$ rows are "actively" reset using a pulse applied to a reset transistor, the others are "continuously" reset using a diode which absorbs the pixel leakage current.

The wafer substrate is p-type and the collection electrode is the n-well employed in the fabrication of PMOS transistors. To maximize the signal-to-noise ratio, the capaci-

tance of the collection electrode has to be minimized. This is achieved by minimizing its size, but this increases the electric field. Therefore a compromise has to be found. In the submitted devices we have adopted a very small collection electrode for some prototypes, and a somewhat larger more conservative collection electrode for some other prototypes. The type and size of the input transistor also influences the overall capacitance of the collection electrode. For each matrix the columns are split in 4 groups. Each group contains pixels with a different input transistor, two sizes of thin oxide PMOS transistors, one size of thick oxide PMOS transistor and one size of NMOS transistor, as shown in fig. 1. The thin oxide transistors exhibit a lower threshold voltage but a higher gate leakage current, which is not an issue for the thick oxide PMOS transistor. The thick oxide PMOS transistor shows lower capacitance. The source to bulk junction in the PMOS transistors is slightly forward biased, therefore care had to be taken to design the PMOS transistor with sufficient margin. An NMOS input transistor which does not exhibit this problem, has also been included, even if it is associated with a much larger parasitic capacitance.

The four matrices differ also in their architectures. The main part of two of them is based on an analog serial readout. Two complementary CMOS switches are used to store the analog voltage levels in each pixel after reset and after a certain tunable time. The difference between the two stored voltage levels corresponds to the signal plus the integral of the pixel leakage current. This readout is very similar to a traditional serial MAPS readout, but in our design the two voltage levels are stored outside the pixel. The analog levels previously stored are serially shifted-out by a second complementary CMOS switch. For too large pixel leakage currents charge in the pixel could be lost before the readout of the full matrix is complete. Storing the signal outside of the pixel avoids this problem and decouples the duration of the sensitive period from the readout time. The advantage of this analog readout is that it is a useful tool to characterize the detector. The main part of the other two matrices is based on a readout chain of a preamplifier a shaper and a discriminator. This solution allows to detect and digitally store a particle hit as soon as the signal charge is collected onto the pixel. After a certain sensitive time the digital signals for all pixels are read out serially [2]. The shaping of the preamplifier signal allows the circuit to be even less sensitive to leakage current than for the analog serial readout previously described. It is difficult to estimate *a priori* the leakage current because this technology is usually implemented on a different type of the substrate with a nominal operating voltage of 1.2 V. The advantage of this digital readout architecture is that it seems to be more suitable for the super-LHC environment. The ASICs submitted will be produced and delivered by early summer 2010. The first measurements will be focused on the diode structures to prove the principle and characterize the sensor material. Thereafter the prototype matrices will be tested.

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