IL NUOVO CIMENTO Vol. 31 C, N. 4 Luglio-Agosto 2008
DOI 10.1393/ncc/i2009-10307-x

Commissioning of the ATLAS Pixel Detector

N. Garelli

INFN and Università di Genova - via Dodecaneso 33, 16146 Genova, Italy

(ricevuto il 5 Gennaio 2009; approvato il 12 Gennaio 2009; pubblicato online il 3 Marzo 2009)

Summary. — The ATLAS Pixel Detector is the innermost detector of the ATLAS experiment at LHC. Approximately 80 million silicon sensors allow to detect particle tracks and secondary vertices with very high precision. The ATLAS Pixel Detector is now in its final commissioning phase. A full characterization and qualification of the detector is currently performed: calibration procedures, special DAQ runs for noise studies and combined operations with other ATLAS subdetectors using cosmic-ray events are ongoing. All the aspects of the detector operation including the DAQ system, the calibration procedures, and the first cosmic run results are summarized.

PACS 29.40.Wk – Solid-state detectors.
PACS 29.85.Ca – Data acquisition and sorting.

1. – Introduction

ATLAS [1] (A Toroidal LHC ApparatuS) is a general-purpose experiment to exploit the physics discovery potential of the LHC (Large Hadronic Collider) at CERN (European Organization for Nuclear Research). The ATLAS detector has to meet the LHC design requirements: two proton beams colliding at a centre-of-mass energy of 14 TeV and a luminosity of $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ with a beam crossover (BCO) every 25 ns. With these conditions an average of 23 pp interactions are expected for every BCO. The number of channels of ATLAS ($O(10^8)$) leads to an average event size of ~ 1.5 MB. Therefore ATLAS has to provide an efficient trigger mechanism in order to reduce the BCO rate of 40 MHz to a maximum of ~ 200 Hz which can be written to mass storage. The ATLAS trigger is composed of three levels. The first level trigger (LVL1) selection is based on muon and calorimeter information and it is implemented on hardware processors. It is designed to receive input data at 40 MHz frequency and to reduce it to a maximum of 75 kHz. The second level trigger (LVL2) is based on software algorithms evaluating data within selected regions of the detector and it reduces the LVL1 rate to 2 kHz. The event filter (EF) is the final software selection where complex reconstruction using the complet event data can be performed.

2. – The ATLAS Pixel Detector

Highly segmented silicon semiconductor detectors offer nowadays the best answer to resolve decay lengths of the order of hundred μm, which is crucial to tag and measure heavy quarks and leptons. Therefore, all the experiments at a hadron collider use silicon trackers close to the interaction point.

The Pixel Detector [2] is the vertex tracker of the ATLAS experiment. The basic unit of the Pixel Detector is the *module*, whose sensitive volume is a silicon tile of dimensions $(60.8 \times 16.4)\,\mathrm{mm}^2$ and $250\,\mu$m thickness, segmented in 47232 pixels, mostly of $(50 \times 400)\,\mu$m. These pixels are connected to 16 Front-End (FE) readout chips by bump bonds. A flex hybrid is glued on the sensor backside and distributes power to the FEs and it lodges passive components and a Module Controller Chip (MCC). The whole Pixel Detector consists of 1744 modules, placed in 3 cylindrical sections (at 5, 9 and 12 cm respectively from the beam trajectory) and 3 disks per side covering up to pseudorapidity $\eta = 2.5$([1]).

3. – The ATLAS Pixel Detector readout chain

The charge deposited by the passage of a particle in each pixel is first amplified and then compared to a programmable threshold. The addresses of the pixels above threshold are digitized and the Time Over Threshold (TOT) is calculated. The TOT is the width of the discriminator output signal and is proportional to the deposited charge in the sensor. The TOT and the address of the hit pixels are transferred to the End-of-Column logic circuit (EoC) until an adjustable latency expires or a trigger signal arrives: in the latter case it is transferred to the MCC. The EoC can buffer up to 32 hits. The MCC distributes off-detector Timing, Trigger and Control signals (TTC) to the FEs and performs the first event building per module.

Optical links are used for the data transfer from and to the module. The data and supply lines of the modules are routed to the so-called Patch Panel 0 (PP0) which contains optoboards for the conversion between electrical and optical signals. Either 6 or 7 modules are connected to an optoboard. Each module uses individual fibres: one for the trigger, the clock, the commands and the configuration parameters, one or two different fibres for the event data. The optoboards are the last on-detector readout component in the chain: 80 m fibers connect the optoboards to the Back Of Crate (BOC) cards, located in the experiment control room. Individual links for each module allow an individual trigger adjustment, done through the BOC. Each BOC is paired with a Read-Out Driver (ROD) card, a 9U VME board. The ROD steers the trigger distribution to the modules and the hit extraction from the modules.

4. – The calibration procedures

The readout electronics need to be calibrated in order to optimize the detector performance. The detector has to be constantly tuned, also during LHC operation, in order to spot and eventually disable noisy channels and to maintain an optimal configuration for the best detector response. Some procedures are expected to be performed at each LHC beam fill (it means roughly after 10 h of operation), others every week or every month

([1]) $\eta = -\ln[\tan(\frac{\theta}{2})]$, where θ is the polar angle.

or simply on demand. The calibration scans are all controlled by the ROD and they can be classified in two types:

– The module tuning: scans to optimize the performance of digital components within the module electronics. In particular both, amplifier and comparator, have tunable feedback currents.

– The opto tuning: scans to tune the optical communication between the on-board and off-board cards.

4˙1. *The module tuning.* – For a reliable operation of the detector, the electronics thresholds have to be set to an appropriate value and adjusted for each pixel. Two different types of measurements are needed: the threshold scan, measuring the as-is threshold of each pixel, and the threshold tuning, which adjusts module parameters in order to reach a desired threshold value. To perform these scans, a charge is directly injected to the module by applying a voltage step to a calibrated capacitor embedded in each FE.

Due to irradiation the modules parameters have to be changed to compensate radiation damage of the sensors and electronics. Therefore, the tuning procedures have to be applied regularly during ATLAS operation in order to optimize the efficiency of the Pixel Detector.

4˙2. *The optical tuning.* – In order to obtain an error-free data transmission between on-detector optoboards and off-detector BOCs, all the currents and voltages in the two cards must be regulated. In particular, the module transmission needs to be adjusted by regulating the laser transmission power for the optoboard (ViSet), the delay and the threshold at the BOC (RX delay and threshold). The RX delay determines the phase between the BOC sampling and the incoming data, while the RX threshold determines the threshold for which data are accepted. Known patterns are sent from and to the module to determine the error-free region.

4˙3. *Software challenge.* – The complex calibration procedure represents a software challenge, especially due to the high number of channels which need to be handled in parallel while minimizing the duration of the procedure.

Each calibration procedure starts sending the detector configuration, composed by module and optical parameters, to the hardware and it ends with the calculation of an updated configuration. For this purpose, a custom Pixel Database Server has been implemented which efficiently handles the configurations using a caching mechanism, allowing to transfer the 500 MB detector configuration data to the hardware within ~ 1 minute.

Finally, the calibration scans produce a huge amount of histograms, both for on-line and off-line use. These data must be analyzed on-line to decide which channels need to be further tuned or disabled. A dedicated Pixel Histogram Server was implemented which achieves an efficient on-line histogram dispatching using multi-threaded and distributed software.

5. – Commissioning milestones

The final stage of the Pixel Detector commissioning started in July 2007, when the detector was lowered into the ATLAS cavern and inserted inside the Inner Detector.

In the following winter, the so-called sign-off was performed: the light transmission to and from detector was tested, the analog and digital low-voltage supplies were verified,

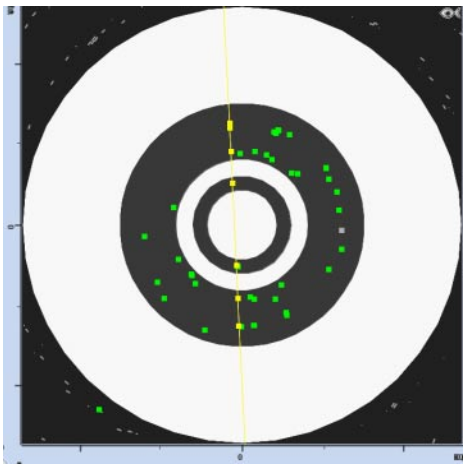

Fig. 1. – Screen shot of the on-line ATLAS event display. The first cosmic track passing through the Pixel Detector is shown; the event is composed of 7 Pixel hits and 16 SCT hits, projected to the plane perpendicular to the beam axis.

and the high voltage and the bump connectivity of each pixel were checked. In addition, the Pixel Detector performed some ATLAS combined runs just with the data acquisition chain. Unfortunately, the schedule was constrained by the commissioning of the evaporative cooling system, which has recovered from some major problems. This prevented the Pixel Detector to be continuously in use and thus, slowing down its commissioning schedule.

The first cosmic run with all the other ATLAS subdetectors was performed on September the 14th 2008. Figure 1 shows the first track of a cosmic muon containing Pixel hits. This has been an important milestone for the collaboration.

6. – Cosmic events

The Pixel Detector joined 30 days of ATLAS cosmic running collecting 2.5×10^5 tracks with Pixel hits, as shown in fig. 2.

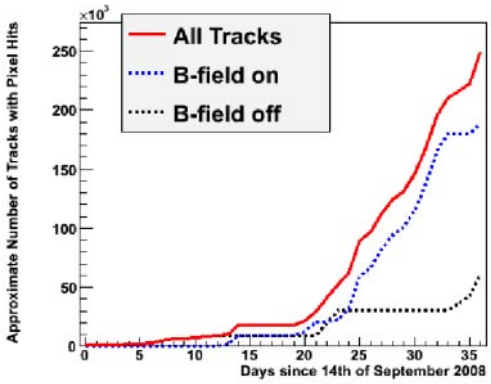

Fig. 2. – (Colour on-line) Number of tracks with Pixel hits. The two dashed lines indicate runs performed with (blue) and without (black) field of the ATLAS solenoid magnet.

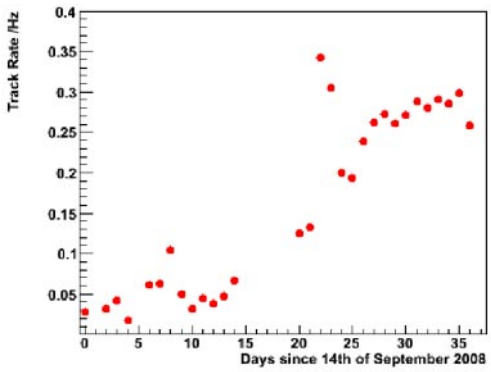

Fig. 3. – Rate of recorded tracks containing Pixel hits. After 20 days of running, the LVL2 was commissioned and the track rate increased significantly to up to 0.35 Hz.

During the cosmic run, roughly 5% of the modules were disabled: either because they have shown problems during the calibration procedure or they were disabled due to non-functional cooling loops. The goal for the run in 2009 is to enable the highest number of the modules. Unfortunately, 1% of the detector is already known to be not recoverable: one module has a short in an on-detector connection, while others have problems either with the optical communication or with the high-voltage supply.

For each module configuration, a map of noisy pixels was produced off-line and applied before the following run to minimize the signal noise. In total, 0.006% of the pixels were found to be noisy, *i.e.* with an occupancy greater than 10^{-5} hits/event.

The main goal of the ATLAS cosmic run was to provide data for the detector alignment and to spot hardware and software problems before actual proton collisions. The trigger signal for cosmic muons was provided by the muon chambers, the Resistive Plate Chambers (RPC) and the Thin Gap Chambers (TGC), and by the calorimeters. Since many of the RPC chambers are located perpendicular to the direction of the cosmic muons, they represented the most efficient trigger for the Inner Detector.

The initial rate of tracks through the Pixel Detector was about 0.03 Hz, while the simulation was predicting 0.5 Hz. This behaviour was caused by a not optimal trigger: the RPC timing needed further improvements and no track algorithm was used at LVL2 or EF [3]. Under these conditions, the RPC trigger rate had to be artificially reduced by a factor of 20 in order to keep the event recording rate below 200 Hz.

At the beginning of October, the RPC timing improved and the LVL2 was commissioned: the trigger chain and the number of tracks recorded to disk were optimized. The efficiency of the algorithms was tuned and it reached about 97%, allowing to increase the rate of tracks with Pixel hits from 0.03 Hz to 0.35 Hz, as is shown in fig. 3 and thus approaching the expected rate.

7. – Conclusion

The ATLAS Pixel Detector performed successfully the last commissioning phase in 2008. Waiting for LHC collisions, an extensive optimization program is ongoing: software improvements, analysis of the cosmic data for detector alignment purposes and noise studies, and recovery of the modules which were disabled during the data-taking runs.

REFERENCES

[1] Aad G. *et al.* (ATLAS Collaboration), *JINST*, **3** (2008) S08003.
[2] ATLAS Pixel Collaboration, *JINST*, **3** (2008) P07007.
[3] Aad G. *et al.*, *Expected Performance of the ATLAS Experiment: Detector, Trigger and Physics* (CERN, Geneva) 2008.