

Northumbria Research Link

Citation: Wang, Xiang, Wu, Haimeng and Pickert, Volker (2019) Design of an Advanced Programmable Current-Source Gate Driver for Dynamic Control of SiC Device. In: 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 17-21 March 2019, Anaheim, California, USA.

URL: https:/doi.org/10.1109/APEC.2019.8721941 < https:/doi.org/10.1109/APEC.2019.8721941 >

This version was downloaded from Northumbria Research Link: http://nrl.northumbria.ac.uk/42624/

Northumbria University has developed Northumbria Research Link (NRL) to enable users to access the University's research output. Copyright © and moral rights for items on NRL are retained by the individual author(s) and/or other copyright owners. Single copies of full items can be reproduced, displayed or performed, and given to third parties in any format or medium for personal research or study, educational, or not-for-profit purposes without prior permission or charge, provided the authors, title and full bibliographic details are given, as well as a hyperlink and/or URL to the original metadata page. The content must not be changed in any way. Full items must not be sold commercially in any format or medium without formal permission of the copyright holder. The full policy is available online: http://nrl.northumbria.ac.uk/policies.html

This document may differ from the final, published version of the research and has been made available online in accordance with publisher policies. To read and/or cite from the published version of the research, please visit the publisher's website (a subscription may be required.)





Design of an Advanced Programmable Current-Source Gate Driver for Dynamic Control of SiC Devices

Xiang Wang School of Engineering, Newcastle University Newcastle upon Tyne, UK <u>x.wang108@ncl.ac.uk</u> Haimeng Wu School of Engineering, Newcastle University Newcastle upon Tyne, UK haimeng.wu@ncl.ac.uk

Abstract—Silicon carbide (SiC) power devices outperform Silicon-based devices in operational voltage levels, power densities, operational temperatures and switching frequencies. However, the gate oxide of SiC-based device is more fragile compared with its Si counterpart. The vulnerability of the gate oxide in SiC power devices requires the development of a gate driver that is able to have more control during the turn-on and turn-off process. This paper proposes an innovative currentsource gate driver where the gate current can be fully programmed. The novelty of the gate driver is that the dynamic switching transients and the static on/off-state can be controlled independently. In order to achieve this approach, a signal decomposition and reconstruction technique is proposed to apply the separate control over the dynamic switching transient and the static on/off-state gate voltage respectively. The fundamental principle of the proposed circuit is verified in simulation. In addition, a prototype of the active gate driver has been built and tested to validate the effectiveness of the flexible control over the gate voltage.

Keywords—active gate driver, SiC devices, current-source, dynamic control

I. INTRODUCTION

SiC is widely recognized as one of the next generation power semiconductors due to its superior feature for high voltage, high frequency, high power density and high temperature applications [1]-[4]. However, the material advantages of SiC devices have not been fully exploited, and optimized gate driver circuit is required for SiC device to achieve better dynamic performance [5]. The limitation of the conventional gate driver is that the on/off behaviour of the device is predominately determined by the gate resistor which is a fixed value. In general, a small gate resistor is preferred to reduce the switching time which brings down the switching losses. However, unacceptable overshoot and ringing will be induced if the value of gate resistor is too small [6]. Furthermore, besides the influence on dynamic performance of the device, the gate driver has also significant impact on the health condition of the gate oxide [7], as the gate oxide of SiC devices is more vulnerable compared to Si devices [8]. The so-called interfacial electron trapping effect is reported as a significant problem in SiC device, reducing the inversion channel mobility severely [9]. Although all the trapping phenomena are suppressed by using purer substrate [10], the high density of electrically active defects of SiO₂/SiC remains a limitation, as the magnitude is at least 1-2 orders higher compared to the SiO₂/Si system [11]. As the SiC device is more sensitive to the gate voltage/current signal, the conventional voltage source gate driver can pose reliability problem to SiC device. Therefore, developing an advanced gate driving technique is of great significance for the reliable operation of SiC device.

Volker Pickert School of Engineering, Newcastle University Newcastle upon Tyne, UK volker.pickert@ncl.ac.uk

Nowadays, various types of active gate drivers have been investigated to improve the performance of SiC power devices. According to the control strategy, active gate drivers are usually classified into three categories: resistance controlled gate driver[12][13], voltage controlled gate driver[14] and current controlled gate driver[15]. For the group resistance controlled gate driver the circuit commonly uses a digital interface which is easy for isolation implementation, however, the gate voltage level is fixed and a discrete resistance network has to be employed with a very large number of integrated resistors. The gate voltage control method overcomes the fixed digital voltages thus it is more versatile. This method requires only one gate resistance. High bandwidth linear isolation techniques are required to drive SiC devices at high frequency for an acceptable resolution. Gate current control techniques directly control the gate current, which shows the flexibility to adjust gate driving signals with a reduced gate oscillation, however, the existing reported current-source active gate drivers are either designed with limited functions or too complicated for implementation [12][13].

This paper presents an innovative current-source gate driver, which is able to generate a programmable gate current to achieve the flexible control over gate voltage, including a dynamic control during switching transient, as well as the static on/off-state gate voltage. The structure of the proposed gate driver is illustrated in section II with the detailed explanation of the function of every module. The current control strategy is analysed in section III, followed by the specific circuit design presented in section IV. Then, the simulation results of the proposed circuit is demonstrated in section V and a functional prototype is built and tested to validate the effectiveness of dynamic control in section VI. Finally, the work is summarized and the possible application of the proposed gate driver is discussed in the conclusion.

II. STRUCTURE OF THE PROPOSED GATE DRIVER

The diagram of the proposed gate driver structure is shown in Fig. 1. This gate driver circuit can be divided into 4 functional modules.

The first part of the circuit is the control signal generation module. A high-speed DSP controller is used as the master processor to generate the digital control signals for a high resolution digital to analogue (DAC) waveform generator via SPI communication. In order to reduce the communication duration time between the control system, the profile of the control signal is pre-programmed and stored in the internal RAM of the DAC. Thus, this analogue control signal is generated based on the digital data and the amplitude and offset of the signal can be adjusted through programming.

The second function module is used for the isolation between the control circuit and the power circuit. The galvanic isolation for analogue arbitrary waveform is much more challenging than isolation required for on/off signals, as a wide bandwidth is required. In general, there are three common methods for electrical isolation. The magnetic approach using transformer is a widely applied electrical isolation method [18] where the signal and power are transferred by way of magnetic induction rather than current flow. However, the DC component of the gate driving signal will bring the magnetic core into saturation, inducing signal distortion. A newer form of isolator using capacitive connectivity is available for signal transmission as well as power transfer, called digital isolator[19]. The digital isolator is made up of a transimitter (TX) and a receiver (RX) which are isolated by capacitive coupling. As the capacitive connection blocks analogue signals, only pulse signal can be transferred. Therefore, it is difficult for analogue signals to be transmitted. In addition to magnetic approach, optical solution employing optocoupler can be used in the gate driver design [20]. It is made up of an infrared LED and photo-transistor, usually a BJT with an open collector. The transistor is turned on and off according to the states of the LED. The linear optocoupler or optical isoltion is able to transmit DC signal and low-frequency signal, but it is not fast enough for the switching transient control. Therefore, a signal decomposition and reconstruction technique is proposed for the first time to achieve high bandwidth signal transmission and isolation. The gate signal is firstly decomposed into high-frequency component and low-frequency component. The highfrequency component, named AC signal, is used to control the dynamic swithing transient. The low-frequency component, named DC signal, is used to control the static ON- and OFFstate gate voltage. Then the two components are isolated seperately: AC signal is isolated by a transformer; DC signal is isolated by a linear opto-coupler.

In the signal combination module, the isolated two components are combined and the gate signal is reconstructed. An analog signal adder serves as the function unit in the module. However, this reconstructed signal is the voltage signal having little driving capability. Thus, a functional signal conversion module is designed where a current mirror circuit is used to convert the voltage signal to the current signal which enhances the driving capability.



Fig. 1. The structure of the proposed gate driver consists of 4 parts: control signal generation, signal isolation, signal combination and signal conversion.

III. CURRENT SOURCE CONTROL STRATEGY

Different from conventional voltage source gate drivers, the proposed gate driver adopts current source control strategy to achieve active gate driving technique. The principle of the gate voltage control is illustrated in Fig.2.

As is shown in Fig.2, the waveform on the top represents the decomposited DC component of the input signal, the second waveform is the decomposited AC component of the input signal. The bottom waveform is the correspondent output gate voltage signal. The profile of two input control waveforms are pre-programmed and stored in the DAC and the magnitude of the waveforms are adjustable cycle by cycle as shown in the dotted line in Fig.2. The DC component changes the offset of the gate voltage, a positive i_{gDC} increases the ON-state gate voltage while a negative i_{gDC} reduces it, the magnitude of the DC component determines how fast the static state gate voltage is changing. When a desired driving condition is reached (-5V/+15V for example), the DC component is tuned to zero. Therefore, the static on/off-state gate voltage is no longer a fixed value as in a conventional gate driver, but an adjustable range (-8V to -3V and +12V to +20V for example). The AC component has much higher magnitude than DC component, changing the gate voltage from ON-state to OFF-state or vice versa. The intervals of the gate current determine the frequency of the gate driving signal. The magnitude of the AC component influences the voltage slope of the dynamic transient. The higher I_{gAC1} induces a faster voltage increasing while a lower I_{gAC2} slows the process down. Therefore, through programming, the dynamic performance of the device can be controlled through variable current step magnitude and its duration time.

Under the proposed control strategy, the voltage can be flexibily controlled by the amount of gate charge which is subject to the input gate capacitance of the device. The relation of on/off-state gate voltage and input current signal is expressed in (1) and (2).

$$V_{goff} = \frac{1}{C_{iss}} \cdot \int_0^t i_{gDC} \cdot dt = \frac{1}{C_{iss}} \cdot \sum I_{gDCi} \cdot t_{gDCi}$$
(1)

$$V_{gon} = V_{goff} + \frac{1}{C_{iss}} \cdot I_{gAC1} \cdot t_{gAC1} + \frac{1}{C_{iss}} \cdot I_{gAC2} \cdot t_{gAC2}$$
(2)

Where V_{gon} is the on-state gate voltage, V_{goff} is the off-state gate voltage, C_{iss} (equals $C_{\text{GS}}+C_{\text{GD}}$) is the input capacitor of the device, i_{gAC} is AC component of the injected gate current, and t_{gAC} is the duration time of i_{gAC} . The off-state voltage depends totally on the injected offset signal, i_{gDC} and its duration time t_{gDC} . The switching transient, including



Fig. 2. The current source control strategy illustration: AC component controls dynamic process, DC component controls static process.



Fig. 3. The diagram of the designed circuit, including AC isolation circuit, DC isolation circuit, signal combination circuit and signal conversion circuit.

switching speed and switching duration time, is determined by the AC component signal, i_{gAC} and it duration time t_{gAC} . The on-state voltage is controlled by the combination of AC and DC signals. Therefore, the profile of the gate voltage is shaped by proper input signals.

IV. GATE DRIVER CIRCUIT DESIGN

According to the aoforementioned theoretical analysis, a circuit is designed to achieve the gate driving signal control functions. The diagram of the designed circuit is illustrated in Fig.3.

The designed gate driver circuit includes 4 functional subcircuits, namely AC isolation circuit, DC isolation circuit, signal combination circuit and signal conversion circuit. $V_{\rm ac}$ represents the AC component of the input signal, which is used to control the dynamic switching transient. $V_{\rm ac}$ is isolated by the AC isolation circuit, consist of a transformer and ampilifer. V_{dc} is the DC component of the input signal, which is used to control the static state voltage as mentioned in section III. V_{dc} is isolated by the DC isolation circuit, consist of the linear optocoupler and the amplifiers. After $V_{\rm ac}$ and $V_{\rm dc}$ are isolated, they are added together by the summator. Finally, the processed signal is connected to the current mirror. The voltage signal produces a programmed current in control side of the current mirror, the other side of the current mirror therefore generates a current with the same profile to the output. Eventually the programmed control signal is converted into a current-source signal to the output of the gate driver circuit.

V. SIMULATION VERIFICATION

In order to verify the fundamental principle of the proposed gate driver circuit, the signal processing circuit and the proposed control strategy has been designed in the simulation. As the simulation focuses on the effectiveness of the proposed control strategy and designed circuit, a capacitor is connected to the output of the prototype to represent the gate-source capacitance of the device. The results of the control strategy simulation is presented in Fig.4.

In the simulation results waveform shown in Fig.4(a), V_{AC} (the waveform on the top) is the amplitude controlled gate current input signal and V_{DC} (the waveform in the middle) represents the input DC tuning signals. Both the AC and DC components of the gate current are processed and amplified to

drive the SiC device, which produces a magnitude and offset controlled gate voltage signal V_{out} (the waveform on the bottom). In this displayed case, it is illustrated that flexible gate voltage can be generated within several periods, while the magnitude of the gate voltage is determined by V_{AC} , the offset of the gate voltage changes according to V_{DC} . When the magnitude of the input AC component increases, the voltage differences between ON-state gate voltage and OFF-state gate voltage become larger. When the input DC component is positive, the offset of the gate voltage increases and both ONstate gate voltage and OFF-state gate voltage is rising accordingly. If the V_{DC} is tuned to zero and V_{AC} is tuned to a constant value, the driving condition reaches a steady state and the on/off-state gate voltage is kept fixed.



(a) The simulation results over a few switching periods



(b)Zoomed-in view of the voltage rising transient



(c)Zoomed-in view of the voltage falling transient

Fig. 4. Simulation results of the proposed current source control strategy: the blue line is the input AC signal, the green line is the input DC signal and the red line is the output gate voltage signal

The zoomed-in view of the detailed process of the switching transient is demonstrated in Fig.4(b) and (C). The shape of the input AC signal can be pre-programmed and stored in the controller. As the magnitude of AC component is alterable, the charging slope is controllable according to the gate current value. This simulation result illustrates that a two-step AC input signal induces two-speed charging process. The gate voltage changes faster during the high step period, while the charging speed slowed down during the low step period. Moreover, multiple-step gate current signal can be developed to achieve multiple switching speed control in different period of a single switching process. Therefore, the dynamic control over the gate voltage during the switching transient can be achieved.

VI. EXPERIMENTAL VALIDATION

A prototype of the proposed driver circuit has been built and tested to validate the functionality of the proposed signal processing technique, as is shown in Fig.5. The layout of the proposed gate driver is illustrated in Fig.5 (a) with a size of 100mm×70mm circuit board. SMA connectors are used to connect the two input analogue signals with the circuit board, which is able provide a high-bandwidth signal transmission with low distortion With necessary peripheral circuit, the two signals are isolated respectively. The symmetrical input AC signal is isolated by a RF transformer (10kHz to 200Mhz) while the linear optocoupler (2MHz) is utilized to isolate the relatively low frequency input DC signal. After isolation, the two components are recombined through the amplifier as one voltage-source signal. Finally, the recombined voltage signal is injected to a current-mirror circuit to convert the signal to a current-source signal. Therefore the current-controlled driving signal is produce from the output of the circuit board. The photo of the proposed gate driver prototype is shown in Fig.5 (b).



Fig. 5. The prototype of the proposed gate driver, (a) PCB layout of the proposed gate driver, (b) the photo of the proposed gate driver prototype.

The experiments on the proposed gate driver prototype have been carried out to validate the gate current control strategy. As the focus of the study is on the gate driver rather than the specific power device, a 20nF capacitor is used as the load of the proposed gate driver prototype, which is from the MOSFET datasheet of a SiC module (CREE CAS300M12BM2) where an input capacitance is 20nF. The experimental results are demonstrated in Fig.6 (a) and the detailed zoomed-in view of the charging and discharging process is presented in Fig.(b) and (c) respectively. The V_i waveform on the top is the input AC signal, whose shape is pre-programmed as a two-step signal and stored in the controller. The frequency of the input control signal is 150kHz. The first charging step has a value of 3V that lasts for



(a)Experimental result of several periods



(b)Zoomed-in view of charging proccess



(c)Zoomed-in view of discharging proccess

Fig. 6 Experimental illustration of the dynaimic switching transient control over the gate voltage

270ns while the second charging step has a value of 1V that lasts for 400ns. The symmetric input signal is converted to a current output as is shown in the I_G waveform in the middle. The output current has a similar shape to the input signal, rising to a top value of about 1.5A in the first 270ns and falling to 0.5A for 400ns. The V_G waveform on the bottom is the voltage across the capacitor, rising from -6V to 15V under positive input control signal and falling from 15V to -6V under negative input control signal. In the zoomed charging process, it is shown that the slope of the output voltage is changing from about 63V/us to about 23V/us. Therefore, the charging speed can be dynamically controlled for the power device.

The input signal is programmed and its resolution is related to the performance of the DAC. In the experiment, the 150 Mhz DSP 28335 is used as the controller and the 180Mhz high-performance DAC AD 9106 is employed as the waveform generator. The time resolution is 13ns, which means in principle the output signal can be changed every 13ns. Moreover, the 15bit input of the DAC enable the gate driver to generate the arbitrary waveform to control over the value of the output analogue signal. Therefore, a wide range of output voltage from -6V to 15V can be achieved using the proposed gate driver with a proper input signal.

VII. CONCLUSION

This paper presents an innovative programmable currentsource gate driver for SiC device to flexibly control the dynamic switching transient as well as the static on/off-state gate voltage. A signal decomposition and reconstruction technique is proposed to achieve the signal isolation with a wide bandwidth. The analysis of the proposed current control strategy is presented. The circuit of the proposed gate driver is demonstrated and simulated to verify the function of signal processing and the current control strategy. Moreover, a prototype is built to validate the effectiveness of the proposed circuit. The experimental results demonstrate high flexibility over the gate voltage control, which provide possibilities to improve the dynamic performance of the SiC power device through switching transient control.

ACKNOWLEDGMENT

This work was supported by the Engineering and Physical Sciences Research Council (EPSRC), UK, for the project of Reliability, Condition Monitoring and Health Management Technologies for WBG Power Modules (EP/R004366/1)

Reference

- X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, 2017.
- [2] A. Castellazzi, A. Fayyaz, G. Romano, L. Yang, M. Riccio, and A. Irace, "SiC power MOSFETs performance, robustness and technology maturity," *Microelectron. Reliab.*, vol. 58, no. 5, pp. 164–176, Mar. 2016.
- [3] H. Luo, X. Wang, C. Zhu, W. Li, and X. He, "Investigation and Emulation of Junction Temperature for High-Power IGBT Modules Considering Grid Codes," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 2, pp. 930–940, 2018.
- [4] H. Wu, V. Pickert, X. Deng, D. Giaouris, W. Li, and X. He, "Polynomial Curve Slope Compensation for Peak-Current-Mode-Controlled Power Converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 470–481, 2019.
- [5] L. F. S. Alves, P. Lefranc, P. O. Jeannin, and B. Sarrazin, "Review on SiC-MOSFET devices and associated gate drivers," *Proc. IEEE Int. Conf. Ind. Technol.*, vol. 2018–Febru, pp. 824–829, 2018.

- [6] T. D. Batzel and T. R. Leach, "Gate Drive and Efficiency Analysis for a Silicon Carbide MOSFET Based Electric Motor Drive," *5th IAJC-ISAM Int. Conf.*, 2016.
- [7] U. Karki and F. Z. Peng, "Precursors of Gate Oxide Degradation in Silicon Carbide MOSFETs."
- [8] P. Fiorenza, G. Greco, F. Giannazzo, F. Iucolano, and F. Roccaforte, "Effects of interface states and near interface traps on the threshold voltage stability of GaN and SiC transistors employing SiO₂ as gate dielectric," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.*, vol. 35, no. 1, p. 01A101, 2017.
- [9] N. S. Saks and A. K. Agarwal, "Hall mobility and free electron density at the SiC/SiO2interface in 4H-SiC," *Appl. Phys. Lett.*, vol. 77, no. 20, pp. 3281–3283, 2000.
- [10] N. Sghaier, J. Bluet, A. Souifi, G. Guillot, E. Morvan, and C. Brylinski, "Study of trapping phenomenon in 4H-SiC MESFETs: dependence on substrate purity," *IEEE Trans. Electron Devices*, vol. 50, no. 2, pp. 297–302, Feb. 2003.
- [11] P. Fiorenza et al., "Electrical characterization of trapping phenomena at SiO2/SiC and SiO2/GaN in MOS-based devices," *Phys. status* solidi, vol. 214, no. 4, p. 1600366, 2017.
- [12] H. C. P. Dymond *et al.*, "A 6.7-GHz Active Gate Driver for GaN FETs to Combat Overshoot, Ringing, and EMI," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 581–594, 2018.
- [13] K. Miyazaki *et al.*, "General-Purpose Clocked Gate Driver IC With Programmable 63-Level Drivability to Optimize Overshoot and Energy Loss in Switching by a Simulated Annealing Algorithm," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2350–2357, 2017.
- [14] N. Idir, R. Bausiere, and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 849–855, Jul. 2006.
- [15] M. Vamshi Krishna and K. Hatua, "Current controlled active gate driver for 1200V SiC MOSFET," pp. 1–6, 2016.
- [16] A. P. Camacho, V. Sala, H. Ghorbani, and J. L. R. Martinez, "A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9032– 9042, 2017.
- [17] P. Anthony, N. McNeill, and D. Holliday, "High-Speed Resonant Gate Driver With Controlled Peak Gate Voltage for Silicon Carbide MOSFETs," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 573–583, 2014.
- [18] B. Chen, "Isolated half-bridge gate driver with integrated high-side supply," *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.*, pp. 3615–3618, 2008.
- [19] I. Josifović, J. Popović-Gerber, and J. A. Ferreira, "Improving SiC JFET switching behavior under influence of circuit parasitics," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3843–3854, 2012.
- [20] R. Kelley, A. Ritenour, D. Sheridan, and J. Casady, "Improved twostage DC-coupled gate driver for enhancement-mode SiC JFET," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 1838–1841, 2010.