A Sinusoidal Current Driver With an Extended Frequency Range and Multifrequency Operation for Bioimpedance Applications

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***Abstract*—This paper describes an alternative sinusoidal current driver suitable for bioimpedance applications where high frequency operation is required. The circuit is based on a transconductor and provides current outputs with low phase error for frequencies around its pole frequency. This extends the upper frequency operational limit of the current driver. Multifrequency currents can be generated where each individual frequency is phase corrected. Analysis of the circuit is presented together with simulation and experimental results which demonstrate the proof of concept for both single and dual frequency current drivers. Measurements on a discrete test version of the circuit demonstrate a phase reduction from 25° to 4° at 3 MHz for 2 mAp-p output current. The output impedance of the current driver is essentially constant at about 1.1 MΩ over a frequency range of 100 kHz to 5 MHz due to the introduction of the phase compensation. The compensation provides a bandwidth increase of a factor of about six for a residual phase delay of 4°.**

***Index Terms*—Bioimpedance, current driver, feedback, multifrequency, phase compensation, phase error, wideband operation.**

I. Introduction

ACCURATE sinusoidal current drivers are required for bioimpedance applications including bioimpedance spectroscopy of biological tissues (e.g., for identifying cancers) and electrical impedance tomography for imaging [1], [2]. In some applications such as breast tissue characterization and imaging wideband operation is important [3], [4]. At higher frequencies restrictions in the generation of current into tissue via electrodes are encountered due to stray capacitance and limitations in the current driver performance [1]. Stray capacitance is a significant problem in some applications due to the use of one common current driver and multiplexing over lengths of cable to many electrodes [5]. An alternative method has each current driver closely connected to its electrode [6] and the stray capacitance effects are minimized but are always present to some degree.

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The upper frequency limitations in current driver performance are the phase delay of the output current and to a lesser extent the driver output impedance. Excessive phase delay can be a problem in accurate bioimpedance measurements, due to its use in synchronous/phase-sensitive demodulation/detection [7]. The Howland current driver circuit is in common use [8]–[13]. Ideally its output impedance is infinite, but in practice it depends on the specification of the opamps used and the degree of matching of the resistors in the positive and negative feedback paths [8]. It is well adapted to discrete designs, where the set of very accurate resistors required are readily available. Generalized impedance converter (GIC) circuits to minimize the effects of stray capacitance are often used to boost the output impedance of the Howland current driver and achieve wideband operation [9], [12]. In some applications, especially those employing active electrodes (requiring the electronics to be encapsulated within the electrode shell [6], [14]), it is an advantage to miniaturize the current drivers by employing integrated circuit designs [15]. A current driver topology suitable for integration has been described in [16]. It can provide the high output impedance required and high frequency operation, but its accuracy relies on an on-chip reference (sense) resistor which would need to be corrected by some means for high accuracy. An improved integrated circuit current driver based on [16] has been presented recently in [17]. It was implemented in a 0.6 μm high voltage CMOS technology. The upper frequency of operation of this circuit is limited by the phase delay present at high frequencies. A summary of available current drivers is detailed in [17].

The circuit proposed in this paper is a design based on a linear feedback circuit as in [16] but significantly reduces the output phase delay at high frequencies, allowing increased operational bandwidth for a given technology. In addition, the accuracy of the output current need no longer rely on the absolute value of a sense resistor, but can depend instead on the quality of matching of resistors on chip which is superior. The aim of this paper is to demonstrate the proof of concept of the proposed circuit.

The paper is organized as follows. A description of the principle and performance of the proposed current driver is presented in Section II. This is followed in Section III by details of the phase compensation circuit and then experimental results in Section IV. In Section V a dual frequency example with experimental results is presented. Finally, discussion and conclusion follow respectively in Sections VI and VII.

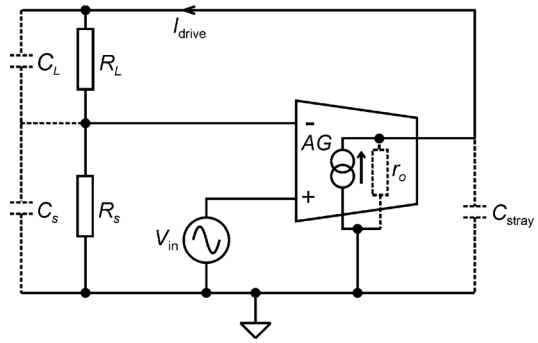

Fig. 1. Basic linear feedback current driver. Two gain stages are necessary in practice. A is a voltage amplifier and G a transconductor, r_o the output resistance of G, R_L the load resistor and R_s the sense resistor. C_s and $C_{\rm stray}$ are parasitic capacitances and C_L is the capacitance associated with the load.

II. Basic Current Driver

A. Linear Feedback Circuit

The principle used in the linear feedback current driver in [16] forms the basis of the alternative current driver. Fig. 1 shows the linear current driver circuit. In summary the drive current $I_{\rm drive}$ is

$$I_{\rm drive} = \frac{V_{\rm in}}{Z_s}\frac{1}{1+\frac{1}{AGZ_s}\left(1+\frac{Z_L+Z_s}{z_o}\right)} \tag{1}$$

where A is a voltage amplifier and G a transconductor, z_o the output resistance of G including $C_{\rm stray}$, Z_L the load and Z_s the sense impedance. The amplifier-transconductor AG has two poles one of which is dominant (low frequency). There are added poles associated with the capacitances shown in Fig. 1. By suitable choice of R_s the pole frequency of Z_s due to stray capacitance C_s can be made sufficiently high that at operational frequencies $Z_{\rm s}$ can be approximated to the resistance R_s. The stray capacitance $C_{\rm stray}$ associated with z_o must also be small to avoid significant extra phase delay in the loop gain. These limits can be achieved in the topology used in integrated circuits [17] where stray capacitances are typically below 1 pF. The capacitance C_L in the load impedance Z_L may have large values (nF), but provided $z_o \gg Z_L$ the influence of Z_L variations on the loop gain is small. The loop gain is then mainly influenced by the poles in AG.

Equation (1) can be simplified to

$$I_{\rm drive} = \frac{V_{\rm in}}{R_s}\frac{1}{1+\frac{1}{AGR_s}\left(1+\frac{Z_L+R_s}{r_o}\right)}. \tag{2}$$

For $r_o \gg Z_L + R_s$ and $AGR_s \gg 1$, $I_{\rm drive} = V_{\rm in}/R_s$. AG normally has two poles one of which is dominant to ensure stability. As frequencies approach their upper limit the output current phase delay increases depending on the designated phase margin. For example, in a typical second order circuit with feedback, when using a phase margin of 45° at a frequency of about 1/12 of the closed-loop bandwidth, the phase delay between input and output is 4° [18].

The load Z_L contributes an added inaccuracy in (2) which can be expressed as an output impedance $Z_{\rm out}$ where

$$Z_{\rm out} = r_o + (AGr_o + 1)R_s. \tag{3}$$

If $AGr_o \gg 1$ and $AGR_s \gg 1$

$$Z_{\rm out} = AGR_s r_o. \tag{4}$$

In (4) due to the low frequency dominant pole ω_d in the two pole loop gain AGR_s, the output impedance at high frequencies is not resistive but approximately a capacitance C_p where

$$C_p = \frac{1}{\omega_d R_s AGr_o}. \tag{5}$$

C_p can be in the order of 2–10 pF and is in addition to any added stray capacitances.

B. Alternative Feedback Current Driver

Fig. 2 shows an alternative circuit based on a voltage driver in [19] but designed to provide a current drive ($I_{\rm drive}$) rather than voltage drive by using a sense resistor R_s to monitor the current. The feedback principle is similar to the linear circuit of Fig. 1 and similar equations apply, but it has the advantage that the dominant pole required for stability does not affect its high frequency performance, although its transient response will be longer. The amplitude of the ac voltage across R_s is converted to a dc voltage $V_{\rm LP}$ by some form of rectification which can be a rectifier, peak detector, linear multiplier or a switching multiplier,[1] followed by a low pass filter (ac-dc). To introduce phase compensation and for a multiple frequency generator (considered in Section V) only the latter two types of multiplier (M_1 in Fig. 2) can be used. The multiplying function requires $\sin\omega t$ inputs at the desired frequency of operation. The resulting (dc) voltage $V_{\rm LP}$ is compared to the dc control voltage $V_{\rm cont}$ and amplified by A. The output of amplifier A is connected to input 1 of multiplier M_2. Input 2 is a sinewave at the desired operational frequency of $I_{\rm drive}$. The output of M_2 is an ac signal whose amplitude is controlled by the output of A. The output of transconductor G drives the load and R_s. The steady state ac output of G is unaffected by the dominant pole used in the integrator.

The dc component of the output of multiplier M_1 is respectively $0.5V_p$ for a linear and $(2/\pi)V_p$ for a switching multiplier, where V_p is the peak voltage of the input ac signal at terminal 1 of M_1. In the case of the linear multiplier a 2ω component must be attenuated to an acceptable level at the lowest expected operational frequency of $I_{\rm drive}$, otherwise harmonics with frequencies at ω and 3ω will appear at the output of transconductor G due to the multiplier M_2. Similar conditions would apply to the switching multiplier, but there are additional higher harmonics to attenuate.

Unlike the rectifier or peak detector, in the linear or switching multiplier version the accuracy of the conversion of the amplitude of the ac signal to the dc signal (ac-dc) is affected by the phase delay between inputs 1 and 2 of the multiplier M_1. This directly causes an added inaccuracy in $I_{\rm drive}$. In both types of

[1] A switching multiplier uses four switches to perform full wave rectification [20].

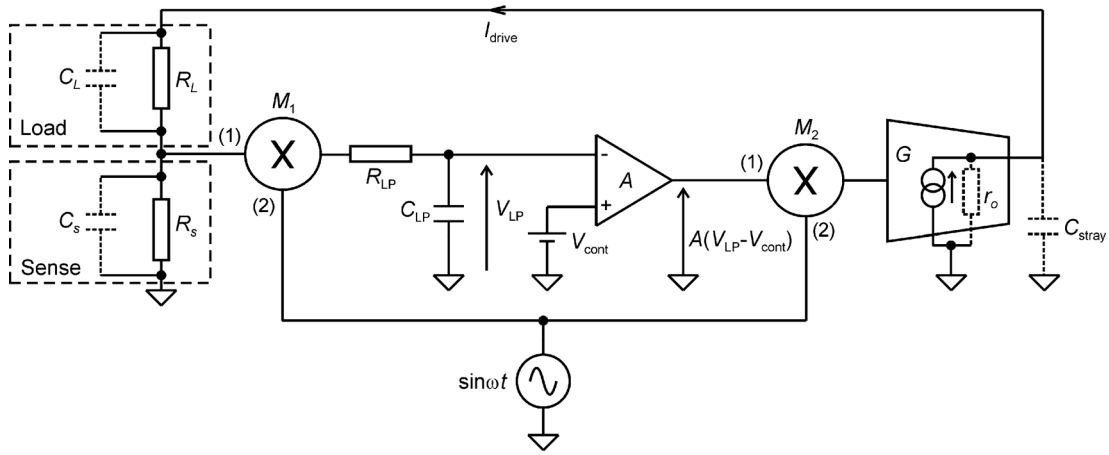

Fig. 2. Basic alternative current driver circuit.

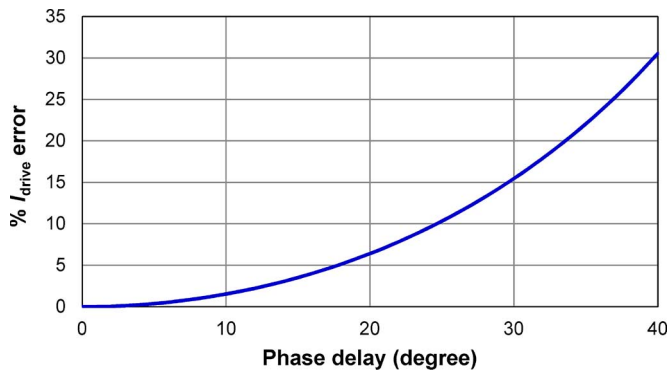

Fig. 3. % error in $I_{\rm drive}$ caused by phase delay between the two multiplier inputs in the ac-dc converter.

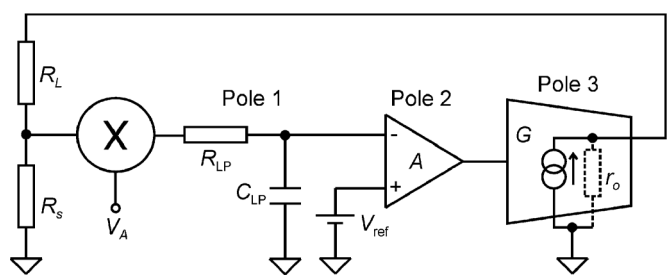

Fig. 4. Linear equivalent used to check the transient response and stability.

multiplier, when there is a phase delay ϕ between inputs 1 and 2 of M_1, the ac-dc transfer is reduced by a factor $\cos\phi$. The error in $I_{\rm drive}$ is inversely proportional to $\cos\phi$ and is shown in Fig. 3.

For the higher frequencies the phase delay due to M_2 and G will be large near their pole frequency. Fig. 3 shows the % error in $I_{\rm drive}$ amplitude due to the phase delay in M_2 and G. For a 0.25% error a phase delay of $<4^\circ$ is necessary and the highest operational frequency would be restricted to about one tenth of the pole frequency of the transconductor G. To ensure accurate ac-dc conversion at high frequencies phase compensation is a necessary requirement.

C. Transient Response and Harmonic Distortion

In Fig. 2 because the transient response of the circuit is relatively slow compared with the high frequencies at the output of the transconductor G the stability of the circuit can be considered by use of a conventional linear equivalent shown in Fig. 4, which is similar to that in Fig. 1. In Fig. 2 at low frequencies the components M_2, G and M_1 combined with the integrator $R_{\rm LP}$ and $C_{\rm LP}$ can be replaced in Fig. 4 by the integrator ($R_{\rm LP}$ and $C_{\rm LP}$) and transconductor (G). The linear equivalent circuit is valid provided the transient response operates over more than about 10 cycles of the frequency of $I_{\rm drive}$. Pole 1 provides the integrator function, pole 2 is caused by the dc (or baseband) amplifier A and pole 3 is a relatively high frequency in the transconductor. V_A is the 0.5 dc attenuation factor due to the multiplier M_1 in Fig. 2. Pole 1 is primarily used to filter out the unwanted frequency component at the output of M_2. The addition of pole 2 can be advantageously used to significantly increase the suppression of the unwanted 2ω component at the output of M_1 (Fig. 2). As it has potential to cause feedback instability a balance must be struck between 2ω signal suppression and suitable phase margins.

Fig. 5 shows an example of the improvement of the harmonic distortion. Fig. 5(a) shows distortion for single pole feedback and Fig. 5(b) for two pole feedback with a phase margin of 45°. The operational frequency of $I_{\rm drive}$ is 100 kHz. For one pole feedback there is a 300 kHz harmonic with attenuation of 1/400 and a further 500 kHz harmonic attenuated by 1/322000. The 300 kHz harmonic causes a 400 kHz component at the output of multiplier M_1 (Fig. 2) and a 500 kHz component at the output of multiplier M_2 (Fig. 2). For two pole feedback the 300 kHz is attenuated by 1/102000, and any 500 kHz component is below the noise in the FFT (fast Fourier transform). This result shows the significant improvement in harmonic distortion possible when using a two pole system. However, in general it extends the transient step response time by a factor of about 3. This factor is essentially independent of the loop gain or dominant pole. In the case of the simulated results shown in Fig. 5, where the dominant pole is 15.9 Hz and the loop gain is 200 V/V, for a phase margin of 45° the times to settle to within 0.05% of the final value were 414 μS and 1200 μS for one pole and two poles, respectively. The steady state high frequency performance is not affected. The harmonic distortion is less at higher operating frequencies.

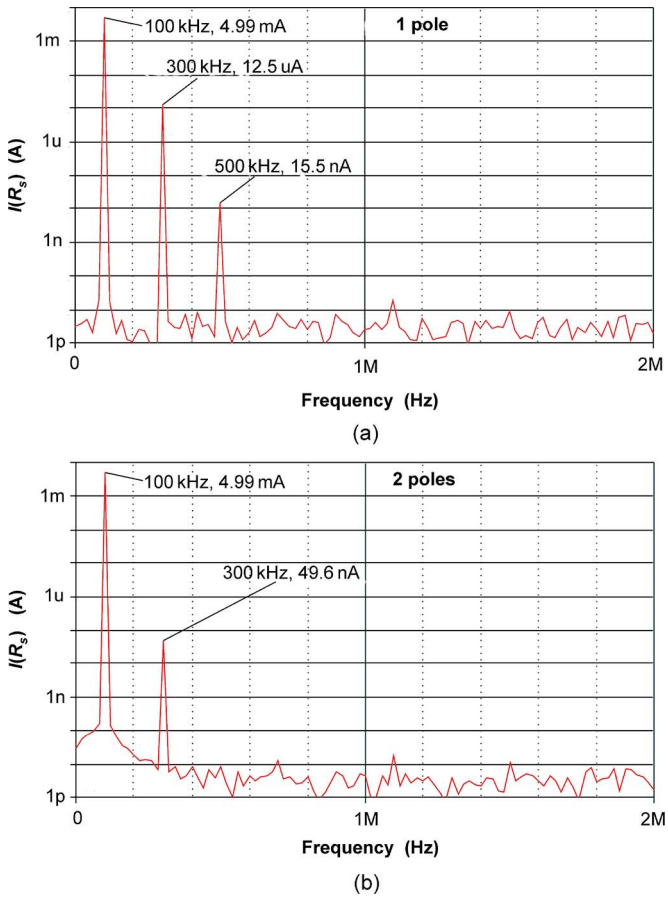

Fig. 5. Simulated FFTs of the current in the sense resistor R_s showing the harmonics generated using feedback with (a) one pole and (b) two poles.

III. Phase Compensation

A. Circuit Design

As shown in Fig. 3 the phase delay of M_2 and G will significantly affect the accuracy of the drive current I_{drive} at higher frequencies when using the multiplier in ac-dc converters. To extend the accuracy of I_{drive} at the higher frequencies its phase delay must be reduced. Fig. 6 shows a circuit which significantly reduces the phase delay of I_{drive} to beyond the pole frequencies of (M_2, G_1) and (M_4, G_2). In Fig. 6 the upper circuit with M_1 and M_2, driven by $\sin \omega t$, is the basic current generator supplying the current into the load (R_L, C_L) as in Fig. 2. The lower circuit, which is nearly identical to the upper circuit but has multipliers M_3 and M_4 driven by $\cos\omega t$ and zero control voltage, provides delay compensation. The voltage across the sense resistor R_s is applied to input 1 of M_3. The circuit with M_3 and M_4 senses the amplitude of the out-of-phase component of the voltage across R_s and generates an amplified version of it. The output of transconductor G_2 is added to the output of G_1 and by feedback (nearly) cancels out the out-of-phase component of the voltage across R_s.

B. Analysis of the Phase Compensation

For efficient compensation G_1 and G_2 must be well matched. The output current of G_2 is then always at 90° to G_1 at all frequencies. For tractable analysis it is assumed that amplifiers $A\,(A_1, A_2)$, linear multipliers $M\,(M_1 - M_4)$, and transconductors $G\,(G_1, G_2)$ are ideal and that there are poles ω_0 in G_1 and G_2. The effect of r_o in the transconductors is ignored.

The upper and lower circuits process the sine and cosine signals separately. For the lower circuit assume there is an out-of-phase voltage across R_s due to the current from G_1. That is

$$IR_s\cos(\omega t - \phi) = IR_s(\cos\omega t\cos\phi + \sin\omega t\sin\phi) \tag{6}$$

where I is the amplitude of the current from G_1 and

$$\phi = \tan^{-1}\left(\frac{\omega}{\omega_0}\right). \tag{7}$$

Considering the out-of-phase feedback loop, let a dc voltage at the input 1 of A_2 be V_x. The output current of G_2 is

$$-AGV_x\cos(\omega t - \phi) = -AGV_x(\cos\omega t\cos\phi + \sin\omega t\sin\phi) \tag{8}$$

where the magnitude response of G is

$$|G| = \frac{G_o}{\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}} \tag{9}$$

and G_o is the dc transconductance. The voltage across R_s as a result of the addition of the currents from G_1 and G_2 is

$$IR_s(\cos\omega t\cos\phi + \sin\omega t\sin\phi) - AGV_xR_s(\cos\omega t\cos\phi + \sin\omega t\sin\phi). \tag{10}$$

Equation (10) is the voltage input to terminal 1 of M_3. The output voltage of M_3 is

$$IR_s\cos\omega t\,(\cos\omega t\cos\phi + \sin\omega t\sin\phi) - AGV_xR_s\cos\omega t\,(\cos\omega t\cos\phi + \sin\omega t\sin\phi). \tag{11}$$

The dc component of the output of M_3 extracted by the low pass filter (R_{LP2} and C_{LP2} in Fig. 6) is

$$V_{\text{LP2}} = \frac{1}{2}(IR_s\cos\phi - AGV_xR_s\cos\phi). \tag{12}$$

Equating V_{LP2} to V_x and rearranging

$$V_x = \frac{1}{2}IR_s\frac{1}{1 + \frac{AGR_s\cos\phi}{2}}\cos\phi. \tag{13}$$

The out-of-phase voltage component in (10) is

$$IR_s\cos\omega t\cos\phi - AGV_xR_s(\cos\omega t\cos\phi). \tag{14}$$

Combining (13) and (14) the out-of-phase component is modified to

$$IR_s\left(1 - \frac{\frac{AGR_s\cos\phi}{2}}{1 + \frac{AGR_s\cos\phi}{2}}\right)\cos\omega t\cos\phi. \tag{15}$$

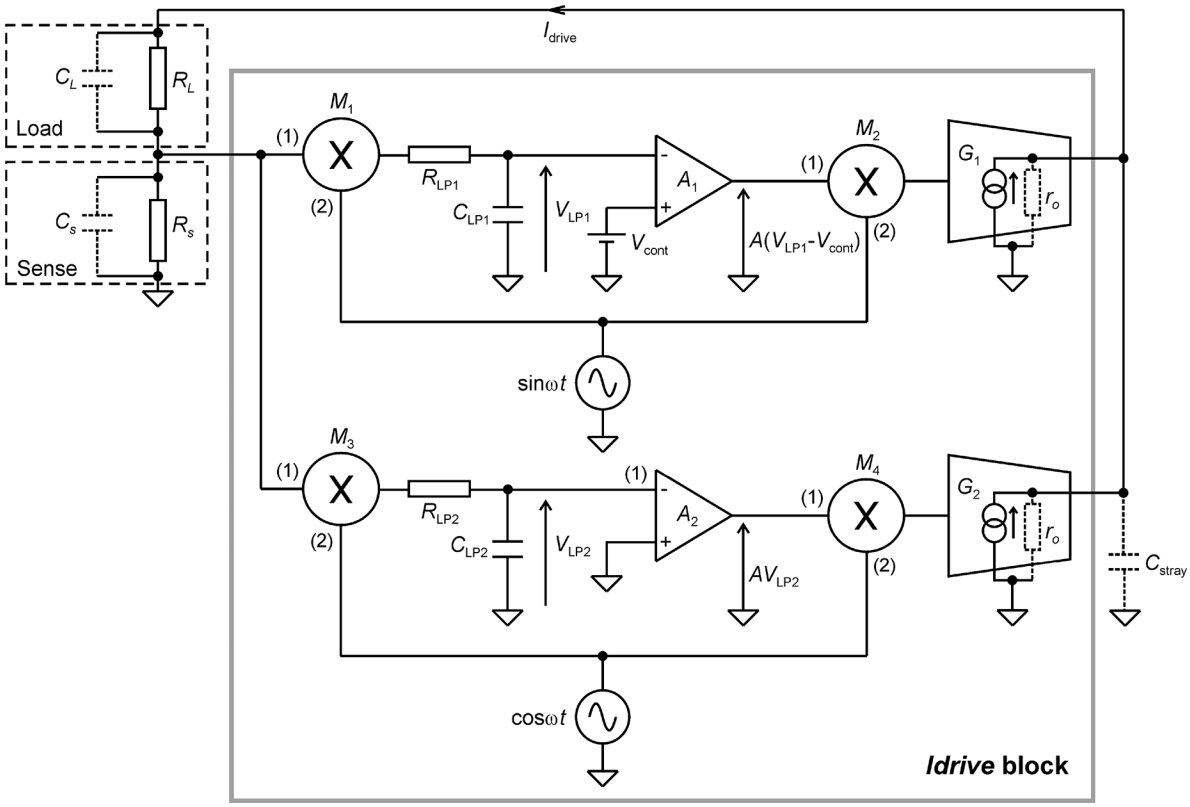

Fig. 6. Adding a compensating circuit to cancel the phase delays in M_2 and G_1.

If $AGR_s \cos\phi \gg 1$ the out-of-phase component is cancelled. Note that G and ϕ are functions of ω and the $AGR_s \cos\phi$ will reduce with frequency.

In (10) there is an added in-phase component

$$IR_s \sin\omega t \sin\phi - AGV_x R_s \sin\omega t \sin\phi. \tag{16}$$

Combining (13) and (16) the added in-phase component is

$$IR_s \left(1 - \frac{\frac{AGR_s \cos\phi}{2}}{1 + \frac{AGR_s \cos\phi}{2}}\right) \sin\omega t \sin\phi. \tag{17}$$

If $AGR_s \cos\phi \gg 1$ the in-phase component is cancelled. Since the out-of-phase component has been cancelled and the voltage across R_s is now in phase, the current in R_s will be substantially constant over a wide frequency range provided $AGR_s \cos\phi \gg 1$ still applies.

Simulation results of the circuit in Fig. 6 are shown in Fig. 7. The simulation used ideal amplifiers, linear multipliers and transconductors. In each transconductor a pole was inserted using single *RC* low pass filters. The poles (1.6 MHz) were chosen so that a 2 MHz sinewave without compensation was heavily delayed to better illustrate the operation. Fig. 7(a) shows how the two currents from transconductors G_1 and G_2 combine in the sense resistor R_s to provide an accurate in-phase current (I_{drive}). Fig. 7(b) shows the sinewave input to multipliers M_1 and M_2 for reference.

Fig. 8 demonstrates in simulation the cancellation over a wide frequency range using ideal components but with 1.6 MHz poles

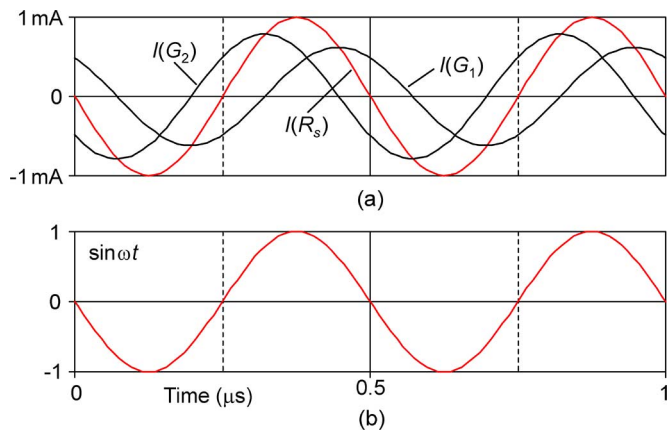

Fig. 7. Simulated waveforms demonstrating phase compensation. (a) Out-of-phase currents from transconductors G_1 and G_2, and the phase corrected current through R_s. (b) Reference 2 MHz sinewave.

added to G_1 and G_2. Fig. 8(a) shows how the error in I_{drive} amplitude due to phase delay in the ac-dc transfer is significantly reduced with compensation (the amplitude is 1.2% lower at 5 MHz compared with that at 100 kHz). The phase cancellation is shown in Fig. 8(b).

C. *Effect of Stray Capacitance*

The compensating circuit cancels out any potential phase delay in the current flowing through the sense resistor R_s. Fig. 9 shows the equivalent circuit associated with the sense resistor as used in the circuit of Fig. 6. The effect of C_s, which takes some of the current from R_s can be minimized by suitable choice of

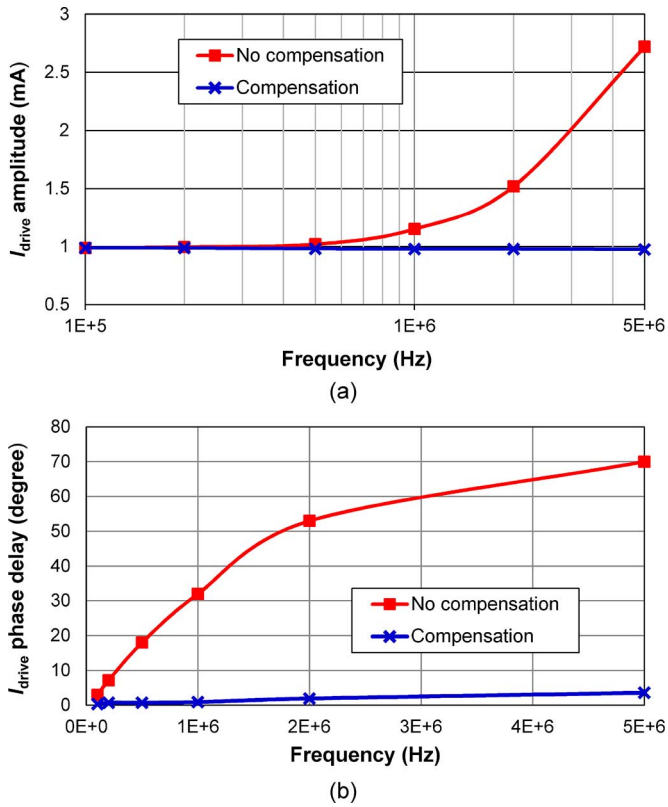

Fig. 8. Simulated results with and without compensation. G_1 and G_2 had poles at 1.6 MHz. (a) Effect of compensation on output current $I_{\rm drive}$. (b) Effect of compensation on phase delay of $I_{\rm drive}$.

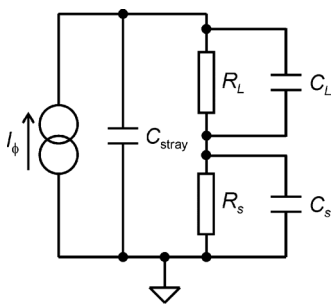

Fig. 9. Effect of stray capacitance. I_ϕ is a current generator with phase delay.

R_s. For phase delay test purposes in the discrete measurements $C_L = 0$. The compensating circuit cancels phase delays both due to the delayed current I_ϕ and the effect of $C_{\rm stray}$. Their relative values will depend on the circuit topology. In the discrete test circuit described in Section IV[2] the main delay is due to $C_{\rm stray}$ which includes the effect of printed circuit board tracks, interconnections and transconductor outputs. In integrated circuit designs (e.g., [17]) $C_{\rm stray}$ will be very much lower, and the delays in the transconductors are more significant. The compensating circuit will reduce the delay whether due to $C_{\rm stray}$ and/or transconductors.

[2]Due to relatively large stray capacitances the discrete component circuit described in Section IV cannot be an exact replica of an integrated circuit version in terms of performance.

IV. Experimental Results

A. Circuit Design

As a proof of concept, discrete test measurements were made using the circuit of Fig. 10 implemented on a two-layer printed circuit board using available components with regulated power supplies of ± 5 V. The multiplier AD835 has -3 dB bandwidth of 250 MHz. This ensures an accurate multiplication over the desired operating frequency range of the current driver (100 kHz to $\geq$5 MHz). The transconductor OPA861 has a -3 dB bandwidth of about 75 MHz with a load resistance of 500 Ω. The associated parasitic capacitances added in the construction of the circuit in Fig. 10 together with the resistive load (1.7 kΩ) reduced the bandwidth associated with the two transconductors to approximately 5.5 MHz (sufficient for demonstration of phase reduction at $>$1 MHz). In the low frequency section, the LM741 opamp had a feedback gain of 200 V/V and a pole at approximately 5 kHz. This provided a useful second pole for improved harmonic attenuation (see Section II-C). The $\sin \omega t$ and $\cos \omega t$ voltage input signals were generated by a TTi TGA12104 waveform generator. The oscilloscope was Agilent MSO-X 2024A. It was connected via a matched 50 Ω cable. A second scope input recorded the $\sin \omega t$ signal for reference. The value of the sense resistor included the 50 Ω. All multipliers and amplifiers were trimmed to minimize any dc offsets.

Fig. 11 shows oscilloscope traces demonstrating phase reduction of the current in the sense resistor. The phase delay of the current is reduced from 25°to 4°at the operating frequency of 3 MHz.

Fig. 12(a) shows the effects of phase compensation on the drive current (measured as peak-peak voltage, Vp-p, across 50 Ω). The phase reduction at higher frequencies is shown in Fig. 12(b). While the phase compensation demonstrates reduction at the higher frequencies, the reduction is noticeably less compared with the simulated example in Fig. 8 which uses ideal components. However, from Fig. 12(b) without compensation the 4° phase delay occurs at below 500 kHz (which will cause an amplitude error due to ac-dc conversion of about 0.25%) while with compensation a 4° phase error occurs at 3 MHz, representing an increase in bandwidth of a factor of about 6.

Fig. 13 shows the peak drive current I_p in R_s versus the applied control voltage $V_{\rm cont}$ measured at a frequency of 100 kHz. The slope should be $2/R_s = 1/100$. The estimated error due to the feedback gain and phase delay is 0.5%. The 6% error shown is attributed to errors in the ac-dc transfer linear multiplier M_1. The phase of the current changes with the polarity of $V_{\rm cont}$.

The output impedance from (4) applies, but there is no dominant pole involved. For a loop gain AGR_s of 200 V/V and a measured transconductor (AD861) output resistance in the region of 20 kΩ, the predicted maximum output impedance of the test current driver in Fig. 10 is 2 M Ω (note in Fig. 10 there are two transconductor outputs in parallel). Since the effect of C_s is minimized by the phase compensation, the measured

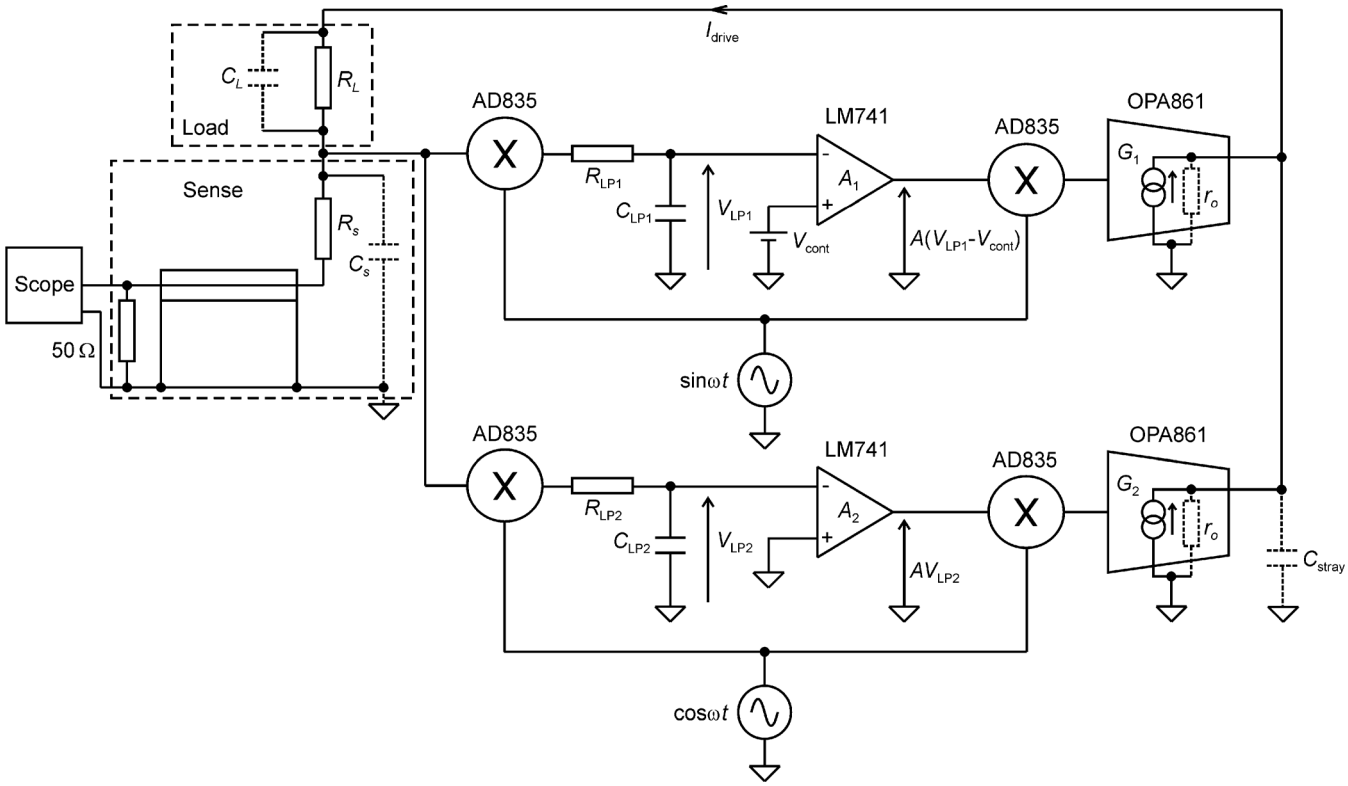

Fig. 10. Discrete test circuit. Voltage amplifiers A_1 and A_2 have feedback gains of 200 V/V and poles 5 kHz, with additional circuits to adjust dc offsets. R_s = 200 Ω, R_L = 1.5 kΩ, G_1 = G_2 = 10 mA/V. Low pass poles (LP) = 15.9 Hz. Multipliers and transconductors were installed following manufacturer instructions.

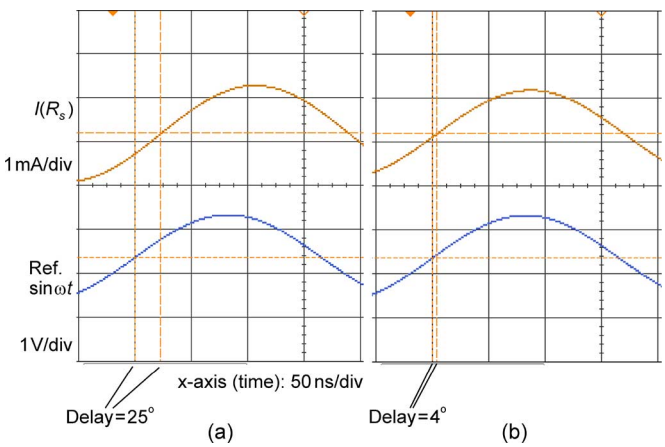

Fig. 11. Scope traces showing phase delays of the current trough R_s for a 3 MHz sinewave. (a) With no compensation. (b) With compensation.

output impedance of the current driver (obtained using the method described in [17]) was essentially constant over the measured frequency range of 100 kHz to 5 MHz (measured at spot frequencies of 100 kHz, 500 kHz, 1 MHz, 2 MHz and 5 MHz). Its mean value was 1.1 M Ω with an accuracy of ±40%. The spread is due to the practical difficulty in measuring very small differences between two large numbers with the available test equipment. Note that for circuit topologies such as in [17] the effect of associated parasitic capacitance is not automatically minimized.

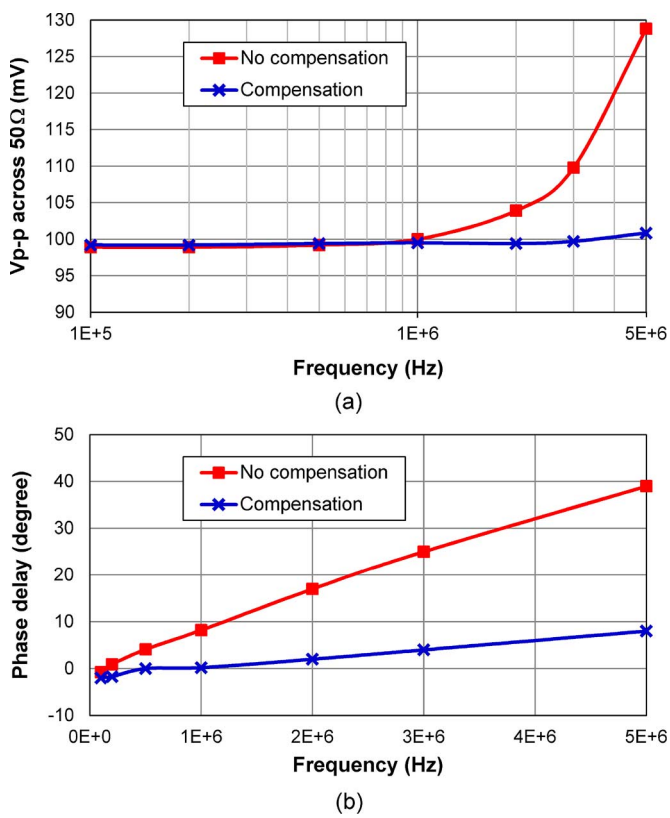

Fig. 12. Variation of output amplitude (a) and phase (b) with frequency, with and without phase compensation.

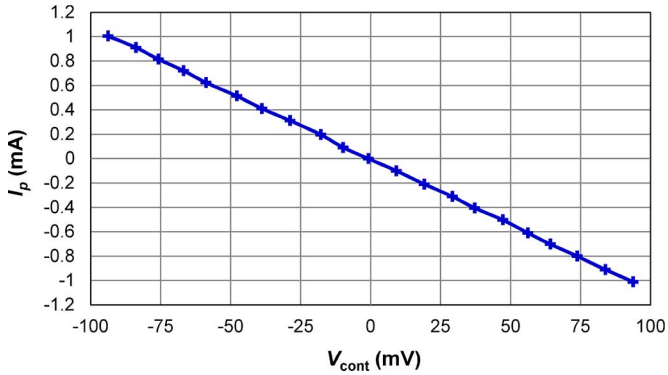

Fig. 13. Variation of peak amplitude of the ac drive current with control voltage $V_{\rm cont}$.

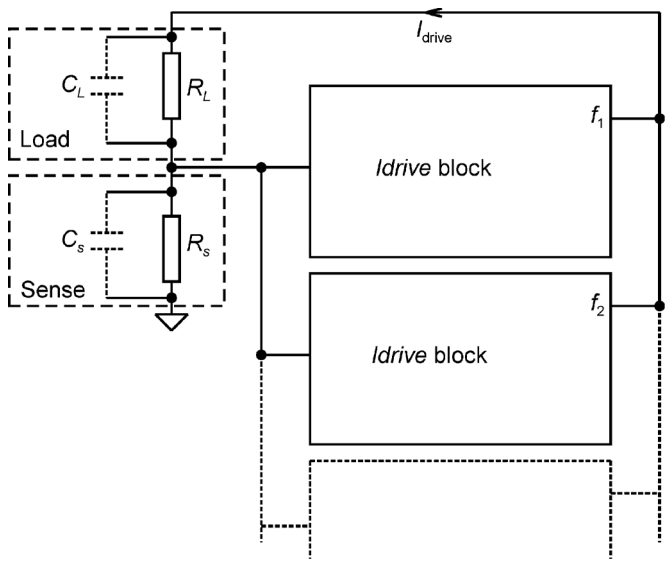

Fig. 14. Multifrequency current generator circuit.

V. Multifrequency Circuit

A. Circuit Design

Multifrequency currents can be generated by adding extra *Idrive* blocks as shown in Fig. 14, each operating at a different frequency. The summed currents flow through R_L and R_s. Each block selects its current component frequency in R_s and provides appropriate feedback. In this way each *Idrive* block compensates for any phase delays at its stated frequency. Note that the integrators in each block must adequately attenuate any signals caused by frequency differences between blocks. For example the first multipliers of *Idrive*-f_1 (M_1, M_3 Fig. 6) will have a component $(f_2 - f_1)$ at their outputs which must be suitably attenuated by the integrators.

B. Experimental Dual-Frequency Results

Two *Idrive* blocks each using the circuit of Fig. 6 with frequencies 1 MHz and 5 MHz, (chosen to emphasize the effect of phase delay) were connected as in Fig. 14. Fig. 15 shows the FFTs of the voltage across R_s and the compensation obtained. The spectrum analyzer was Agilent E4411B. The transconductor currents are added halving the output resistance (the currents could be added before the final stage so that a high output resistance (Fig. 6) is maintained). In Fig. 15(b) due to phase delay at 5 MHz the uncompensated amplitude of the measured current is 2.9 dB higher than that at 1 MHz. In Fig. 15(c) the difference has been reduced to 0.3 dB as a result of phase compensation. The compensation performance is not affected when operating with dual (or more) frequencies.

VI. Discussion

The circuit examined is particularly suitable for higher frequency integrated circuit applications. Although discrete circuits were used to demonstrate the operation for both single and dual frequency current drivers, the relative complexity of the circuits and the need for well-matched transconductors favors an integrated circuit design. The high frequency performance is isolated from the stability of the feedback. The loop gain is a combination of the dc amplifier and the ac transconductor gain. The balance of gains between the two can take account of the different design demands of the dc amplifier and the high frequency transconductor.

The low frequency, low pass filter necessary for integration and suppression of harmonics results in a relatively high operational low frequency limit and a slow transient response compared with the linear current generator (Fig. 1). However, the peaking of the $I_{\rm drive}$ at high frequencies caused by low phase margin in the linear feedback circuit does not occur in the proposed current driver. In multifrequency applications there is a minimum frequency difference allowed which is dictated by the low pass filter in the ac-dc function.

In simulation phase cancellation is shown to be almost complete over frequencies to above the pole frequencies of the transconductors G_1 and G_2. For frequencies near the pole frequencies in the discrete circuit tests, while still producing appreciable phase reduction, the phase cancellation is less than the simulation results. Simulation suggests that this is due to parasitic capacitances (e.g., $C_{\rm stray}$ in Fig. 9) as a result of the discrete nature of the circuit and mismatch of the value of the transconductors G_1 and G_2 (Fig. 10). When designing an integrated circuit version these limitations will be further explored.

The circuit relies on an accurate ac-dc converter. In the discrete proof of concept version the multiplier used in the conversion is analog (AD835). For accurate conversion the multipliers M_1 and M_3 (Fig. 6) in the ac-dc converter must have very low phase difference (e.g., $<4^\circ$) between their two sinusoidal inputs. This is conveniently provided by the added compensation circuit. A switched multiplier version in an integrated circuit can provide suitable rectification without the dc offsets and gain errors expected in an analog multiplier. A second component of the ac-dc converter is the provision of a low frequency pole to provide the integration. Shown as a separate component to the dc amplifier in Fig. 2 the low frequency pole (and any second pole) can be a part of the dc amplifier design. In an integrated circuit implementation the design must take into consideration the minimization of dc offsets (e.g., by the use of chopping or autozeroing [20]). For example, in Fig. 10 using a 200 Ω sense resistor (R_s), a 10 μV input dc offset in the dc amplifier (A) is equivalent to $V_{\rm cont} = 10$ μV, and will generate an ac current error of 0.1 μA amplitude. In the discrete component design the dc offsets were trimmed out.

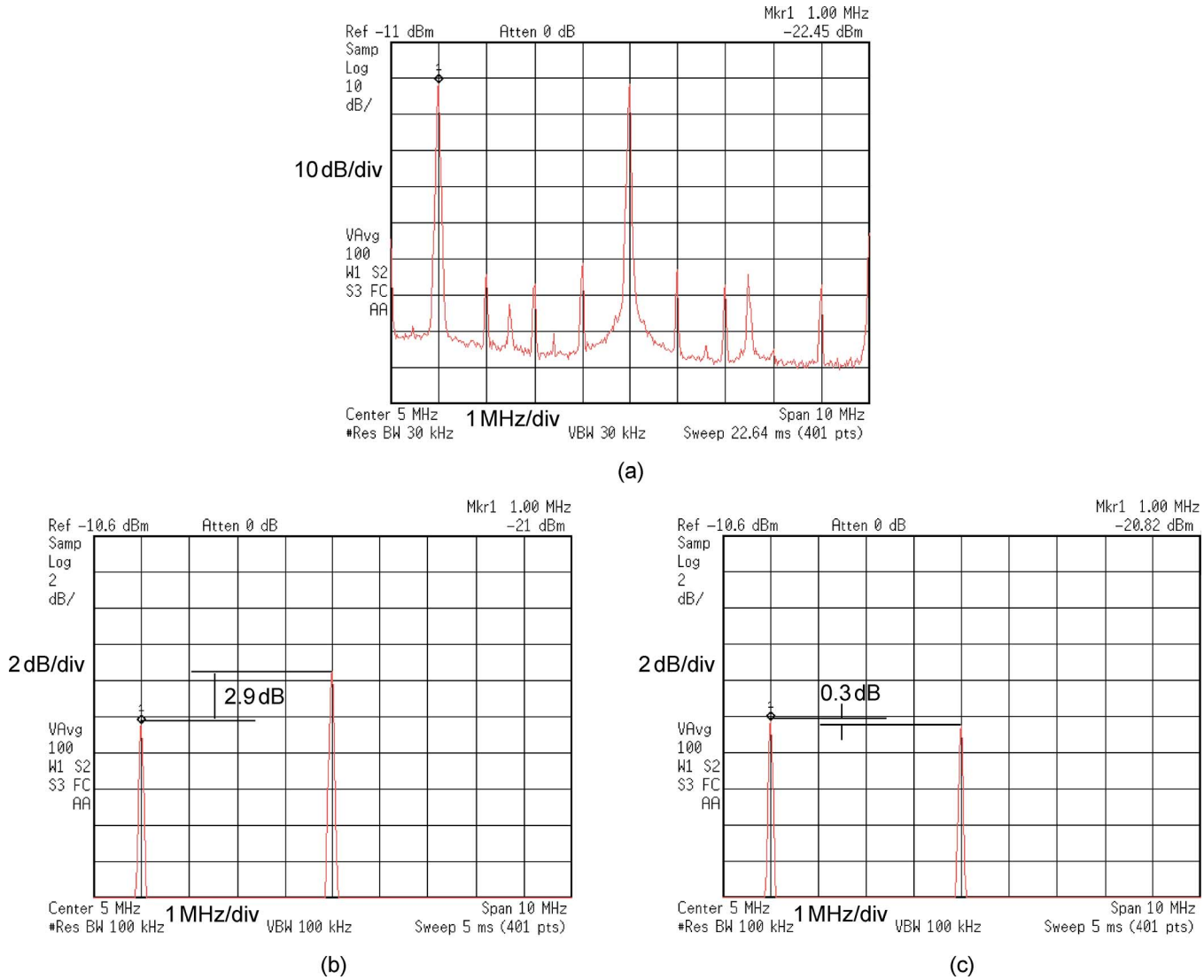

Fig. 15. (a) Two sinewaves at 1 MHz and 5 MHz with compensation. Two sinewaves at 1 MHz and 5 MHz showing the effect of compensation: (b) without compensation (zoomed in), (c) with compensation (zoomed in).

TABLE I
COMPARISON OF BANDWIDTH AND OUTPUT IMPEDANCE

	[9]	[13]	[15]	[22]	[17]	This work
Architecture	Modified Howland with GIC	Modified Howland	Differential Transconductor	Current Conveyor	Linear Feedback	Nonlinear Feedback
Bandwidth	10 Hz – 2.2 MHz	1 kHz – 1 MHz	10 kHz – 1 MHz	10 kHz – 250 kHz	> 500 kHz	100 kHz ~ 5 MHz
Output Impedance	11 MΩ @ 100 kHz 1 MΩ @ 2.2 MHz	670 kΩ @ 100 kHz 70 kΩ @ 1 MHz	>1 MΩ @ 100 kHz > 500 kΩ @ 500 kHz	149 kΩ @ 100 kHz < 30 kΩ @ 500 kHz	665 kΩ @ 100 kHz 372 kΩ @ 500 kHz	1.1 MΩ @ 100 kHz 1.1 MΩ @ 5 MHz

The amplitude of $I_{\rm drive}$ has been controlled here by a dc voltage source $(V_{\rm cont})$. The absolute value of a resistor fabricated in an integrated circuit is inaccurate [21]. By replacing the (dc) voltage control with a (dc) current control through an on-chip resistor whose value is matched to the sense resistor (R_s), the sinusoidal output current $I_{\rm drive}$ is related to the dc control current with the much superior matching between resistors on chip. At high frequencies the output impedance of the linear feedback circuit is an equivalent capacitance caused by the low frequency dominant pole (4). In the proposed circuit it is the high frequency pole of the output transconductor G (Fig. 2) which is relevant and the resulting equivalent capacitance is very small (however, there will still be stray capacitance (Fig. 9) which cannot be ignored).

The variation of the loop gain of the transconductors (e.g., due to power supply variations) is a function of the value of G. Provided the loop gain (AGR_s) is high this variation will be small in negative feedback. In this test discrete design the power supply was regulated.

Table I provides a comparison with previous work. The discrete implementation of the proposed current driver features a wide bandwidth (100 kHz to 5 MHz) and a large, constant

(1.1 MΩ) output impedance due to the introduction of the phase compensation. From (4) the output impedance can be increased by: i) increasing the loop gain, ii) increasing the output resistance of the transconductors G_1 and G_2 (Fig. 6), and iii) summing the output of the multipliers M_2 and M_4, enabling the use a single transconductor.

VII. Conclusion

An alternative sinusoidal current driver circuit suitable for bioimpedance measurement applications has been described. It can provide current outputs with low phase error for frequencies near the pole frequency of the transconductor, thus extending the upper frequency operational limit of the current driver. Measurements on a test version using discrete components show that for a 4°phase delay (from an uncompensated phase delay of 25°) there is an increase in bandwidth of a factor of about six. Multifrequency currents can be generated where each individual frequency is phase corrected. While a discrete version of the circuit has demonstrated the proof of concept, the circuit is more suited to an integrated circuit design due to its complexity. Future work will focus on an integrated circuit implementation of the alternative current driver.

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