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Hybrid Methods for Function Generation

- by -

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SUMMARY

A method of function generation is discussed based on the use of hybrid digital analogue techniques.

A brief description of a quantizer is given together with some experimental results. The purpose of this unit is to give the derivative with respect to time (in quantized form) of a variable. Units of this type used in conjunction with pulse modulators, which are also described, are shown to be capable of performing a wide variety of analytic functions. The application to correlation functions, using magnetic core storage for time delays, is also discussed.

Another application is a fast analogue/digital converter with an incremental bit resolution time of one micro-second.

The possibility of extending the application to generation of arbitrary functions of one or more variable is considered and one possible form of instrumentation, based on the use of magnetic core storage, is described.

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1. Introduction

With conventional analogue techniques the multiplication of two or more variables, generation of functions of one or more variables and the simulation of dead time (transportation lag), present a difficult problem usually requiring special computing devices for each particular case.

The aim of this paper is to extend the ideas, outlined in references 1 and 2, as a method of overcoming some of the difficulties associated with pure analogue or continuous variable simulation techniques.

The basic idea is to effect the differentiation with respect to time of a variable, say x , in discrete digital form, i.e. $\frac{\delta x}{\delta t}$. If such a signal is used to modulate another signal representing a variable y , then the output of the modulator is $y \frac{\delta x}{\delta t}$. If this output signal is integrated with respect to time the result is $\int y \cdot \frac{\delta x}{\delta t} dt \doteq \int y dx$.

The facility for generating the function $y \cdot dx$ provides a basis for function generation similar to that which may be achieved by a mechanical differential analyzer, but at a significantly higher computing rate.

2. Generation of Functions by Integration Techniques

As already stated the basic problem is to generate the function $\int y \cdot dx$ which involves the multiplication of y by dx and then integration of the result. This combined operation is the basis of the conventional D.D.A. (incremental) computer.

In the method presented in this paper the function $\int y \cdot dx$ is derived in an approximate manner, from the function $\int y \cdot \frac{\delta x}{\delta t} \cdot dt$, with the restriction imposed that the variables x and y must be single-valued functions of the independent variable, time.

The generation of $\frac{\delta x}{\delta t}$ is based on sampling and quantizing the variable x , in that it is measured only at discrete time intervals separated by $\delta t = T$ (where $\frac{1}{T}$ = sampling rate) and in discrete amplitude steps $\delta x = \pm q$, where q is a constant quantization level. It is necessary therefore, that the amplitude change in x should be less than one step or quantum q in the time T .

$$\text{i. e. } \frac{q}{T} > \left(\frac{dx}{dt} \right)_{\max} \quad (2.1)$$

In fact as discussed later,

$$\frac{q}{T} > 2 \left(\frac{dx}{dt} \right)_{\max} \quad (2.2)$$

If this condition is satisfied, δx may be expressed in the form

$$\delta x = q \cdot u_x \quad (2.3)$$

where u_x is a train of impulses occurring at discrete time intervals T , having unit

magnitude and constant width (less than T) and with positive or negative sign according to the time rate of change of x (see Fig. 1).

Thus

$$\frac{\delta x}{\delta t} = \frac{q}{T} u_x = a u_x \quad (2.4)$$

where a is a constant = $\frac{q}{T}$. (2.5)

The variable x may be reconstituted for the signal u_x by integration with respect to time i. e.

$$a \int u_x dt = \int u_x \cdot a \cdot dt \doteq \int \frac{\delta x}{\delta t} dt \doteq \int dx = x. \quad (2.6)$$

It should be noted that this integration process implies a zero initial condition for x. For a finite initial condition a constant must be added.

The multiplication $\frac{1}{a} y \cdot \frac{\delta x}{\delta t}$ is achieved in a modulator unit, which modulates the signal y by the signal ku_x to give an output signal $y \cdot u_x$. Note k is a scaling constant to suit circuit conditions. This modulator unit is basically a sampling switch giving samples of y of width T modified by the sign of u_x (see Fig. 1).

The function $\int y \cdot dx$ is derived by integrating the product $y \cdot u_x$ with respect to time in a conventional analogue integrator, having a time constant = $\frac{1}{a}$ so that

$$\int y \cdot dx \doteq a \int y \cdot u_x dt. \quad (2.7)$$

In special cases in which y is also in digital form the integrator may be in the form of a reversible digital counter.

The three basic computing units proposed are therefore as follows:-

- (i) a quantizer Q which for an input variable x, gives an output = $k_1 \frac{\delta x}{\delta t} = k_1 a u_x = ku_x$.
- (ii) a modulator M, giving an output signal $y \cdot u_x$, where y and $u_x \cdot k$ are input signals.
- (iii) an integrator I, which in general will be a conventional analogue device with a time constant = $\frac{1}{a}$.

These units are shown diagrammatically in Fig. 1. The pulse train of the quantizer is shown in more detail in Fig. 5, and comprises the two waveforms F and G. The negative and positive impulses are separated for convenience of circuit conditions. Typical detailed waveforms involved in the modulator are shown in Fig. 7.

Four simple applications of such units are illustrated in Fig. 2.

(a) Multiplication of two variables x and y,

i. e. $xy = \int \left(x \frac{dy}{dt} + y \frac{dx}{dt} \right) dt \doteq a \int (x u_y + y \cdot u_x) dt. \quad (2.8)$

(b) Differentiation of y with respect to x, i. e. $\frac{dy}{dx}$,

$$\frac{dy}{dx} = \frac{dy}{dt} \div \frac{dx}{dt} \doteq \frac{1}{a u_x} \frac{dy}{dt} = u_x \cdot \frac{1}{a} \frac{dy}{dt}. \quad (2.9)$$

(c) Function of n variables including independent variable time,

i.e. $f(x_1, x_2, \dots, x_n, \dots, t)$,

$$f(x_1, x_2, \dots, x_n, \dots, t) = \int \left[\frac{\partial f}{\partial x_1} \cdot \frac{dx_1}{dt} + \frac{\partial f}{\partial x_2} \cdot \frac{dx_2}{dt} + \dots + \frac{\partial f}{\partial x_n} \cdot \frac{dx_n}{dt} + \frac{\partial f}{\partial t} \right] dt$$

$$\doteq a \int \left[\frac{\partial f}{\partial x_1} \cdot u_{x_1} + \frac{\partial f}{\partial x_2} \cdot u_{x_2} + \dots + \frac{\partial f}{\partial x_n} \cdot u_{x_n} + \frac{1}{a} \frac{\partial f}{\partial t} \right] dt \quad (2.10)$$

(d) Differential equation with an independent variable which is a function of time.

$$\frac{d^2 y}{dx^2} + A \frac{dy}{dx} + \beta y = f(x) . \quad (2.11)$$

$$\frac{d^2 y}{dx^2} = - \left[-f(x) + A \frac{dy}{dx} + \beta y \right] . \quad (2.12)$$

$$y = \int \frac{dy}{dt} \cdot dt = \int \frac{dy}{dx} \cdot \frac{dx}{dt} \cdot dt \doteq a \int \frac{dy}{dx} \cdot u_x \cdot dt . \quad (2.13)$$

$$\frac{dy}{dx} = \int \frac{d}{dt} \left(\frac{dy}{dx} \right) dt = \int \frac{d}{dx} \left(\frac{dy}{dx} \right) \frac{dx}{dt} \cdot dt \doteq a \int \frac{d^2 y}{dx^2} \cdot u_x \cdot dt . \quad (2.14)$$

$$\frac{d^2 y}{dx^2} = - \left[-f(x) + A \left(a \int \frac{d^2 y}{dx^2} \cdot u_x \cdot dt \right) + B \left(a \int \frac{dy}{dx} \cdot u_x \cdot dt \right) \right] . \quad (2.15)$$

3. The Basic Modulation System

The operation of the quantizer is based on the application of delta modulation principles^(3,4). This application to electronic computation was first proposed in 1956, (Refs. 5 and 6). A broad survey of the problem based on these latter unpublished papers was given in Refs. 1 and 2.

A brief description of the delta modulation system, which was first published in 1947 as a communication link, is now given.

A block diagram of the basic equipment is shown in Fig. 3.

At the transmitting end a pulse generator, which produces pulses of constant height and repetition frequency, is fed to a modulator. In the latter the polarity of the pulses is controlled by a difference voltage, obtained in a comparator, by comparing the modulating signal with an approximate staircase waveform. This approximating waveform is produced by integrating the output pulses from the modulator, so that a positive pulse raises the integrator output voltage by a discrete step, whilst a negative pulse reduces it by the same amount.

If at any particular instant when a new step is formed, the modulating signal is greater than the staircase signal, the polarity of the error is such that a positive pulse is fed to the integrator so that the staircase waveform falls by one step. The output from the pulse modulator is also fed to the transmitter, which however, only transmits the unchanged or positive pulses, with the negative pulses represented by gaps in the pulse train.

Essentially the transmitter arrangement is a feedback control system with the transmitted signal as the error term.

At the receiving end the staircase waveform is reconstructed from the received pulses by means of equipment similar to that used in the transmitter. A local pulse generator, which is synchronised with the one in the transmitter, is fed to a modulator which determines the polarity of the pulses according to the presence, or otherwise, of the received pulses. The output from the modulator is integrated to form a replica of the original staircase waveform, which is then passed through a low-pass filter to give a continuous waveform resembling the original modulating signal.

As already stated a modified version of the technique is used in the design of the quantizer.

Appendix
4. The Basic Computing Units (ref 93)

4.1. The Quantizer

4.1.1. Mode of operation

A block diagram of the unit is shown in Fig. 4(a) and it is seen that it is essentially a feedback control system, the purpose of which is to maintain a correspondence between Y and the input signal X.

The circuit diagram of a prototype unit which was built at the College of Aeronautics, Cranfield, U.K. is shown in Fig. 4(b). A 2(a) A 2(b)

All relevant waveforms in the unit are shown in Fig. 5. Referring to Figs. 4 and 5, the analogue input signal X is added to the integrator output signal Y, which is of opposite sign to X, and the resultant signal is amplified by a directly coupled amplifier to give the waveform A. The latter signal is applied to a two state trigger circuit, which gives a well defined rectangular wave output B. This is fed to an "and" gate together with a pulse train L, which is derived from the basic clock pulse train, having a periodic time between pulses of T secs. as shown in Fig. 5. The "and" gate gives an output pulse when a pulse of L occurs when B is negative, thus producing the waveform C. To avoid any possible variation in pulse width, signal C is applied to a mono-stable multivibrator with an output E, the pulse width of which is just less than T. This waveform and its inverse are strobed by a strobe pulse train K in two "and" gates producing waveforms F and G respectively, which are pulse trains having well defined pulse widths and each pulse leading edge occupying a definite position in time. The strobe pulse train K is also derived from the basic clock pulse train with the pulses occurring in the mid-position of the clock pulses, to achieve the desired result of definite location in time, of pulses F and G. The summation of pulse train G and the inverse of F constitute the quantized waveform $k u_x$ mentioned in previous sections. However, for convenience in operating the quantizer integrator and the modulator units, the waveforms F and G are applied to a bi-stable multivibrator to give rectangular waveforms H and I which are more suitable for switching purposes. Waveform H is applied to the integrator/diode gate combination producing, at the input of the integrator, waveform J, to give the desired form of integrator output Y. The diode gates are used so that the forward path resistance to the integrator input is low, thus allowing the integrator time constant to be chosen low enough to suit dynamic operating requirements. In the reverse

direction of signal flow the diode gates present a high impedance and thus, in respect of leakage effects of the integrator, a high time constant is obtained which minimizes long term integration drift. Waveforms H and I are used as switching waveforms to operate modulator units. These waveforms are in a more suitable form for this purpose than waveforms F and G which constitute the quantized waveform $k u_x$ as already stated.

It will be noted that the waveform Y is a series of ramp functions forming an approximation to input signal X with a time delay = T seconds. In this respect it differs from the delta modulation system. Space limitations do not permit a more detailed description of the circuit configuration and it is hoped that this topic will be the subject of a further paper. However, it will be apparent that the most critical parts of the system are the analogue components, i.e. the directly coupled amplifier and the output integrator. These two components provide a source of drift error and need special attention in this respect.

4.1.2. Dynamic Performance

Let q represent the amplitude quantization level,

and T " " periodic time of the clock pulses.

The maximum rate of change with respect to time is therefore $\frac{q}{T}$ volts/second.

Assume now that the variable, say x , which is to be quantized is of the form

$$x = E \sin \omega t \text{ where } E \text{ is the maximum amplitude,} \quad (4.1)$$

$$\frac{dx}{dt} = \omega E \cos \omega t \quad (4.2)$$

$$\left(\frac{dx}{dt}\right)_{\max} = \omega E. \quad (4.3)$$

For quantizer noise not to exceed $2q$ peak to peak,

$$\omega E = \frac{1}{2} \frac{q}{T} = \frac{1}{2} a \quad (4.4)$$

$$\text{i.e. } \omega_{\max} = \frac{1}{2T} \cdot \frac{q}{E}. \quad (4.5)$$

$\frac{q}{E}$ is a measure of discrimination accuracy.

$$\text{If } \frac{q}{E} = N, \quad (4.6)$$

$$\text{then } \omega_{\max} = \frac{N}{2T}. \quad (4.7)$$

As an example,

$$\text{If } N = 10^{-4}$$

$$T = 10^{-6} \text{ seconds}$$

$$\omega_{\max} = \frac{10^{-4}}{2 \times 10^{-6}} = 50 \text{ rads/sec.} \quad (4.8)$$

Computing frequency may be increased at the expense of discrimination accuracy. As an example,

$$\text{if now } N = 10^{-3} \quad (4.9)$$

$$\omega_{\max} = 500 \text{ rads/sec.} \quad (4.10)$$

Thus it may be seen that N determines the discrimination accuracy and specifies the maximum drift and noise levels allowable in the quantizer unit.

The choice of T obviously affects the maximum computing frequency which may be applied to the unit.

Consider now the integrator of the quantizer unit - If the effective forward time constant of the integrator is T_i , and the effective input voltage through the diode gate = V , then we have the condition,

$$\frac{V}{T_i} = \frac{q}{T} \quad (4.11)$$

Some flexibility in the choice of V and T_i is therefore obtained. However, the feedback capacitor of the integrator should be as high as possible to minimise long term drift effects. Consider now the required bandwidth of the quantizer integrator.

Assume that the input signal x to the quantizer is of the form,

$$x = E \sin \omega t, \quad (4.12)$$

where ω is the highest radian frequency which satisfies a discrimination accuracy of say 0.1%.

This signal results in a symmetrical rectangular waveform J , with a periodic time $\frac{2\pi}{\omega}$, applied to the input of the integrator.

The real Fourier series expansion of the function $J(t)$ is given by

$$J(t) = \frac{4E}{\pi} \sum_{n=1}^{n=\infty} \frac{\sin(n\omega t)}{n} \quad (4.13)$$

with n odd.

The bandwidth of the integrator should just be high enough to pass the highest significant harmonic of $\frac{1}{T_i} \int J(t) dt$, (4.14)

where T_i is the time constant of the integrator.

The k th harmonic may be expressed as ,



$$J_k = \frac{1}{T_i} \int \frac{4E}{\pi} \frac{\sin(k\omega t)}{k} dt \quad (4.15)$$

$$= \frac{4E}{\pi T_i k^2 \omega} [-\cos(k\omega t)] \quad (4.16)$$

and $J_{k \max} = \frac{4E}{\pi T_i k^2 \omega} \quad (4.17)$

For this to be the highest significant harmonic,

$$\frac{4E}{\pi T_i k^2 \omega} < E \times 10^{-3} \quad (4.18)$$

$$\therefore k^2 > \frac{4 \times 10^3}{\pi T_i \omega} \quad (4.19)$$

Now for $q = E \times 10^{-3}$, $\omega_{\max} = 500$ rads/sec, (4.20)

$$\frac{V}{T_i} = \frac{q}{T} = \frac{E \times 10^{-3}}{10^{-6}} = E \times 10^3 \quad (4.21)$$

For $E = 100$ volts

$$T_i = V \times 10^{-5} \text{ seconds} \quad (4.22)$$

Assume $V = 10$

$$\therefore T_i = 10^{-4} \text{ seconds} \quad (4.23)$$

$$\therefore k^2 > \frac{4 \times 10^3}{\pi \times 10^{-4} \times 500} = \frac{40}{5\pi} \times 10^4 \quad (4.24)$$

i.e. $k > 160 \quad (4.25)$

Thus the minimum bandwidth of the integrator is

$$160 \times 500 = 8 \times 10^4 \text{ rads/sec.} \quad (4.26)$$

A filter having this bandwidth should therefore be inserted between the diode output J and the input of the integrator.

This filter has not yet been incorporated in the experimental unit and its effectiveness has not therefore been investigated.

4.1.3. Experimental results - prototype unit

Two prototype units have been built based on the circuit diagram shown in Fig. 4(b), to investigate the possible limitations and difficulties of the unit. The units have been operating satisfactorily with a clock rate of one megacycle per sec. (i.e. $T =$ one microsecond). The discrimination level of the unit is less than 5 milli-volts in a total range of 50 volts. The input transistors of the

differential amplifier are high frequency micro alloy germanium type 2N501 as are the output pair of transistors. Surface barrier germanium type SB 240 transistors are used in the remaining stages.

Tests were carried out with a commercially available electronic valve quantizer integrator with a relatively poor open loop frequency response of 100 cycles per sec. At the clock rate of 10^6 cycles/sec this limitation in bandwidth was apparent as noise products and a transistor integrator with a significant improvement in bandwidth will be used when available.

Temperature effects of the input transistors was investigated. For zero input voltage to the quantizer, the balance was adjusted to give zero output voltage of the quantizer integrator at a certain temperature. The temperature was then altered in stages and the results obtained are given in tabular form below.

TABLE 1 - INPUT VOLTAGE ZERO

Voltage figures in milli-volts

Output Voltage (increasing temperature)	0	2.2	4.5	6	7	8	9.2	10.5	10.8	12.5	14	15
Output Voltage (decreasing temperature)	-	-	-	2	3	4	5	6.0	7.5	9	10	11.5
Temperature ($^{\circ}$ C)	21.5	22	23	24	25	26	27	28	29	30	31	32

These tentative figures give an average drift rate of about 1 milli-volt per degree centigrade. As the unit will be temperature stabilized to $\pm 1^{\circ}$ C. these figures seem to be satisfactory.

Further investigations into the effect of the transistor integrator bandwidth will proceed when the unit at present under development becomes available.

4.2. The Modulator (M)

4.2.1. Mode of Operation

A block diagram of the unit is shown in Fig. 6(a) and the circuit diagram of a prototype unit in Fig. 6(b).

Waveforms H and I from the quantizer are fed through passive differentiating circuits, and the negative going pulses Q and R fed to a bi-stable multivibrator which regenerates symmetrical rectangular waveforms N and O, identical to H and I respectively, with positive and negative limits of 4.5 volts. This procedure is adopted to prevent possible loading effects on the quantizer output. Waveforms N and O are used to gate the analogue signal M through two diode gates A and B.

The sign of M is reversed before being applied to gate B. The output signal from gate A is signal S whilst that from gate B is signal U. The summation of these two signals constitutes signal P which forms the input to an integrator. The output signal P represents the quantity $y \cdot u_x$ for the particular case shown in Fig. 6(b).

4.2.2. Limits on performance

The main limitations on dynamic performance are due to the finite rise time of the switching waveforms N and O and the hole storage effects of the silicon diodes. However, a limit is imposed on the function being switched by the modulator in that its amplitude cannot change by more than $\frac{q}{2}$ in the sample period T where q is the quantization level. Under these conditions it may be shown that, provided the time taken to switch the function of the positive max value to the max negative value, is less than T, the effect of finite rise time is negligible.

Hole storage effects become more significant as T is reduced.

The linearity of the modulator is dependent on the non-linear characteristics of the diodes under the operating conditions and the matching of the two diode bridges. These considerations restrict the accuracy to a value of about 0.1 per cent, of the maximum value of the computing variable y.

4.2.3. Experimental Results - Prototype Unit

The circuit diagram of the prototype unit is given in Fig. 6(b). The main limitation is the limit on voltage amplitude of the transistors feeding the diode bridges. With a voltage range of 30 milli-volt to 3 volts, up to a switching rate of 1 megacycle/sec., the linearity of the unit was found to be about 1%.

Silicon diodes type 1 S 914 were used in the diode bridges.

Improvements in the circuit now under development are as follows:

- (i) A significant increase in voltage range.
- (ii) A method of obtaining good matching in the diode bridges.

It is hoped that an overall accuracy of better than 0.1% for a voltage range of 30 millivolts to 30 volt will eventually be achieved.

4.3. The Integrator (I)

A chopper stabilized transistor integrator is at present under development.

An electronic valve integrator has therefore been used in experiments using the quantizer and modulator.

It is interesting however, to consider the required dynamic response of the unit.

Consider the product $y \cdot u_x$ which forms a possible input signal to the integrator.

Let $y = E \sin \omega t$ (4.27)

and u_x be represented by a symmetrical waveform J of periodic time $\frac{2\pi}{\omega}$.

The real Fourier series expression of $J(t)$ is again given by

$$J(t) = \frac{4}{\pi} \sum_{n=1}^{n=\infty} \frac{\sin(n\omega t)}{n} \quad (4.28)$$

The product of $y \cdot u_x$ will consist of a number of terms having frequencies which are the sums and differences of the multiples of $\frac{\omega}{2\pi}$.

If this product is integrated in the integrator with time constant T_i , the required bandwidth of the integrator is determined by the highest frequency component having a resultant amplitude, after integration, less than the chosen quantization level.

Consider the product $J_k \cdot y$ where J_k is the k th harmonic of $J(t)$.

Let $z = J_k \cdot y$ (4.29)

$$z = \frac{4E}{\pi k} (\sin \omega t \cdot \sin k\omega t) \quad (4.30)$$

i.e. $z = \frac{2E}{\pi k} [\cos(k-1)\omega t - \cos(k+1)\omega t]$ (4.31)

To find the minimum bandwidth the summation terms need only be considered.

Consider now the integral

$$\frac{1}{T_i} \int z \, dt = \frac{1}{T_i} \int \frac{2E}{\pi k} \cos(k+1)\omega t \, dt \quad (4.32)$$

$$= \frac{2E}{T_i \pi k(k+1)\omega} \sin(k+1)\omega t \quad (4.33)$$

For this to be the highest significant harmonic

$$\frac{2E}{\pi k(k+1)T_i\omega} < \frac{E}{1000} \quad \text{for 0.1\% accuracy} \quad (4.34)$$

$$k(k+1) > \frac{2 \times 10^3}{\pi T_i \omega} \quad (4.35)$$

For $\omega = 500 \text{ rad/sec}$

$$k(k+1) > \frac{1.27}{T_i} \quad (4.36)$$

$$\text{Let } T_i = la \quad \text{where } a = \frac{q}{T} \text{ and } l > 1 \quad (4.37)$$

$$\text{then } k(k+1) > \frac{1.27}{lq} \quad (4.38)$$

$$\text{with } T = 10^{-6}; \quad q = 10^{-1}$$

$$k(k+1) > \frac{1.27 \times 10^{-5}}{l} \quad (4.39)$$

and hence k is dependent on the choice of l .

5. High Speed Incremental Analogue Digital Converter (Modified Quantizer)

5.1. The basic arrangement

If the analogue integrator of the quantizer (see Fig. 4) is replaced by a reversible counter, as shown in Fig. 8, this modified quantizer becomes effectively an analogue to digital converter.

The waveform designations in Fig. 8 have the same significance as in Fig. 5. Signal F , which is the pulse train representing positive increments of the input function, and signal G , representing negative increments, are used as the inputs to the counter as shown in Fig. 8(b). Signal F is used as an "add" input and signal G as a "subtract" input. The purpose of the mono-stable multivibrator on each input line is to provide a buffer stage to avoid loading effects on the quantizer and also to reduce the width of the pulses in F and G . The voltages at each binary stage of the counter are applied to appropriately scaled resistors which are connected to a common summing point which is effectively the input of the d. c. amplifier. The contributions from all the currents from the binary stages constitute the analogue feedback signal which is of opposite sign to the input signal $x(t)$ and, in the ideal case, is equal in magnitude to $x(t)$.

With $x(t) = 0$, the counter is arranged to be half full, i. e. a voltage $-V$ representing a "one" on the thirteenth digit of a fourteen digit counter, is present. V represents the maximum amplitude range of the input signal $x(t)$. To give a zero output voltage, for the d. c. amplifier with the input $x(t)$ at zero level, a bias voltage $+V$ is applied through a resistor equal to that of R_{13} to the input of the amplifier.

The arrangement shown in Fig. 8(a) has operated satisfactorily with a periodic time between pulses of one micro-second. The binary representation of $x(t)$ is fed from the counter to any form of storage device for future manipulation. Fourteen binary stages are used at present but further stages could of course be added if required.

5.2. The Counter

The block diagram of three stages of the fourteen stage counter is shown in Fig. 8(b). The operation may be described briefly as follows: -

Assume that all binary stages are 0 in the output of the binary stage as indicated in Fig. 8(b) with the exception of the thirteenth stage which has a "one",

i. e. the counter is half full. With a zero in the output half of a binary stage the output voltage is zero and with a "one" the output voltage is -5 volts. The gates are effectively "and" gates and will only transmit a pulse when both input voltages are negative.

With the arrival of a pulse signal, say F, the first binary stage is changed from "zero" to "one" and opens gate A_1 but closes gate B_2 . Due to the delay in switching the binary stage the pulse is, however, not transmitted through gate A_1 . With the arrival of a further pulse in signal F, this pulse is transmitted through gate A_1 and changes the 2nd binary stage from a "zero" to "one" which opens gate A_2 and closes gate B_2 . The same pulse also changes the first binary stage from "one" to zero, closing gate A_1 and opening gate B_1 . The sequence of operations for adding is repeated in this way.

If now the pulse occurs in signal G this effectively subtracts "one" from the first binary stage, i. e. adds the complement of -1.

In an experimental version of the unit, five transistors are used in each binary stage with each gate comprising one transistor.

The unit has operated satisfactorily with a periodic time of one micro-second and, as already stated, when used as the integrator of the quantizer, results in a very high speed analogue-digital converter.

6. Simulation of Dead Time (Transportation lag)

6.1. Principle of Operation

A block diagram of the basic arrangement is shown in Fig. 9(a) and the associated waveforms in Fig. 9(b).

The function $x(t - nT) = x(t - T_0)$ is derived from $x(t)$, where T_0 is the desired dead time, by passing $x(t)$ through a quantizer unit to give an output $k u_x$ with the negative pulses interpreted as an "0" signal and the positive pulses as a "1" signal. This latter signal is applied to a ferrite core shift register, to which is also applied two shift waveforms which are derived from a pulse generator having the same periodic time as the sampling frequency of the quantizer. The shift register comprises a number of ferrite cores, connected in series, which may be switched to one of two possible states, i. e. 0 or 1, by the application of a 0 or 1 pulse.

The arrangement is conventional in that after each cycle of the shift waveforms, the state of each core is transferred to each adjacent core. Thus for n cores connected in series, the original pulse appears at the output of the n th core after a period of nT seconds where T is the periodic time of the sampler. In this way the original pulse train $k u_x = f(t)$ is regenerated at the output of the register but with a time delay of nT seconds, i. e. the output is $f(t - nT)$.

This signal is fed to an analogue integrator to give an output which closely approximates to $x(t - nT) = x(t - T_0)$ as shown in Fig. 9(b). The dead time T_0 is therefore determined by the number of cores and the sampling period T .

In a proposed experimental version, $n = 1000$ and T is variable from 10^{-8} seconds to 10^{-5} seconds, giving a range $T_0 = 10^{-2}$ seconds to 10 seconds. The lower value obviously may be reduced further by taking the output at the m th core where $m \ll 1000$.

Note:- The total number of cores necessary with the single diode transfer loop used shown in Fig. 10 is $2n$, i.e. 2000.

6.2. The Shift Register

The basic arrangement used in the experimental unit is shown in Fig. 10(a) using ferrox-cube magnetic cores type FX 1508 (2 mm outside diameter) with an idealised hysteresis loop characteristic as shown in Fig. 10(b) with the $+B_R$ state interpreted as a "1" and $-B_R$ state interpreted as a "0".

Referring to Fig. 10 assume initially that all cores are in state zero. Now apply an input pulse train of the form shown in Fig. 9(b). The first positive pulse will switch core 1 to state one. On application of shift current pulse D (also called clock pulse or advance pulse), core 1 will be switched to state zero and the resulting large flux change will induce a large positive voltage across output winding n of core 1. This voltage will drive current through the diode to magnetic core 2 to state "one", i.e. application of D has transferred whatever digit was stored in core 1 to core 2 and reset core 1 to state zero. By use of the diode in the transfer loop, the transfer is isolated to these two cores only. Therefore at the same time digits can be transferred from core 3 to 4, core 5 to 6 and so on, by the same shift current D. Now shift current pulse E is applied. This signal transfers all the digits to the next odd cores from the even cores. Thus the information in the form of a train of pulses can be stepped along a series of cores by a pair of shift pulses.

Transfer occurs only when shift pulses are applied. During the absence of the shift pulses the digits are stored in the magnetic medium of the cores by the residual magnetism.

The associated drive circuits are transistorised based on the use of high frequency power transistors type OC23 with maximum collector current of 1 ampere.

With regard to the number of turns associated with each core figures chosen for the experimental version were as follows :-

Input winding	$n_1 = 5$ turns
Shift winding	$n_2 = 25$ "
Output winding	$n_3 = 25$ "

Factors affecting the choice of turns include the size of the core, back e.m.f. across the shift winding, storage capacitances and inductances. The number of turns in the input winding depends on the transfer current required in the transfer loop. The choice of output winding turns is chosen to be about five times that of the input winding to minimize the backward flow of information.

With the single diode transfer loop, two cores are required to give a delay of T seconds where T is the periodic time of the input pulse train. For $T_0 = 1000T$,

2000 cores are necessary, half the number being driven by the shift waveform D and the other half being driven by the shift waveform E. In addition 2000 diodes are required.

It was found that at least 20 cores with shift windings connected in series could be operated from the shift pulse generator. In the final version of the device a series parallel arrangement of connection of windings is envisaged fed from a number of shift waveform generators. A possible alternative transfer loop based on capacitor delay is being considered (Ref. 7), which may result in a reduction of the number of associated components.

It was found that the shift register operated satisfactorily at a pulse repetition rate of 10^5 cycles/sec.

7. CORRELATION FUNCTIONS

7.1. Introductory Remarks

These functions are of fundamental importance in the statistical analysis and synthesis of dynamical systems.

The auto-correlation function $\phi_{xx}(T_0)$ of a signal $x(t)$ may be defined as

$$\phi_{xx}(T_0) = \lim_{T_1 \rightarrow \infty} \frac{1}{2T_1} \int_{-T_1}^{T_1} x(t) \cdot x(t + T_0) dt \quad (7.1)$$

$$= \lim_{T_1 \rightarrow \infty} \frac{1}{2T_1} \int_{-T_1}^{T_1} x(t) \cdot x(t - T_0) dt \quad (7.2)$$

That is it makes no difference whether the function $x(t)$ is shifted ahead by T_0 seconds and multiplied by $x(t)$ or shifted back before multiplication and time averaging.

As is well known $\phi_{xx}(T_0)$ is qualitatively a measure of the regularity of the function $x(t)$.

It will be noted from the above definition that determination of $\phi_{xx}(T_0)$ requires three distinct operations.

- (a) shifting the time axis to generate $x(t - T_0)$
- (b) multiplying $x(t)$ by $x(t - T_0)$
- (c) taking a time average over a period $2T_1$ which is much longer than the delay period T_0 .

The crosscorrelation function $\phi_{xy}(T_0)$ between two signals $x(t)$ and $y(t)$ may be defined as:-

$$\phi_{xy}(T_0) = \lim_{T_1 \rightarrow \infty} \frac{1}{2T_1} \int_{-T_1}^{T_1} x(t) \cdot y(t + T_0) dt. \quad (7.3)$$

$\phi_{xy}(T_0)$ is not an even function because in the general case shifting $y(t)$ ahead by T_0 seconds does not give the same result as that obtained by retarding $y(t)$ by T_0 seconds.

However, since a shift in $y(t)$ must yield the same result as a shift of $x(t)$ by the same amount in the opposite direction then

$$\phi_{xy}(T_0) = \phi_{yx}(-T_0) \quad (7.4)$$

i. e.
$$\phi_{yx}(-T_0) = \lim_{T_1 \rightarrow \infty} \frac{1}{2T_1} \int_{-T_1}^{T_1} y(t) \cdot x(t - T_0) dt. \quad (7.5)$$

$\phi_{yx}(-T_0)$ may be regarded in a certain sense as a measure of the interdependence of $x(t)$ and $y(t)$ since if both time functions are random signals with no d. c. components and are derived from independent sources, the cross-correlation function is zero.

Again it will be noted that the same three distinct operations are required as for the autocorrelation function, in the generation of the cross correlation function. Several practical types of correlator are in use today based on these three operations.

An arrangement using hybrid techniques will now be described. The cross-correlation function is taken as an example, as the application to the generation of the auto-correlation is obvious.

7.2. Generation of Cross-correlation Function $\phi_{yx}(-T_0)$

The instrumentation is based on a time average over positive time i. e.

$$\phi_{yx}(-T_0) = \frac{1}{T_1} \int_0^{T_1} y(t) \cdot x(t - T_0) dt \quad (7.6)$$

where T_1 is much larger than T_0 . The sample T_1 must be sufficiently long to indicate the lowest frequency components of significance in the signals. A rough guide to a first estimate is that T_1 should be about ten times the largest period of the signal components. If this choice is appropriate then the time averages for a number of different sets of samples for the same T_0 should be the same.

The time T_1 required is obviously of practical significance in generating the function.

Having chosen T_1 a plot of $\phi_{yx}(-T_0)$ as a function of T_0 is required so arrangements must be provided to change the value T_0 .

The block diagram of a system having these facilities is given in Fig. 11.

The signal $x(t)$ is delayed in the dead time simulation by a time $T_0 = nT$ seconds where T is the periodic time of the sampling frequency and n is the number of pairs of cores in the shift register.

Note: T_0 may be altered by changing either T or n . The signal $x(t - T_0)$ is multiplied by $y(t)$ in a form of multiplier described earlier. This product is then integrated in an analogue integrator for a period T_1 . Arrangements must be made to scale the result according to the function

$$\frac{1}{T_1} \int_0^{T_1} y(t) \cdot x(t - T_0) dt .$$

Although an experimental version of the dead time simulator has operated successfully, tests have not yet been made on the operation of such a correlator.

It should be noted that for many applications such as "on-line" correlation, i.e. correlators which are incorporated as elements of a control system, the quantization may be quite coarse, or in other words, the number of discrete levels may be a small number. For such applications ten or less discrete amplitude levels may be satisfactory and a considerably simplified unit would result.

Several workers are studying this aspect and consideration is given to this topic in Ref. 8.

8. Generation of Arbitrary Functions

A generalized method for function generation is indicated in Fig. 2(c), based on the assumption that signals representing partial derivatives of the function are available. Where the function is analytic these derivatives may be generated without undue difficulty.

However, if the function is arbitrary, either an analytic function which approximates the function must be used or alternatively a method is required for setting up the partial derivatives. This latter method is considered first for the specific example of the generation of an arbitrary function of two variables.

Consider the function z , where

$$z = f(x, y) \tag{8.1}$$

$$\frac{dz}{dt} = \frac{\partial z}{\partial x} \cdot \frac{dx}{dt} + \frac{\partial z}{\partial y} \cdot \frac{dy}{dt} . \tag{8.2}$$

As in previous examples approximations to $\frac{dx}{dt}$ and $\frac{dy}{dt}$ may be obtained by feeding x and y respectively through quantizers so that

$$z \dot{=} a \int \left(\frac{\partial z}{\partial x} \cdot u_x + \frac{\partial z}{\partial y} \cdot u_y \right) dt \tag{8.3}$$

where

$$a = \frac{q}{T} \text{ as before .} \tag{8.4}$$



The problem is then basically the generation of $\frac{\partial z}{\partial x}$ for all values of y and the generation of $\frac{\partial z}{\partial y}$ for all values of x .

The block diagram of a possible arrangement is shown in Fig. 12.

The signal x is passed through a quantizer Q whose output (waveforms F and G) is connected to a reversible counter.

Note: Waveform designations in this text have the same meaning as those in Fig. 5.

The reversible counter acts as a digital adder and produces a binary output which represents the value of x at any time. A six stage binary counter is taken as a specific example giving 64 possible values of x , representing the amplitude range $-x_{\max}$ to $+x_{\max}$. This, with the counter half full, represents the condition that x is zero. With this choice of counter the quantization level for the signal x is therefore $\frac{1}{32} \cdot x_{\max}$, i.e. the quantization is rather coarse for the sake of economy.

The 64 possible values of x are derived from the six binary outputs by combining the latter in an appropriate manner and feeding the combination through gates.

The procedure of the y channel is identical to that for x .

The 64 output lines for x and also those for y are connected to two 64×64 magnetic core stores as indicated in Fig. 12. The binary state of each core in the first store is read in, by manual switching or by punched tape, before the start of the computation and represents $\frac{\partial z}{\partial x}$ in a sampled quantization form where the quantum increments in x and z are $\frac{1}{32} \cdot x_{\max}$ and $\frac{1}{32} \cdot z_{\max}$ respectively. The binary state "one" represents a positive increment $\frac{\partial z}{\partial x}$ and the binary state "zero" represents a negative increment $\frac{\partial z}{\partial x}$.

In a similar manner the second store represents $\frac{\partial z}{\partial y}$ for all possible discrete values of x and y . For particular discrete values of x and y , only one core in each store will change its state to give an output pulse on the common output line corresponding to its binary state. The method for achieving this condition is based on conventional lines with the x and y lines for particular values of x and y forming a magnetic circuit for a particular core. The common output line is threaded through each core. Arrangements must also be made to return the particular switched core to its original binary state, i.e. the original information must not be destroyed.

The outputs from stores 1 and 2 then represent in a sampled quantized form $\frac{\partial z}{\partial x}$ and $\frac{\partial z}{\partial y}$ respectively. The pulse trains representing these quantities are passed through pulse shaping networks to overcome the distortion produced in the store. These shaped pulses are then converted into rectangular waves of constant amplitude whose sign is positive when a pulse is present and negative when there is no pulse. A two state trigger circuit could be used for this purpose.

These rectangular waveforms are then fed to the respective modulators where they are switched by the waveforms H and I from the respective quantizers in the manner already described in Section 4.2.

The outputs from the two modulators are added and fed to the input of the analogue integrator I with a time constant $\frac{K}{a}$ to give an output voltage representing $K z(x, y)$ (see equation 8.3).
Note: K is an amplitude scale factor.

A digital representation of z could, of course, be obtained by replacing the analogue integrator by a reversible counter.

Other arrangements for the generation of functions are obviously possible and the above method is included as an illustration of one possible arrangement.

It will be noted that even for the rather coarse quantization level of $\frac{1}{32}$ maximum amplitude range two stores are required each having a total number of 4016 cores.

For the generation of a function of three variables based on a similar arrangement, three stores are required each having a total number of 262,144 cores (64^3). Thus this method would not appear to be economic for this application.

It would appear therefore, on economic considerations, that for the generation of functions of three or more variables, the best approach would be to generate analytic approximations to the required partial derivatives.

This problem is being actively considered at the moment and further work may indicate a better approach to the problem.

9. Conclusions

The basic computing units comprising a quantizer, a modulator and an integrator provide a flexible means for function generation. The main advantage is that integration may be performed with respect to a variable other than time. Experimental results with transistorized prototype units are promising and satisfactory operation has been obtained with a sampling rate of one megacycle per second.

The simulation of dead time is obtained in a relatively easy manner and experimental results are again very promising up to a sampling rate of 100 kilocycles per second. This rate is probably faster than that required for most applications.

It would appear that the generation of functions of two or more variables is possible but no experimental evidence is as yet available, to confirm this view.

10. Acknowledgements

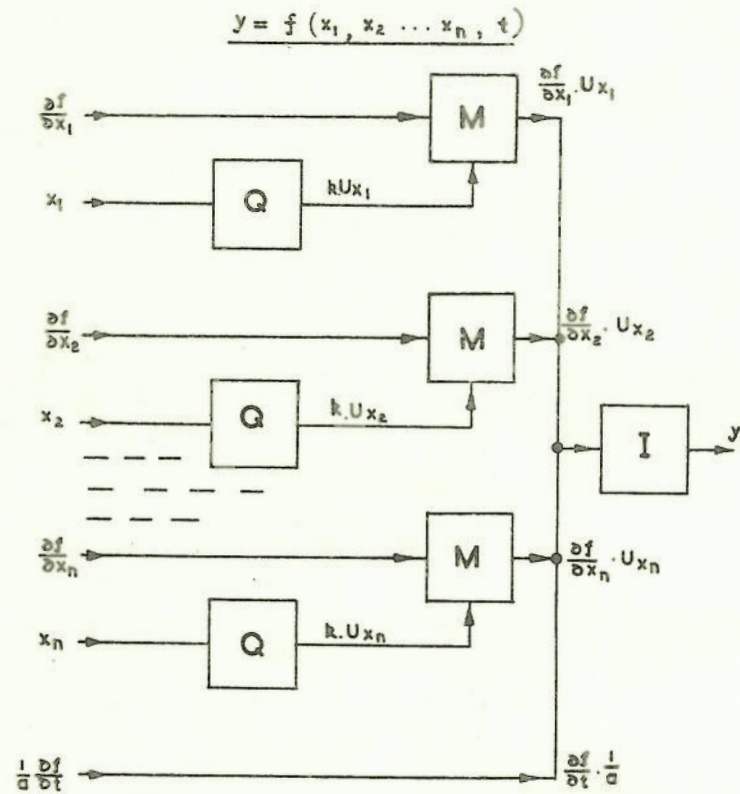
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$$y \doteq \int \left(\frac{\partial f}{\partial x_1} \cdot U_{x_1} + \frac{\partial f}{\partial x_2} \cdot U_{x_2} + \dots + \frac{\partial f}{\partial x_n} \cdot U_{x_n} + \frac{1}{d} \frac{\partial f}{\partial t} \right) dt$$

$$= f(x_1, x_2, \dots, x_n, t)$$

FIG. 2(c) GENERALIZED FUNCTION GENERATION

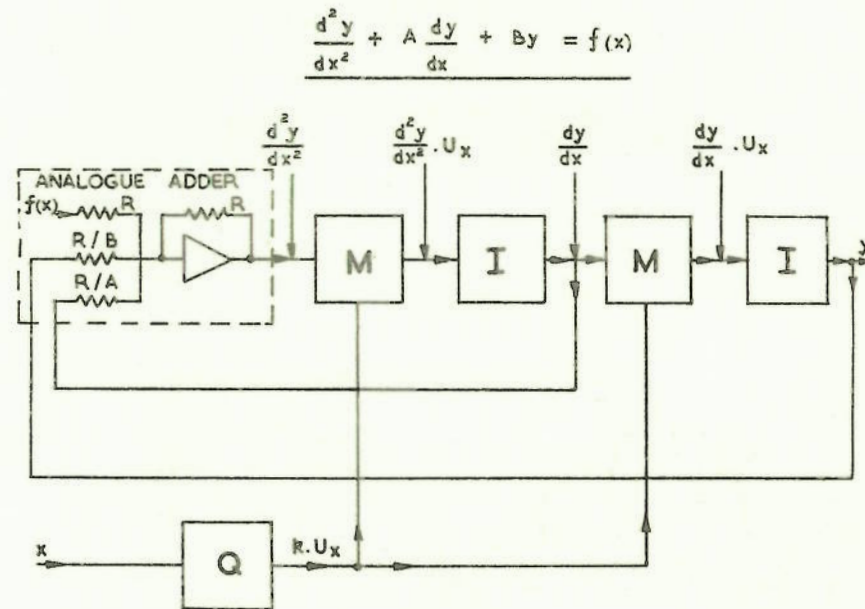
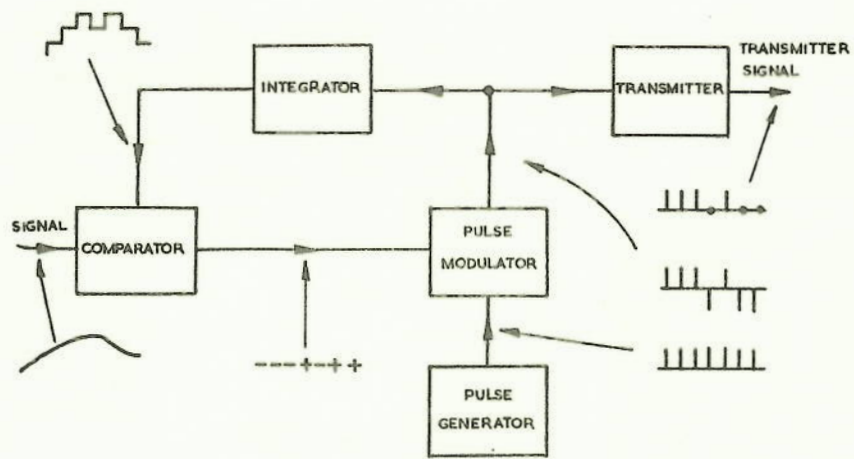
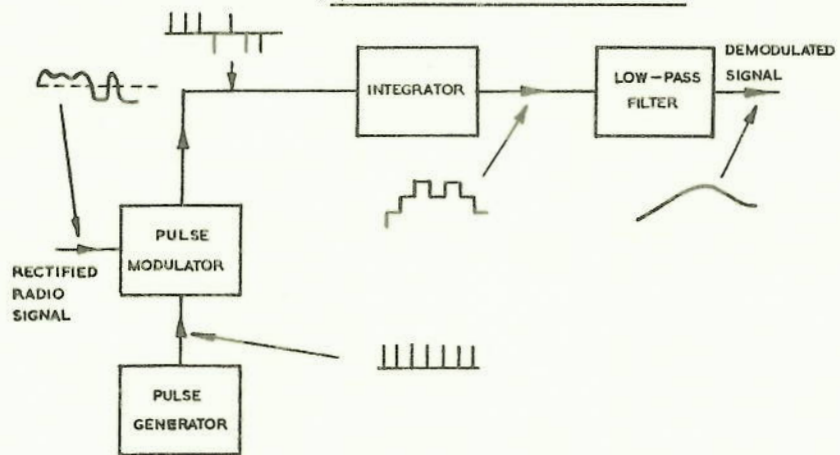


FIG. 2(d) SOLUTION OF DIFFERENTIAL EQUATION

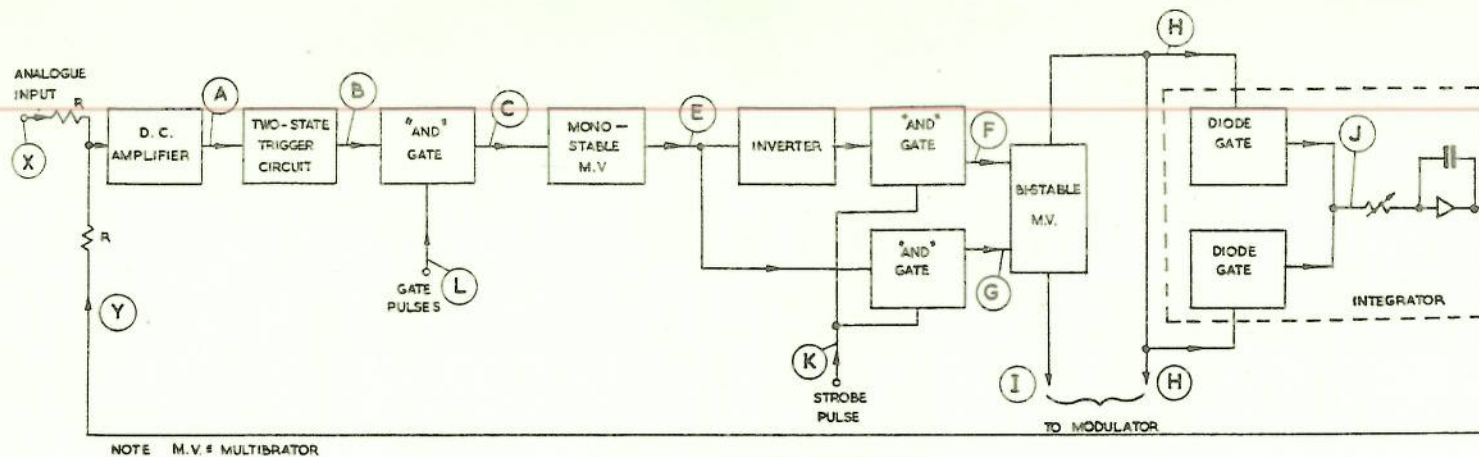


(a) TRANSMITTING EQUIPMENT

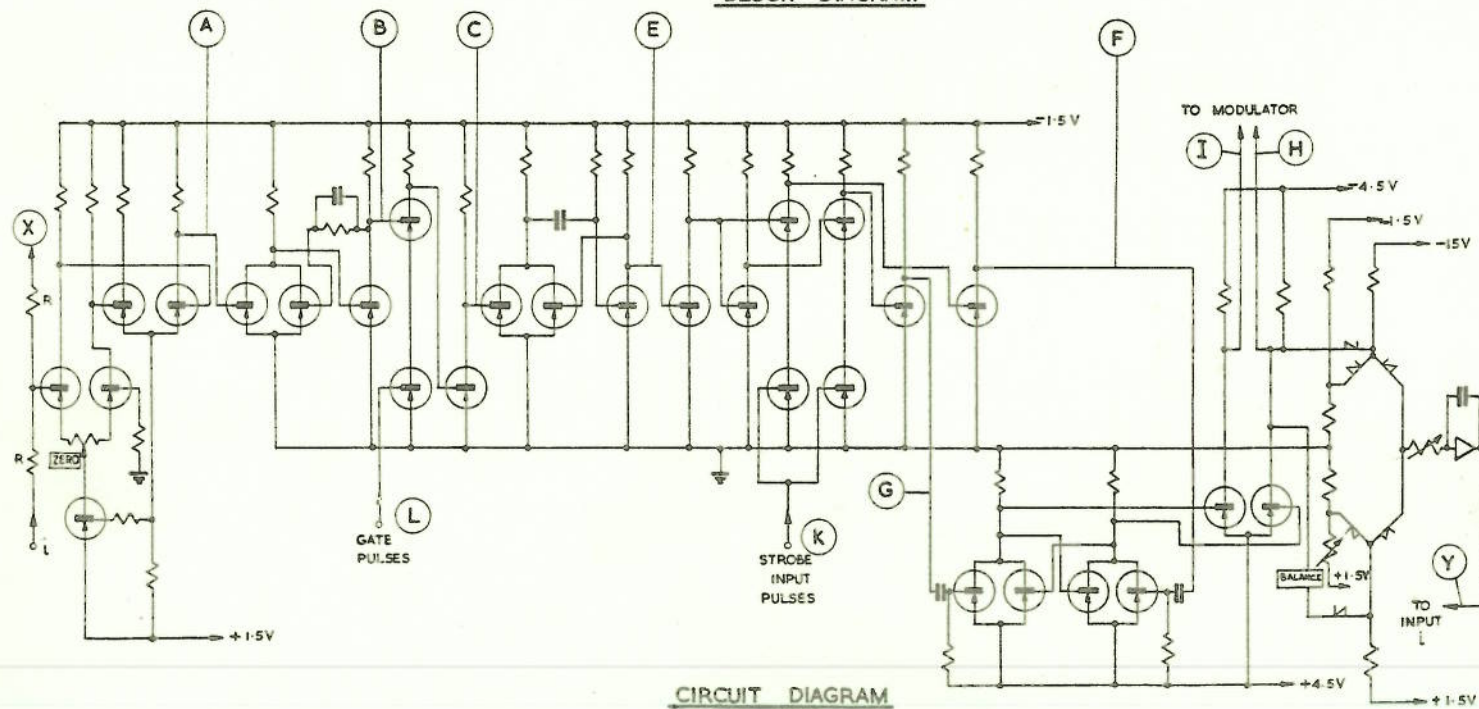


(b) RECEIVING EQUIPMENT

FIG. 3. (a) and (b) BLOCK DIAGRAM OF DELTA MODULATION SYSTEM



BLOCK DIAGRAM



CIRCUIT DIAGRAM

FIG. 4. THE QUANTIZER

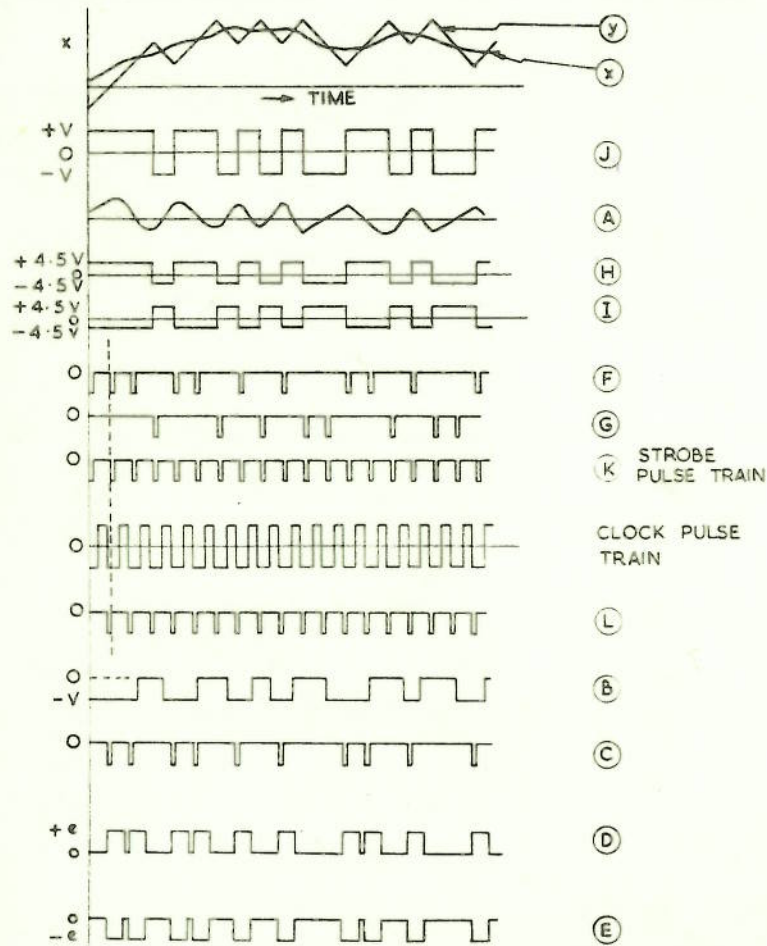


FIG 5. QUANTIZER WAVEFORMS

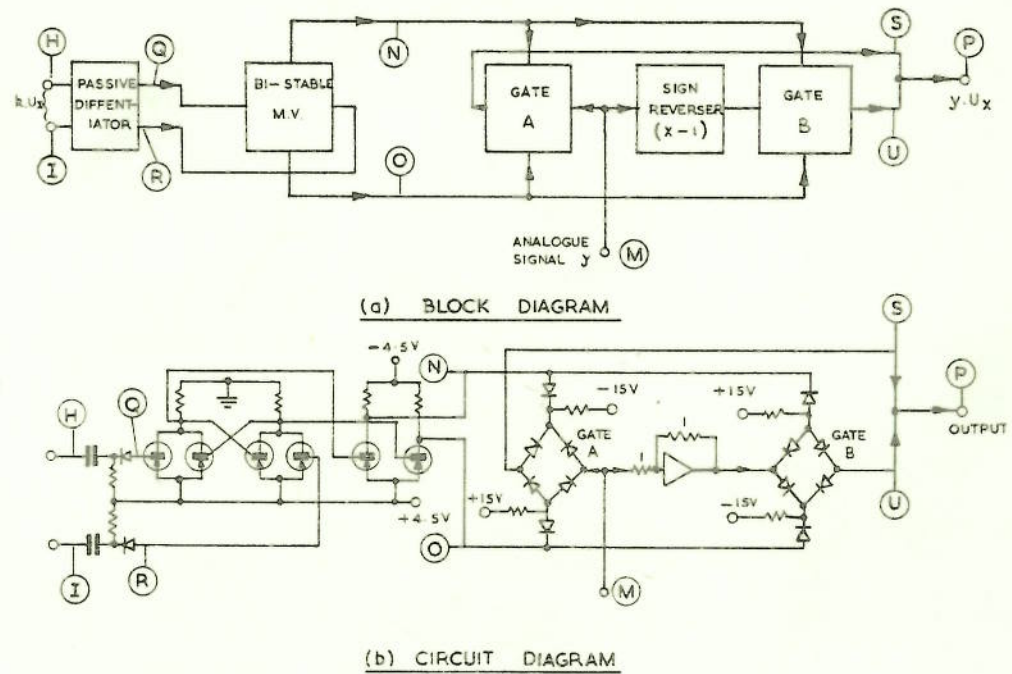


FIG. 6. (a) and (b) THE MODULATOR

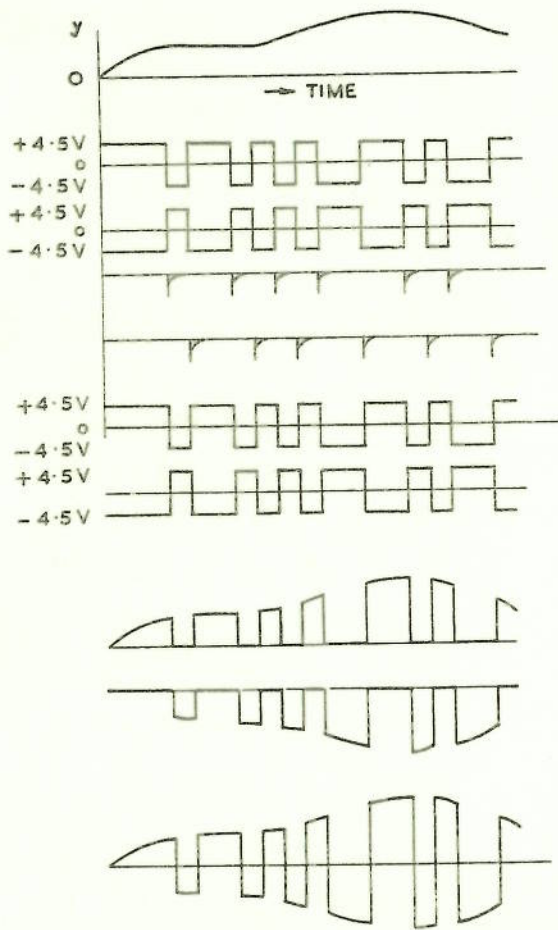


FIG. 7. WAVEFORMS - MODULATOR

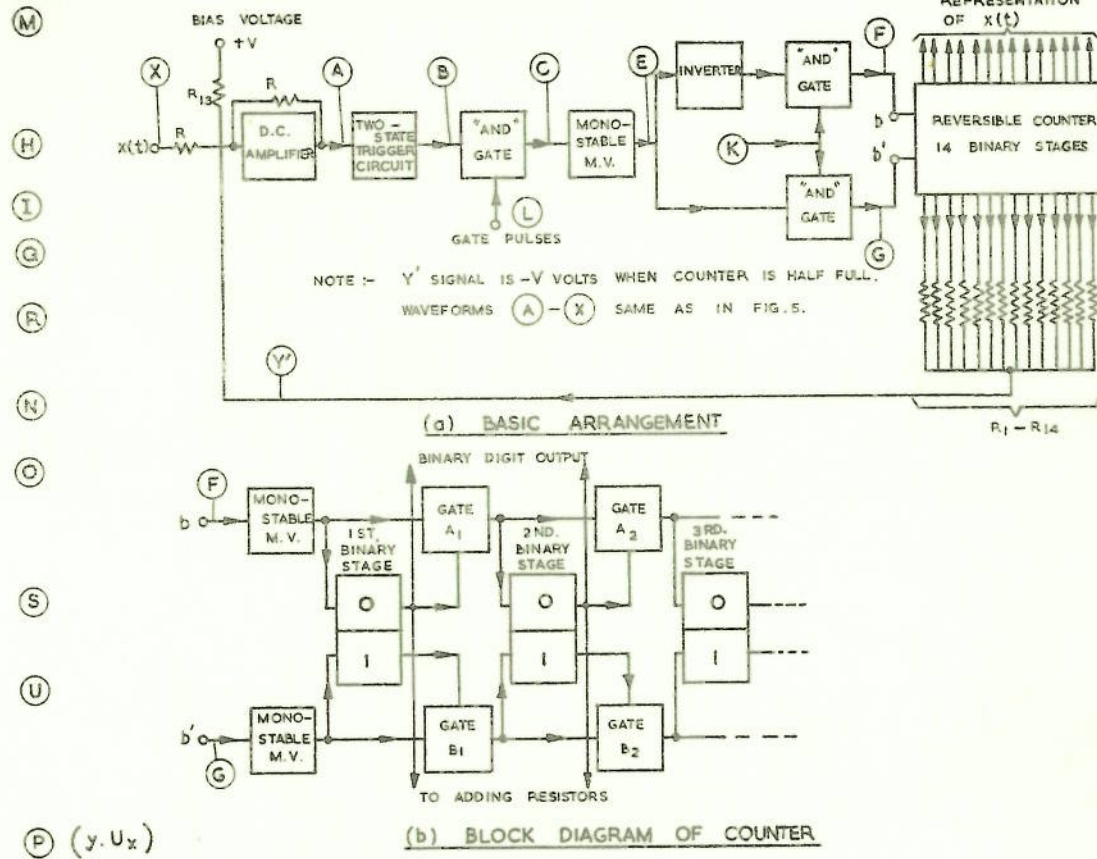
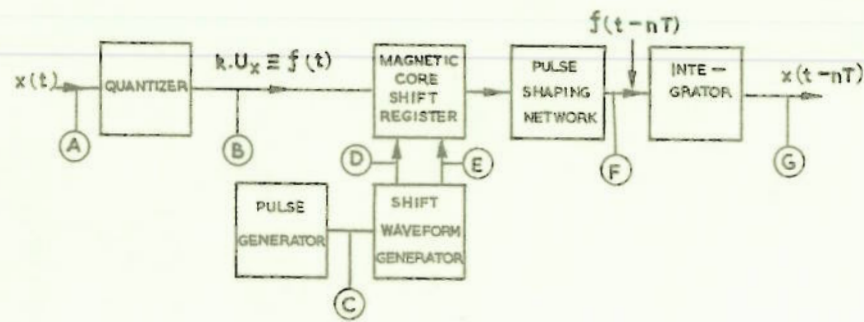
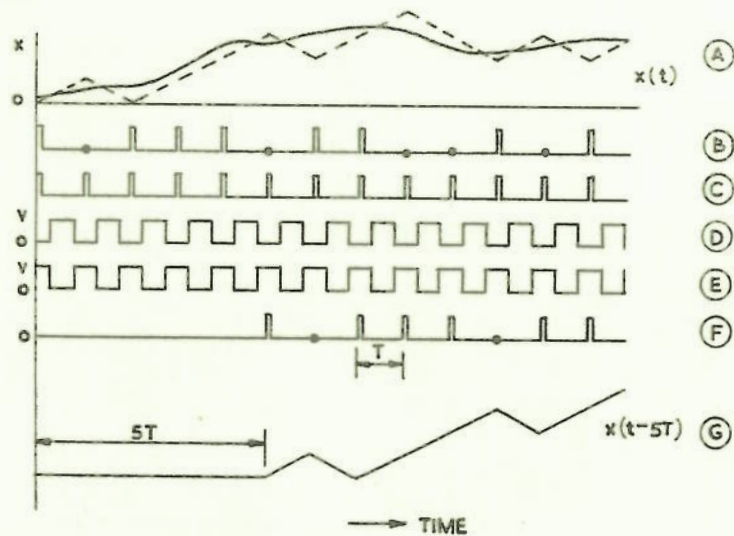


FIG. 8. (a) and (b) ANALOGUE DIGITAL CONVERTER (modified Quantizer)

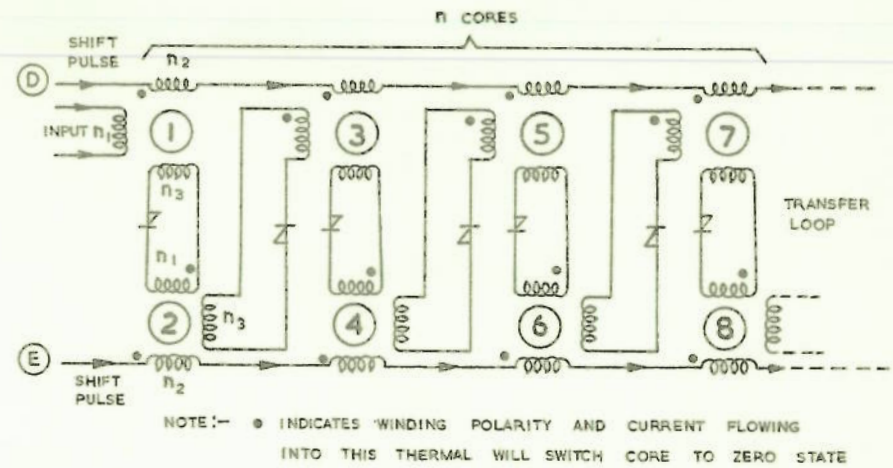


(a) BLOCK DIAGRAM OF BASIC ARRANGEMENT

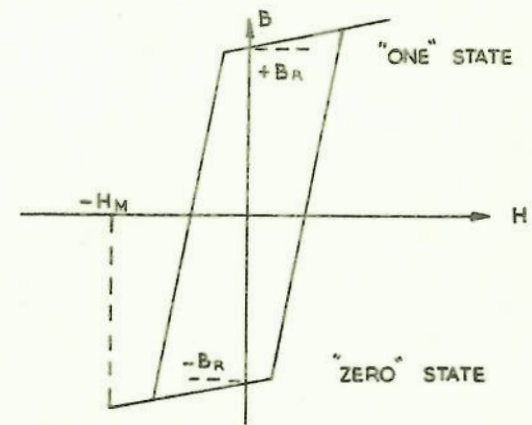


(b) WAVEFORMS

FIG. 9. (a) and (b) SIMULATION OF DEAD TIME ($T_0 = nT$)



(a) SINGLE DIODE TRANSFER LOOP CONFIGURATION



(b) IDEALIZED HYERESIS LOOP OF CORE

FIG. 10. (a) and (b) MAGNETIC CORE SHIFT REGISTER

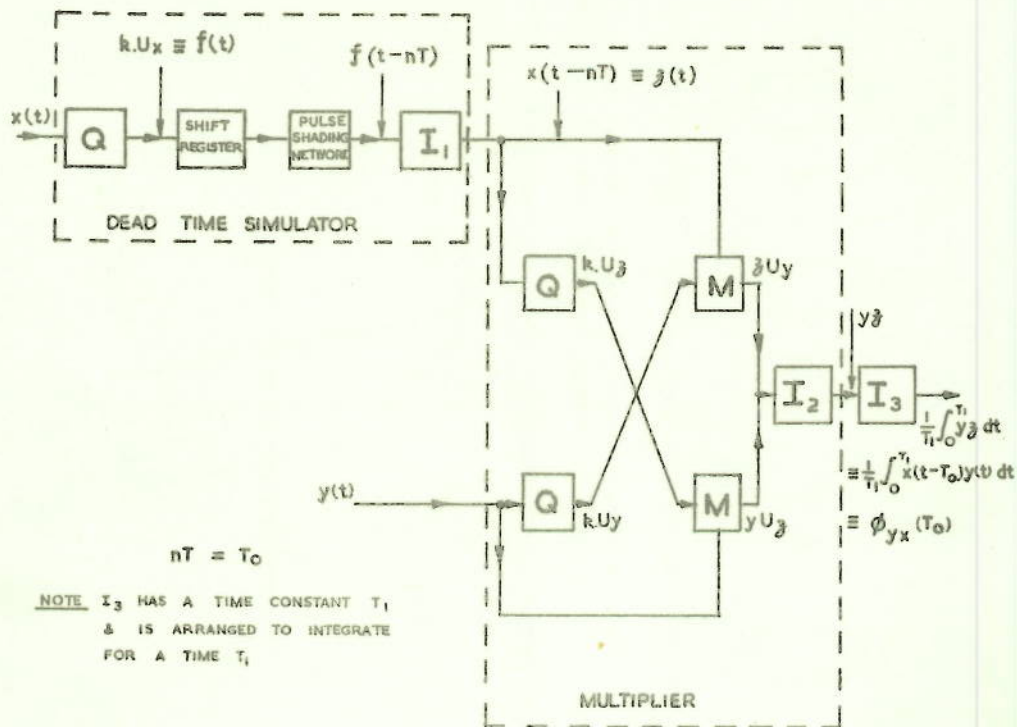


FIG. 11. POSSIBLE ARRANGEMENT FOR CROSS CORRELATOR

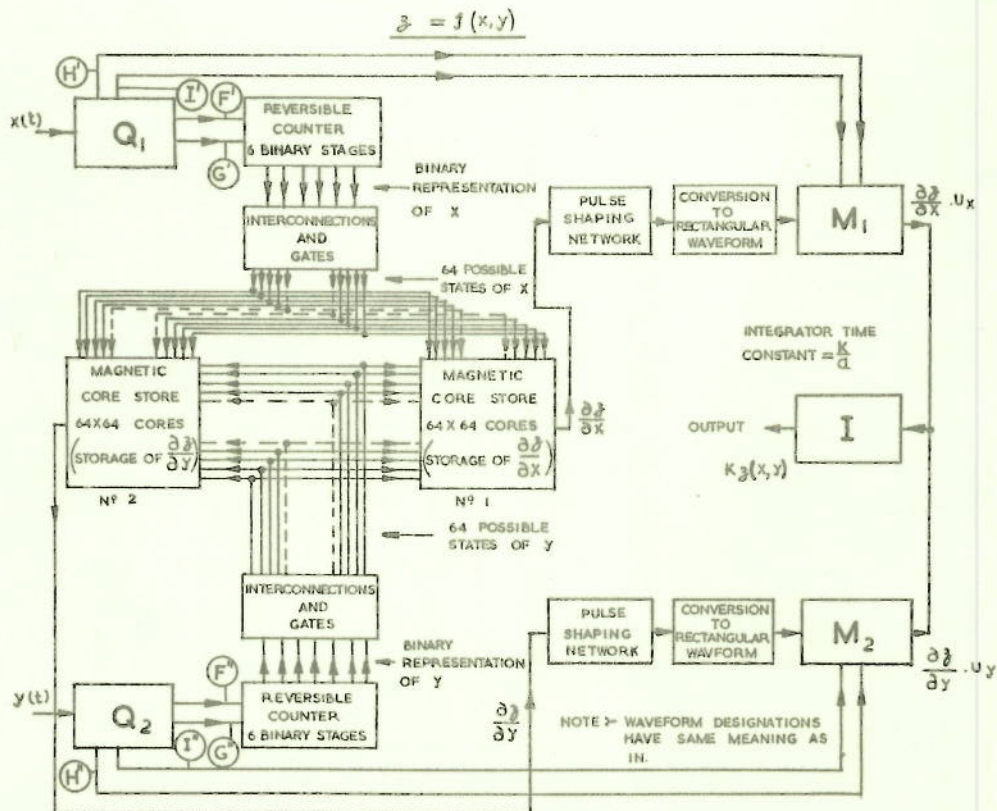


FIG. 12. POSSIBLE ARRANGEMENT FOR GENERATION OF A FUNCTION OF TWO VARIABLES