Note: Phase-locked loop with a voltage controlled oscillator based on a liquid crystal cell as variable capacitance

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A phase-locked loop is demonstrated using a twisted-nematic liquid crystal cell as a capacitance that can be varied as a function of applied voltage. The system is formed by a phase detector, a low-pass filter, as well as a voltage controlled oscillator including such variable capacitance. A theoretical study is proposed and experimentally validated. Capture and locked ranges of hundreds of kHz have been obtained for the configuration used in this circuit. An application as frequency demodulator using a practical implementation of this circuit has been demonstrated. © *2011 American Institute of Physics*. [doi:10.1063/1.3666865]

A phase-locked loop (PLL) is a negative-feedback circuit that allows synchronizing the output signal of an oscillator with a reference signal in frequency and phase.[1] PLLs can be constructed from subcircuits or purchased as medium scale integration devices. There are basically three classes of PLLs: the linear or analog PLL, the digital PLL, and the all-digital PLL. A PLL generally consists of three basic blocks:[2] phase comparator, a low-pass filter, and a voltage-controlled oscillator or as more commonly known, a VCO as shown in schematic form in Figure 1.

Liquid crystals (LCs) are composed of moderate size organic molecules, which tend to be elongated. Because of their elongated shape, under appropriate conditions the molecules can exhibit orientational order, such that all the axes line up in a particular direction. A direct consequence of this ordering is the anisotropy of mechanical, electric, magnetic, and optical properties.[3] In order to build practical devices, liquid crystals are sandwiched between two electrodes showing from an electrical point of view a plane capacitor behavior with a non-ideal dielectric. Liquid crystals are very sensitive to an electric field,[4] and it is precisely this property the most traditionally used for their application to optical device technology. In this way, applications such as displays, optical modulators, variable optical attenuators, spatial light modulators, and optical multiplexers have been widely reported.[5–8]

However, only a few applications for non-optical applications have been described until now and mainly related to microwave region.[9–12]

As it is well known, the capacitance value for a plane capacitor is given by the following expression:

$$C_{LC}(V) = \varepsilon_{LC}(V)\frac{S}{d}, \tag{1}$$

where ε_{LC} is the effective dielectric permittivity of the LC material, which depends on the applied rms voltage across to the device, S is the effective area of the electrodes, and d is the thickness of the device.

In this work, we study the static and dynamic operation of a PLL structure implemented based on a VCO made of a LC nematic cell. Lock and capture ranges have been measured for this circuit, and its right operation as frequency demodulator in the range from 135 kHz to 230 kHz has also been demonstrated.

Various circuits can be used to build a phase detector. The one we present here is a digital phase detector that forms the product of two digital signals. One of these signals is the reference signal and the other is the output of the VCO. On the other hand, the type of the low-pass filter used influences the overall performance of the PLL.

Although there are different alternatives, we will consider a passive *RC* low-pass filter since it is a simple and a suitable solution for this specific application. The VCO is an essential part of a PLL. Typically, it is implemented with a varactor diode whose capacity is tuned by a control voltage. In a previous work, we demonstrated the capability of a twisted-nematic (TN) LC cell to be employed in order to implement a sinusoidal oscillator.[13] In this work, we propose a VCO structure based on a relaxation configuration. This circuit generates a square wave whose oscillation frequency can also be controlled by a dc signal input. The proposed frequency demodulator is based on a PLL circuit as shown in schematic

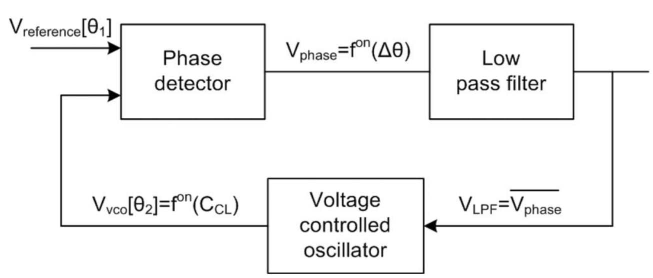

FIG. 1. A schematic of the proposed PLL structure using a TN LC cell as a variable capacitance within VCO.

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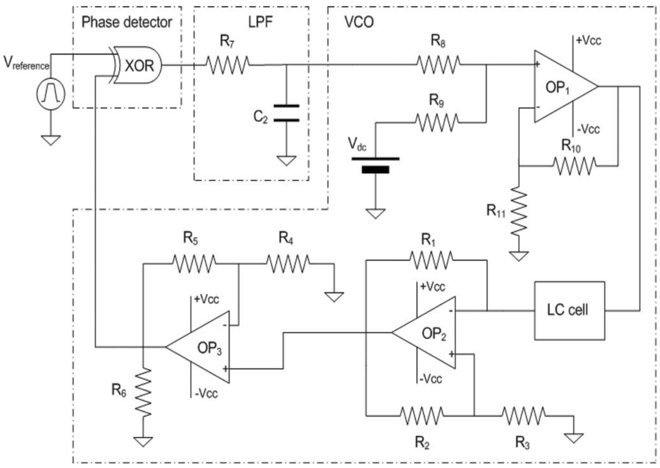

FIG. 2. Circuit PLL implemented including all integrating electronic components.

form in Figure 2. Table I shows the values of the electronic components used in the PLL circuit.

The PLL makes the frequency of the VCO output equal to the frequency of the reference signal by negative feedback under steady-state conditions. If the frequencies are not the same, the voltage output of the filter acts on the VCO so that the frequencies become identical. A phase detector can be made from a XOR logic gate. The output changes the duty cycle in proportion to the phase difference result. Consequently, the XOR output becomes high ("1"), if only one of the inputs is also high ("1"). If both inputs are of equal value, the output results are low ("0"). The low-pass filter, which determines the dynamic characteristics of the PLL, is formed by a resistor and a capacitor. The cutoff frequency is equal to $1/R_7 \cdot C_2$. This value should be chosen to attenuate the higher frequency components. The output of the low-pass filter ($\overline{\upsilon_{XOR}}$) can be expressed in the following way:

$$\overline{\upsilon_{XOR}} = \frac{Vcc \cdot \Delta\theta}{\pi}, \tag{2}$$

where Vcc is the bias of phase detector and $\Delta\theta$ is the phase difference.

The VCO implemented is based on relaxation configuration and may generate a square wave. Thus, the operational

TABLE I. Values of the electronic components used.

Electronic component	Value
R_1	75 kΩ
R_2	220 kΩ
R_3	1 kΩ
R_4	1 kΩ
R_5	1 kΩ
R_6	1 kΩ
R_7	50 kΩ
R_8	10 kΩ
R_9	2 kΩ
R_{10}	2 kΩ
R_{11}	1 kΩ
C_2	1 nF

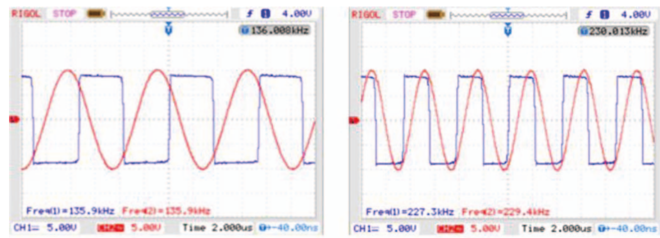

FIG. 3. (Color online) Lock range measured as a function of input voltage for the VCO.

amplifier OP_2, as shown in Figure 2, operates as a comparator, with no negative feedback. Resistors R_1, R_2, and R_3 and the capacitance of the TN LC cell determine the frequency of the output signal. Resistor R_2 has been chosen much greater than R_3 and both act as a voltage divider which put the OP_2 input at fraction the OP_2 output voltage. In this configuration, charge and discharge of the capacitor happen periodically. We may express the relation between the oscillator frequency and the dc input voltage in the OP_2 as

$$f_{VCO} = \frac{1}{2 \cdot R_1 \cdot C_{LC}(V) \cdot ln(1 + (2 \cdot R_3/R_2))}. \tag{3}$$

The capacitance of the TN LC cell has been experimentally measured and its variation ranged from 3.3 nF to 5.5 nF. We assume VCO works over a limited range and it is approximately linear. Figure 3 shows the minimum and maximum frequencies, where the PLL remains in the locked condition.

The theoretical value obtained for minimum [C_{LC} = 5.5 nF] is given by

$$f_0 = 1/[2 \cdot 75k \cdot 5.5\ \text{nF} \cdot ln((2 \cdot 1k + 220k)/220k)]$$
$$= 134.5\ \text{kHz}.$$

This value matches very well with the experimental value $f_0' = 135$ kHz.

On the other hand, the theoretical value obtained for the maximum oscillation frequency [C_{LC} = 3 nF] is f_0 = 245 kHz. The experimental value is, in this case, $f_0' = 230$ kHz.

To verify proper operation of the frequency demodulator, a sinusoidal signal of 200 kHz was applied as the reference input, changing its frequency modulation signal between 500 Hz and 5 kHz. Experimental results are shown in Figure 4.

A new PLL based on a VCO that includes a TN LC cell as a variable capacitance has been proposed and implemented. Theoretical expressions to study its behavior in lock operation have been derived and experimentally validated. The PLL shows a lock range measured between 200 kHz and 230 kHz. An application to show the capability as frequency demodulator has also been proposed.

Experimental results have demonstrated the right operation of the proposed circuit for oscillation frequencies in the range of kHz. Comparing the experimental results and data expected from theory, the disagreement (estimated to be less than 6%) can be explained by the fact that the behavior of the TN LC cell is not fully capacitive in the whole range of

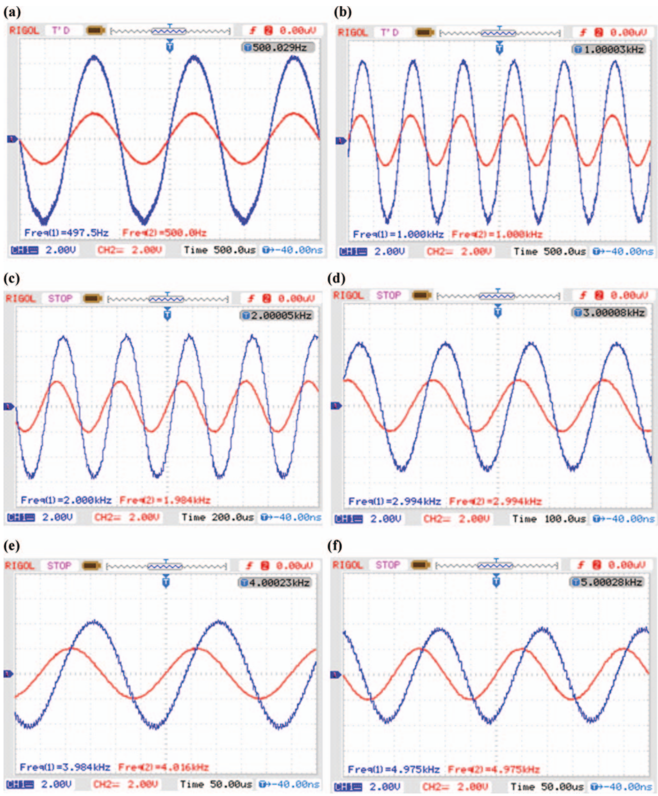

FIG. 4. (Color online) Demodulated signal obtained for different frequency modulation signal: (a) 500 Hz, (b) 1 kHz, (c) 2 kHz, (d) 3 kHz, (e) 4 kHz, and (f) 5 kHz.

frequencies considered. In addition, resistive effects become significant with increasing frequency, which is not taken into account in the model considered. More extended ranges could be achieved with customized liquid crystal cells, adjusting their manufacturing parameters, such as dielectric permittivity, effective area, and thickness, to the capacitance value appropriated. A more detailed theory to describe the electric behavior for the VCO is currently in progress.

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