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Electrical modeling of tristate antiferroelectric liquid crystal devices

Juan Carlos Torres Zafra
Isabel Pérez Garcilópez
Virginia Urruchi del Pozo
José Manuel Sánchez Pena
Carlos Marcos Lucas
Universidad Carlos III de Madrid
Grupo de Displays y Aplicaciones Fotónicas
Departamento de Tecnología Electrónica
Leganés, Spain
E-mail: jctzafra@ing.uc3m.es

Abstract. A new electrical equivalent circuit (EEC) has been proposed to model antiferroelectric liquid crystal devices. This circuit includes a constant phase element to take into account the ferroelectric part of the dielectric response in these devices. Electrical characterization of samples has been carried out using a specific experimental protocol based on impedance spectroscopy. The parameters of waveforms used in impedance measurements have been optimized. The procedure to obtain the components of the EEC has also been explained. Finally, the EEC has been validated by comparing experimental and simulated impedance results. A reasonable agreement between both of them has been obtained in a wide frequency range for all selection voltages. © *2011 Society of Photo-Optical Instrumentation Engineers (SPIE).* [DOI: 10.1117/1.3564817]

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1 Introduction

The most traditional application of liquid crystal (LC) devices is focused on the area of displays. Other photonic applications such as optical-phased arrays for laser beam steering, optical switches and routers, tunable focus lenses, wavelength selective filters and variable optical attenuators have also been described.[1] Additionally, new nonphotonic applications, like tunable electrical filters, are nowadays under research with promising preliminary results.[2]
Although nematics are the LC materials largely used in these applications, in the last decades several devices based on chiral smetic LC have been reported.[3] These materials show a wider viewing angle and a higher contrast ratio and switching speed than nematics. Surface-stabilized antiferroelectric LC (AFLC) devices show a tristate electro-optical response with intrinsic analogue grayscale generation.[4] This feature enables to use them in passive high-end displays and other photonics devices. In this context, AFLC electrical modeling can be useful to design new and optimized drivers.

Several approaches have been reported in order to model the electrical behavior of chiral smectic LC devices. First, an electrical equivalent circuit that gives a physical interpretation of the impedance in ferroelectric devices was proposed.[5] This work demonstrated that charge induced in these devices was comprised of two polarization components (instant and spontaneous polarization), and its behavior could be represented through a suitable combination of passive elements (resistors and capacitors). This passive circuit accounts for physical processes associated with the dynamics of the LC device. Later, that circuit was also used to describe the electrical response of V-shape devices.[6] In this approach, the nonlinear dependence of spontaneous polarization with the voltage applied to the device was taken into account. However, other authors found that the previous electrical equivalent circuit (EEC) required adding two additional resistive components to model the electrical behavior of V-shaped devices when low frequency signals were applied to the LC devices.[7] These resistors performed the function of simulating the conductivity of both the LC material and the device layers.

Until then, EEC was the most comprehensive one allowing working frequencies in a wide range. This circuit considers a device not necessarily symmetric between terminals and allows modeling the effect of the nonsymmetric layers (electrodes, insulation and alignment layers) with different components. However, in this work we have assumed as a working hypothesis, a reasonable symmetry of the cells used in our experiments. Consequently, the EEC displayed in Fig. 1 has been initially considered for modeling the electrical behavior of AFLC devices.

The components of this circuit are related to physical parameters of the sample as follows:

- R_S resistor and C_S capacitor represent, respectively, the resistivity and capacity due to electrodes, insulation, and alignment layers.
- C_{st} capacitor represents the device capacitance associated to the no ferroelectric part of the dielectric response.
- R_{hx} and C_{hx} components are related to the ferroelectric part of the dielectric response.
- Finally, R_{P1} and R_{P2} resistors simulate the conductivity of the device layers and the LC material, respectively.

An experimental protocol, designed and checked in previous works,[8,9] has been implemented to derive the values of components in the EEC of AFLC devices. As a result of this work, a modified EEC from the previous one displayed in Fig. 1 has been proposed and experimentally validated.

As it is well known, capacitors are one of the key elements in integrated circuits and are extensively used in many electronic systems. However, it has been demonstrated that an ideal capacitor cannot exist in nature because an impedance of the form $1/(j\omega C)$ does not fulfils the causality criterion.[10,11] In fact, dielectric materials exhibit a

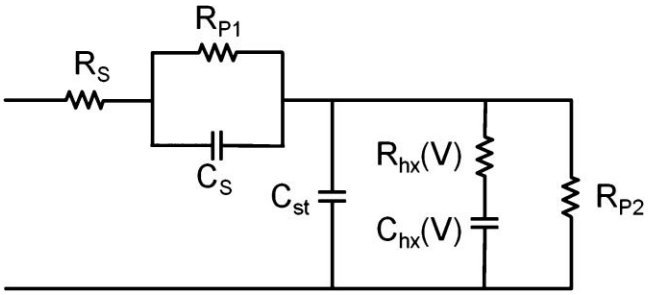

Fig. 1 Initial proposal of EEC to model the electrical behavior of AFLC devices.

fractional behavior yielding electrical impedances of the form $1/(j\omega C)^{\alpha}$.[12] The constant phase element (CPE) was traditionally used to model many systems related to electrochemistry, thermal engineering, acoustics, electromagnetism, among others.[13] Our proposal is based on a new EEC including a CPE to take into account the ferroelectric part of the dielectric response in these devices. This component does not explain the nature of the dynamical behavior of the LC material, but can reproduce its electrical response.

2 Experimental Protocol

The electrical equivalent circuit of AFLC devices has been derived by using an experimental protocol based on impedance spectroscopy.[14] This technique consists of the measurement of complex impedance (magnitude and phase) as a function of frequency. These measurements have been carried out for different switching voltages. Each voltage is related to one intermediate level of optical transmission, which is simultaneously monitorized. The research protocol also includes the EEC components fitting and the EEC impedance simulation. The diagram of the whole procedure is shown in Fig. 2.

2.1 *Impedance Measurement*

The block diagram of the experimental setup to carry out simultaneously measurements of complex impedance and optical transmission in AFLC devices has been displayed in Fig. 3. This measurement system consists of a Solartron

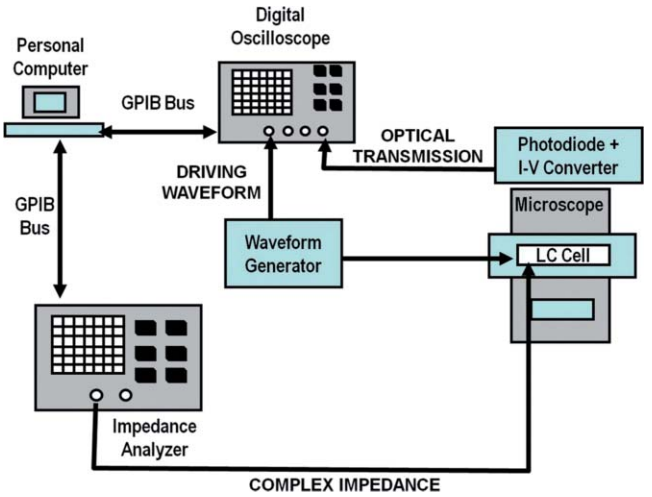

Fig. 3 Experimental setup to acquire impedance measurements.

1260 impedance analyzer, a personal computer (PC) with a National Instruments GPIB communication card, a Linkham LTS-E350 programmable hot-stage, a Nikon Eclipses E600 polarized microscope, a Hamamatsu S1337 large area photodiode with a conditioning circuit (current to voltage converter), and a Lecroy WaveRunner 6100 four channel digital oscilloscope.

Monopixel AFLC samples have been placed between crossed polarizers, with the optical axis of input polarizer parallel to the smectic layers normal. Sample electrodes were connected to the impedance analyzer input connectors. This instrument has an output to a GPIB bus connected to the PC. Communication between the PC and the impedance analyzer was made using two specific Solartron commercial software programs: ZPLOT and ZVIEW. ZPLOT allows selecting the impedance measurement frequency range and generating the suitable voltage waveform to take measurements. Additionally, graphical results can be represented, in real time, on the PC screen by means of ZVIEW software.

In the experiments, the measurement frequency range was from 5 Hz to 1 MHz. The first is the minimum measurement

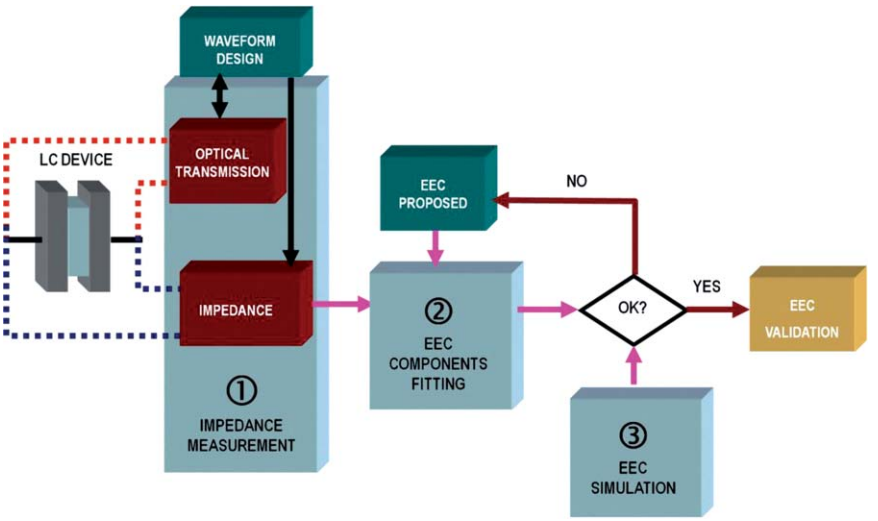

Fig. 2 Diagram of the experimental protocol to derive the EEC for LC devices.

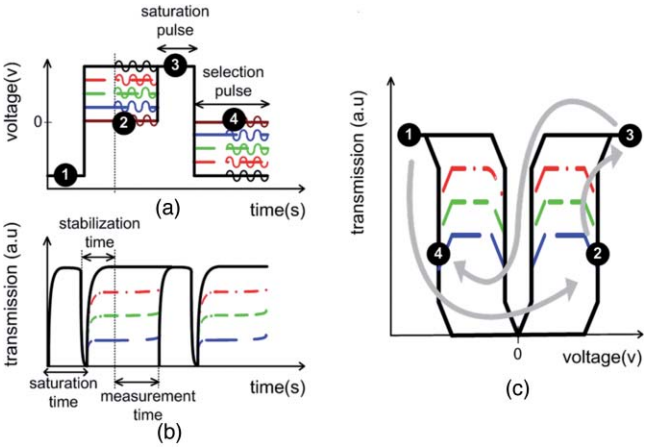

Fig. 4 Applied signals for characterization of AFLC devices by impedance spectroscopy. Timing not to scale: (a) Voltage waveform applied. (b) Optical transmission with saturation blanking. (c) Low frequency electro-optic response.

frequency allowed by the Solartron 1260 impedance analyzer when the dc level voltage is higher than 5 V. The EEC for frequencies higher than 1 MHz has a pure resistive behavior.

Acquisition of impedance measurements after optical transmission becoming stable has been considered especially relevant, thus forcing an optimal waveform design for checking these measurements. The procedure used for this waveform optimization is described in Sec. 2.2.

2.2 *Electro-Optic Characterization and Waveform Optimization*

Complex impedance in LC devices is related to its optical transmission. Both measurements depend on selection voltage applied between the cell electrodes. In AFLC samples, several waveforms have been proposed to obtain intermediate stable transmission levels, between the minimum and the saturation levels.[15] In this work, the waveform shown in Fig. 4 has been demonstrated to be the most suitable to perform impedance measurements. This voltage waveform consists of a variable selection pulse [circles 2 and 4 in Figure 4(a)], to obtain intermediate levels of optical transmission and a fixed saturation pulse [circles 1 and 3 in Fig. 4(a)], to blank the cell before applying the next selection pulse.

The signal period was calculated taking into account the following characteristics:

- A saturation time, to reach the maximum optical transmission level. This time is fixed to 6 s; a delay time for the impedance analyzer switches the selection voltage applied to the cell.
- A stabilization time, to maintain the optical transmission of the intermediate levels. This time is measured experimentally for each sample.
- A measurement time, to acquire impedance measurements by the impedance analyzer. This time depends on the measurement frequency range and the number of acquired points.

Figure 4(b) shows the optical transmission profile when the previously described voltage waveform is applied to an AFLC device.

3 Impedance Measurements by Impedance Spectroscopy

Experiments were performed with monopixel test cells of a tristate AFLC commercial mixture CS-4001 aligned with rubbed Nylon and a SiO_2 barrier layer with a thickness of 1.5 μm and an electrode area of 0.5 cm^2.

Experimental protocol has been applied as follows. Optimized addressing waveforms as previously described were applied to the devices and electric limitations arising from the impedance analyzer have been taken into account. A dc compensated waveform consisting of a saturation pulse and a selection pulse was used. A 50 mV sinusoidal signal has been added to the addressing waveform during measurement time [Fig. 4(a)]. The impedance of the samples (magnitude and phase) has been analyzed in the 5 Hz to 1 MHz range (near 6 decades) and 10 measurements per decade were recorded.

The effect of the selection levels on the magnitude and phase impedance is shown in Fig. 5. A set of impedance measurements has been depicted for negative data levels.

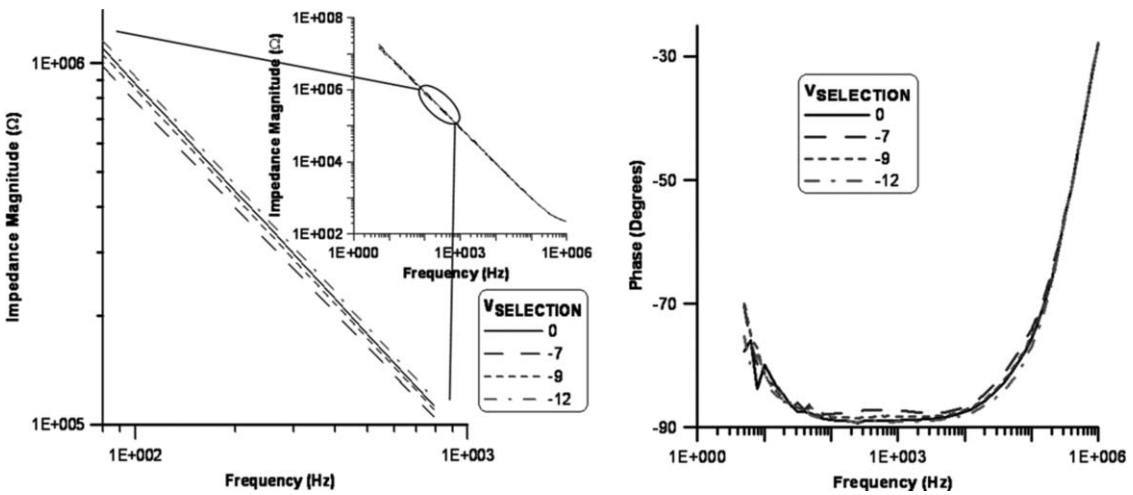

Fig. 5 The effect of the data levels on the impedance measurements for AFLC devices. Note that axes are in logarithmic units for magnitude, but lineal for the phase.

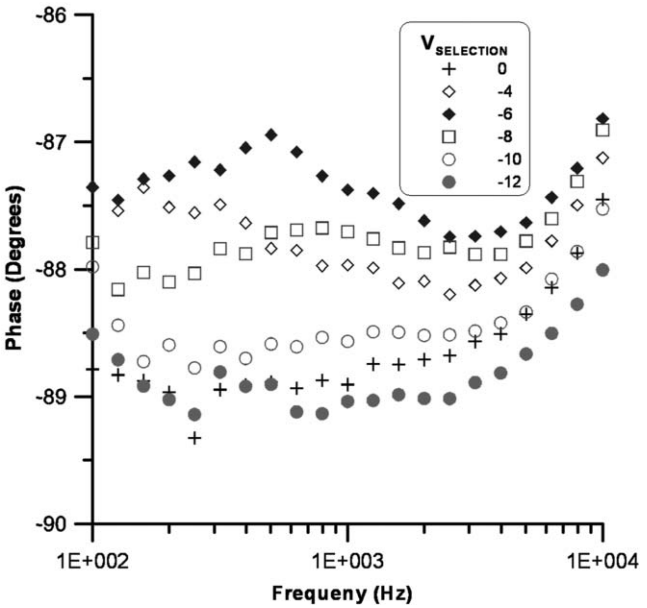

Fig. 6 Detail of the impedance phase magnitude in the 100 Hz to 10 kHz range for AFLC devices.

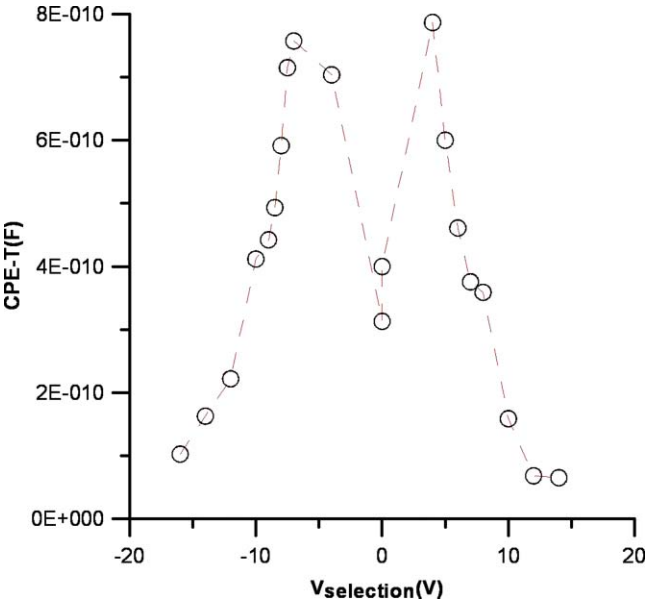

Fig. 8 Selection voltage dependence of capacitance CPE(V) for AFLC devices addressed with optimized waveforms.

The magnitude profile (logarithmic) is linear in almost the whole frequency range and its value decreases more than 4 orders of magnitude as frequency increases for both positive and negative data levels.

Specifically, a thorough analysis of the impedance phase in the 100 Hz to 10 kHz frequency range has been carried out. A direct relationship between the impedance phase and the selection pulse in this frequency range (see the details in Fig. 6) has been observed. Indeed, the selection levels determine the capacitive electric response provided that homogeneous switching is generated over the whole device. A phase range smaller than 3° has been checked and the impedance phase in this working region is near $-90°$, suggesting an almost pure capacitive electrical response.

4 Electrical Equivalent Circuit: A Constant Phase Element

Electrical equivalent circuits of antiferroelectric devices used in this work are based on models for chiral smectic LC devices that have been briefly described above. In order to match both the electrical responses of AFLC devices and the EEC simulated, a modified equivalent circuit has been proposed (Fig. 7). The complex impedance is $Z(\omega, a_k)$ with a_k the circuit components, $a_k = [R_S, C_S, R_{P1}, C_{st}$, CPE (V), R_{hx} (V), $R_{P2}]$.

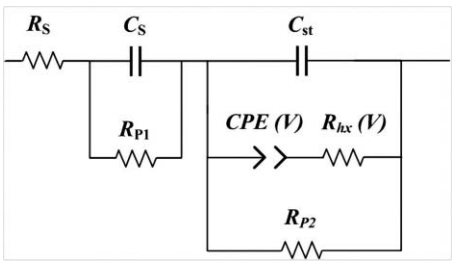

Fig. 7 Schematic of the new proposed electrical equivalent circuit to model AFLC devices.

A voltage dependent CPE (V) has been proposed to model the ferroelectric part of the dielectric response. In fact, this element makes the AFLC device modeling possible by adjusting two parameters, T and P. The frequency dependence of CPE is determined from Eq. (1),

$$Z_{\mathrm{CPE}} = \frac{1}{T \cdot (j\omega)^P} \tag{1}$$

with T the equivalent capacitor and P the exponent.[16]

The EEC proposed has been designed to emulate the AFLC device switching. The value or the initial order of magnitude associated with some components can be estimated from experimental measurements as follows. These conditions must be predefined for this circuit to be fitted:

a. Behavior of capacitors C_S, C_{st} and CPE (V) in the high frequency range (MHz) may be comparable to short circuits. In this way, impedance of the device has been considered equal to R_s in those frequencies,

$$|Z|_{f\to\infty} = R_S. \tag{2}$$

Typical R_S values are some hundreds of ohms.

b. A complementary calculation in the low frequency range gives an estimation of the order of magnitude of $(R_{P1} + R_{P2})$. In these frequencies, capacitors have been considered like open circuits, so that the circuit presents only resistive impedance equal to $(R_S + R_{P1} + R_{P2})$,

$$|Z|_{f\to 0} = R_S + R_{P1} + R_{P2}. \tag{3}$$

Moreover, since R_S has a very small value, impedance magnitude tends to $(R_{P1} + R_{P2})$. Resistive impedance of the device usually has a value of some hundreds of megaohms in low frequencies.

$$|Z|_{f\to 0} \cong R_{P1} + R_{P2}. \tag{4}$$

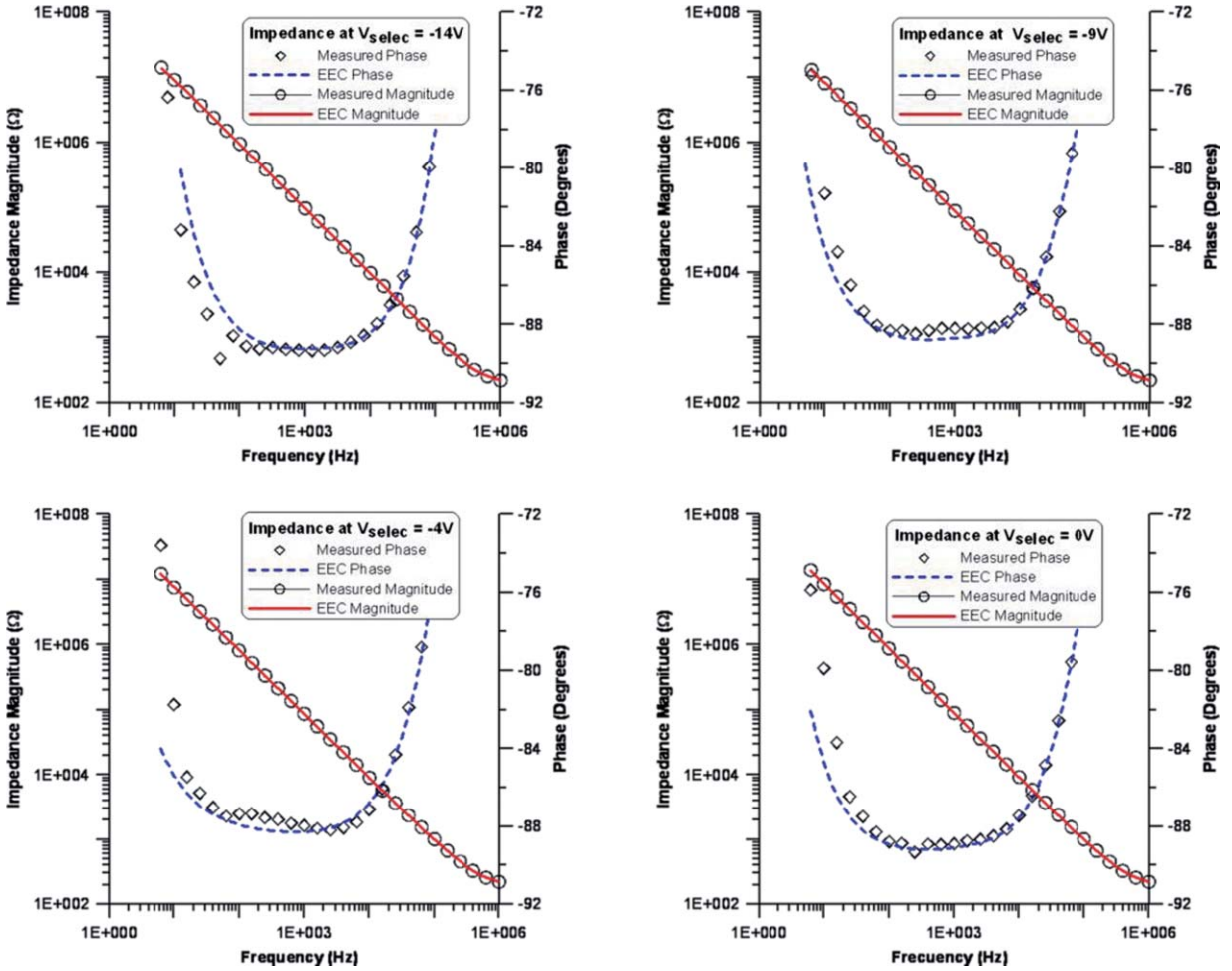

Fig. 9 Comparison between measured and simulated impedances (magnitude and phase) for AFLC devices. Simulations have been made using the proposed fitting method with a constant phase element. Note that impedances correspond to negative selection levels.

c. Series of C_S and C_{st} capacitors has an experimental capacitive impedance in the range of nanofarads.

The rest of the components' values have been derived by complex nonlinear least squares fitting with the experimental impedance data. Levenberg–Marquardt algorithm has been used with a specific program developed with MATLAB. R_S, C_S, C_{st}, $R_{P1,}$ and R_{P2} values have been considered independent of voltage. On the other hand, R_{hx}(V) and CPE(V) have been optimized for all applied voltages.

The profile of the T parameter of the CPE-T as a function of selection voltage, has been drawn in Fig. 8. Nearly symmetric response, for positive and negative selection voltages, as well as a significant nonlinear voltage dependence have been observed. Specifically, the highest capacitive response seems to be related to an intermediate level between ferroelectric and antiferroelectric states.

4.1 *Comparison of Experimental and Simulated Impedance Results*

The last step of the protocol consists of a comparative study of the measured and simulated impedances. Once all the components have been optimized for every selection voltage using the previous fitting method, the EEC has been simulated with all passive electrical elements included. Impedance simulation has been carried out using an input signal like the previous one optimized.

Results are summarized in Fig. 9 for negative selection levels. A fairly good agreement between the measured and simulated impedances for all selection voltages is observed. Specifically, the simulated impedance magnitude matches the experimental data noticeably in the whole frequency range considered. Small deviations between the measured and simulated impedance phases are shown only in the lowest frequency range. This may be attributed to the diffusion of charge that affects the effective impedance at those frequencies. However, phase curves match reasonably in the rest of the frequency range.

5 Conclusions

In this work, an electrical model for tristate AFLC cells has been presented. This model includes a CPE component that takes into account the changes on phase impedance profiles of these devices at specific ranges of frequency. An experimental protocol to carry out impedance measurements has been used.

Optimized values for the EEC components have been derived by fitting EEC simulation and impedance measurements. A reasonable agreement between both of these has been obtained in a wide frequency range for all selec-

tion voltages. The dynamic response in time domain of the tristate AFLC devices, using the previously described electrical model, is under study at the present time.

Acknowledgments

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Juan Carlos Torres Zafra received his MS degree in industrial engineering in 2001 from the Polytechnic University of Valencia, Spain and his PhD degree in electrical, electronic, and automatic engineering from Carlos III University of Madrid in 2009. He is currently an assistant professor at the Department of Electronic Technology of Carlos III University of Madrid. His research interests include drivers design, advanced electronic instrumentation, and electro-optical optimization of LCDs.

Isabel Pérez Garcilópez received her MS degree in telecommunication engineering in 1995 from Polytechnic University of Madrid and her PhD degree in telecommunication engineering from Carlos III University of Madrid in 2003. She is an associate professor at the Electronic Technology Department of the Carlos III University of Madrid. Her main research interests include electro-optical characterization of LC devices and LC applications in photonics and electronics.

Virginia Urruchi del Pozo received her MSc degree and her PhD degree in telecommunication engineering from the Universidad Politécnica de Madrid, Spain, in 1999 and 2004, respectively. She has been an assistant professor at the Universidad Carlos III of Madrid from 2001 to 2009. Since 2010, she has been an associate professor. She has been involved in liquid crystals since 1998 and her research interests are the identification of new liquid crystal mixtures and technologies specifically for photonic (display and nondisplay) applications, electro-optic characterization, driving waveform design, and electrical simulation. She has contributed to the development of a national patent (Spain) about driving and method of fabrication of antiferroelectric liquid crystals displays without holding voltage.

José Manuel Sánchez Pena received his MS and PhD degrees in telecommunication engineering from Polytechnic University of Madrid in 1988 and 1993, respectively. From February to September of 1993, he was a visiting researcher at Exeter University (UK) engaged in modeling of the electro-optical properties of LCDs. In March 1995, he joined Carlos III University of Madrid, where he is currently a full time professor and head of Displays and Photonic Applications Group at Electronic Technology Department His main research interests include electro-optical characterization of LCDs, optical sensors, and optoelectronic instrumentation for rehabilitation technology applications and optical communications. He is a senior member of SPIE and a member of ILCS.

Carlos Marcos Lucas received his MS degree in industrial engineering in 2006 from Carlos III University of Madrid. He is an assistant professor in the Electronic Technology Department of Carlos III University of Madrid. He is currently working toward a doctoral degree on electro-optical optimization and addressing OLED microdisplays.