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PROYECTO FIN DE CARRERA

Design and Analysis of a Low Noise Amplifier for Ultra-Wide Band

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Resumen

En el presente estudio, se realiza un amplificador de bajo ruido para la tecnología Ultra-Wide Band (UWB) con líneas de transmisión y componentes discretos. El amplificador y sus componentes son examinados y simulados. El amplificador de bajo ruido es el primer componente y la clave en el receptor y éste es uno de los principales obstáculos en varios estándares de comunicación. El amplificador de bajo ruido es una parte independiente y se requiere que proporcione un consumo de corriente muy bajo, una baja distorsión de la señal y una ganancia muy alta.

El primer y más importante paso en el diseño del amplificador de bajo ruido es la elección del transistor. La tecnología GaAs pHEMT es la elegida para el diseño del amplificador de bajo ruido a nivel del transistor. Un figura de ruido alrededor de 1,2 dB se logra para asegurar que la contribución de ruido del amplificador es tan baja como sea posible y una ganancia de alrededor de 13 dB.

El programa ADS de Agilent ha sido utilizado para simular el esquema y la herramienta Momentum para optimizar el layout del diseño. Una vez se consigue tener el layout optimizado se procesa la PCB y se realizan las medidas experimentales pertinentes.

El PFC se lleva a cabo bajo una beca Erasmus en la Universidad de Stuttgart (Alemania) en el “Institut für Elektrische und Optische Nachrichtentechnik”.

Abstract

In the present study, a Low Noise Amplifier (LNA) for Ultra-Wide Band (UWB) with transmission lines and discrete components is built. These existing LNA components are examined and simulated. The Low Noise Amplifier is the first and a key component in the receiver and this is one of the main obstacles for various communication standards. The Low Noise Amplifier as a stand-alone product is required to provide a very low current consumption, low signal distortion and high signal voltage gain transfer.

The first and most important step in a Low Noise Amplifier design is the transistor selection. GaAs pHEMT technology has been chosen for the design of the LNA at the transistor level. A noise figure around 1.2 dB is achieved to make sure noise contribution of the amplifier is as low as possible and a gain around 13 dB.

ADS Agilent program has been used to simulate the schematic and Momentum tool of ADS Agilent has been used to layout it.

The PFC is carried out under Erasmus student at the University of Stuttgart (Germany) in the “Institut für Elektrische und Optische Nachrichtentechnik".

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Capítulo 1

Introducción

La transmisión inalámbrica de datos es cada vez más importante. La gran demanda de circuitos de banda ancha está siendo impulsada por la recién introducida tecnología Ultra-Wide Band (UWB), que es capaz de transmitir señales de baja potencia con velocidades de datos muy altas sobre un amplio espectro de bandas de frecuencia. En todo caso, el requisito básico en el transceptor UWB es un amplificador de banda ancha de bajo ruido. Este amplificador requiere una alta ganancia, baja figura de ruido y alta linealidad en toda la banda con un bajo consumo de energía.

Ultra-Wide Band (UWB) ha sido diseñado para aportar comodidad y la movilidad de la comunicación inalámbrica de alta velocidad a hogares y oficinas. El corto rango de la tecnología UWB también complementará otras normas inalámbricas como Wi-Fi y Wi-Max. Se puede transmitir datos dentro de un radio de 10 metros desde el dispositivo host. La tecnología UWB está diseñada para ofrecer un rango corto, conexión de energía muy bajo con mucho más ancho de banda que el cable. Desde que UWB se comunica con impulsos de corto rango, se puede utilizar para el seguimiento de diversos objetos.

Capítulo 2

Diseño y Simulación

El primer paso en el diseño es la selección del transistor y una vez elegido este transistor se pasa a elegir el circuito más adecuado. Después, se realizan las simulaciones de los distintos circuitos elegidos, simulaciones de los parámetros S y la figura de ruido. Una vez elegido el circuito se procesa el circuito impreso(PCB, Printed circuit board de ahora en adelante) y se miden experimentalmente.

El programa utilizado para llevar a cabo las simulaciones necesarias de tanto del transistor como del esquema del amplificador se realizaron con el programa ADS de Agilent.

2.1. Figuras de mérito

A la hora de la elección tanto del transistor como del esquema a usar es importante saber a partir de que parámetros decidiremos cual es la mejor opción.

Las Cinco figuras de mérito clave de un amplificador de bajo ruido son la ganancia, el ancho de banda, la figura de ruido, linealidad, la adaptación de impedancia y el consumo de energía. En el diseño del amplificador el primer paso es la elección del transistor. Las dos características más importantes de un transistor son su capacidad para amplificar (importante para analógica y electrónica de RF) y su capacidad de actuar como un interruptor (importante para electrónica digital), en nuestro caso se considera la primera característica. En un transistor se debe tener en cuenta la ganancia, los límites de frecuencia, la potencia de salida y la figura de ruido mínima como figuras de mérito.

En primer lugar, las curvas $V_{ce} - I_c$ son útiles en la elección del punto de funcionamiento óptimo de un transistor utilizado como amplificador. Este punto

debe ser elegido en la región activa, donde el cambio en la corriente de colector es proporcional al cambio en la corriente de base. Esta región lineal es ideal para el uso de la amplificación.

Otra figura importante de mérito es la frecuencia de tránsito f_T. La frecuencia de tránsito también se llama frecuencia de ganancia unitaria y se obtiene estableciendo la ganancia de pequeña señal igual a 0 dB.

$$h_{fe} = \frac{i_c}{i_b} = \frac{g_m}{i_B} v = \frac{\beta}{1 + jw(C_{j,BE} + C_{d,BE}) r_\pi} \Rightarrow h_{fe} = 1 \Rightarrow f_T = \frac{1}{2\pi\tau} \quad (2.1.1)$$

$$\tau = \frac{C_{j,BE} n V_T}{I_E} + \frac{w_B'^2}{2D_{1,B}} = \tau_E + \tau_B \quad (2.1.2)$$

Mientras que la frecuencia de ganancia unitaria es una figura importante de un transistor bipolar, otra figura más importante es la frecuencia de oscilación máxima f_{max}. Esta figura de mérito indica la frecuencia máxima a la que se puede esperar ganancia de potencia útil de un dispositivo.

$$f_{max} = \frac{f_T}{2\pi R_B C_{j,BC}} \quad (2.1.3)$$

Hayamos estas frecuencias a través de las curvas de MAG (Maximum Available Power Gain), MSG (Maximum Stable Power Gain) y U (Unilateral power gain), como se observa en la siguiente figura.

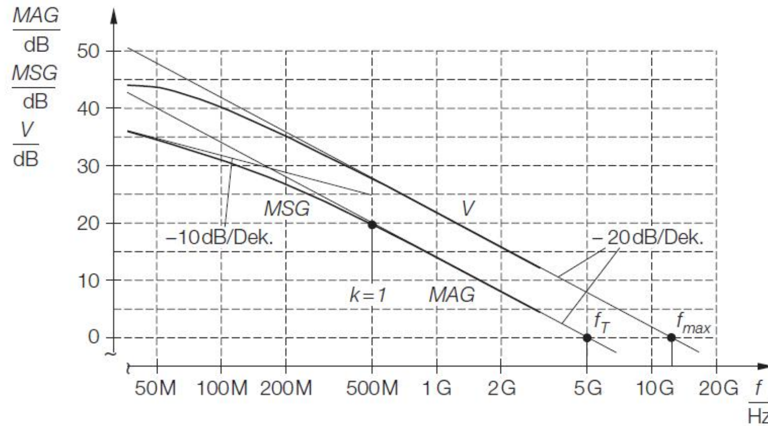

Figura 2.1: Máximas ganancias de potencia de un transistor

La MAG asume el valor 1 o 0 dB en la frecuencia de tránsito f_T del transistor. La U es mayor que uno, incluso por encima de la frecuencia de tránsito. La frecuencia con la que U asume el valor 1 o 0 dB se llama la frecuencia máxima de oscilación f_{max}.

La figura de ruido y la ganancia son figuras de mérito muy importantes en la elección tanto del transistor como del circuito a ser implementado.

2.2. Transistor

El transistor debe exhibir alta ganancia, tener una baja figura de ruido y bajo consumo de corriente y, por supuesto, el transistor debe cubrir el ancho de banda requerido para la aplicación, en este caso desde 6,5 hasta 8 GHz.

Las tecnologías elegidas son semiconductores SiGe y GaAs por sus características en alta frecuencia. En primer lugar se realizaron las simulaciones de los transistores FPD200P70 (pHEMT GaAs) del fabricante RR Micro Devices y del transistor BFP740 (SiGe HBT) del fabricante Infineon. Los mejores resultados se obtuvieron para el transistor FPD200P70 y a continuación mostramos estas simulaciones.

La simulación de la curva $V_{DS} - I_{DS}$ no es correcta, como se ve en la figura 3.1. Los valores de I_{DS} deberían llegar hasta los 100 mA y nosotros conseguimos como máximo 60 mA. Nosotros realizamos la simulación con el parámetro V_{GS} en vez del parámetro V_G como se ve en el gráfico del datasheet del transistor (figura b) y por esto obtenemos valores diferentes. El transistor es alimentando normalmente con $V_{DS} = 3V$ y $I_{DS} = 30mA$ y estos serán los valores que utilizaremos.

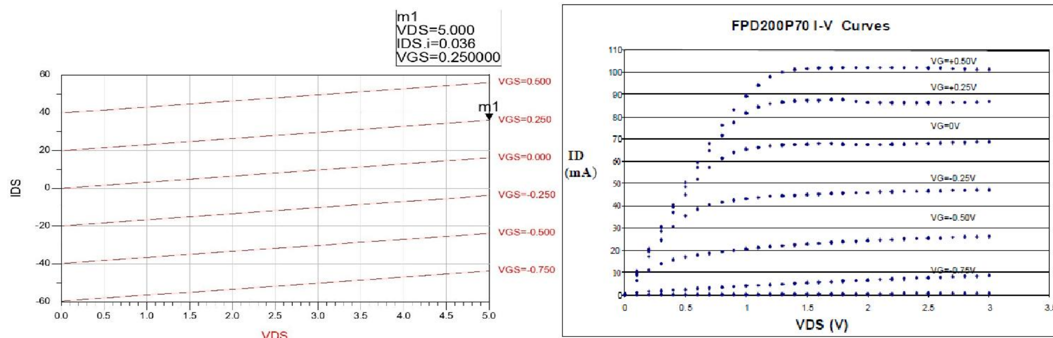

Figura 2.2: Curvas Vds-Ids del transistor FPD200P70

En la figura siguiente se observa la MAG (Maximum Available Gain), el parámetro S_{21} y la ganancia del transistor. El datasheet provee una MAG de 17 dB a 5,5 GHz y nosotros obtenemos casi 20 dB a esa frecuencia. En la figura se aprecia fácilmente la similitud entre nuestra simulación y la provista por el datasheet.

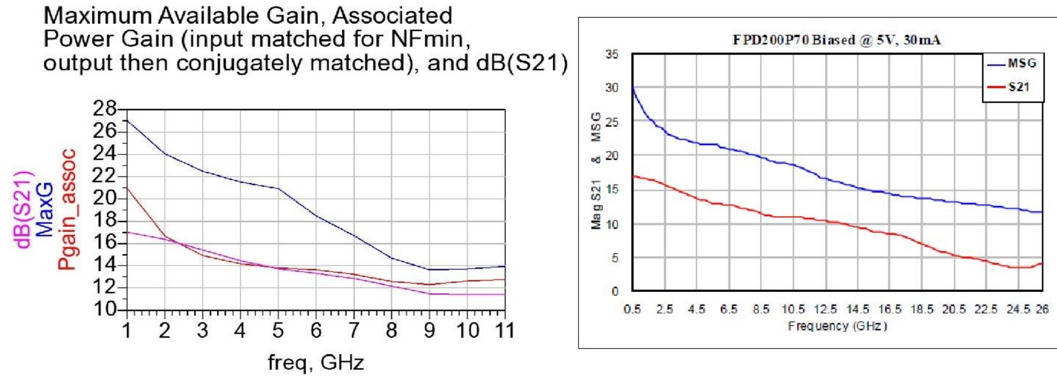

Figura 2.3: MAG, S21 (dB) and ganancia del transistor FPD200P70

La figura de ruido crece desde 0,4 hasta 1,4 dB en el rango de frecuencias de 1 GHZ hasta 11 GHz. La simulación se realizó alimentando a $V_D = 3V$, así que debemos comparar nuestra simulación con la línea roja del gráfico provisto por el datasheet. El datasheet da valores de 0,15 dB hasta 1,28 dB desde 0,8 GHZ hasta 11 GHz, por lo tanto obtenemos similares resultados.

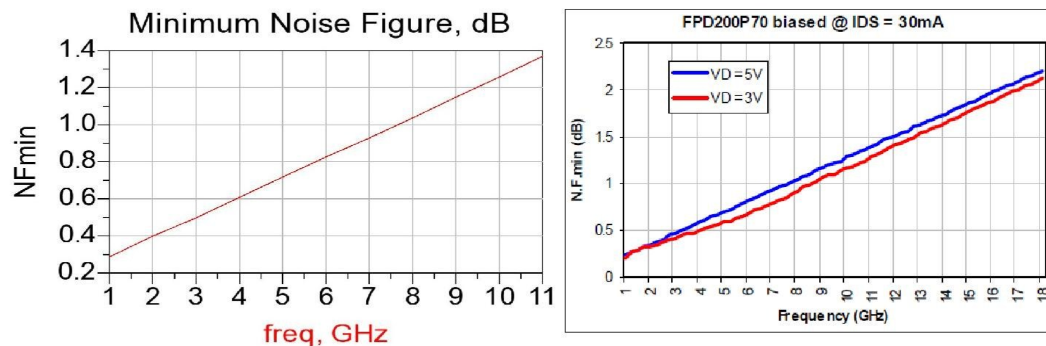

Figura 2.4: Figura de ruido del transistor FPD200P70

Una vez hemos comprobado que nuestro transistor funciona correctamente y obtenemos los resultados que necesitamos, alta ganancia y bajo ruido en un gran ancho de banda, el siguiente paso es elegir el circuito a utilizar.

2.3. Esquemático

El primer pensamientos fue utilizar elementos discretos para el circuito, pero sopesando los pros and cons, decidimos utilizar un circuito con lineas de transmisión finalmente. Los resultados obtenidos en las primeras simulaciones para circuitos con elementos discretos estuvieron muy por debajo de las especificaciones necesarias, la ganancia no era suficiente y, además, abarcaba un rango muy pequeño de frecuencias y la figura de ruido era mayor de 4 dB normalmente.

A continuación se va a presentar el circuito elegido finalmente y sus simulaciones.

El circuito elegido es un híbrido entre líneas de transmisión microstrip y elementos discretos, como el transistor, condensadores y resistencias.

En primer lugar tenemos el transistor, como se mencionó anteriormente es el transistor FPD200P70. Necesitamos adaptar las impedancias de entrada y salida a nuestro transistor (50 Ω) en el ancho de banda deseado (6-8,5 GHz). Por lo tanto se calculan las redes de adaptación de entrada y salida. El cálculo de estas redes se llevo a cabo con stubs en circuito abierto o cerrado y la ayuda de la carta de Smith. En el datasheet del transistor podemos observar un diseño de referencia, el cual hemos utilizado para nuestro diseño. El rango de frecuencias utilizado en este diseño de referencia es de 5,15 GHz hasta 5,8 GHz y nosotros ajustamos este circuito para el rango de frecuencias desde 6 GHz hasta 8,5 GHz. Para extender el ancho de banda se jugó con la longitud de las líneas de transmisión, utilizando la herramienta "tuned" del programa ADS de Agilent se eligieron estas longitudes y se cambiaron sus valores hasta conseguir el resultado necesario.

Para el circuito de alimentación, la puerta necesita aproximadamente una referencia negativa de 0,2 V en cuanto a la fuente, la entrada de un transistor HEMT es básicamente un pequeño diodo y en operación normal estos diodos son alimentados negativamente en referencia con la fuente, por lo tanto la puerta del transistor es alimentada a -0,5 V y el drenador a 5 V, la fuente está conectada a tierra. Se ha utilizado una "bias T", queremos DC en un puerto y RF en los otros dos puertos y lo logramos colocando un stub radial, éste crea un cortocircuito en el lugar donde es colocado. Uno de los mayores problemas en este método de alimentación es que la alimentación negativa debe ser encendida primero y apagada en último lugar.

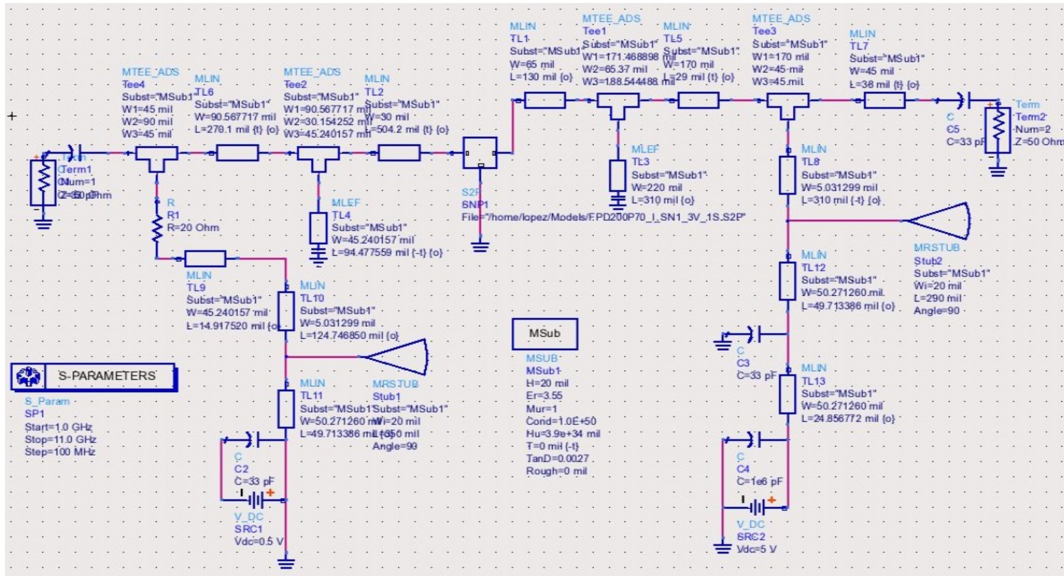

Figura 2.5: Esquema del Amplificador de Bajo Ruido

A continuación se muestran las simulaciones realizadas con este esquemático.

En la primera figura se puede observar la simulación de los parámetros S. El ancho de banda del circuito cubre desde 5,4 GHz hasta 10,4 GHz, más que suficiente, ya que nosotros solo necesitamos un ancho de banda de 6 a 8,5 GHz. La frecuencia central se encuentra en los 7,3 GHz con un valor de 14,554 dB del parámetro s_{21}, en 6 GHz este valor es de 11,059 dB y para 8,5 GHz es de 11,469 dB, por lo tanto el esquemático está funcionando apropiadamente en ganancia. Los parámetros s_{11} y s_{22} se encuentran por debajo de 0 dB, por lo tanto podemos asegurar que el amplificador no tiene reflexiones en los puertos de entrada y salida teóricamente.

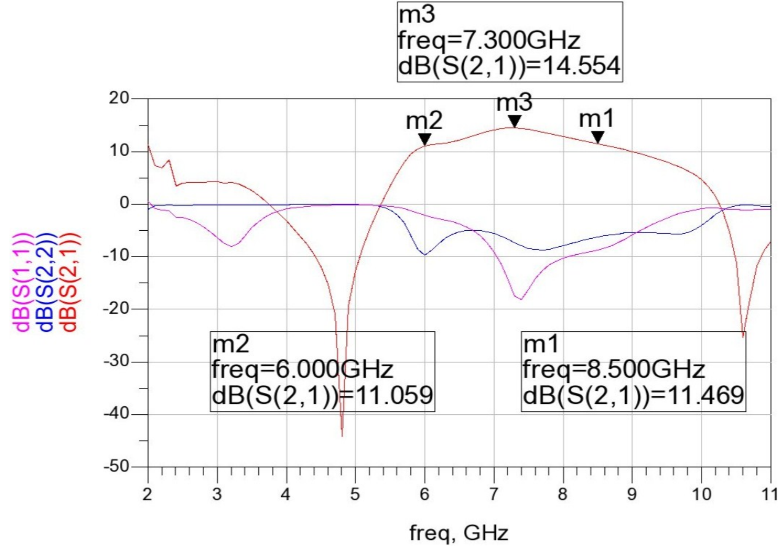

Figura 2.6: Simulación de los parámetros S del amplificador

La siguiente figura muestra diferentes tipos de ruido. Para poder entender mejor el gráfico explicamos estos distintos tipos de ruido.

nf(k) es la figura de ruido en el puerto k, es decir, cuando la figura de ruido es calculada en ese puerto los otros puertos en la red están terminados en sus respectivas impedancias. Por lo tanto nf (2) es la figura de ruido en el puerto 2 cuando el puerto 1 está terminado por su impedancia.

NF_{min} es la mínima figura de ruido que el circuito produce cuando la fuente tiene un coeficiente de reflexión óptimo, S_{opt}.

En la figura se observa una figura de ruido de alrededor 1-1,5 dB, la cual es muy pequeña como se desea en nuestro caso. Podemos decir que el amplificador también está funcionando correctamente en ruido.

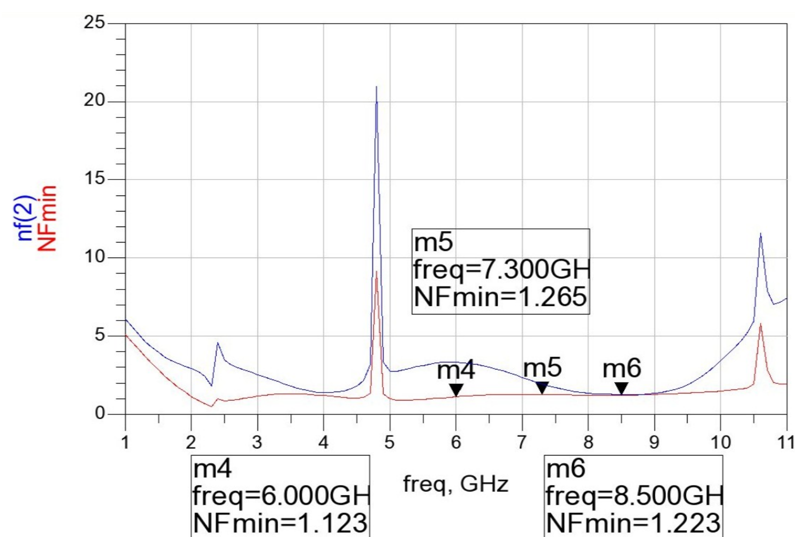

Figura 2.7: Simulación de la figura de ruido del amplificador

Una vez hemos comprobado que teóricamente obtendríamos los resultados necesarios con este circuito, el paso siguiente es crear el layout del amplificador, como se explica en la sección siguiente, paso previo al procesado de la placa (PCB).

2.4. Layout del Amplificador de Bajo Ruido

Para realizar el layout del circuito se utilizó la herramienta Momentum del programa ADS de Agilent. Este proceso fue llevado a cabo en partes, en primer lugar se creó el layout de la red de adaptación de entrada y después de la red de adaptación de salida. Una vez estabamos seguro de que los layout eran correctos, se juntaron los dos layouts previos en uno solo.

El programa automáticamente abre la ventana de layout y genera el layout del circuito. La orientación de éste es diferente a la del circuito, porque el layout es dibujado de izquierda a derecha, empezando por el primer componente, por esta razón se debe reorganizar el layout generado, para que las líneas de transmisión no se solapen entre ellas.

Se requiere un sustrato como parte del layout, éste se describe como el medio donde el circuito existe. Para nuestro circuito se utilizó un sustrato con las siguientes capas:

- Un plano de tierra.

- Una capa de aislamiento, llamada MSub1_1.
- Una capa de metal para el microstrip.
- Una capa de aire por encima del microstrip.

A continuación se cambio el cable por líneas de transmisión (el mínimo ancho y largo de éstas es de 50 mm, para procesar después la PCB). Las resistencias y los condensadores fueron cambiados por modelos, y finalmente se definieron los puertos de entrada y salida. Por último se añadieron conectores SMP, ya que en la futura implementación de la PCB serán necesarios para alimentar el circuito.

El resultado final se muestra a continuación.

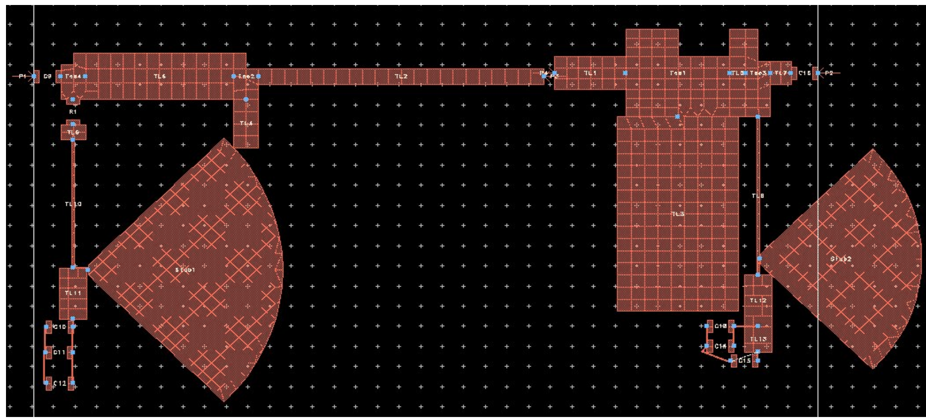

Figura 2.8: Layout del Amplificador de Bajo Ruido

Las simulaciones finales se llevan a cabo con el layout generado anteriormente. Este layout es convertido en un componente, para poder añadir el transistor y la alimentación del circuito, como se observa en la figura.

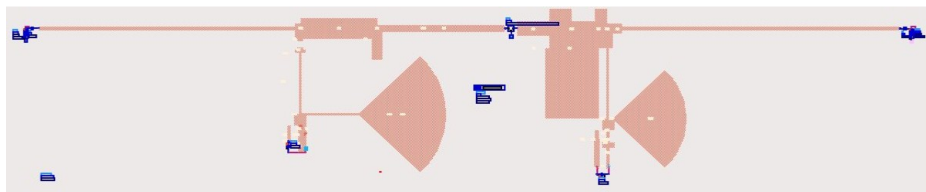

Figura 2.9: Amplificador de Bajo Ruido, layout más los componentes discretos

En la simulación de los parámetros S se obtuvieron los siguientes resultados, el ancho de banda del amplificador cubre desde 5,5 hasta 9 GHz, pero los valores

sufren una degradación en los lados, esto es debido a la red de adaptación de salida, que tiene un ancho de banda menor que la de entrada. Aún así los valores obtenidos son suficientes para nuestro propósito.

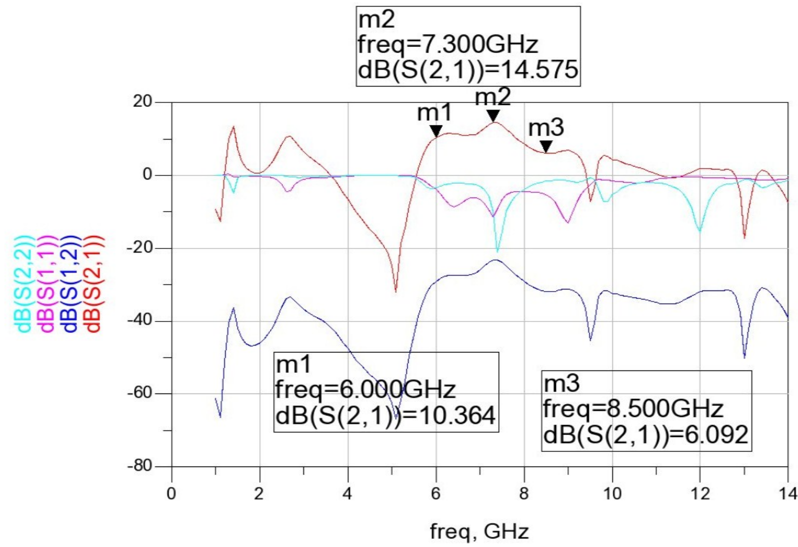

Figura 2.10: Simulación final de los parámetros S

Para el ruido, los resultados son similares a los obtenidos en la simulación del circuito.

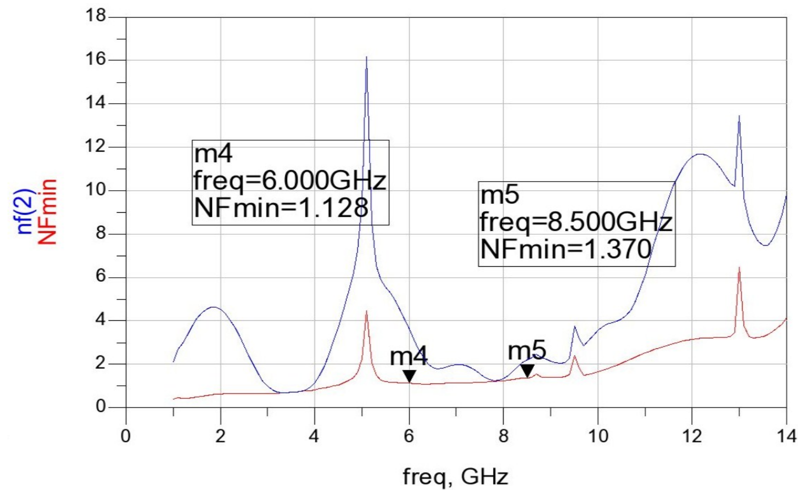

Figura 2.11: Simulación final de la figura de ruido

Capítulo 3

Implementación y PCB Test

3.1. Procesamiento del Amplificador de Bajo Ruido

Una vez estamos seguros de los resultados obtenidos teóricamente para nuestro amplificador de bajo ruido, el último paso es procesar la PCB y medirla. El layout obtenido anteriormente se exporta en formato gerber para producir la placa. Esta placa es insertada en una fijación para hacer más fácil su medición. Además los conectores SMP son añadidos, los elementos discretos son soldados, resistencias, condensadores y el transistor. Se muestra el resultado final en la figura siguiente.

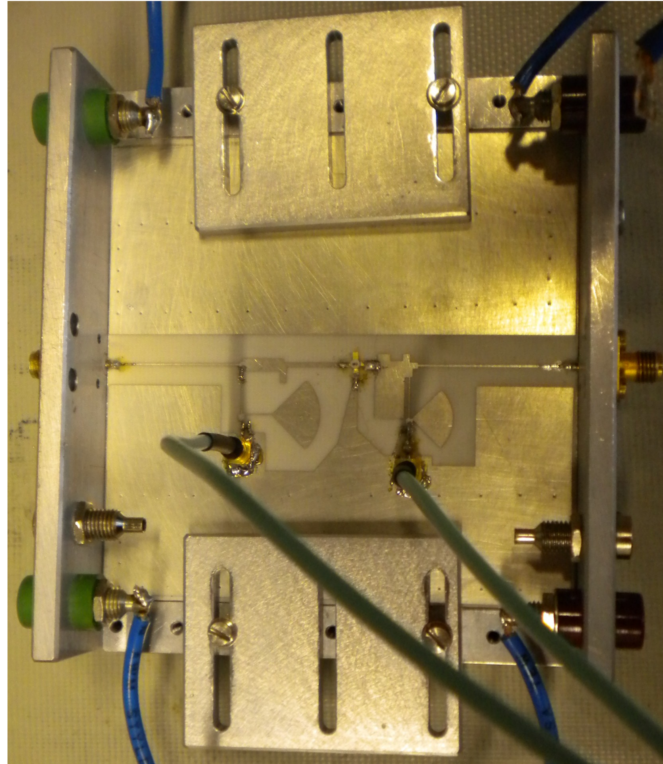

Figura 3.1: Circuito impreso del Amplificador de Bajo Ruido

3.2. Banco de pruebas

Una vez hemos obtenido la PCB, el siguiente paso es realizar las medidas experimentales necesarias.

En primer lugar, se verifica la continuidad de la PCB. La resistencia de un circuito eléctrico determina cuánta corriente fluye en el circuito cuando un cierto voltaje se aplica. Para hacer las pruebas de continuidad el procedimiento es el mismo que al medir resistencias, se utiliza el multímetro en ohmios y se comprueba si el circuito ofrece una baja resistencia o muy pocos ohmios. Se utilizó la opción de 2K o 20K ohmios, ya que ofrecen un voltaje de 1-2 voltios, que no es tanto para nuestro circuito, sin embargo, se evitó utilizar el multímetro en 200 ohmios y la opción de continuidad, ya que ofrecen 5-6 voltios y este valor es muy alto para nuestro circuitoy así se evitan daños al circuito.

Una vez que verificó la continuidad de la placa, se miden los parámetros S de la PCB. El montaje utilizado se explica a continuación.

En primer lugar está la PCB, seguidamente se coloca un atenuador de 20 dB, porque no se pueden insertar más de 17 dBm en la máquina utilizada, con el atenuador estamos seguros de no introducir más. El último elemento de la figura es un bloqueador de corriente continua, de nuevo, no se puede insertar corriente continua en la máquina y este bloque evita introducir la corriente continua proporcionada por la PCB. Hemos utilizado dos fuentes de alimentación, hay dos conectores SMP en el circuito, para alimentar la puerta a -0,5 voltios y el drenador a 5 voltios.

Por último, en la siguiente sección se muestran las medidas de los parámetros S que hemos logrado.

3.3. Resultados de las medidas

Las medidas experimentales de la PCB se llevaron a cabo con una máquina de parámetros S. Se obtuvo un documento de texto con los valores para cada parámetro S. Este documento de texto es procesado con Matlab. Como hemos añadido un atenuador de 20 dB después de la PCB, se tienen que añadir 20 dB al parámetro s_{21}. El aislamiento hacia atrás (parámetro s_{12}) debe ser alto y la atenuación externa no debe afectar a las perdidas de retorno de entrada y salida (parámetros s_{11} y s_{22}), ya que es perfecto 50 Ω.

La siguiente figura muestra los resultados de los parámetros S medidos.

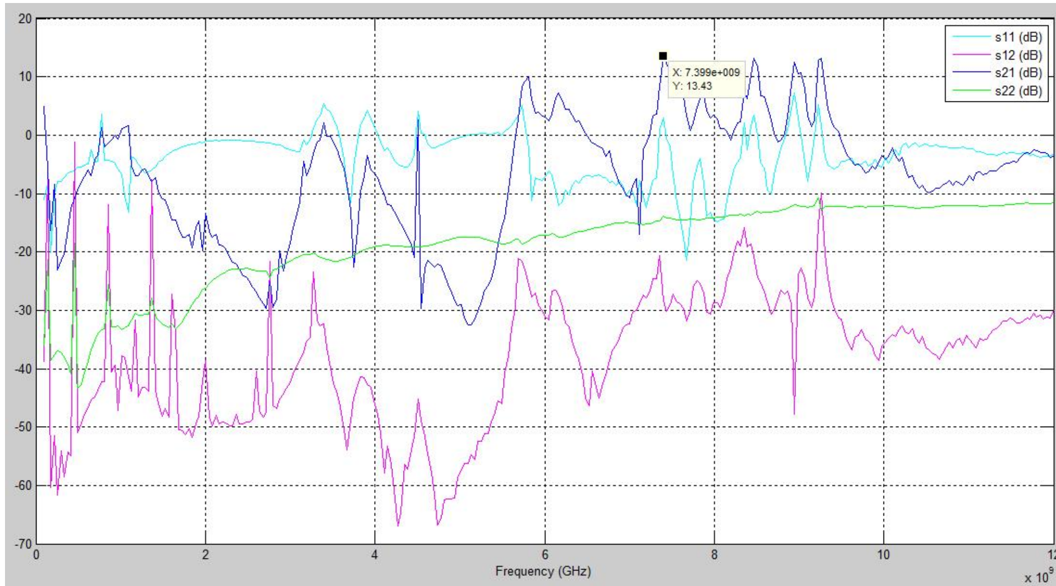

Figura 3.2: Resultados de los parámetros S medidos

Se observa que el ancho de banda es de 7 a 9,5 GHz. El valor mas alto se consigue a 7,4 GHz con 13,43 dB, el problema es que el resultado del parámetro s_{21} no es plano en el ancho de banda, porque el transistor produce oscilaciones al no ser estable en todo el rango de frecuencias. La figura siguiente muestra la estabilidad del transistor de 1 a 11 GHz. El transistor es estable cuando el valor de K es mayor de 1 dB, lo que ocurre en el rango de 5 a 11 GHz, posiblemente este sea el problema.

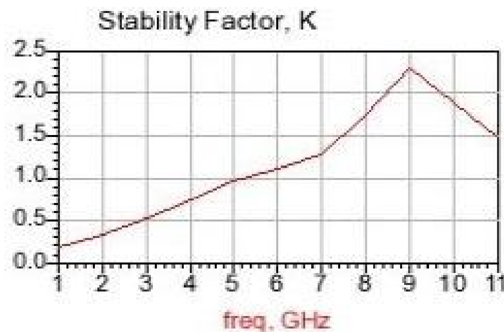

Figura 3.3: Estabilidad del transistor. Valor K

Además, tenemos que mencionar que el transistor, finalmente fue alimentado a -0,3 voltios en la puerta y 3 voltios en el drenador, si no los resultados eran

peores. En este punto nos dimos cuenta de que primero se debe activar la tensión de alimentación en la puerta y desactivar en último lugar, si no el transistor comienza a oscilar y no funciona correctamente.

Capítulo 4

Conclusión

El objetivo principal de este proyecto fue diseñar un Amplificador de Bajo Ruido que podría ser utilizado para aplicaciones de UWB (Ultra-Wide Band). Fue pensado para que el amplificador sea capaz de proporcionar suficiente ganancia en el rango de frecuencia de 6 a 9 GHz (especificado para la tecnología UWB en Europa) con el mínimo ruido.

La tecnología GaAs fue la elegida para el proyecto. El diseño propuesto tiene una ganancia de alrededor de 13 dB en el rango de frecuencia de 5,5 a 9 GHz, en la simulación, después comienza a disminuir. La figura de ruido es de alrededor de 1 dB.

Los resultados de las medidas experimentales no son tan buenos como los resultados de las simulaciones, pero es un comienzo para mejorar la ganancia en el ancho de banda necesario.

Apéndice A

Memoria en inglés

En las siguientes páginas se presenta la memoria llevada a cabo en la Universidad de Stuttgart (Alemania).

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Design and Analysis of a Low Noise Amplifier for Ultra-Wide Band

Diplomarbeit

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Abstract

In the present study, a Low Noise Amplifier (LNA) for ultra-wide band (UWB) with transmission lines and discrete components is built. These components are examined and simulated. The Low Noise Amplifier is the first and a key component in the receiver and this is one of the main obstacles for various communication standards because the low noise amplifier as a stand-alone product is required to provide a very low current consumption, low signal distortion and high signal voltage gain transfer.

The first and most important step in a Low Noise Amplifier design is the transistor selection. GaAs pHEMT technology has been chosen for the design of the LNA at the transistor level. A noise figure around 1.2 dB is achieved to make sure noise contribution of the amplifier is as low as possible and a gain around 13 dB.

It was processed a Printed Circuit Board for the Low Noise Amplifier designed. The measurement results must to improve in gain, but the bandwidth achieved is enough for the purpose of the ultra wide band application.

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Abbreviations and Symbols

Abbreviations

Abbreviation	*Explanation*
UWB	Ultra-Wide Band
LNA	Low Noise Amplifier
FCC	Federal Communications Commission
HDR	High-Data-Rate
LDR	Low-Data-Rate
GPR	Ground-penetrating Radar
VSWR	Voltage Standing Wave Ratio
BER	Bit error ratio
RF	Radio frequency
DUT	Device-under-test
S/N	Signal-to-Noise
NF	Noise Figure
F	Noise Factor
IC	Integrated circuit
FPGA	Field Programmable Gate Array
MEMS	Micro Electro Mechanical Systems
CMOS	Complementary metal oxide semiconductor
SiGe	Silicon Germanium
GaAs	Gallium Arsenide
HEMT	High Electron Mobility Transistors
FET	Field-effect transistor
BJT	Bipolar junction transistor
HBT	Heterojunction bipolar transistor
MESFET	Metal semiconductor field effect transistor
MOSFET	Metal–oxide–semiconductor field-effect transistor

JFET	Junction field-effect transistor
IGFET	Insulated-gate field-effect transistor
AlGaAs	Aluminium gallium arsenide
MAG	Maximum available power gain
MSG	Maximum stable power gain
U	Unilateral power gain
SoC	System-on-Chip
CE	Common emitter
PCB	Printed circuit board
R&D	Research and Development
V_{max}	Maximum voltage on the standing wave
V_{min}	Minimum voltage on the standing wave
V_i	Incident voltage wave amplitude
V_r	Reflected voltage wave amplitude

Symbols

Symbol	*Explanation*	*Unit*
Latin Characters		
C	Capacitance per unit length	F/m
F	Noise Factor	-
f_0	Resonant frequency	Hz
f_{max}	Maximum oscillation frequency	Hz
f_T	Transit frequency	Hz
G	Conductance per unit length	S/m
G_a	Available gain	dB
G_i	Insertion gain	dB
G_t	Transducer gain	dB
g_m	Transconductance	S
h_{fe}	Transistor's AC current gain	-
I_b	Base current	mA
I_c	Collector current	mA
I_{ce}	Collector-emitter current	mA
I_{ds}	Drain-source current	mA
K	Rollett stability factor	-
L	Inductance per unit length	H/m
NF	Noise Figure	dB
Q_L	Quality factor	-
R	Resistance per unit length	Ω/m
R_n	Noise Resistance	Ω
V_{ce}	Collector-emitter voltage	V
V_d	Drain voltage	V
V_{ds}	Drain-source voltage	V
V_g	Gate voltage	V
V_{gs}	Gate-source voltage	V
Y	Shunt impedance	$1/\Omega$
Z	Series impedance	Ω
Z_0	Characteristic impedance	Ω
Z_{in}	input impedance	Ω

Z_{oc}	Open-circuited transmission line impedance	Ω
Z_S	Source impedance	Ω
Z_L	Load impedance	Ω
Greek Characters		
α	Attenuation constant	N_p/m
β	Phase constant	rad/m
β	Transistor's DC current gain	-
γ	Propagation constant	-
Γ	Reflection coefficient	-
ϵ_0	Electric permittivity	$8.854 \cdot 10^{-12}$ F/m
ϵ_{ff}	Effective relative dielectric constant	-
ϵ	Dielectric constant	F/m
ϵ_r	Relative dielectric constant	-
λ	Wavelength	m
ν_p	Phase velocity	m/s
ω	Angular frequency	rad Hz

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1. Introduction

The wireless data transmission is becoming increasingly important. The demand for very broadband circuits is being driven by the newly introduced Ultra-Wide Band technology, which is capable of transmitting low-power signals with very high data rates over a wide spectrum of frequency bands. In every case, the basic requirement in the UWB transceiver is a wideband Low Noise Amplifier. This UWB LNA requires high gain, low noise figure and high linearity over the entire band with low power consumption.

Ultra-Wide Band (UWB) technology has been designed to bring convenience and mobility of high speed wireless communication to homes and offices. The short range UWB technology will also complement other wireless standards such as Wi-Fi and Wi-Max. It can transmit data within the radius of 10 meters from the host device. UWB technology is designed to provide a short range, very low power connection and much more bandwidth than cable. Since UWB communicates with short range pulses, it can be used for tracking various objects.

2. Theoretical Fundamentals

2.1. Ultra-Wide Band (UWB)

Ultra-Wide Band (UWB) of 3.1 to 10.6 GHz was released in 2008 by the Federal Network Agency in Bonn, Germany. The UWB technology is intended primarily for broadband connections up to 1 Gbps at close range (up to 10 m). UWB is best described as a kind of radios that use signals of bandwidth unusually wide to achieve the objectives of application. These radios can operate in a wide range of frequencies and with different signal characteristics.

The main point of this technology are low power levels offset by the high bandwidth, which offers sufficient performance for its economically attractive. The low power levels of UWB appears to be a major problem, but instead, can be compensated by the large available bandwidth, allowing the technology to operate at high transmission speeds.

Before UWB, spectrum is divided in frequency bands and only allowed a strict coincidence between authorized services. In contrast, UWB has been purposely designed to overlap a large part of other services. Regulators initially authorized UWB, think that a higher priority service tend to dominate UWB when it need spectrum, but UWB would be available additional frequencies where to move if this happened. The regulators were trying to increase the amount of spectrum that was available for a growing volume of communication needs. This logic has since proven to be somewhat less than perfect, but it was the prevailing opinion when the Federal Communications Commission (FCC) made her first performances in 2002. The FCC reserved the frequency band from 3.1 GHz to 10.6 GHz unlicensed for indoors wireless communication systems. Standards such as IEEE 802.15.3a (high data rate) and IEEE 802.15.4a (low data rate) are based on UWB technology.

The Ultra-Wide Band (UWB) transmission has recently received considerable attention in both, academic and industry, applications such as wireless communications. UWB has many benefits, including high speed data, low cost transceivers, low transmit power and low interference. Works with emission levels that correspond to common digital devices such as laptops, Palm Pilots, and pocket calculators. Moreover, the UWB system of the Department of Defense (DoD) are different from commercial systems, concerns about interference. Despite the efforts of R&D in recent years has shown that UWB is a promising solution for high-rate wireless communications, short and moderate range. Thorough research, testing and development are needed to produce UWB communication systems efficient and effectives. The centimeter accuracy in reach offers unique solutions for applications including logistics, security applications, medical applications, electromechanical control, search and rescue, family communication, supervision of children and military applications.

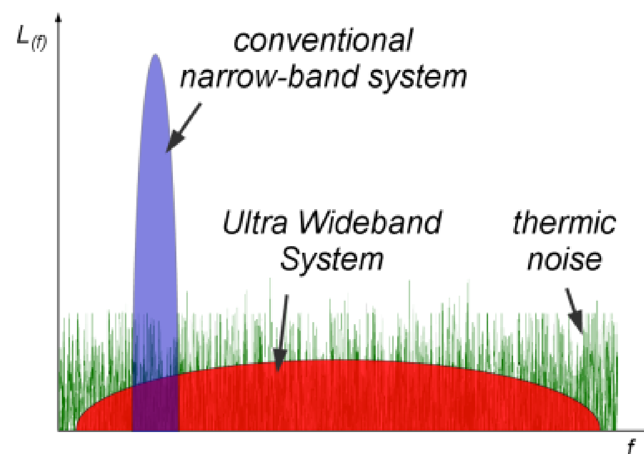

Figure 2.1.: Ultra-Wide Band versus Narrow Band [21]

More practical applications are grouped into four broad categories including High-Data-Rate communications (HDR), Low-Data-Rate communications (LDR), imaging in general and automotive radar. The applications are grouped this way because the regulatory procedures have been developed around these groups. This structure is also a reflection of the market, there is a market where one hand of these products are promoted and otherwise develop the standards.

High-Data-Rate communications (HDR) is the first group of applications. HDR applications are emerging for personal computers (PC), consumer electronics (CE) and mobile telephony sectors. These applications share a common need of a very high-speed radio data can be built at low cost and operating within a single space (usually less than 10 m). Data rates for HDR designs ranging from a 110 Mbps at levels above 1 Gbps. HDR applications are grouped in the frequency range 3.1 to 10.6 GHz This spectrum was part of the original assignment of the FCC for UWB and is the basis for the rest of the world uses as a starting point in their rulemaking procedures. To be a little more specific, HDR applications can be divided into file transfer, asynchronous communications, streaming video and streaming audio. File transfers can be an exchange point-to-point. Similarly, transfer images from a digital camera to a printer, upload a movie to a portable video player or download a game from a kiosk, all applications are considered point-to-point. [1]

The second class of applications is Low-Data-Rate communications (LDR from now). Low-power sensors are deployed within an building, in a factory, farm fields or elsewhere. Sensor networks are used for lighting and intelligent energy management within an building, industrial automation and storage applications. Typically, these applications involve the transfer of very small volumes of data between battery-powered transceivers. Some applications have requirements for monitoring the physical location of goods and use the unique characteristics of a UWB signal to establish a precise physical location of the transmitter. Sensor networks compensate commercial peak performance for extended range. [1]

The third category of applications called imaging. It is a category that includes the GPR (Ground-penetrating radar), images in-wall, images through-wall and security perimeter. GPR is used by utilities, construction companies and archaeologists in search of objects that are below the surface of the earth. Image in-wall is used by the police and the military to search for people, obstacles and hazards in adjacent rooms. Image through-wall is used in the building to search for hidden items such as pipes, wires and poles on a wall. The security perimeters using the properties of radar UWB to establish a “virtual fence”. The intruders crossing the fence are detected and a warning is appropriate. In these applications of image processing, GPR is referenced more often in regulatory processes and other publications. GPR module volume is expected to be much lower than

either HDR or LDR.[1]

The fourth and last of these applications is the automotive collision avoidance radar. In this application, UWB is used by the car as a radar to activate automatic braking when a collision is considered imminent. By forcing the car to stop involuntarily, the impact force is substantially reduced. The automaker expects that this new capability saves a significant number of lives. Like radar, automotive radar is developed by their image properties and is not used for communications. In addition, the automotive radar is the only application that currently uses UWB 24 GHz, not use the 3.1-10.6 GHz range what is used by HDR, LDR and GPR applications.[1]

2.2. Transmission Line Concepts [3]

A transmission line is intended to direct the transmission of energy from one place to another, this energy has the form of electromagnetic waves, and the transmission of electricity.

Transmission lines can, in some cases, be analyzed by using a generalized lumped-element model as shown in Fig. 2.2. Fundamentals and definitions that can initially be obtained from a circuit model of a transmission line carry over to waveguides, where the analysis is more complicated. Viewed as a two-port network, the transmission line receives power from the source and delivers power to the load. The length l of the transmission line is divided into many identical sections "deltax" (Δx). Each section deltax is modeled by a resistance R per unit length (R in Ω/m), an inductance L per unit length (L in H/m), a capacitance C per unit length (C in F/m), and a conductance G per unit length (G in S/m). These parameters are assumed to be constant along the transmission line.

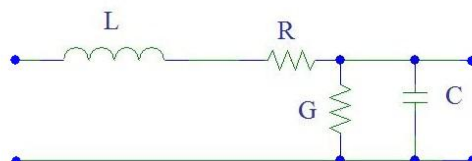

Figure 2.2.: Transmission line electrical model

After explaining this model, we can establish the relationship between the phase constant, frequency, phase velocity and wavelength. The relationship between the phase constant and the wavelength is very simple, since there are 2π radians in a wavelength.

$$\beta = \frac{2\pi}{\lambda} \tag{2.2.1}$$

And the constant phase is function of frequency:

$$\beta = \omega\sqrt{LC} = 2\pi f\sqrt{LC} \quad rd/m \tag{2.2.2}$$

Here some different ways of expressing the wavelength:

$$\lambda = \frac{2\pi}{\beta} = \frac{2\pi}{\omega\sqrt{LC}} = \frac{1}{f\sqrt{LC}} \tag{2.2.3}$$

The general form for the propagation constant from the series impedance and shunt admittance of the transmission line model:

$$Z = R + j\omega L \tag{2.2.4}$$

$$Y = G + j\omega C \tag{2.2.5}$$

$$\gamma = \sqrt{ZY} = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.2.6}$$

The general expression of the characteristic impedance is:

$$Z_0 = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.2.7}$$

In its general form, the characteristic impedance is a complex number, but this happens only if R and G are nonzero. In practice, we try to achieve transmission lines almost without losses, thus we have the following relations:

$$G \ll j\omega C$$
$$R \ll j\omega L$$

therefore, $Z_0 = \sqrt{\frac{L}{C}}\ \Omega$

Sometimes not all of the incident energy is absorbed by the load on a transmission line, this occurs when the transmission line is terminated with a load value of Z_L instead of a load equal to the characteristic impedance of the transmission line, Z_0. The energy not absorbed is reflected, so that creates a voltage standing pattern on the transmission line due to the phase addition and subtraction of the incident and reflected waves. There is a relationship between the maximum and minimum voltage is known as the Voltage Standing Wave Ratio (VSWR) and the successive peaks and troughs are separated by 180°.

$$VSWR = \frac{V_{max}}{V_{min}} = \frac{V_i + V_r}{V_i - V_r} \tag{2.2.8}$$

Additionally we define:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.2.9}$$

And if the equation for VSWR is solved for the reflection coefficient, it is found that:

$$Reflection\ Coefficient = \rho = |\Gamma| = \frac{VSWR - 1}{VSWR + 1} \tag{2.2.10}$$

Consequently,

$$VSWR = \frac{1 + \rho}{1 - \rho} \tag{2.2.11}$$

There are four important cases of the transmission line: the matched line, the short-circuited line, the open-circuited line, and the quarter-wave line.
In the matched transmission line shown in Fig. 2.3, we obtain that $\Gamma_0 = 0$, $Z_{IN}(d) = Z_L$, and VSWR=1. That is, there is no reflected wave, the input impedance is Z_0 at any location d, and the VSWR has its minimum value of one.
In the short-circuited transmission line ($Z_L = 0$) shown in Fig. 3, it follows that $\Gamma_0 = 1$, so there is total reflection from the load and consequently the VWSR has

its largest value of infinity. and the input impedance at a distance d is

$$Z_{in}(d) = jZ_0 tan(\beta d) \tag{2.2.12}$$

In the open-circuited transmission line ($Z_L = \infty$) shown in Fig. 3 it follows that $\Gamma_0 = 1, VSWR = \infty$, and the input impedance at a distance d, called $Z_{oc}(d)$, is given by

$$Z_{oc}(d) = -jZ_0 cot\beta d \tag{2.2.13}$$

Again, there is total reflection from the load since $|\Gamma_0 = 1|$, and consequently the VSWR has its largest value of infinity.

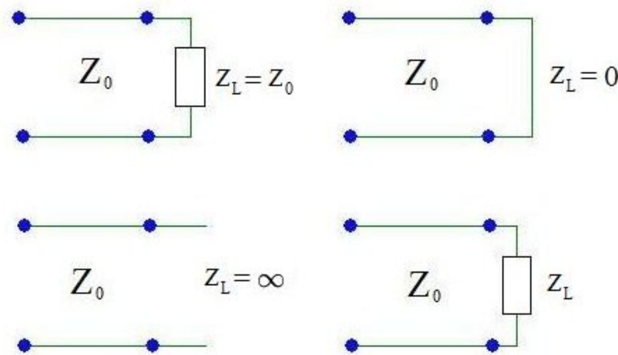

Figure 2.3.: Cases of transmission lines

The last important transmission line is the quarter-wave transmission line shown in Fig. 3. Its with $d = \lambda/4$, gives

$$Z_{IN}(\lambda/4) = \frac{Z_0^2}{Z_L} \tag{2.2.14}$$

Equation 2.2.14 shows that a quarter-wave line with real characteristic impedance of value $Z_0 = \sqrt{Z_{IN}(\lambda/4)Z_L}$ can be used in order to transform a real impedance Z_L to another real impedance given by $Z_{IN}(\lambda/4)$

Finally on the transmission lines will say that there are three types: the two-wire transmission line, coaxial transmission line and microstrip transmission line, as shown in Fig 4. The two-wire transmission line might therefore be applied to new microwave circuits and antennas. The coaxial cable is a flexible transmission line and typically is used to connect two electronic instruments together. The microstrip transmission line is more appropriate for the construction of microwave amplifiers.

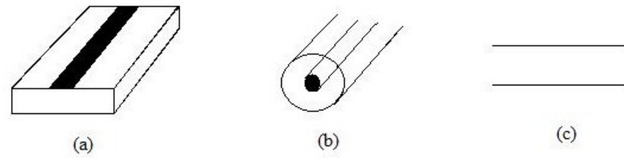

Figure 2.4.: Types of transmission lines

Microstrip lines

Microstrip lines have great advantages in the construction of microwave transistor amplifiers, because they are easily fabricated using printed-circuit techniques. In addition, network interconnections and the placement of lumped and transistor devices are easy to make on its metal surface. A microstrip line is, by definition, a transmission line consisting of a strip conductor and a ground plane separated by a dielectric medium. The dielectric material serves as a substrate and sandwiched between the conductor strip and ground plane. The relative dielectric constant of the substrate, ϵ_r, and ϵ are related by $\epsilon = \epsilon_r \epsilon_0$, where $\epsilon_0 = 8.854 \times 10^{-12} F/m$. The effective relative dielectric constant of the microstrip is related to the relative dielectric constant of the dielectric substrate and also takes into account the effect of the external electromagnetic fields.

The characteristic impedance and the wavelength of the microstrip line can be expressed as:

$$Z_0 = \frac{1}{v_p C} \tag{2.2.15}$$

$$\lambda = \frac{v_p}{f} = \frac{c}{f\sqrt{\epsilon_{ff}}} = \frac{\lambda_0}{\sqrt{\epsilon_{ff}}} \tag{2.2.16}$$

Where $Z_0 = \sqrt{L/C}$, $v_p = 1/\sqrt{LC}$ and λ_0 is the free-space wavelength.

There are different methods for determining ϵ_{ff} and C and, of course, closed-form expressions are of great importance in microstrip-line design. At higher microwave frequencies the longitudinal components of the electromagnetic fields are significant and the quasi-TEM assumption is no longer valid.

2.3. Matching Networks

A network is matched when the input impedance at each port is equal to Z_0 when all other ports end in matching charges. Because of this, the reflection coefficient at each port is zero, in other words, when a signal incident does not reflect anything of that signal (but only that port). We can find out if a device is matched, watching its scattering matrix, if all diagonal elements are 0, then the device is matched.
Therefore, the main purpose of a matching network is to achieve $\Gamma_{in} = 0$. If you look at the the reflection coefficient expression:

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{2.3.1}$$

if Γ is zero, then $Z = Z_0$.

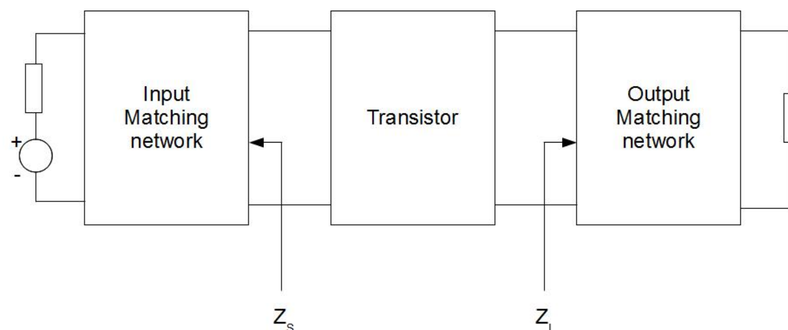

Figure 2.5.: Block Diagram of a microwave amplifier

The need for matching networks in the amplifier is designed to provide maximum power to a load, this is achieved by properly matching the input and output ports. Figure 5 illustrates a transistor with impedances Z_S and Z_L. To provide maximum power to the load of 50 ohms should design the matching networks properly. The input matching network is designed to transform the generator impedance to the source impedance (Z_S), and the output matching network transforms the 50 ohm termination to the load impedance (Z_L).

Although many different types of matching networks can be designed, there are eight possible two-component matching networks, also known as Ell sections, they are not only simple to design but quite practical. The matching networks are lossless in order not to dissipate any of the signal power. Regarding the Ell matching networks is that only those with an inductor and a capacitor can be used to provide a match between a resistive load and an input resistance.

In a resonant circuit, the ratio of its resonant frequency f_o to its bandwidth is known as the loaded Q of the circuit. This parameter describes the influence by the resonance effect in the design of the matching network:

$$Q_L = f_0/BW \tag{2.3.2}$$

Knowing the matching network quality factor we can obtain its bandwidth.
We can estimate the network quality factor by the nodal quality factor. In any L-type matching network, at each circuit node can find:

$$Q_n = |X_S|/R_S \tag{2.3.3}$$

$$Q_n = |B_p|/G_p \tag{2.3.4}$$

$$Q_L = Q_n/2 \tag{2.3.5}$$

In some cases, the bandwidth of the matching network is an important design parameter. A matching network can be adjusted or fine-tuned as necessary,

for example, if the load impedance varies in a certain range. In general, the matching networks are designed with reactive components that no loss is added to the network.

Lumped elements can be used in matching networks for frequencies up to about 1 GHz.The capacitors and inductors must be small enough in relation to the wavelength. The Smith chart can be used to design such networks. This design involve to move along a circle of constant resistance or constant conductance from an impedance or admittance to another. Add a reactance in series produces a motion along a circle of constant resistance and add a shunt susceptance produces a motion along a constant conductance circle on the Smith chart. Moving along the constant circles we must reach the center of the Smith chart (matched condition).

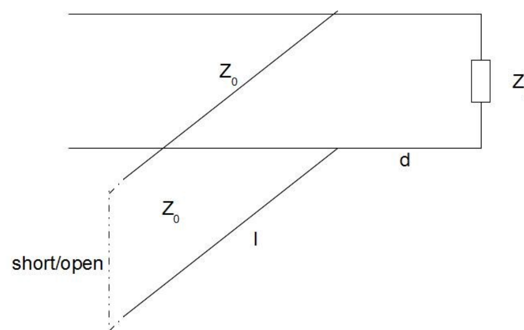

Figure 2.6.: Single Stub Matching

In the design of matching networks can also make use of the properties of transmission lines. We can use the transmission lines as single stub tuners or double stub tuner. Using single stub tuners, with the proper length of the terminated transmission line shorted or open-circuit, can get any value of the reactance or susceptance. The single stub tuner is very flexible matching any load impedance of a transmission line. However, if the load impedance varies an adjustable tuner is required, the single stub tuner requires that the position of the stub tuner also varies. A double stub tuner allows a adjustable matching network using stub lengths adjustable to a fixed position. Ideal lumped element and single stub matching networks provide perfect matching ($\Gamma = 0$) at only one frequency. These configurations are illustrated in Figures 2.6 and 2.7.

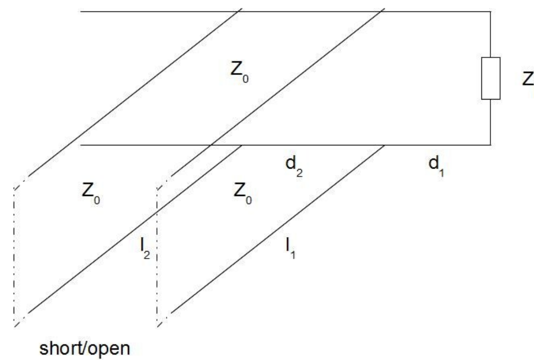

Figure 2.7.: Double Stub Matching

2.4. Noise Concepts

The word noise often means any unwanted sound. In communications, it is called noise all unwanted signal that is mixed with the useful signal to be transmitted. Is the result of various types of disturbances which tends to mask information when present in the frequency band of the signal spectrum, ie, within its bandwidth. The noise is due to multiple causes: the electronic components (amplifiers), the thermal noise of the resistors, to interference from external signals, etc. It is impossible to totally eliminate the noise, since electronic components are not perfect. However, it is possible to limit its value so that the quality of communication is acceptable.

Among the various types of noise is the thermal noise (or Johnson-Nyquist noise). This kind is present in all circuits and devices and is produced by random variations in the current or voltage, in turn, caused by the random motion of charge carriers.

The shot noise is another type of noise is a uncorrelated electromagnetic noise produced by the random arrival of component carriers (electrons and holes) in the output element of a device, such as a diode, a transistor (field effect or bipolar) or a vacuum tube. Shot noise is juxtaposed to any noise present, and it is additive with respect to thermal noise and himself.

Modern receivers often must process very weak signals and the components of the system tends to weaken even more these signals by adding noise. There are parameters, that allow us to know the ability of a device to process these weak signals, like the sensitivity (S), the bit error ratio (BER) and the noise figure (NF). Another important parameter is the signal to noise ratio (SNR).

The sensitivity of an electronic device, for example a communications receiver, is the low magnitude in the input signal required to produce a given magnitude in the output signal. In summary, sensitivity is the ability to detect waves or signals more accurately. If a device does not have greater sensitivity, it will have more problems in detecting waves or signals. Bit Error Ratio (BER) is the number of bits incorrectly received of the total of bits sent during a specified interval of time. The signal to noise ratio is defined as the margin between the power of the transmitted signal and the noise power.

$$S/N = \frac{Signal \quad power}{Noise \quad power} \tag{2.4.1}$$

The magnitude of the noise generated by an electronic device can be expressed by so-called noise factor (F), which is the result of dividing the signal to noise ratio at the input by the signal to noise ratio at the output, expressed as:

$$F = \frac{Si/Ni}{So/No} = \frac{SNRi}{SNRo} \tag{2.4.2}$$

The noise factor given in dB is the noise figure, defined as:

$$NF = 10 \cdot log(F) = 10 \cdot log(\frac{SNRi}{SNRo}) \tag{2.4.3}$$

3. Analysis of Low Noise Amplifier

This chapter will make an analysis of the low noise amplifier. First reviewing the state of the art and introducing some previous works. It will also discuss the different figures of merit required to analyze a low noise amplifier. Finally, what requirements must have the low noise amplifier.

3.1. State of the Art

The figure 3.1 shows a wireless communication system. The transmitter consists of a Profibus interface, followed by digital signal processing (based on an Field Programmable Gate Array , FPGA), an analog-digital converter and a bandpass filter as the last block. The first block in the receiver is the Low Noise Amplifier (LNA), followed by digital-analog converter, a digital signal processing (also based on a FPGA) and the Profibus interface.

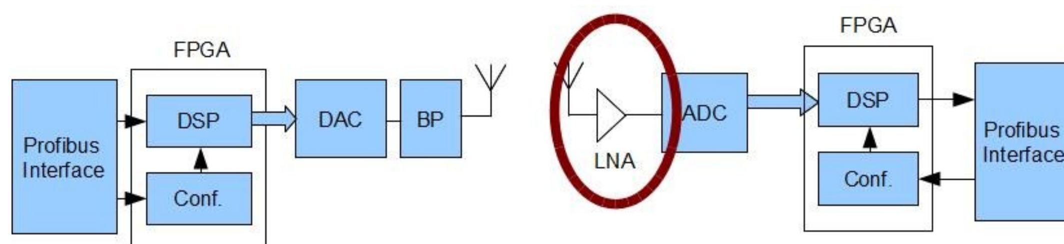

Figure 3.1.: Diagram Block of Wireless Transmission of UWB

The development of wireless communications is constantly increasing, desired transceivers must have sufficient requirements to support multiple bands and multiple standards, WLAN, Wi-Fi, Bluetooth, WiMAX, UWB. The Low Noise

Amplifier (LNA) as a stand-alone product is required to provide a very low current consumption, low signal distortion and high signal voltage gain transfer, this is one of the main obstacles for various communication standards. The challenges include a good input matching, flat frequency response of power gain, low noise figure (NF), and high enough linearity within the desired bands. Numerous methods have been implemented to develop this stage. A direct method implements separate multiple narrow-band amplifiers, each designed for a different frequency band. Another different approach are the switched or reconfigurable LNA by capacitors, inductors, transistors or RF micro electro mechanical systems (MEMS). These methods however suffers from high power dissipation, a large chip area, degrades the noise figure, in the case of reconfigurable LNAs, only one band can be selected at time and therefore a significant increase in costs.

The wide-band LNAs that cover the bands of interest are alternative while strong unwanted blockers are amplified together with the desired frequency bands and significantly degrade the receiver's sensitivity. To circumvent the above problems, concurrent LNAs were developed. The concurrent LNAs enable simultaneous multi-band operations in the same circuitry, and therefore present lower power consumption and reduced chip area. It should also be noted that multiple bands handling capability is the main drawback for this concept, which makes the linearity significant for this situation. Among wideband LNAs [10], the distributed amplifiers absorb all circuit parasitic capacitances by incorporating on-chip transmission lines and provide wide bandwidth at the expense of delay. These LNAs demand high-quality transmission lines, making them less attractive to low-cost on-chip solutions due to the large chip area. The resistive feedback amplifiers can achieve wideband input matching, reducing the NF by the local feedback with a feedback resistance and high voltage gain.

A previously reported work is shown in Table 1. We show results of three different technologies, CMOS, SiGe and GaAs pHEMT. The best noise figure was achieved with GaAs pHEMT technology in a range of 0.5-1.7 dB, but the bandwidth is small, from 2.4 to 5.8 GHz, this depends on the application wanted, but it is desirable a higher bandwidth. It was achieved the best bandwidth for SiGe technology. Finally, in terms of gain, the technology choice in this case does not depend on this parameter, since none has better values than others. We will have to keep in mind also the power consumption, the chip area and the costs.

Bandwidth	Gain	NF	Current	Technology
[GHz]	[dB]	[dB]	[mA]	
0.6-22	7.3	4.3-6.1	-	0.18 μm CMOS
0.05-23.5	17	6	27.8	SiGe
2.4-5.2	24.6-15.8	2.41-3.4	9	SiGe HBT
2.4-5.8	12.2-15.3	0.53-1.43	10	GaAs pHEMT
1.3-12.3	9.1	4.4-4.6	2.5	0.18 μm CMOS
2.7-9.1	10	3.8-6.9	-	0.18 μm CMOS
3.1-10.6	16	3.8-4.0	5.3	0.18 μm CMOS
8-18	18.8	5	24	0.35 μm SiGe
2.4-5.2	11.79-10.03	3.89-3.73	10	CMOS
2.4-5.8	16.8-17.7	1.5-1.7	18	GaAs E-pHEMT
2-12	11	8-10	40	0.25 μm SiGe
2.4-5.2	14.2-14.6	4.4-3.7	6	CMOS

Table 3.1.: Previous reported work of LNAs [8] [9]

3.2. Figure of Merit

Five key figures of merit of the Low Noise Amplifier are the gain and bandwidth, noise figure, linearity, impedance matching and power consumption. In the LNA design we have to make a first transistor choice, first we need to know which are the figures of merit of our transistor. The two most important features of a transistor are its ability to amplify (important for analog and RF electronics) and its ability to act as a switch (important for digital electronics), in our case we consider the first ability. For a transistor we must consider the Gain, the frequency limits, the output power and the minimum noise figure as figures of merit. In this section we define the figures of merit that we use to choose our best system.

In first instance, the $V_{ce}-I_c$ [4] curves are useful in choosing the optimal operating point of a transistor used as an amplifier. To make this curves, V_{be} is set to a value and V_{ce} is swept while measuring I_c. This is done for several fixed values of V_{be} and thus the chart is presented for differente values of V_{be}. This point should be chosen in the active region, where the change in collector current is proportional to the change in base current. This linear region is ideal for the use

of amplification, allowing the output waveform to be expanded reliable copy of the input waveform. This active region of the transistor is shown in Figure 3.2. Operating in this area has the characteristics that change in the collector current I_c is more sensitive to changes in base current I_b in this region and the collector current I_c does not change much with the collector-emitter voltage V_{ce} for any base given the current I_b.

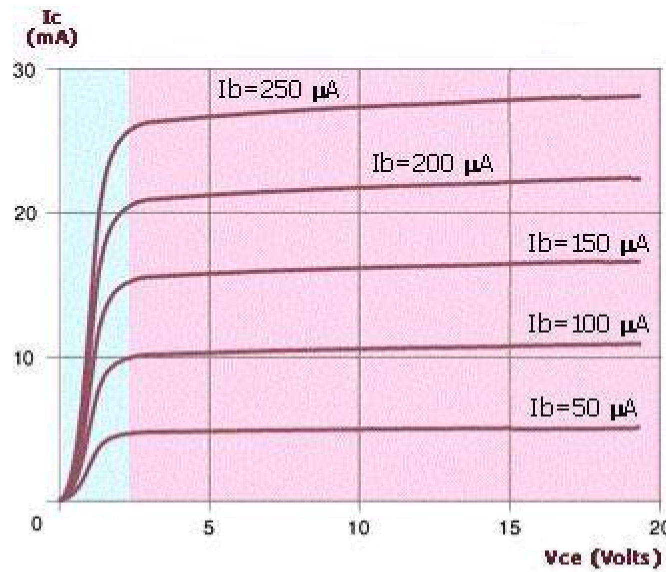

Figure 3.2.: The $V_{ce} - I_c$ Curves of an NPN transistor for different values of I_b (Common-emitter Collector Characteristics) [18]

Another important figure of merit in the choice of our transistor is the transit frequency f_T. The transit frequency also called the unity gain frequency is obtained by setting the small signal current gain equals to 0 dB. There are two current gains, h_{fe} and h_{FE}, the first corresponds to the dynamic characteristics of the device at high frequencies. The h_{FE} refers to the static characteristics. We are interested in h_{fe}.

$$h_{fe} = \frac{i_c}{i_b} = \frac{g_m}{i_B} v = \frac{\beta}{1 + jw(C_{j,BE} + C_{d,BE}) r_\pi} \Rightarrow h_{fe} = 1 \Rightarrow f_T = \frac{1}{2\pi\tau} \quad (3.2.1)$$

$$\tau = \frac{C_{j,BE} n V_T}{I_E} + \frac{w_B'^2}{2D_{1,B}} = \tau_E + \tau_B \quad (3.2.2)$$

While the unity gain frequency is an important figure of merit of a bipolar transistor, another even more important figure of merit is the maximum oscillation frequency f_{max} [19]. This figure of merit predicts the unity power gain frequency and as a result indicates the maximum frequency at which useful power gain can be expected from a device.

$$f_{max} = \frac{f_T}{2\pi R_B C_{j,BC}} \quad (3.2.3)$$

We find these frequencies through the curves MAG (Maximum Available Power Gain), MSG (Maximum Stable Power Gain) and U (Unilateral power gain) as seen in the figure 3.3. Plus, we can obtain the value of these curves through the next formulas.

$$MAG = \left(\frac{s_{21}}{s_{12}}\right)\left(K - \sqrt{K^2 - 1}\right) \quad (3.2.4)$$

$$MSG = \left|\frac{s_{21}}{s_{12}}\right| \quad (3.2.5)$$

$$U = \frac{1/2\left|\frac{s_{21}}{s_{12}} - 1\right|^2}{K\left|\frac{s_{21}}{s_{12}} - Re\left\{\frac{s_{21}}{s_{12}}\right\}\right|} \quad (3.2.6)$$

The maximum available power gain (MAG) assumes the value 0 dB at the transit frequency f_T of the transistor. The unilateral power gain (U) is higher than one even above the transit frequency since the reverse transmission is eliminated. The frequency at which U assumes the value 0 dB is called the maximum oscillation frequency f_{max} .

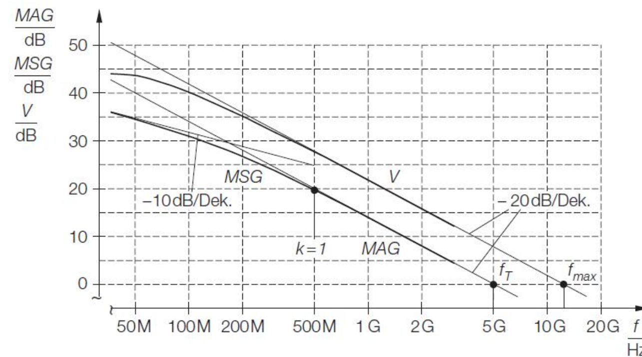

Figure 3.3.: Maximum power gains of a transistor [5]

The noise figure and gain are very important figures of merit in the choice of both the transistor and the schematic to be implemented. In Section 2.4 we defined already these two figures. Our goal is to find the lowest noise figure in contrast to a high gain. We also need a bandwidth from 6 to 8.5 GHz, the frequency band for UWB in Europe.

3.3. Requirement Engineering and Analysis

The Low Noise Amplifier is the most sensitive component in a typical RF receiver. Its main role is to improve the level of the incident signal at its input, without introducing significant noise and distortion. The LNA determines the noise and linearity of the system in general, as it is the first element of signal processing after the antenna. As we want build a Low Noise Amplifier for Ultra-Wide Band (UWB), some of the most important requirements for UWB applications are: good input impedance match, low power consumption, low noise performance, sufficient gain with good S/N for the following stages, and small size.This is what we want to achieve with our LNA.

To understand the importance of the gain and noise figure in the LNA we must explain the total noise figure of a cascade of several noise-inducing components. The total noise factor is defined as:

$$F_{cascade} = F_1 + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 \cdot G_2} + ... \tag{3.3.1}$$

where G_n and F_n correspond respectively to the gain and noise figure of the nth stage of the cascade. As the LNA is the first component in this cascade, as we can see in figure 3.1, its noise figure adds directly to the overall noise. Consequently, in order to reduce the total noise of the receiver, the LNA should present the lowest possible noise.

The input power of wireless standards extends over a wide range, in our case, UWB is from 3.1 to 10.6 GHz. The LNA should be able to receive and treat this entire range. The linearity comes into play due to saturation of the transistors, since the gain is saturated when a high input power. The LNA should be linear up to powers beyond the highest power likely to enter it. For maximum power handling capability of the transmission line and minimal cable losses the ports should be matched to impedances of 50 Ω. The impedance matching is important because the LNA is placed immediately after the antenna and is followed by a RF filter, thus avoiding signal reflections or changes in the characteristics of the filter that is sensitive to the terminating impedances.

A LNA design presents a considerable challenge because of its simultaneous requirements for gain and bandwidth, noise figure, linearity, impedance matching and power consumption. Trade offs have to be made depending on the standard for which the LNA is destined and reach an agreement between the different parameters.

4. Design and Simulation

The first step in the design is the selection of the transistor, this is the most important step in the design. We have to assure the right behavior of the transistor. The next step is the selection of the schematic for the Low Noise Amplifier, here we take into account different ways to build it, schematics with lumped elements of with transmission lines.

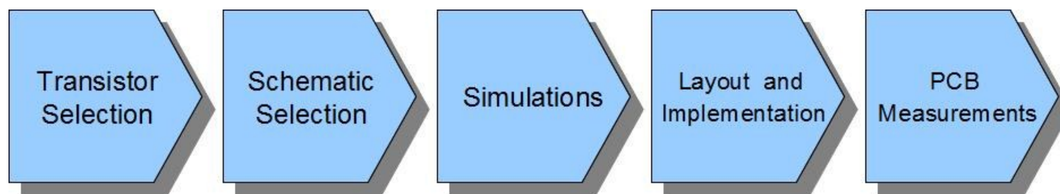

Figure 4.1.: Steps in the design of a Low Noise Amplifier

After, the simulations of those schematics, S parameters and noise figure simulations. Once we select the transistor and its schematic, we create the layout and it is simulated again. When the simulation are correct, the Printed Circuit Board (PCB) is processed. Finally, the PCB is measured.

4.1. Transistor

First of all, the transistor was chosen for the low noise amplifier. The first thing was looking for information about the State of the Art of transistors. In the next section, "Technology choice", a brief summary is presented about the different kinds of transistors and the semiconductor material used. Also, it has been explained what transistor was chosen finally and the reasons. In the next section, "Simulations", it is showed the different results obtained.

The transistor should exhibit high gain, have a low noise figure and low possible current consumption, while preserving relatively easy matching at frequency of operation. To meet most of these conditions, the parameter trade-offs must to be carefully understood. And of course, the transistor should cover the bandwidth required for application, in this case, a UWB LNA, from 6.5 to 8 GHz.

4.1.1. Technology choice

Transistors are categorized by different ways, here they have been categorized by their structure and the semiconductor material used. Two basic transistor structures are Bipolar transistors and FETs (Field-Effect Transistor).

In the first case, the output current is controlled by the voltage across a pn junction. The carrier injection is varied by changing the voltage across the junction. Here we have BJTs (Bipolar Junction Transistor) and HBTs (Heterojunction Bipolar Transistor). In FETs the output current is controlled by a perpendicular field. The conductivity of the channel is varied by changing the potential of a control electrode (gate). We mentioned here three different types, MESFETs (Metal Semiconductor FETs), HEMTs (High Electron Mobility Transistor) and MOSFETs (Metal-Oxide-Semiconductor FET).

Field-Effect Transistors (FETs)

The four terminals of the FET are named source, gate, drain, and body (substrate).

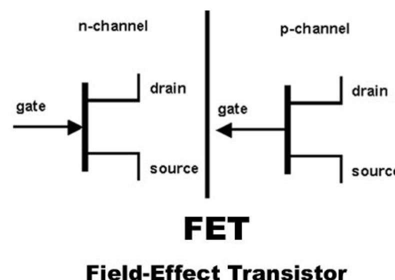

Figure 4.2.: FET, Field-Effect Transistor [30]

In a FET [19], the drain-to-source current flows via a conducting channel that connects the source region to the drain region. The conductivity is varied by the electric field that is produced when a voltage is applied between the gate and source terminals, hence the current flowing between the drain and source is controlled by the voltage applied between the gate and source. As the gate–source voltage (V_{gs}) is increased, the drain–source current, (I_{ds}), increases exponentially for V_{gs} below threshold. FETs are further divided into depletion-mode and enhancement-mode types. For enhancement mode, the channel is off at zero bias, and a gate potential can enhance the conduction. For depletion mode, the channel is on at zero bias, and a gate potential can deplete the channel, reducing conduction.

FETs are divided into two families: junction FET (JFET) and insulated gate FET (IGFET). The IGFET is more commonly known as a metal–oxide–semiconductor FET (MOSFET), reflecting its original construction from layers of metal (the gate), oxide (the insulation), and semiconductor. Most IGFETs are enhancement-mode types. The JFET gate forms a PN diode with the channel which lies between the source and drain. Nearly all JFETs are depletion-mode. They both have a high input impedance, and they both conduct current under the control of an input voltage.

Metal–semiconductor FETs (MESFETs) and the HEMTs (high electron mobility transistors, or HFETs) are especially suitable for use at very high frequencies (several GHz).

Bipolar Transistors

Bipolar junction transistor (BJT) is fabricated basically on a single germanium, silicon or gallium arsenide monocrystal. On the glass substrate, are contaminated three zones, two of which are of the same type NPN or PNP, leaving two junctions formed NP. The area elements N donor of electrons (negative charges) and the P of acceptors or "holes" (positive charges).The BJT has three terminals, an emitter, a base, and a collector. It is useful in amplifiers because the currents at the emitter and collector are controllable by a relatively small base current.

Collector current is approximately β (common-emitter current gain) times the base current.

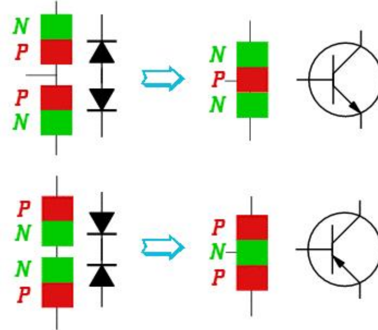

Figure 4.3.: BJT, Bipolar-Junction Transistor [27], (a) NPN transistor (b) PNP transistor

There is now a strong competition of GaAs (Gallium arsenide), SiGe (Silicon Germanium) and even Si bipolar and Si CMOS products for the different wireless communication applications. The main advantage of the SiGe technology over pure Si technologies is the higher performance, while the main advantage over the GaAs technologies is that it enables a high level integration.

CMOS [12] devices offer the advantages of high f_T and f_{max} as well as superior linearity and lower voltage operation, due to lower threshold voltages (CMOS VT vs bipolar VBE). BJT devices offer the advantages of excellent noise performance and an improved transconductance. The density differences for different circuit applications are also of practical interest. For RF low-noise amplifiers, SiGe HBT circuits occupy one-quarter to one- third the area of CMOS circuits of equivalent functionality. While for dense caches in a microprocessor, CMOS circuits occupy one quarter to one third of the area of BJT circuits for the same functionality.

SiGe and GaAs semiconductor materials have been chosen in regard to the characteristics listed above. In the next section the simulations of a SiGe BJT and GaAs HEMT are showed.

4.1.2. Simulations

In this section is showed simulations of the BFP740 transistor of Infineon and the FPD200P70 transistor of RFMD. The final choice is explained in the next section. The figures of merit we use here to compare both transistors are explain in section 3.2.

First of all we do a DC simulation to know the $V_{ce} - I_c$ curves of each transistor. Figure 4.6 shows the simulation of BFP740 simulation. The operating point used in the datasheet is a common-emitter voltage, $V_{ce} = 3V$, and a collector current, $I_c = 25mA$ (except for the noise figure where the collector current is $8mA$), this is the one used for the simulations.

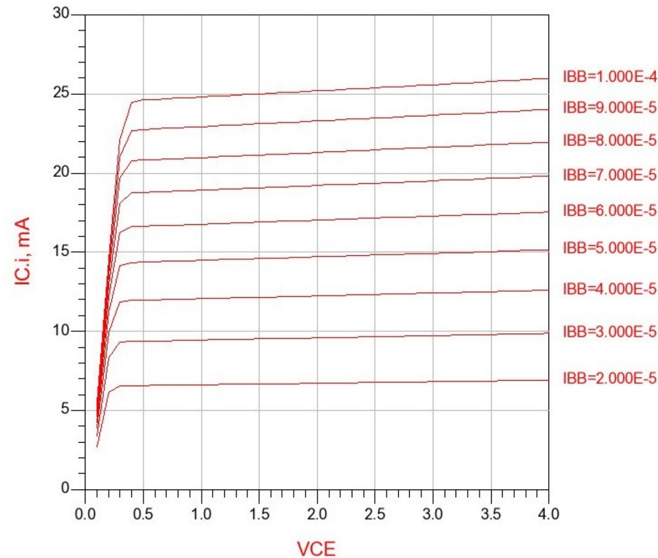

Figure 4.4.: Vce-Ic curves of transistor BFP740

The next simulation concerns the transit and maximum frequency, f_T and f_{max}. In this case, the f_T is 22.8 Ghz for the BFP740 transistor and the f_{max} is 31.5 Ghz. On the other hand, the datasheet of the BFP740 transistor provides a MAG data of 17 dB at 6 GHz, as we see in the figure 4.7 is 16.8 dB, therefore, the transistor is operating correctly in gain.

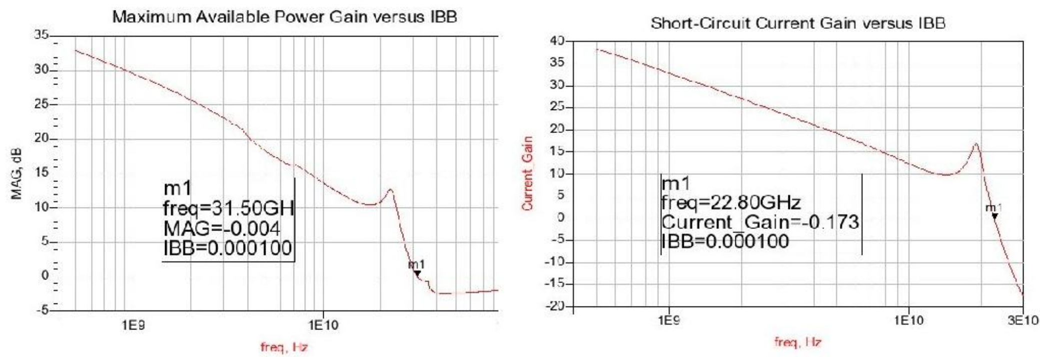

Figure 4.5.: (a) Maximum frequency of BFP740 transistor, (b) Transit frequency of BFP740 transistor

The last simulation is about the noise figure of each transistor. As we can see in the figure 4.8, for the BFP740 transistor, the noise figure grows from 0.4 to 1 dB. For noise figure, the datasheet gives values of 0.5 dB at 1.8 GHz and 0.85 dB at 6 Ghz, in the simulations, we obtain values of 0.405 dB and 0.63 dB respectively, we get better noise figure in theory.

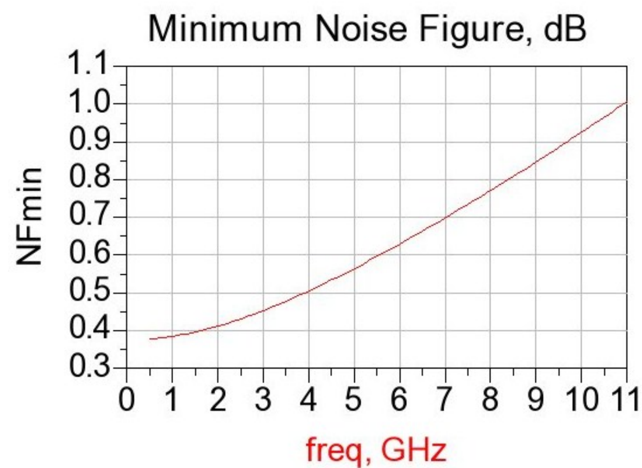

Figure 4.6.: Minimum noise figure of BFP740 transistor

For the FPD200P70 transistor we compare the simulations obtained with the results provides for the datasheet.

Simulations for $V_{DS} - I_{DS}$ curves are not correct, as seen in the figure 4.8. The results for I_{DS} should reach up to 100 mA and we get a maximum of 60 mA. The problem must be that the simulation was performed on V_{GS} instead of V_G as in the chart on the datasheet (Figure b) and that is why the difference in values. The transistor FPD200P70 (Figure 4.6(b)) is usually biased at $V_{DS} = 3$ V and $I_{DS} = 30$ mA and we used this one for the simulations.

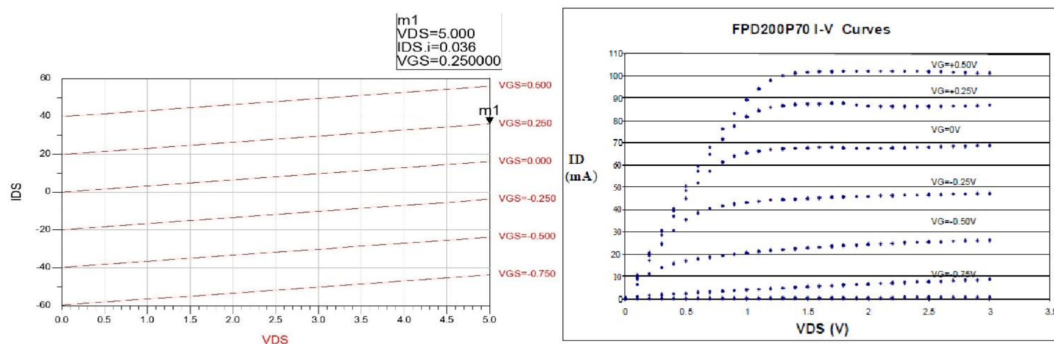

Figure 4.7.: Vds-Ids Curves of transistor FPD200P70

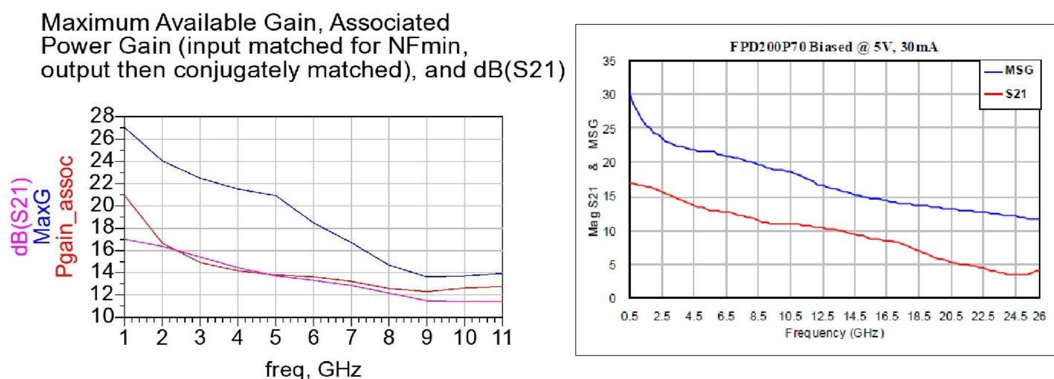

Figure 4.8.: MAG, S21 (dB) and Power Gain of transistor FPD200P70

In the above figure we can see the maximum available gain (MAG), S_{21} parameter and the Power Gain of FPD200P70 transistor. The datasheet of the FPD200P70 provides a MAG of 17 dB at 5,5 GHz and we obtain almost 20 dB at this frequency. In the figure is easy to appreciate the similarity between ours simulations and the chart provides in the datasheet. In the datasheet is only provided the MAG and the S_{21} parameter.

The noise figure grows from 0.4 to 1.4 dB from 1 GHz to 11 GHz. The simulations was done for $V_D = 3V$, so we have to compare with the red line in the chart provide for the datasheet. The datasheet gives values of 0.15 dB to 1.28 dB from 0.8 to 11 GHz, therefore, we obtain again similar results.

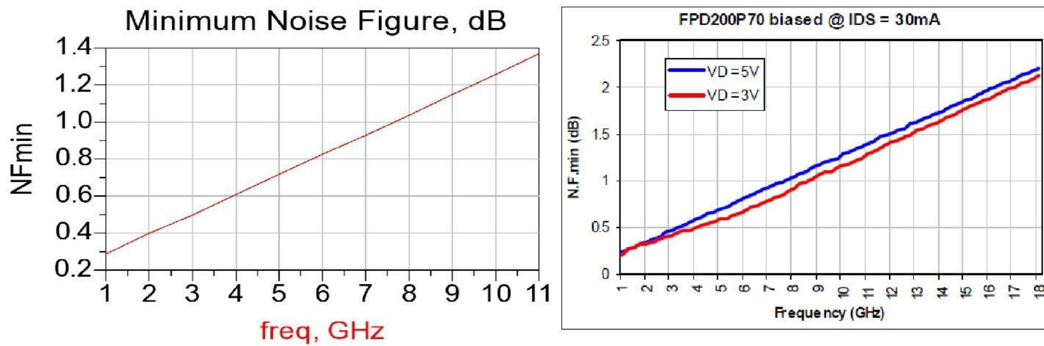

Figure 4.9.: Noise Figure of transistor FPD200P70

4.1.3. Final choice

Our final choice is the transistor FPD200P70 of RFMD.

The main reason of the choice is the final schematic, we will use a schematic with transmission lines as we explain in the section 4.2, and the transistor used for this schematic is the FPD200P70.

Even so, comparing the transistors discussed above, the difference between them is the type of technology used to manufacture them, the BFP740 is a NPN SiGe RF transistor and the FPD200P70 is a GaAs pHEMT transistor, the differences, advantages and disadvantages of these technologies are explained in the section 4.1.1.

About the technical characteristics of each transistor, the FPD200P70 obtained higher values of gain than the BFP740 and the transit frequency of the FPD200P70 transistor is much higher than the BFP740 transistor.

4.2. Schematic

The first thought was to use a schematic with discrete elements, but weighing the pros and cons, we decided to use a schematic with transmission lines. Anyway we present in the next section the schematics chosen and theirs simulations.

On one hand, classical wideband amplifier topologies, e.g., feedback and distributed amplifiers have difficulty to meet all the requirements of a near-to-minimum noise figure, low-power consumption, small area, and low cost. On the other hand, an LNA implemented with multisection matching networks provides more degrees-of-freedom to achieve both a low noise figure and flat power gain without increasing the power consumption. However, as the multisection input and output matching networks have more circuit components, the LNA noise figure and power gain can be more sensitive to the statistical variations of the passive components, either they are lumped inductors and capacitors or distributed passives, e.g., using microstrip transmission lines.

The schematics with transmission lines present improved bandwidth over schematics with discrete components. The reason is that power losses and parasitic capacitances are avoided to be able to place matching networks closer to the transistors. Perhaps the main advantage is that this technology achieves a lower noise figure. Another great advantage is the combination of features multicircuitales without wired networking, allowing the production of compact microstrip lines. This technology also reduces the size of the circuit. We could summarize the benefits and improvements in noise figure with the following specifications, typical of this type of hybrid circuits:

- Higher linearity and low noise.
- Internal feedback, which facilitates impedance matching over a wider bandwidth.
- Unconditional stability over a wider range of frequencies.

4.2.1. Schematics with lumped elements

First we must introduce some techniques used in these schematics like the emitter follower stage or the inductive emitter degeneration.

The emitter follower is a circuit with deep negative feedback, i.e., all of its output $v_{out} = v_e$ is fed back to become part of its input v_{be}.

Due to this deep negative feedback, the voltage gain of the emitter follower is smaller than unity. However, the circuit is drastically improved in terms of its input and output resistances. In fact the emitter follower acts as an impedance transformer with a ratio of $\beta + 1$. Although the emitter follower does not amplify voltage, due to its high input resistance drawing little current from the source, and its low output resistance capable of driving heavy load, it is widely used as both the input and output stages for a multistage voltage amplification circuit.

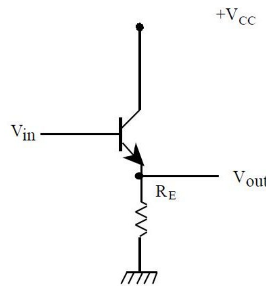

Figure 4.10.: Emitter follower stage

In the emitter follower stage the output (emitter) voltage is simply related to the input (base) voltage by a diode drop of about 0.6 eV. An ac signal of 1 V amplitude on the input will therefore give an AC signal of 1 volt on the output, i.e. the output just “follows” the input. As we will see later, the advantage of this circuit is as a buffer due to a relatively high input and low output impedance.

The process of intentionally inserting additional inductance between device emitter connections and RF ground is a commonly employed method used for influencing device input/output match, noise match, stability and linearity. Inductive degeneration does not seriously impact noise figure performance as resistive degeneration does. Inductive emitter degeneration is used to improve amplifier low-frequency stability and impedance matching.

3 Stages Schematic [23]

The first schematic has 3 stages. The first stage is the input transistor in common emitter configuration, this is the noise determining part of the circuit.

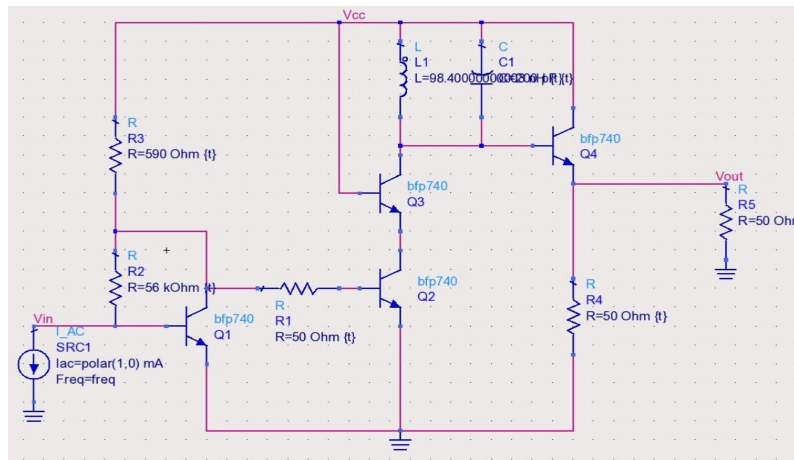

Figure 4.11.: 3 Stages Schematic

In the second stage, two transistors in a cascode configuration to reduce the Miller effect (C_{BC}) due to the base collector capacitance and with a parallel resonance circuit as load, tuned to the operational frequency. And the third stage with an output emitter follower, used as the third stage provides a low output impedance.

Schematic with Cascade Configuration [24]

In this schematic a cascade of two inductively loaded CE (Common Emitter) stages which were both optimized for low noise was chosen. Each of the CE stages has its own base current bias which can be adjust through pads.

The first stage also uses inductive emitter degeneration which improves matching and linearity. In a radio receiver, an LNA is commonly followed by a mixer which is a non-linear device whose input impedance will change when modulated with the local oscillator signal. In order to match the input impedance of the LNA to 50 Ω, the first stage uses inductive emitter degeneration which increases the

input resistance by $2\pi f L_3$. Due to the feedback at high frequencies the linearity is improved as well.

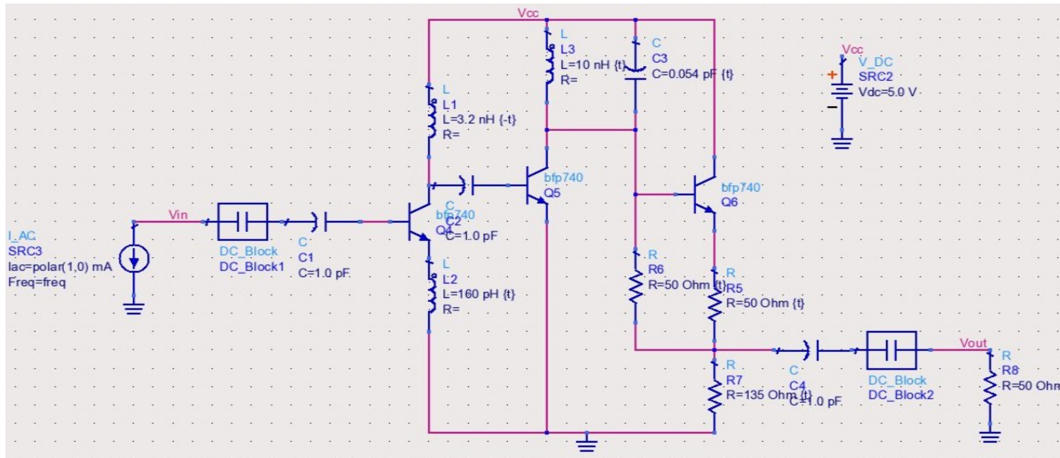

Figure 4.12.: Schematic with Cascade Configuration

In the second, the load of this stage, which is formed by the parallel resonance of inductor L_3, capacitor C_3 and the base-collector junction capacitance of Q_5, has been tuned to the frequency of interest. In order to desensitize the LNA from load changes have used an emitter follower as output stage and uses resistive feedback R_5, R_6, to stabilize the output stage at the desire frequency.

One Stage Schematic [26]

This schematic has only one stage. The base inductance plays an important role in minimizing group delay variation. The feedback resistance controls input impedance as well as a 3-dB bandwidth and noise performance, thus requiring careful optimization of its value to achieve low noise performance with a wideband operating frequency range.

An inductive peaking technique are incorporated to enhance the overall LNA performance in terms of noise, gain flatness, input/output matching, linearity, and dc power consumption over the entire UWB band from 3 to 10 GHz. The inductor peaking technique extends the bandwidth sacrificing phase response of S_{21}, which is very crucial feature for wideband system. The value of peaking

inductor, L_1 in Figure is carefully chosen not to degrade the linear phase of S_{21} over the entire band.

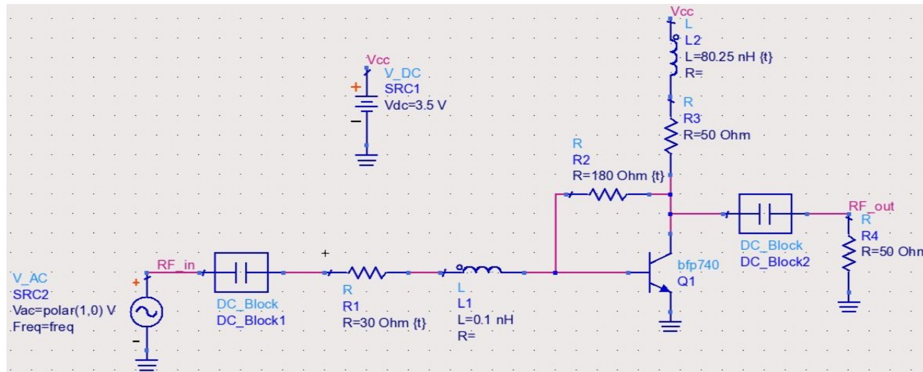

Figure 4.13.: One Stage Schematic

Schematic with Cascode Configuration [25]

The LNA presented incorporates both shunt base emitter capacitance and weak resistive feedback in a cascode architecture with inductive degeneration (improves matching and linearity), as shown in Figure 4.14. The load inductor L_1 widens the bandwidth at high frequency by causing inductive peaking, which offsets the gain rolloff introduced by a capacitive load. The second and last stage is a simple emitter-follower, providing a low output impedance.

The noise performance of an amplifier is determined mainly by its minimum noise factor and noise contribution that occurs when input source admittance is different from its optimum admittance.

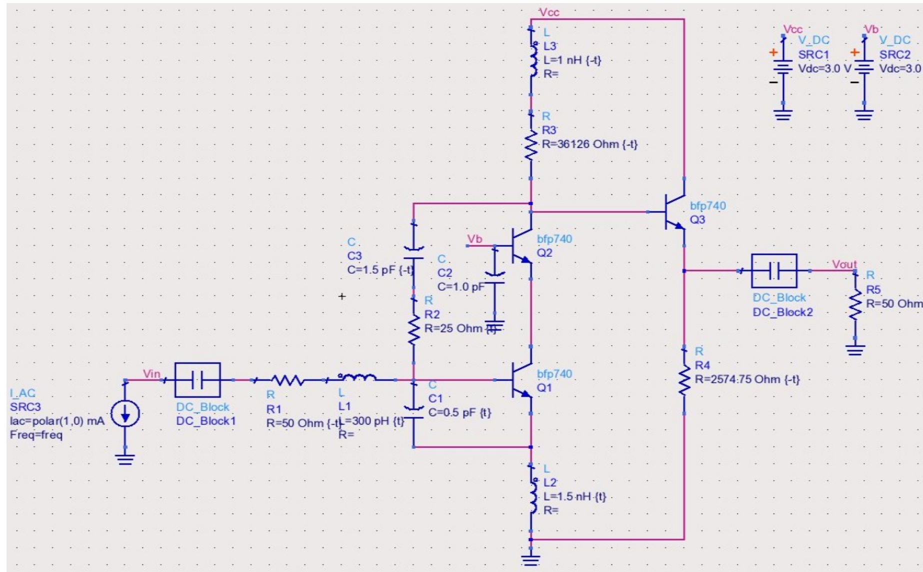

Figure 4.14.: Schematic with Cascode Configuration

Simulations

In this section we show the simulation results of the schematics. It was simulated the gain voltage, the S parameters and the noise figure for every schematic.

The next expressions are explain for the better compression of the noise chart.

nf(k) in the dataset is the noise figure at output port k. When noise figure is calculated at a port, the other ports in the network are terminated in their respectives impedances. [31]

$$F = \frac{SNR_i}{SNR_{out}} \tag{4.2.1}$$

The transmitted input noise represents the portion of the incident thermal noise (kTB) which passes through the system. So nf(2) is the noise figure of the circuit, because we only have two port, the input port (port 1) and the output port (port 2).

NF_{min} is the minimum noise figure that the circuit can produce, when the source has the optimum reflection coefficient, S_{opt}.

For the first schematic the simulations are showed in the next figures.

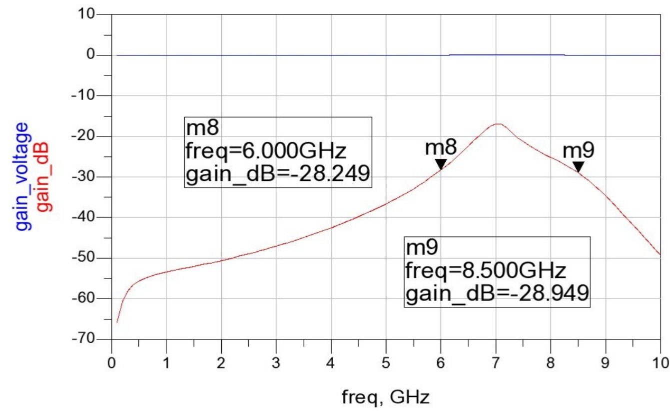

Figure 4.15.: Gain voltage simulation of 3 Stage Schematic

In the figure below it can be see that the operational frequency is set at 7 GHz, but the values achieved for the gain voltage are very low, between -20, -30 dB. The operational frequency is set by the inductor L_1 and the capacitor C_1 in the Figure 4.16, as we explain before.

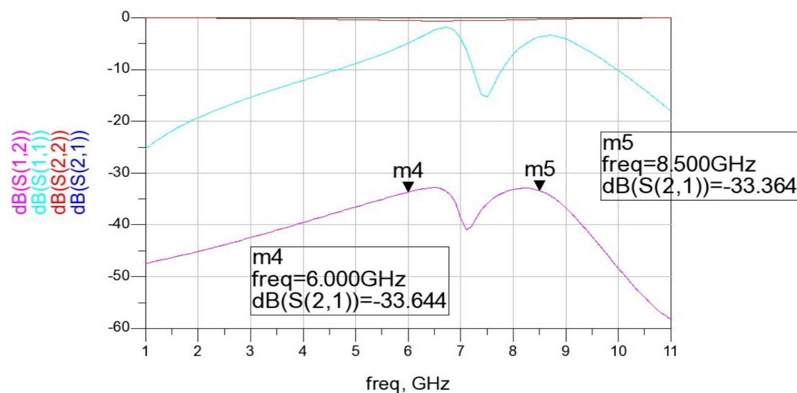

Figure 4.16.: S parameter simulation of 3 Stage Schematic

The results of the S parameters are similars as before. The values are very low again, thus $s_{11} = s_{22}$ and $s_{12} = s_{21}$ which does not have any sense, because we need that s_{21} was the gain of the circuit, so this value need to be high than 0 dB and, on the other hand, we do not need reflexions, so s_{12} has to be lower than 0 dB.

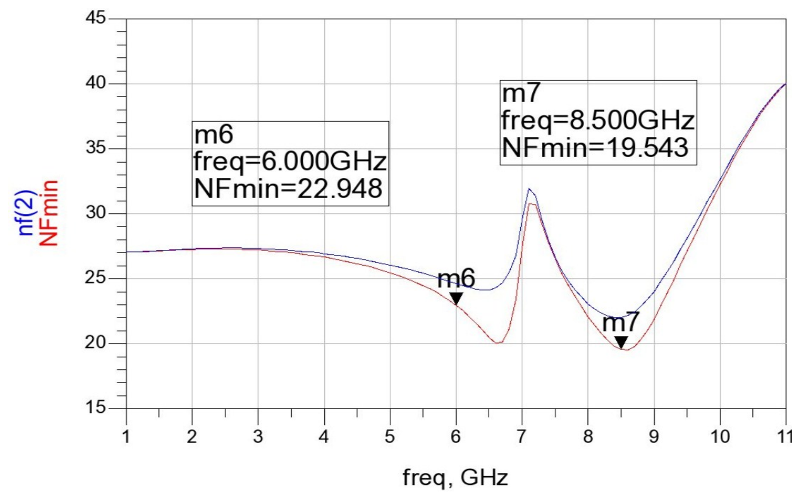

Figure 4.17.: Noise figure simulation of 3 Stage Schematic

Again the results are not correct, the value of the noise figure is between 10 and 30 dB which is very high for the purpose of the application. If the signal is weak and the noise is intense, the SNR will be low and the reception will be less reliable. The design of communications equipment aims to produce the SNR high as possible. Accordingly, this schematic do not accomplish the requirements needed for the Low Noise Amplifier.

The simulations of the second schematic are showed in the next figures.

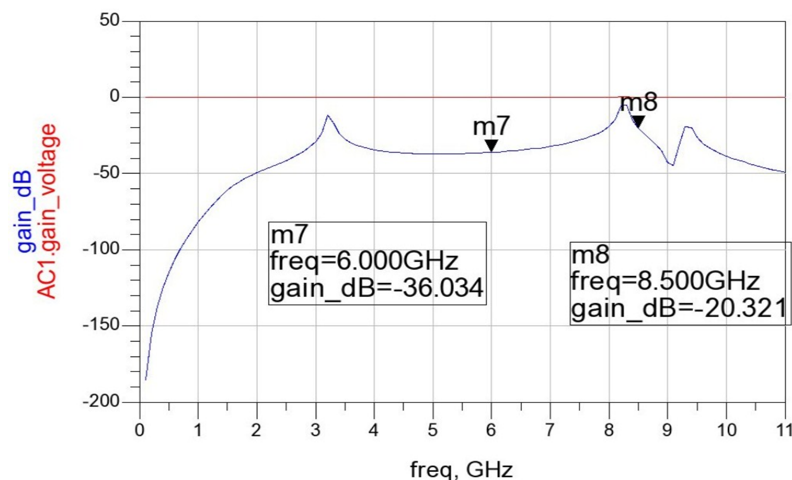

Figure 4.18.: Gain voltage simulation of Schematic with Cascade Configuration

In the figure we can look the same result like in the schematic before, the values of the gain voltage are very low again and in this we can consider any operational frequency.

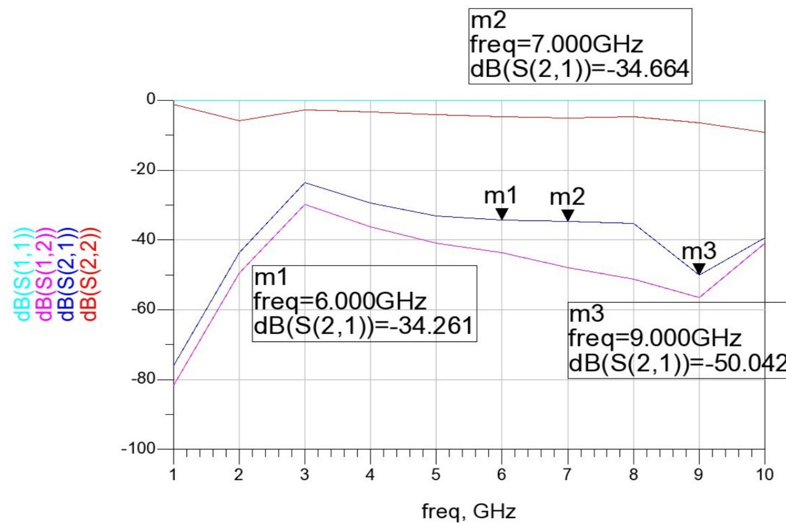

Figure 4.19.: S parameter simulation of Schematic with Cascade Configuration

Here again we achieve bad results, but in this case the results of the parameter s_{11} is a good result, because is around 0 dB, what means no reflexions in the input port.

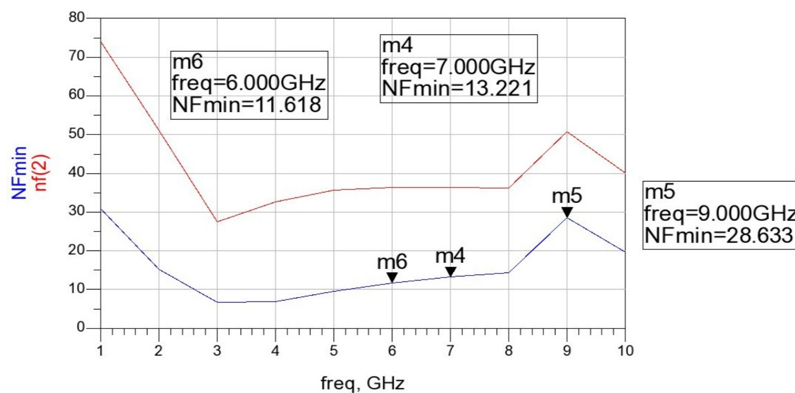

Figure 4.20.: Noise figure simulation of Schematic with Cascade Configuration

Now the results of noise figure are better, between 8 and 12 dB, but still high for the purpose of the Low Noise Amplifier as we explain before. If the signal

is weak and the noise is intense, the SNR will be low and the reception will be less reliable. The design of communications equipment aims to produce the SNR high as possible. Again we have to exclude this design.

For the third schematic the simulations are showed in the next figures.

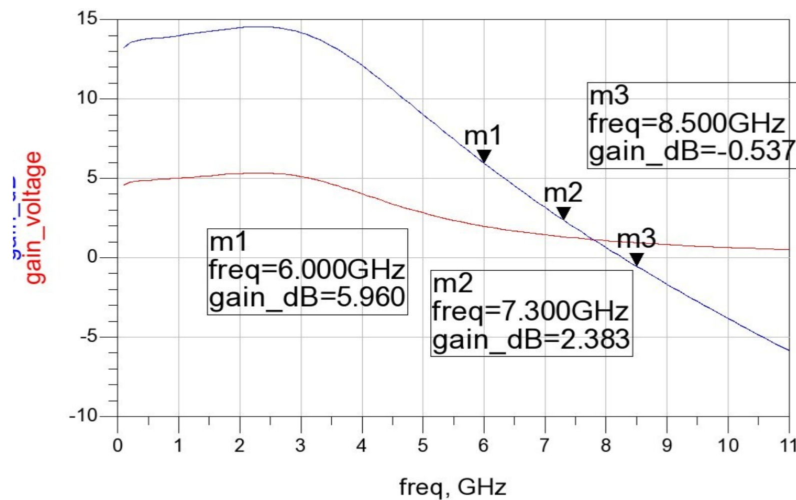

Figure 4.21.: Gain voltage simulation of One Stage Schematic

Here we obtain the first good results. The values of the gain voltage are from 15 dB to 0 dB in the range of 1 - 8 GHz, even, we need obtain more than 10 dB in the range of 6 - 8.5 GHz and from 2.5 GHz to 8 GHz the gain voltage decrease very fast.

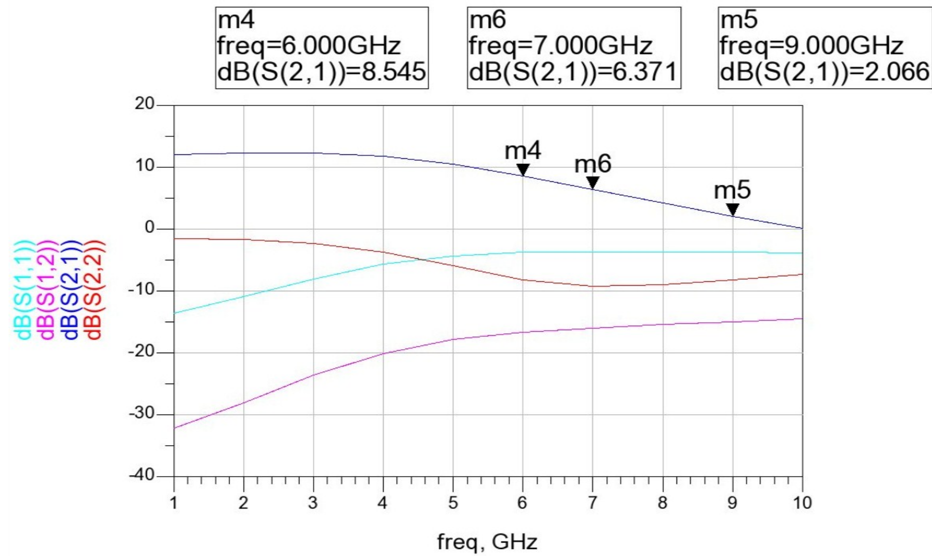

Figure 4.22.: S parameter simulation of One Stage Schematic

Here the conclusion is similar as with the chart before, the results for the parameter s_{21} are good, but insufficients.

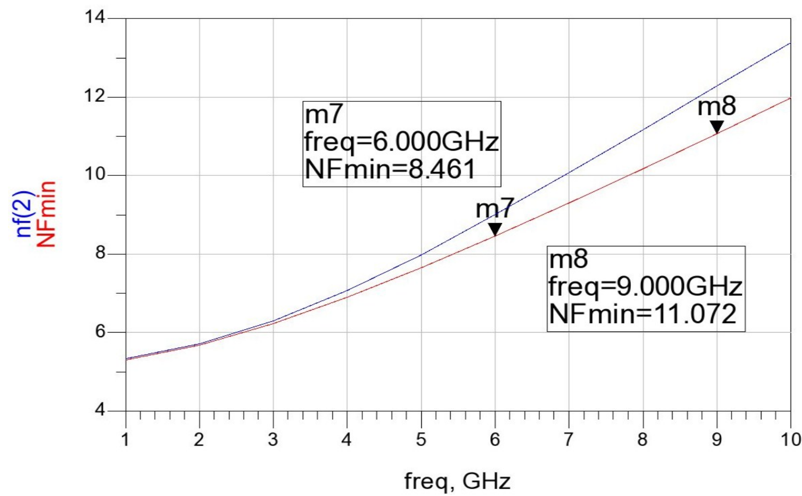

Figure 4.23.: Noise figure simulation of One Stage Schematic

Again the results from figure 4.23 are better than before, but still we need values lower, for the noise figure around 1 dB and here we achieve 8-12 dB.

The simulations of the fourth schematic are showed in the next figures.

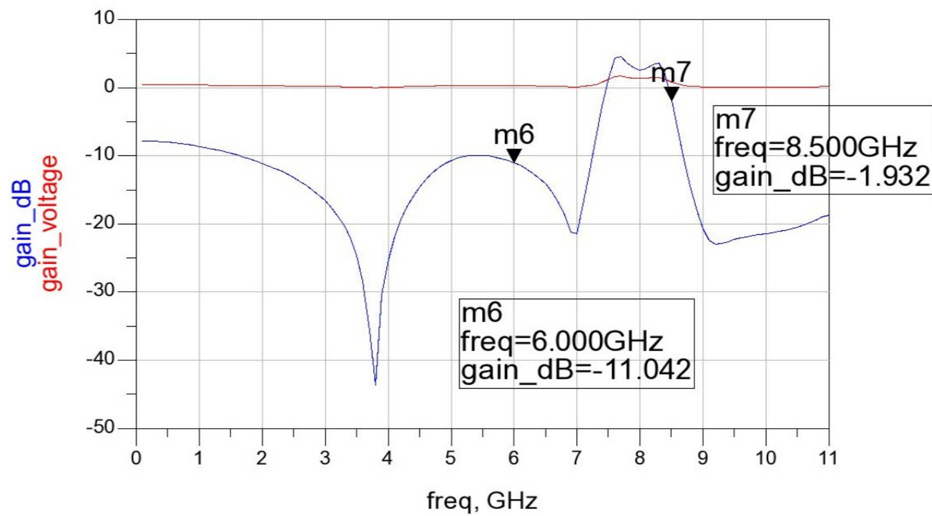

Figure 4.24.: Gain voltage simulation of Schematic with Cascode Configuration

The results in figure 4.24 for the gain voltage are very confused, the values are random and low than 0 dB.

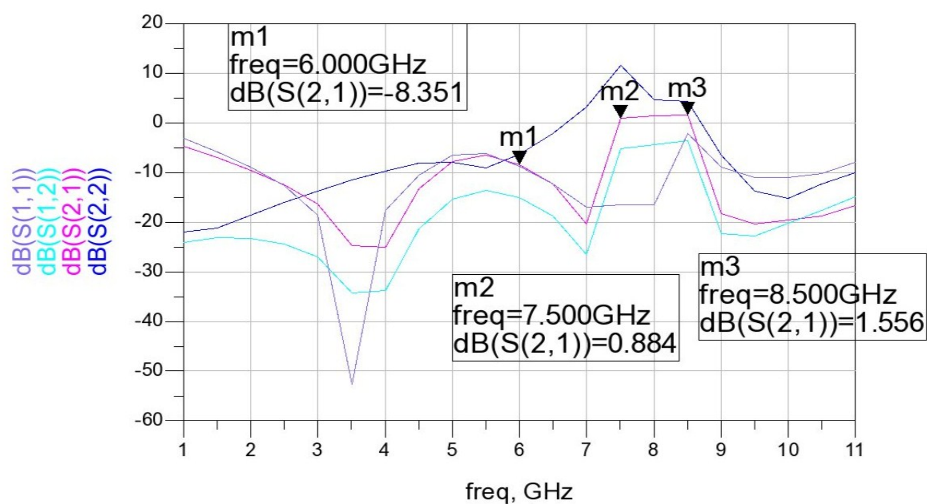

Figure 4.25.: S parameter simulation of Schematic with Cascode Configuration

In figure 4.25 is the same, the values are random and low again.

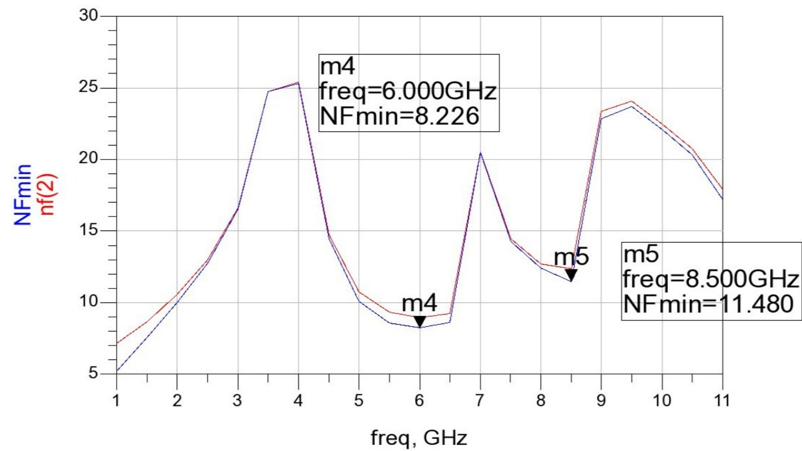

Figure 4.26.: Noise figure simulation of Schematic with Cascode Configuration

Again the results in figure 4.26 of noise figure are very high. Therefore we exclude this schematic also.

Another reason for use a schematic with transmission lines were the results we have achieved with the schematics with lumped elements.

In every schematic the S parameters results were confused and the noise figure was high. We think that maybe this is a problem of the bias circuit, but we did not have enough time to try everything and we decided to try with a different kind of schematic.

4.2.2. Schematics with transmission lines

The final scheme used is as follows. The circuit is a hybrid of microstrip lines and discrete elements such as transistor, capacitors and resistors.

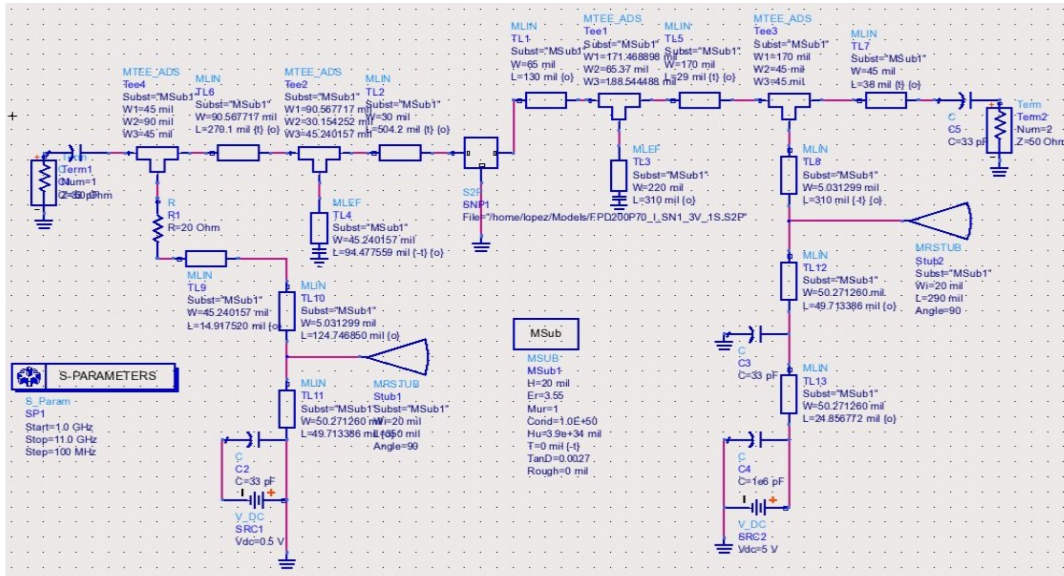

Figure 4.27.: Low Noise Amplifier final schematic

First we have the transistor [34], as mentioned earlier, is the transistor FPD200P70 of RFMD. We need to adapt the transistor input and output impedances (50 Ω) in the desired bandwidth (6-8.5 GHz). Thus we see the input and output matching networks. The calculation of these two networks has been carried out with open or closed circuit stubs and the help of the Smith chart. In the datasheet of the transistor (attach in Anex A) we can find a reference design, which we have used for our design. In the reference design the range used are from 5.15 GHz to 5.8 GHz and we have adjusted it for a range from 6 GHz to 8.5 GHz. To extend a bandwidth we have to play with the longitude of the transmission lines, so using the tuned tool of ADS Agilent we selected these longitudes and we changed theirs values until achieved the result we need for the UWB application.

For the bias circuit, the gate need to be approximately 0.2 V negative referenced to the source, the input of a HEMT is basically a small tunnel diode and in normal operation these diodes are negative biased, effectively making the gate a low value capacitor, therefore the transistor gate is supply at -0.5 V and the drain at 5 V, the source is grounded. It is basically designing a bias T, we want DC in one port and RF in the other two ports, the radial stub is born to realize a short circuit at the point where it is placed. One of the biggest issue of this biasing method is, the negative supply must turn ON first, and turn OFF last,

as we have verified when the measurement part was carried out. We also used feedthrough capacitors for DC supplies, these kinds of capacitors are designed for DC power line in RF system. It passed through the DC but blocks the RF energy, they let the signal pass through but will stop the RF from escaping from the device through that hole to the outside wiring.

Simulations

It was simulated the S parameters and the noise figure of the schematic above.

In figure 4.28 we can look the S parameter simulation. The bandwidth of the circuit cover from 5.4 GHz to 10.4 GHz, more than sufficient, because we only need a bandwidth between 6 to 8.5 GHz. The central frequency is set at 7.3 GHz with a value of the s_{21} parameter of 14.554 dB, more than enough for the purpose of the application. For 6 GHz this value is 11.059 dB and for 8.5 GHz is 11.469 dB, so we can say the LNA is working properly in gain. The parameters s_{11} and s_{22} are low than 0 dB, therefore we can assure the LNA do not have reflexions in the input and output ports.

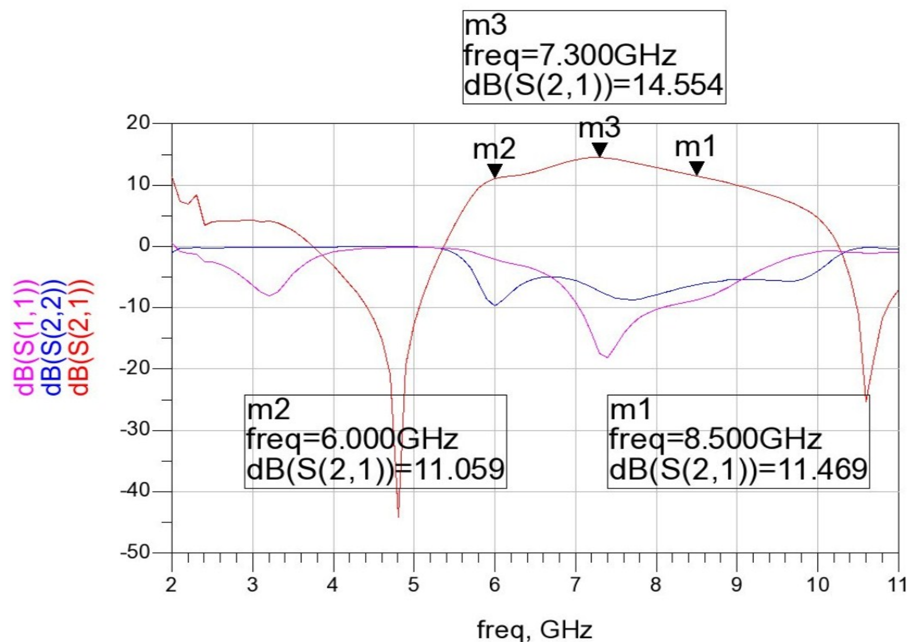

Figure 4.28.: S parameters simulation of the LNA schematic

In figure 4.29 we show different kinds of noise. These values were explained in the simulations section of the schematics with lumped elements. The value of the minimun noise figure is around 1-1.5 dB. Here we can say again that the LNA is working properly in noise.

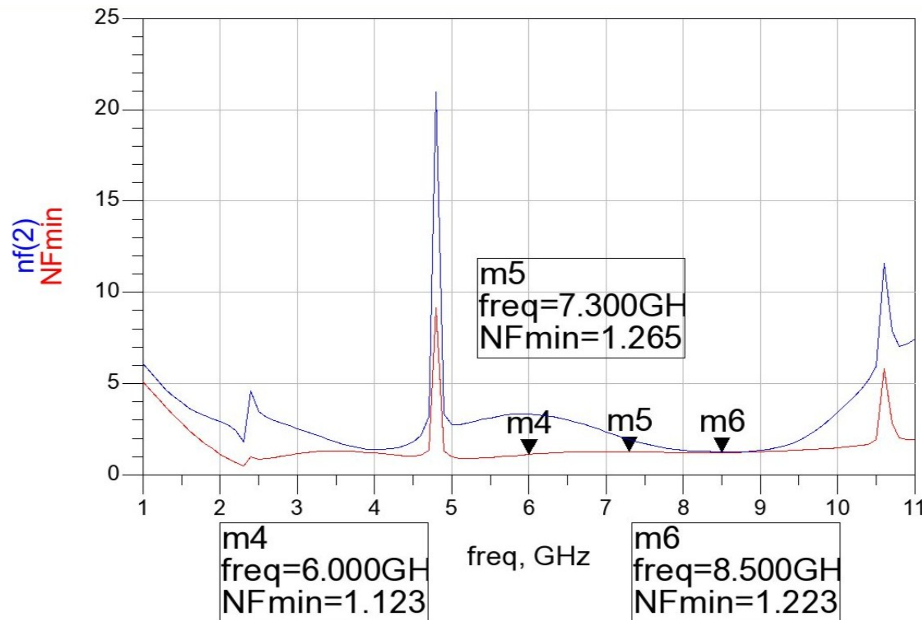

Figure 4.29.: Noise Figures simulation of the LNA schematic

4.2.3. Final choice

As we just explained in the sections before, the schematic with transmission lines is the best choice. We can list the reasons like the small size of the PCB in the future and, of course, the results of the simulations. The simulations for the schematics with lumped elements are not correct in any case and the simulations of the schematic with transmission lines are close of the results we need to realize the Low Noise Amplifier, relatively high gain and low noise figure.

We achieved almost 15 dB for the S_{21} parameter at the frequency of 7.3 GHz, this a very good result, because is more or less the central frequency we want and there we get the maximum value for the S_{21} parameter and this value is higher than 10 dB. The bandwidth is from 5 GHz to 10 Ghz what is more than we need,

that is from 6 GHz to 8.5 GHz. And finally, the noise figure we get is very low, around 1-1.5 dB.

4.3. Low Noise Amplifier Layout

To make the layout of the schematic it was used the tool Momentum of ADS Agilent. This process was done in parts, in the first place we made the layout of the input matching network and after that the output matching network layout. Once we are confident that the previous layouts are correct, we join the two previous layouts in one single layout.

If all data is contained in the schematic, it is very simple to create a layout.

A substrate is required as part of the layout. The substrate describes the media where the circuit exists. For our schematic, a substrate with the following layers will be used:

- A ground plane.
- A layer of insulation, we called it MSub1_1.
- A metal layer for the microstrip.
- An air layer above the microstrip.

The next figures show us the substrate layers and the metal layers. The figure above contains the substrate layers which looks like as we have explained before. The MSub1_1 substrate correspond to a ROGER 4003 substrate with a permitivity, ϵ_r, of 3.55, a loss tangent of 0.0027 and a thickness of 20 μm.

In the figure below a metal layer is added, the cond layer. The word strip defines the layer such that the microstrips are metal and what surrounds the microstrips on that layer is air or dielectric.

Then it was exchanged the existing cable for transmission lines (the minimum width or length value for these is 50 mm, to perform the PCB after). The resistors and capacitors are exchanged for existing models, and finally define the ports of input and output. When you add ports, you must consider not using the ground

port component in circuits that will be simulated using Momentum. Either add ground planes to the substrate or use the ground reference ports.

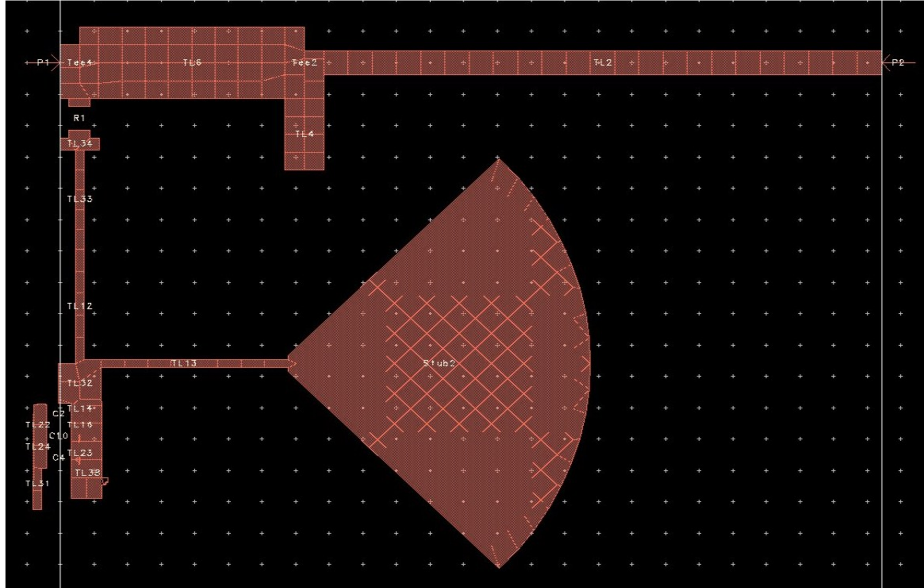

Figure 4.30.: Input Matching Network layout

In order to perform a simulation, Green's functions that characterize the behavior of the substrate must be computed. Once done, you do not do it again every time you want to simulate the layout.

A mesh is required too in order to perform a simulation.

A mesh is a grid-like pattern of triangles and rectangles that is applied the surfaces of a circuit. Using the mesh, the current within each triangular or rectangular area is calculated during the simulation.

The Momentum simulation process combines the Green's functions that were calculated for the substrate, plus the mesh information, and solves for currents in the circuit. Using the current calculations, S-parameters are then calculated for the circuit.

As we can see the S parameters s_{11} is equals to s_{22} and the same with s_{12} and s_{21} parameters, which means that the network is reciprocal and symetrical. Beside the S parameters are less than 0 dB which again means that is a passive network. So, we can confirm the network is working properly.

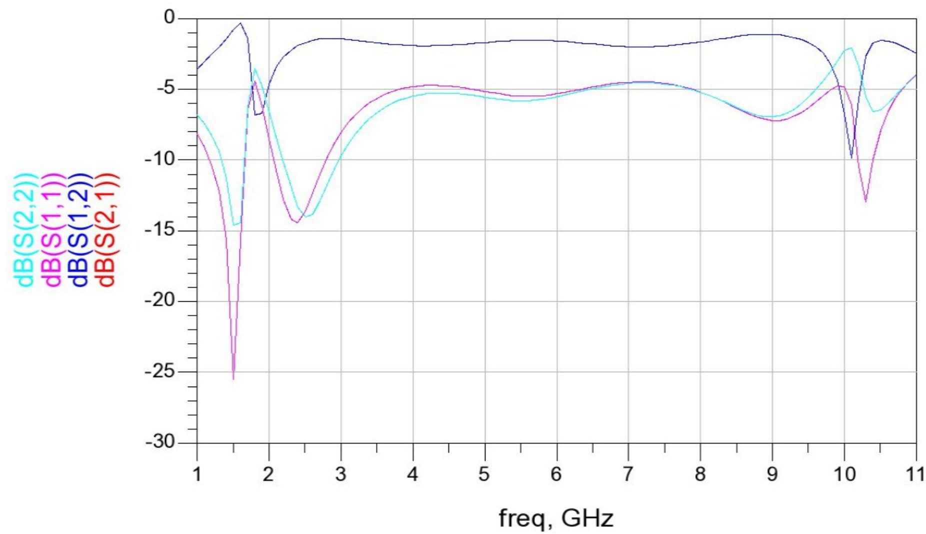

Figure 4.31.: S parameters simulation of Input Matching Network layout

The same process is performed for the output matching network, the results obtained are shown in the figure 4.33. The same result as the input matching network is achieved, but in this we can see clearly that in the range from 6 to 8.5 GHz the results are better and this is the bandwidth we need for the purpose of the application.

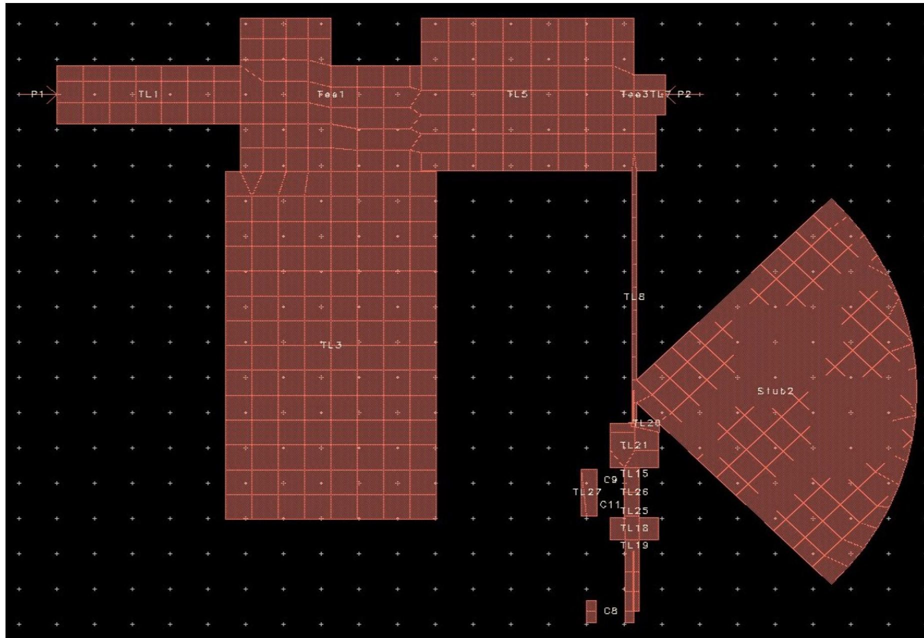

Figure 4.32.: Output Matching Network layout

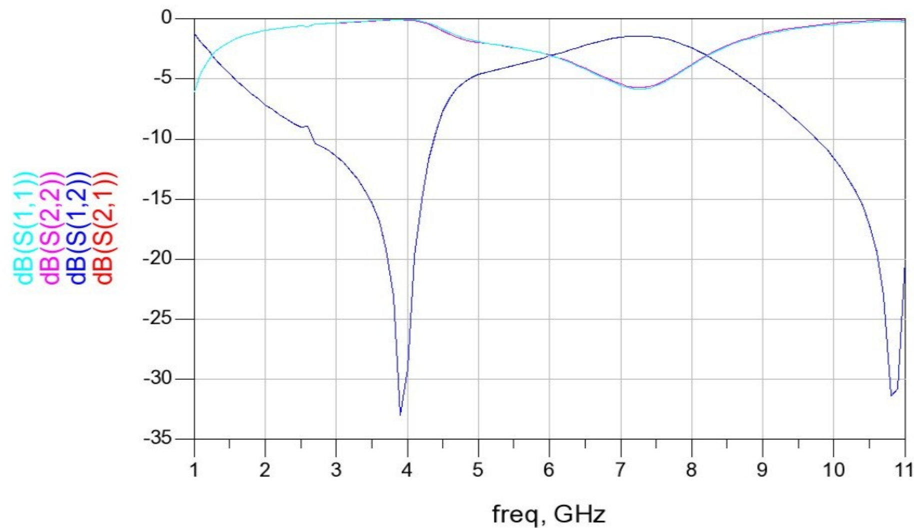

Figure 4.33.: S parameters simulation of Output Matching Network layout

One after confirming the correct performance of the input and output matching networks, they join each other without the transistor, because is a discrete element and therefore we must leave its space in the layout. The transmission lines

at the input and the output of the layout are enough long to get a standard board of the institute, with dimensions of 90 by 90 mm.

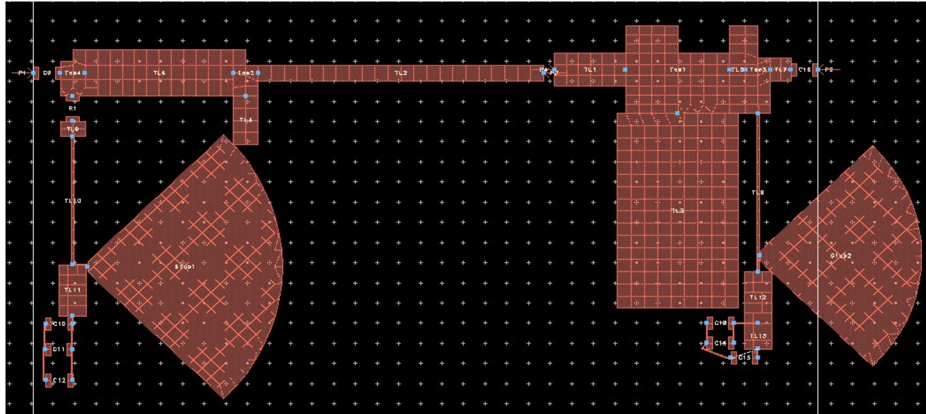

Figure 4.34.: Low noise amplifier layout

A SMP connectors were added, in the future implementation of the PCB we used these connectors to supply the voltage to the circuit. The SMP interface is a subminiature interface in the same scale as MMCX connectors but offers a frequency range of DC to 40 GHz. It is commonly used in miniaturized high frequency coaxial modules and is offered in both push-on and snap-on mating styles.

Figure 4.35.: SMP connector

The final result of our layout is showed in the figure 4.37.

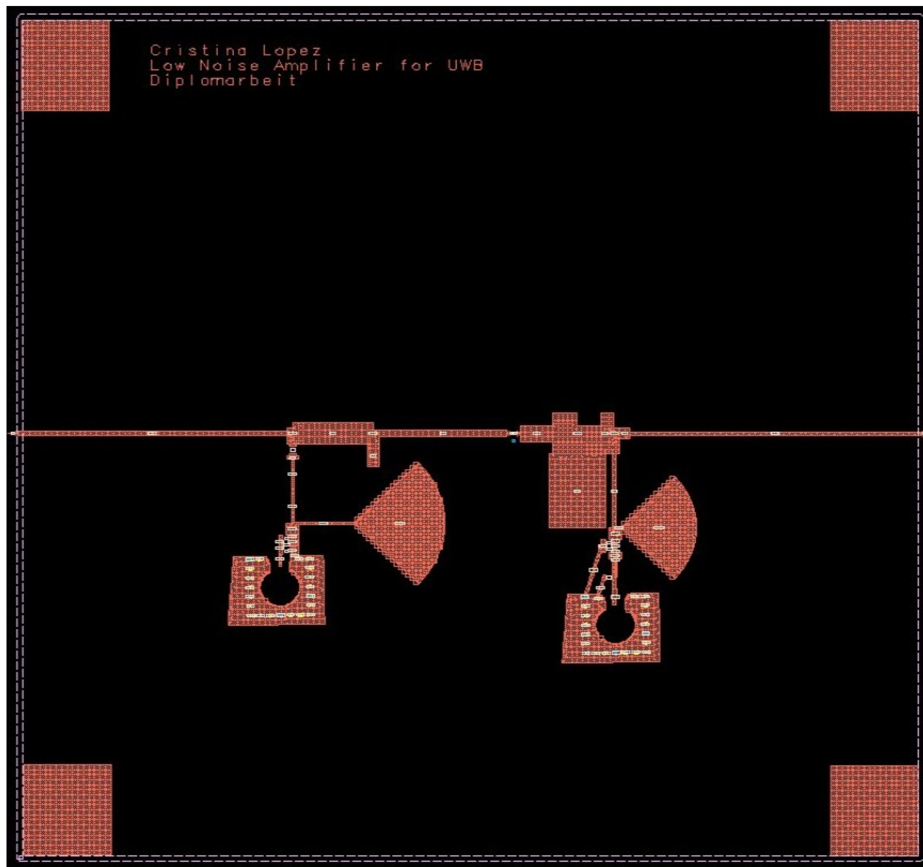

Figure 4.36.: Low noise amplifier layout

We performed a final simulation of the full layout (the layout show in the figure 4.37), in the next section we show the results.

4.4. Final Simulations

The final simulations are performed with the previously generated layout (layout in the figure 4.37), the way to export the layout is converted as a component part, once that is done, we place the transistor, the voltage supplies and the ground, as observed in Figure 4.40, and we can perform simulations required, they were on S-parameters and noise figure.

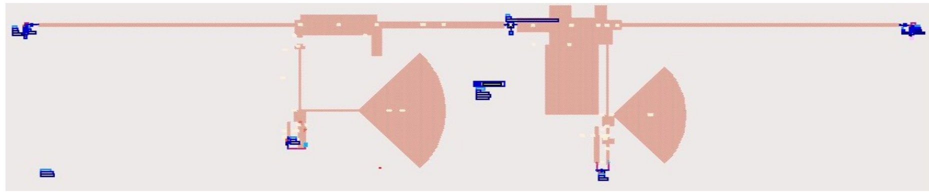

Figure 4.37.: Low noise amplifier layout

In the S parameter simulation we have obtained almost the same result as in the schematic simulation, the bandwidth of the LNA if from 5.5 to 9 GHz, but the values suffer a degradation in the sides, this is because the simulation result in the output matching network layout, which has less bandwidth than in the input matching network layout. Anyway the values obtained are sufficient for the purpose of the UWB application.

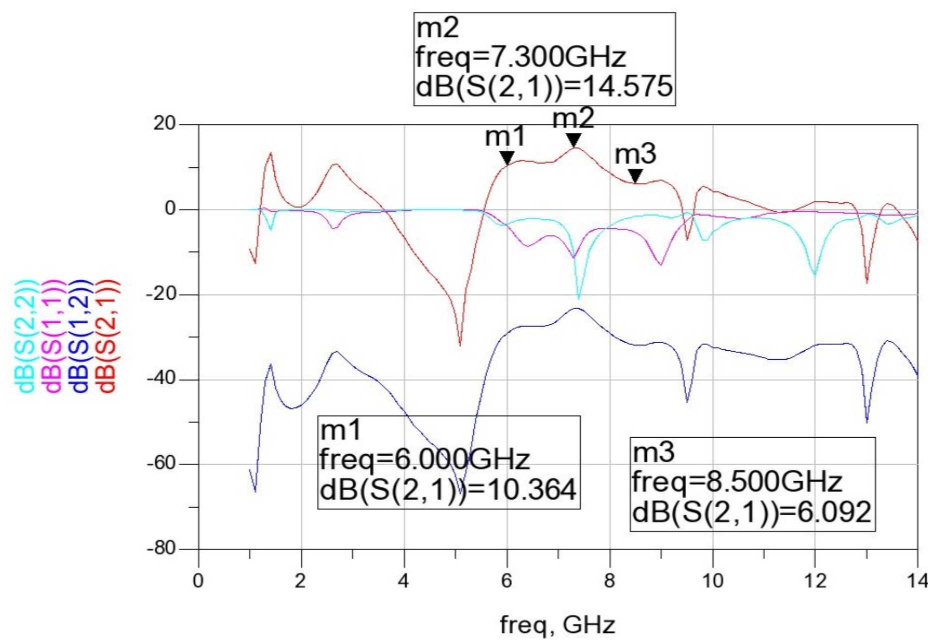

Figure 4.38.: Final S parameter simulation

As for noise, the results are more similar to the simulation of the schematic (figure 4.40)

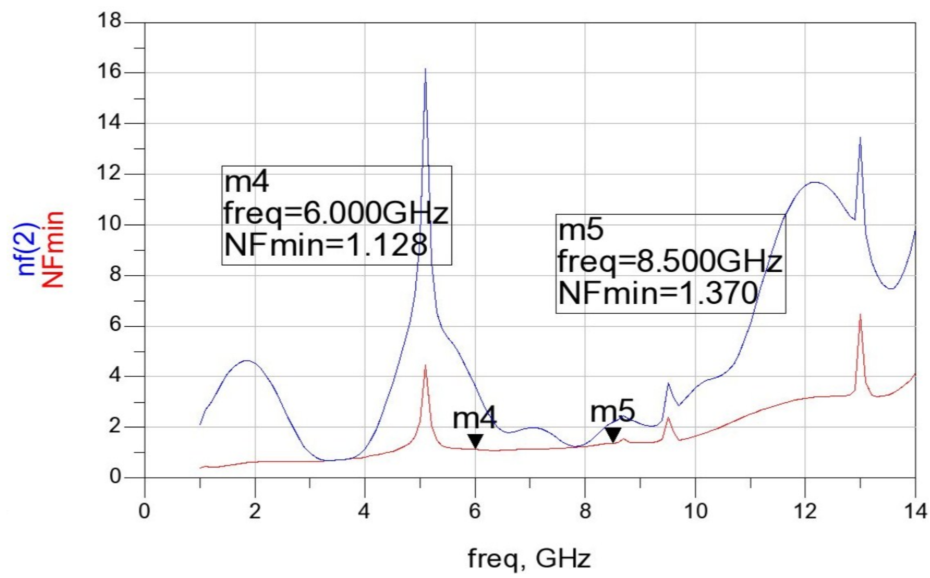

Figure 4.39.: Final noise figure simulation

With these results, we finally produce the Printed Circuit Board (PCB) as it is explained in the next chapter.

5. Implementation

5.1. Realization of Low Noise Amplifier

This section will introduce as carried out the implementation of the Low Noise Amplifier for Ultra-Wide Band.

Once we got the final layout of our amplifier (it was explained in the section before), it was exported in gerber format to produce the Printed circuit board (PCB).

The format type Gerber file contains the information necessary for manufacturing the printed circuit board or PCB.

In ADS, when a hole is created in a geometrical figure (like polygon), a cutline is introduced. This is a false edge connecting the outer boundary of the polygon with the inner boundary. This polygon is actually a single re-entrant polygon. We have three options, Holes as cutlines, Holes as polygons and Preserve holes. When you select Holes as cutlines this re-entrant polygon is translated to Gerber as-is.When Holes as polygons is selected, holes are exported as filled elements. Therefore the polygon will appear to have no holes. When Preserve holes is selected, the resultant polygon in Gerber contains a dark area and empty area. This option is not available for exporting Gerber files in RS274X format. The option we use is Holes as cutlines, because we want this holes act like a via between the GND and the metal layer.

The figure 5.1 shows the result of our PCB.

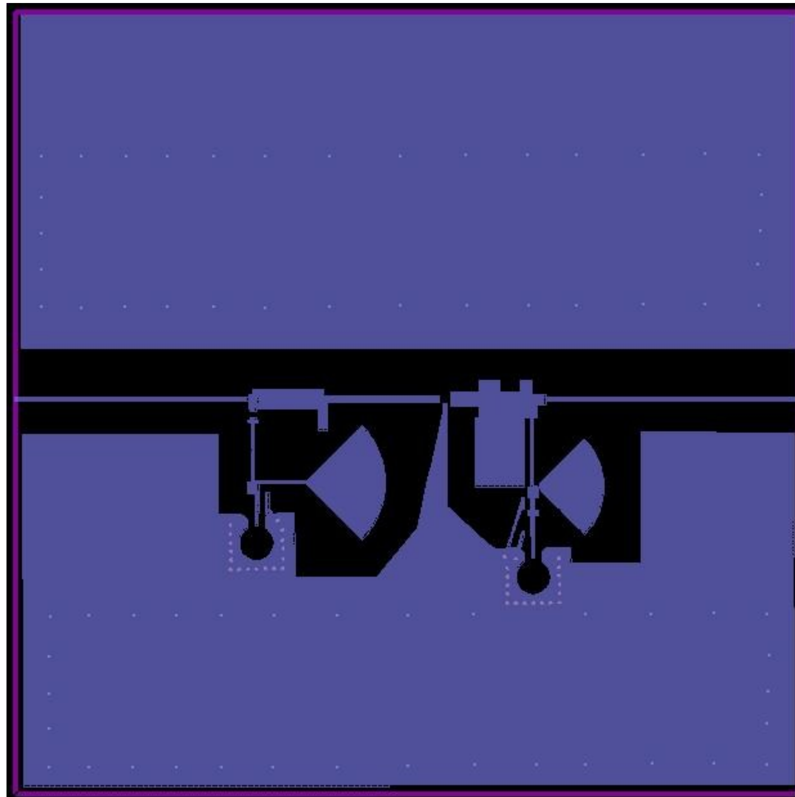

Figure 5.1.: PCB view through the gerber files generated

Finally, once we have gotten the gerber files, the PCB was produced and we can see the result in the next figure.

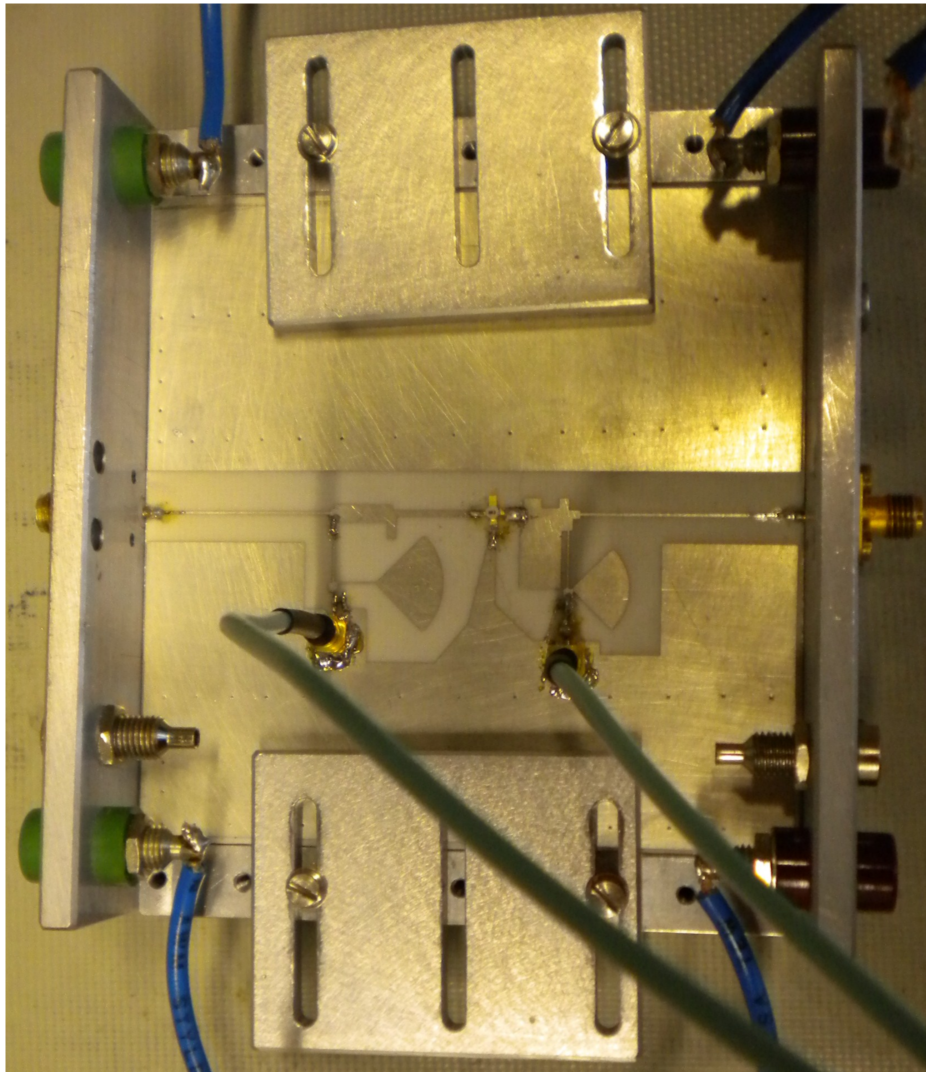

Figure 5.2.: Printed Circuit Board of the Low Noise Amplifier

The PCB is inserted in a fixation to make easier measure later. Although the SMP connectors are connected. The lumped elements were soldiers, the resistance, capacitors and the transistor.

5.2. Test PCB

Once we have obtained the PCB, the next step is to measure it. We start checking the continuity of the PCB and next we measure the S parameters of the PCB.

5.2.1. Testbench

First, we check the continuity of the PCB. The resistance of an electric circuit determines how much current flows in the circuit when a certain voltage is applied. To do continuity tests the procedure is the same as measure resistances, we use the multimeter in ohms and we check if the circuit offers low resistance or very few ohms. We used the option 2 K or 20 K ohms, because they offer a voltage of 1-2 volts, which is not so much for our circuit, however was avoided using the multimeter at 200 ohms and in continuity options, because they offer 5-6 volts and this value is very high for our circuit, so this was avoided to prevent damage to the circuit.

Once we check the continuity of the PCB, the next measure was the S parameters of the PCB. In the next figure we show the assembly used to carry out the measurements of the parameters S.

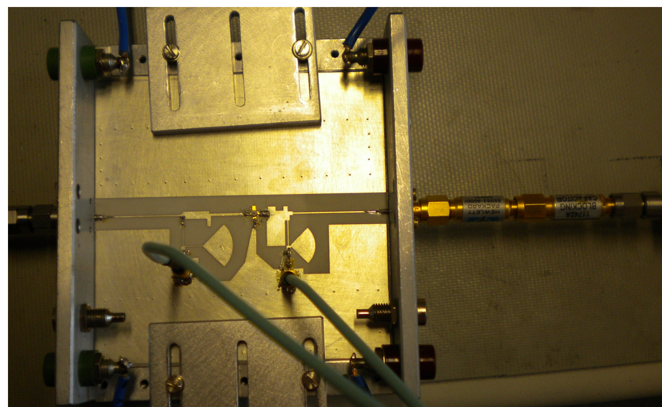

Figure 5.3.: Assembly used to measure the S parameters

In first place is the PCB, next we placed a 20 dB attenuator, the reason is because we can insert more than 17 dBm in the machine used for do this measurements,

with the attenuator we are sure not to introduce more. The last element in the figure is a DC block, again, we can insert DC in the machine and this element block the DC provides for the PCB.

Although, we used two power supplies, as it can see in the figure, there is two SMP connectors connect to the circuit, as we just explained we use them to supply voltage to the PCB, the right with -0.5 volts and the left with 5 volts.

Finally, in the next section we show the S parameters measurements we have achieved.

5.2.2. Measurement results

The measure of the PCB was carried out with a S parameters machine, it was explained in the section before. With the previous assembly the next result were achieved.

We obtain a text document with the values of every S parameter. This text document was processed with Matlab (the Matlab code is shown in the Appendix B). As we added a 20 dB attenuator after the PCB, it has to add 20 dB to the S_{21} parameter. The backward isolation (s_{12} parameter) should be high and the external attenuation should not affect the input and output return loss (S_{11} and S_{22} parameters), since it is perfect 50 Ω.

The next figure shows the S parameters measurement results.

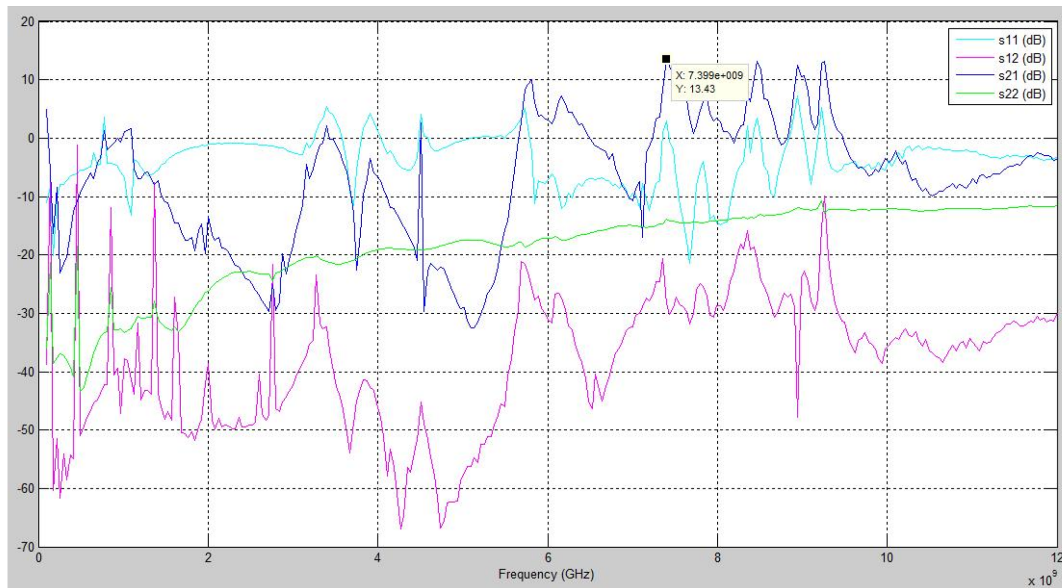

Figure 5.4.: S parameters measurement results

From 7 to 9.5 GHz our bandwidth is place. The high value is achieved at 7.4 GHz with 13.43 dB, the problem is that the S_{21} parameter result is not flat in the bandwidth, because the transistor produces oscillations if it is not stable in the whole range of its frequency. The next figure shows the stability of the transistor from 1 to 11 GHz, the transistor is stable when the K value is up to 1 dB, we obtained this value in the range from 5 to 11 GHz, perhaps this is the problem.

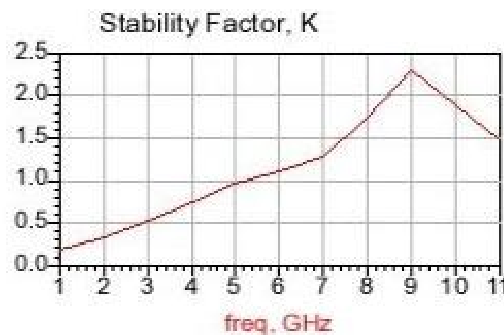

Figure 5.5.: Stability of the transistor

Also, we have to mention that the transistor finally was biased at -0.3 volts at

the gate and 3 volts at the drain, if not the results were worst. At this point we realized that first we must turn ON the supply voltage for the gate and turn OFF last, if not the transistor is oscillating and it is not working properly.

6. Conclusion and Outlook

The primary objective of the thesis was to design a Low Noise Amplifier that could be used for UWB applications. It was intended to have the LNA be capable of providing enough gain within the frequency range 6 to 9 GHz (specified for UWB technology in Europe) with minimal noise.

In Chapter 2, various aspects of the UWB standard were studied, although a briefly explanation of concepts as Transmission lines, matching networks and noise. Chapter 2 analyses the Low Noise Amplifier state of the art, the figure of merit needed and a requirement Engineering and Analysis. Chapter 4 describes various useful and popular LNA topologies. This chapter also gives good understanding of the proposed design, transistor selection, schematic of the design, simulated results, and illustrates the layout of the design. Chapter 5 finally describes the implementation of the Low Noise Amplifier and the measurements results of the Printed Circuit Board.

Over the throughout of the project the best transistor was chosen for the low noise amplifier, which was the FPD200P70, GaAs pHEMT technology, this step consumed a quarter of the time spent on the project. This transistor ensures provide the characteristics of bandwidth, gain and noise required for the purpose of the application. Once chosen this transistor, the next step was to choose the amplifier schematic, it was simulated distinct schematic with discrete elements without good result and finally the choice was a schematic with transmission lines.The proposed design has a gain around 13 dB from 5.5 to 9 GHz, in simulation, after which it starts decreasing. The target noise figure was around 1 dB and simulations show that the proposed architecture has succeeded in achieving that.

The measurement result are not so good as the simulations result, but it is a begin to improve the gain in the bandwidth achieved.

The next step in this project will improve the experimental results, now we have more information and experience and we can learn from our past mistakes. Also should recheck the schematic with discrete elements simulations, in order to get better results and design another low noise amplifier with this kind of schematics.

A. Appendix A

Listing A.1: Code Matlab for processing text data of S parameters measures

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                                                                    %
% Autor: Cristina López Fernández                                    %
% Date: 08/02/2012                                                   %
% Processing a text document that contains the values of the         %
% S parameters measures.                                             %
%                                                                    %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Acquisition S-parameters

M21= 20*log10(abs(test.S(:,1))); %S11
M22= 20*log10(abs(test.S(:,2))); %S12
M23= 20*log10(abs(test.S(:,3)))+20; %S21 plus 20 dB
M24= 20*log10(abs(test.S(:,4))); %S22

%Plot of S parameters
figure;
plot(test.freq,M21,'c');
grid
hold on;
plot(test.freq,M22,'m');
plot(test.freq,M23,'b');
plot(test.freq,M24,'g');
xlabel('Frequency (GHz)');
legend('s11 (dB)','s12 (dB)','s21 (dB)','s22 (dB)')
```

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