UNIVERSIDAD CARLOS III DE MADRID
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TESIS DOCTORAL

CONTRIBUTION TO THE DESIGN OF CONTINUOUS-TIME SIGMA-DELTA MODULATORS BASED ON TIME DELAY ELEMENTS

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Leganés, Marzo de 2008.

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Abstract

The research carried out in this thesis is focused in the development of a new class of data converters for digital radio. There are two main architectures for communication receivers which perform a digital demodulation. One of them is based on analog demodulation to the base band and digitization of the I/Q components. Another option is to digitize the band pass signal at the output of the IF stage using a bandpass Sigma-Delta modulator. Bandpass Sigma-Delta modulators can be implemented with discrete-time circuits, using switched capacitors or continuous-time circuits.

The main innovation introduced in this work is the use of passive transmission lines in the loop filter of a bandpass continuous-time Sigma-Delta modulator instead of the conventional solution with *gm-C* or *LC* resonators. As long as transmission lines are used as replacement of a *LC* resonator in RF technology, it seems compelling that transmission lines could improve bandpass continuous-time Sigma-Delta modulators. The analysis of a Sigma-Delta modulator using distributed resonators has led to a completely new family of Sigma-Delta modulators which possess properties inherited both from continuous-time and discrete-time Sigma-Delta modulators.

In this thesis we present the basic theory and the practical design trade-offs of this new family of Sigma-Delta modulators. Three demonstration chips have been implemented to validate the theoretical developments. The first two are a proof of concept of the application of transmission lines to build lowpass and bandpass modulators. The third chip summarizes all the contributions of the thesis. It consists of a transmission line Sigma-Delta modulator which combines subsampling techniques, a mismatch insensitive circuitry and a quadrature architecture to implement the IF to digital stage of a receiver.

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Glossary of terms

A/D	Analog-to-Digital (Converter)
CAD	Computer-Aided Design
CMOS	Complementary Metal-Oxide-Semiconductor (Technology)
CT-ΣΔM	Continuous-Time Sigma-Delta Modulator
D/A	Digital-to-Analog (Converter)
DEM	Dynamic Element Matching
DNL	Differential Non-Linearity
DR	Dynamic Range
DT-ΣΔM	Discrete-Time Sigma-Delta Modulator
DWA	Data Weighted Averaging
DSP	Digital Signal Processing
ENOB	Effective Number of Bits
GPRS	General Packet Radio Services
GSM	Global System for Mobile communication
HD3	Third harmonic power divided by input power
IC	Integrated Circuit
IIR	Infinite Impulse Response
IF	Intermediate Frequency
I/Q	In-phase and Quadrature signals
IRR	Image Rejection Ratio
IM3	Third inter modulation product
IMD	Inter modulation distortion

INL	Integral Non-Linearity
MFB	Multiple feedback
MFF	Multiple Feedforward
MOS	Metal-Oxide-Semiconductor
NRZ	Non-Return-to-Zero
NTF	Noise Transfer Function
OSR	Over Sampling Ratio
RDE	Retarded Differential Equations
RLS	Retarded Linear Systems
RF	Radio Frequency
RZ	Return-to-Zero
ΣΔM	Sigma Delta Modulator
SFDR	Spurious-Free Dynamic Range
S/H	Sample and Hold
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SPI	Serial Programming Interface
STF	Signal Transfer Function
TL	Transmission Line
TL-ΣΔM	Transmission Line Sigma Delta Modulator
UMTS	Universal Mobile Telecommunications System
VDSL	Very High-Speed Digital Subscriber Line
VLSI	Very Large Scale Integration
WCDMA	Wideband Code Division Multiple Access

WLAN	Wireless Local Area Network

Introduction

The semiconductor electronics industry has achieved an explosive growth over the last few decades since the invention of monolithic integrated circuits (ICs) in the early 1960's. This progress is a direct consequence of rapid advances in information technologies and large-scale system design. The use of ICs in high-performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. A number of different IC fabrication technologies are available to us. Because of its intrinsic feature in low-power consumption, low noise margins, and ease of design, CMOS emerged as the dominant Very-Large-Scale Integration (VLSI) IC technology and can be regarded as the main driver for semiconductor device scaling. Nowadays, CMOS VLSI ICs are widely used to develop RAM chips, microprocessor chips, digital signal processor chips, application specific integrated circuits, and system-on-chip design solutions. The continuous introduction of new VLSI CMOS products with the enhanced performance, smaller feature sizes, lower energy consumption per binary transition, faster transistor switching speed, and lower cost has revolutionized the existing market as well as created new commercial opportunities with intention to further dominate the market [Wes92].

One of the main applications where CMOS technology is used is in wireless communication systems. In most of these applications, the "physical" information comes as analog signals. Therefore, these systems require Analog-to-Digital Converters (ADC) as long as Digital-to-Analog Converters (DAC) to connect with the "real world".

The application of digital techniques to process analog modulated RF signals in radio receivers requires high linearity and high-resolution ADCs. In portable applications these converters must have an extremely low-power consumption to allow a long standby time. In low-cost signal processing applications these converters are combined with a digital signal processing system onto a single chip. Today digital signal processing systems use advanced CMOS technologies requiring the ADC to be implemented in the same (digital) technology. Such an implementation requires special circuit techniques [Pla97].

These converters contain both digital and analog circuitry, and their speed and accuracy is usually limited by that of the analog components. As the speed and accuracy of the internal Digital Signal Processing (DSP) increases, the corresponding requirements on these converters also become harder to meet. Also, while state-of-the-art IC processes help with the design of

faster analog as well as digital circuits, they are detrimental rather than helpful in meeting the analog accuracy specifications due to their reduced dimensions and supply voltages [Moo99].

There are two main architectures for communication receivers which perform a digital demodulation. One of them is based on analog demodulation to the base band and digitization of the I/Q low pass components. For this purpose, Sigma-Delta Modulators (ΣΔM) have been used extensively. Another possible choice is to digitize the band pass signal at the output of the IF stage in a superheterodyne receiver. In that case, subsampling pipeline ADCs are the most common option although Bandpass Sigma-Delta modulators (BP-ΣΔM) are another alternative. Bandpass ΣΔMs have considerably evolved [Sch06], [Luh06] since its conception [Pau]. Compared with a receiver with base band A/D conversion, a receiver with a bandpass A/D converter at IF has the advantages of being free from interferences such as DC offset, flicker noise, LO leakage and allows digital I/Q demodulation. Bandpass ΣΔMs can be implemented with discrete-time (DT) circuits, using switched capacitors (SC) or continuous-time (CT) circuits, usually using g_m-C or LC resonators. Switched capacitor ΣΔMs are able to produce robust performance, but only at low speed. The major drawback of a high speed SC-ΣΔM is the settling time of the SC filter, which requires the opamps to have a very large bandwidth. On the other hand, CT-ΣΔMs are able to operate at much higher sampling frequencies compared with their SC counterparts. However, conventional CT-ΣΔMs implementations are limited by effects such as clock jitter, low resonator Q or feedback loop delay.

Motivation and objectives of the thesis

A LC resonator was the key component of classical bandpass CT-ΣΔMs [Sch96] [Tro93]. Transmission lines are used as replacement of a LC resonator at high frequencies in RF technology. The original idea of the thesis was to exploit this analogy between a LC resonator and a transmission line, because it seemed compelling that transmission lines could improve bandpass CT-ΣΔMs. In the development of such bandpass converters, the author has found that the mathematical modeling of a transmission line ΣΔM leads to a completely new family of ΣΔMs.

The main advantage of using transmission lines instead of LC or gm-C resonators in a ΣΔM is that the system behavior resembles more to a discrete time modulator than a continuous time modulator, inheriting its robustness. Yet, it uses continuous time circuitry without

switches or opamp settling constraints. In particular, building a band-pass ΣΔM with the approach presented in this thesis, benefits from the high Q factor of transmission lines, allows sub-sampling of the input [Kap05], permits a fixed loop delay [Her04] and has a smaller clock jitter sensitivity than that of an equivalent CT solution [Her03]. Moreover, the I and Q paths of a quadrature ΣΔM may be time multiplexed through a single loop filter if it is implemented with transmission lines [Ree07], eliminating any mismatch.

On the other hand, to fully seize the properties of transmission line bandpass ΣΔMs, we would need to integrate the transmission lines together with the associated active elements in a single chip. This is nowadays only possible at very high frequencies. The demonstration circuits that we present in this thesis operate at a sampling rate of hundreds of megahertz and therefore require off-chip coaxial transmission lines.

A full integration of the transmission lines in a chip could be possible, but the technological aspects of such integration are beyond the scope of this thesis. In this work we have preferred to focus on the theoretical development of the transmission line ΣΔMs and their applications, which is a preliminary step before fully integrated solutions can be implemented as competitive options for the market. However, we believe that the advantages of transmission line ΣΔMs to implement data converters at very high frequencies may motivate more research on the field, especially in the achievement of a full integrated solution.

As a consequence, the main objectives that we have targeted for this thesis are:

- To develop the basic mathematical theory that permits to design a ΣΔM using continuous time delays (Chapter 2).
- To make a survey of the possible implementations alternatives for such modulators (Chapter 3)
- To analyze the advantages and implementation problems of ΣΔMs using continuous time delays implemented with transmission lines (Chapter 4).
- To validate experimentally the concepts developed in the thesis with three demonstration chips (Chapters 5, 6 and 7).

Structure of the thesis

This document is divided into two main blocks. The first block comprises the theoretical modeling and the analysis of the implementation issues of transmission lines ΣΔMs. The second block comprises the experimental work showing the design details and measurements of the three demonstration chips. The structure of the document is shown in the following diagram:

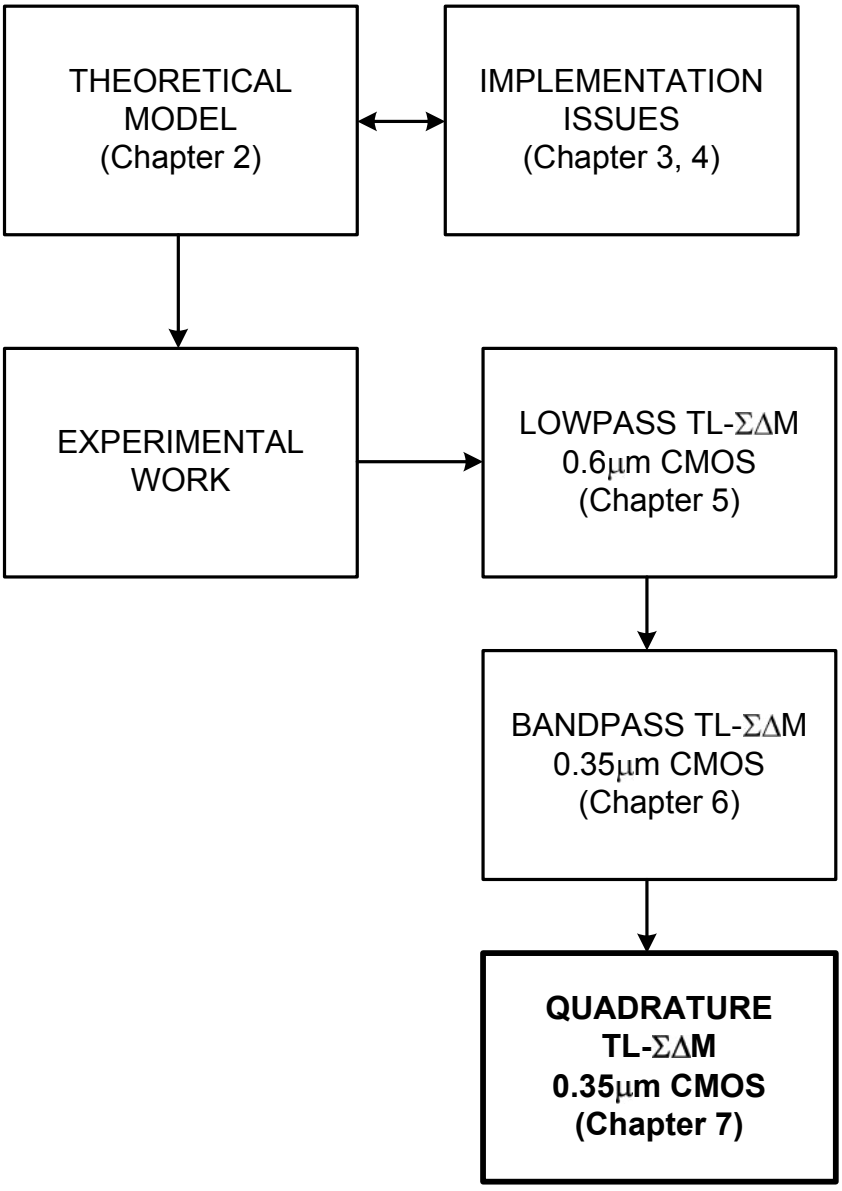

Figure I.1. Structure of the document.

CHAPTER 1
Introduction to Sigma-Delta A/D Converters for Radio Receivers

1.1 Introduction

The Sigma-Delta (ΣΔ) ADC is the converter of choice for modern voice band, audio, and high-resolution precision industrial measurement applications. The highly digital architecture is ideally suited for modern fine-line CMOS processes, thereby allowing easy addition of digital functionality without significantly increasing the cost. Because of its widespread use, it is important to understand the fundamental principles behind this converter architecture.

The ΣΔ ADC architecture had its origins in the early development phases of pulse code modulation (PCM) systems—specifically, those related to transmission techniques called delta modulation and differential PCM [Max91]. Delta modulation was first invented at the ITT Laboratories in France by E. M. Deloraine, S. Van Mierlo, and B. Derjavitch in 1946 [Del46]. The principle was "rediscovered" several years later at the Phillips Laboratories in Holland, whose engineers published the first extensive studies both of the single-bit and multi-bit concepts in 1952 and 1953 [Jag52], [Weg53].

In 1954 C. C. Cutler of Bell Labs filed a very significant patent which introduced the principle of oversampling and noise shaping with the specific intent of achieving higher resolution [Cut54]. His objective was not specifically to design a Nyquist ADC, but to transmit the oversampled noise-shaped signal without reducing the data rate. Thus Cutler's converter embodied all the concepts in a ΣΔ ADC with the exception of digital filtering and decimation which would have been too complex and costly at the time using vacuum tube technology.

Occasional work continued on these concepts over the next several years, including an important patent of C. B. Brahm filed in 1961 which gave details of the analog design of the loop filter for a second-order multibit noise shaping ADC [Brah65]. Transistor circuits began to replace vacuum tubes over the period, and this opened up many more possibilities for implementation of the architecture.

In 1962, Inose, Yasuda, and Murakami elaborated on the single-bit oversampling noise-shaping architecture proposed by Cutler in 1954 [Ino62]. Their experimental circuits used solid state devices to implement first and second-order ΣΔ modulators. The 1962 paper was followed by a second paper in 1963 which gave excellent theoretical discussions on oversampling and noise-shaping [Ino63]. These two papers were also the first to use the name delta-sigma to describe the architecture. The name delta-sigma stuck until the 1970s when AT&T engineers began using name sigma-delta. Since that time, both names have been used; however, sigma-delta may be the more correct of the two.

It is interesting to note that all the work described thus far was related to transmitting an oversampled digitized signal directly rather than the implementation of a Nyquist ADC. In 1969 D. J. Goodman at Bell Labs published a paper describing a true Nyquist ΣΔ ADC with a digital filter and a decimator following the modulator [Goo69]. This was the first use of the Σ-Δ architecture for the explicit purpose of producing a Nyquist ADC. In 1974 J. C. Candy, also of Bell Labs, described a multibit oversampling ΣΔ ADC with noise shaping, digital filtering, and decimation to achieve a high resolution Nyquist ADC [Can74].

The IC ΣΔ ADC offered several advantages over the other architectures, especially for high resolution, low frequency applications. First and foremost, the single-bit ΣΔ ADC was inherently monotonic and required no laser trimming. The ΣΔ ADC also lent itself to low cost foundry CMOS processes because of the digitally intensive nature of the architecture. Since that time there have been constant streams of process and design improvements in the fundamental architecture proposed in the early works cited above.

Nowadays, the current explosion of interest in the realization of mixed-signal systems on chip using VLSI technologies has motivated the use of oversampling ΣΔ ADCs to implement the front-end of such systems. This type of ADCs, composed of a low-resolution quantizer embedded in a feedback loop, uses oversampling (a sampling frequency much larger than the Nyquist frequency) to reduce the quantization noise and ΣΔ modulation [Ino62] to push this noise out of the signal band. The combined use of redundant temporal data (oversampling) and filtering (ΣΔ modulation) results in high-resolution, robust ADCs, which have lower sensitivity to circuitry imperfections and are more suitable than traditional Nyquist-rate ADCs for the implementation of A/D interfaces in a standard CMOS technology.

The efficiency of ΣΔ ADCs has been demonstrated in a large number of ADC Integrated Circuits (ICs) for digitizing lowpass signals with diverse bandwidths and applications [Nor97]. Recently, the principle of ΣΔ modulation has been extended to bandpass signals, leading to a new type of ΣΔ ADCs, named Band Pass ΣΔ ADC (BPΣΔ-ADC) [Sch89], which are especially suited to convert bandpass signals with a narrow bandwidth. This has an obvious application at the front-end of modem wireless communication systems such as mobile phones, digital radio receivers, etc.

1.2 Analog-to-digital interfaces for digital radio receivers

A Radio Frequency (RF) receiver is a system that extracts a desired low-power signal (typically 1μW) in the presence of other noisy and higher power (30-60 dB) interfering signals of the RF electromagnetic spectrum. The performance of an RF receiver is characterized by two figures [Viz95], [Raz98]: *sensitivity* and *selectivity*. The former measures the ability to detect signals in the absence of any interference other than noise, while the latter characterizes the capacity of the receiver to discriminate between the desired signal and large adjacent-channel interferers [Ros00].

Fig. 1.1 shows the block diagram of an analog *superheterodyne* RF receiver composed of three fundamental parts [Hay94]:

a) The RF section, where after filtering and amplifying, the incoming RF signal is translated to a fixed Intermediate Frequency (IF) through the combination of a mixer and a Local Oscillator (LO) (of adjustable frequency). As the sensitivity of the superheterodyne RF receiver is primarily dominated by the noise of this stage, a Low-Noise Amplifier (LNA) is normally used (see Fig.1.1) to reduce the noise contributions of subsequent stages in the receiver.

b) The IF section, where the IF signal is filtered, amplified and downconverted to baseband. The selectivity of the receiver is mainly determined by the channel select filtering performed at this stage. This is because in practice it is easier to achieve high-Q bandpass filters centered at IF (typically in the MHz range) than at RF (in the GHz range).

c) The demodulation section, which retrieves the information from the modulated carrier (demodulation process).

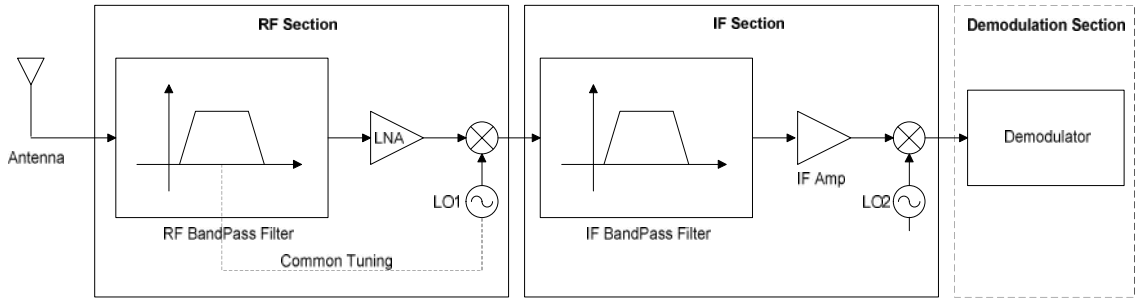

Figure 1.1. Analog RF superheterodyne receiver.

In recent years, the market of digital RF communication portable devices (mobile phones, digital AM/FM radio receivers, wireless LANs ...) is rapidly expanding with the development of new services and applications. On the one hand, the variety of new applications and devices has led to the proliferation of a large number of communication standards with different modulation schemes, carrier frequencies, channel bandwidths, dynamic range requirements, etc. On the other hand, consumers demand low-cost, low-power, and small form devices that satisfy those communication requirements.

This market demand together with the continuous scaling of CMOS technologies makes it possible to integrate a RF receiver onto a single chip with two main objectives. On the one hand, increasing integration will reduce the receiver cost and the power dissipation. On the other hand, aggressive utilization of VLSI technology enables the combined integration of an ADC along with the front-end stages of the receiver. In this manner, the back-end signal processing (channel-selection and demodulation) can be shifted from the analog into the digital domain. This offers two main advantages. First, to take full advantage of the smaller geometries by reducing the die size, it is desirable to perform most RF receiver functions using digital circuits, which, unlike the analog circuits, scale with technology. Second, Digital Signal Processing (DSP) simplifies the implementation of programmable filters, thus allowing the adaptability of the RF receiver to multiple communication standards in different countries [Abi95].

Fig.1.2 shows the ideal block diagram of a digital RF receiver [Fel98]. In this approach, the RF signal is directly digitized by the ADC. Hence, the channel selection and demodulation process is performed in the digital domain. Unfortunately, the receiver of Fig.1.2 is unrealizable because it would require realizing the A/D conversion of a signal at 900MHz-2.5GHz (depending on the carrier frequency) with accuracy of 14-18bits. Hence, a more realistic digital radio receiver would contain an Analog Signal Processing (ASP) section including signal conditioning, i.e.: frequency translation, amplification and filtering.

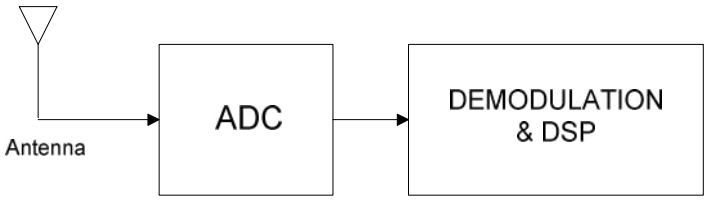

Figure 1.2. Ideal digital RF receiver.

The implementation of these analog functions can be realized in different manners resulting in several RF receiver architectures. Fig.1.3 shows the most significant ones [Raz98]. Fig.1.3.a is a *digital superheterodyne* receiver, where the signal is first down-translated to IF and then to baseband where it is digitized and demodulated. This is the more conventional architecture. However, it is not appropriate for fully-integrated RF receivers because high-frequency high-Q bandpass filters (in both the RF and the IF sections) are required.

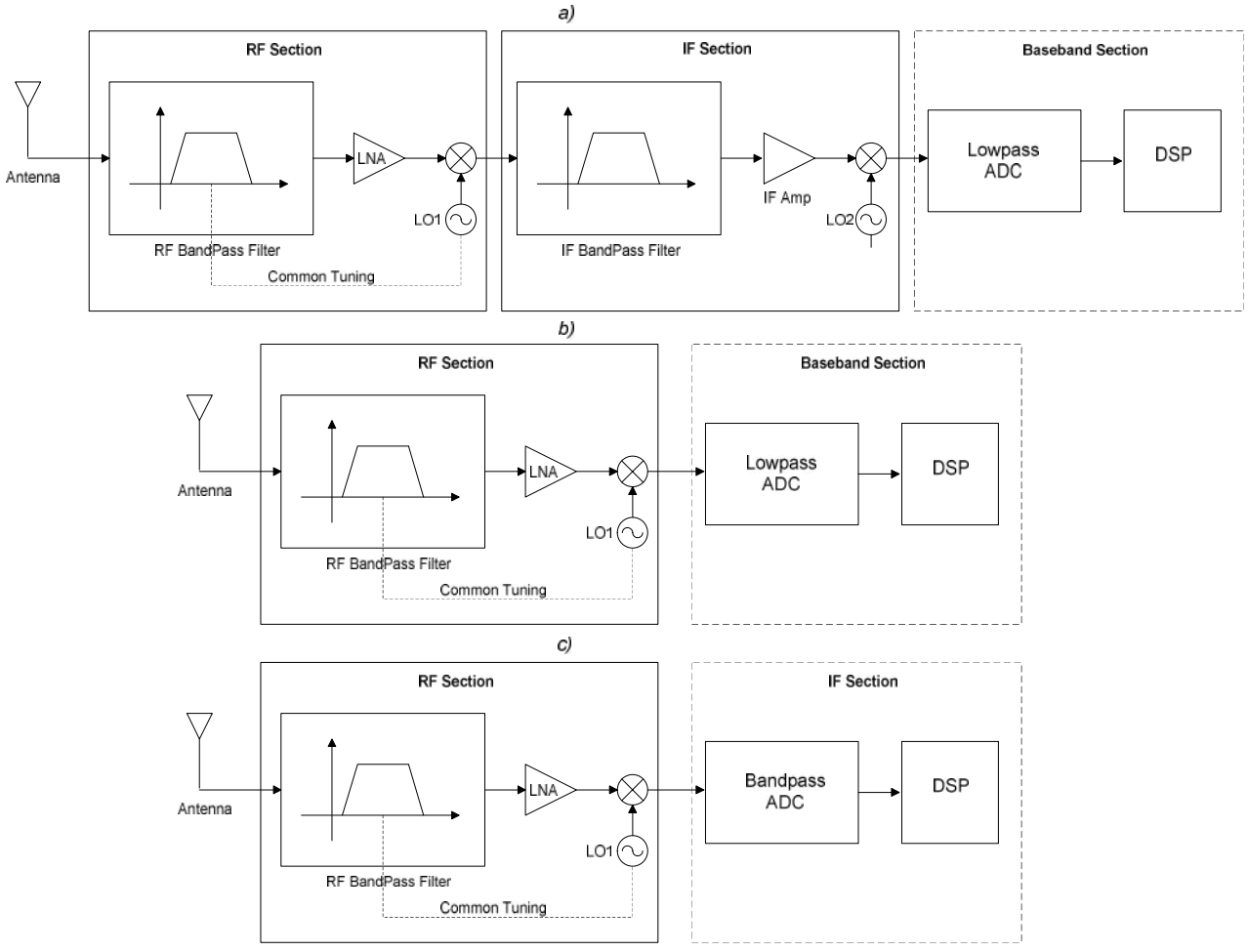

Figure 1.3. Digital RF receivers. a) Superheterodyne. b) Direct conversion. c) IF conversion.

Fig. 1.3.b shows the block diagram of a *direct conversion* receiver. In this architecture, the RF signal is mixed-down directly to baseband where is digitized. This approach is more suited to integration than the superheterodyne because it eliminates the IF section. Hence, only

off-chip RF filters are required. However, non-idealities of the mixer (offset and flicker noise) can severely degrade the performance of this type of receiver.

Many of the problems arising in the mentioned architectures can be eliminated using the *IF conversion* receiver, shown in Fig. 1.3.c. In this architecture the incoming signal at the antenna is first mixed-down to IF where it is digitized. Hence an ADC capable of digitizing IF bandpass signals, often called bandpass ADC, is required.

In all the architectures shown in Fig.1.3, the ADC is one of the most critical blocks for several reasons. On the one hand, the sensitivity of the digital receiver depends on the accuracy with which the signal is digitized. On the other hand, in some architecture such as the one shown in Fig. 1.3.c, part of the signal channel selection is performed by the ADC itself.

The rest of the chapter is devoted to describing the fundamental principles of Sigma-Delta modulators. This type of converters has been demonstrated to be the optimum solution for digitizing IF signals in a large number of ICs as will be seen in Section 1.4.

1.3 Oversampling ΣΔ Analog-to-Digital Converters

By embedding the quantizer in a feedback loop, it is possible to reduce the inband quantization noise power of an ADC significantly beyond what can be achieved by simply using oversampling. This is the basic principle of ΣΔ converters, introduced by Inose et al. in 1962 [Ino62] [Ros00].

Oversampling ΣΔ ADCs operate with redundant temporal data, obtained using oversampling with low-resolution quantizers (one-bit quantizers in many cases), and apply signal processing techniques (averaging in the simplest case) to combine these temporal data, thus increasing the effective resolution.

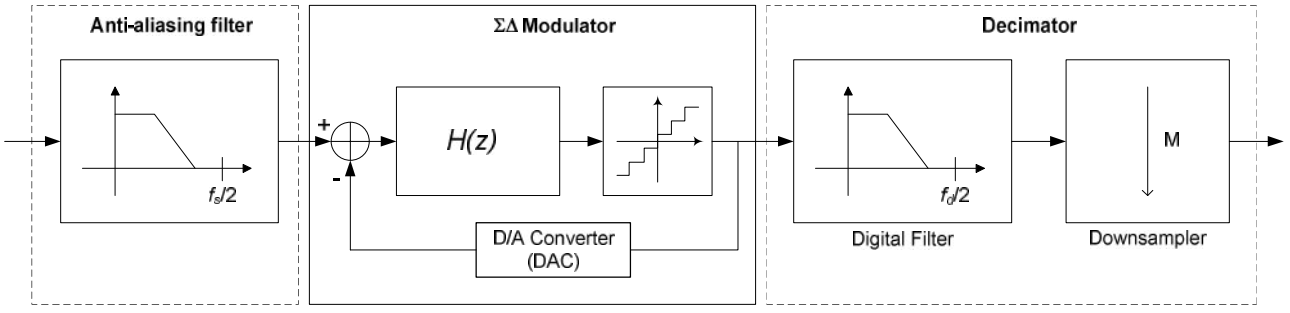

Figure 1.4. Block diagram of an oversampling ΣΔ ADC.

Figure 1.4 shows the block diagram of an oversampling ΣΔ ADC which includes three basic components: an anti-aliasing filtering, a ΣΔ modulator (ΣΔM), and a digital decimator. The signal is oversampled and quantized in the modulator. This block also filters the quantization error, by shaping its PSD in such a way that most of its power lies outside of the signal band, where the error is eliminated by digital filtering. This fact has resulted in the qualifier *noise-shaping*, which is also used to name the ΣΔMs. The modulator output - coded into a reduced number of bits - is passed through the decimator, where, after filtering all the components out of the signal band, data are decimated to reduce f_s down to f_d. The result is the signal coded in a large number of bits and clocked at f_d.

Among the converter blocks, the modulator is the hardest to design since oversampling simplifies the analog anti-aliasing filter requirements and the decimator is a pure digital block whose design can be highly structured and automated [Nor97].

1.3.1 Basic architecture of a ΣΔ modulator

Figure 1.5.a shows the basic scheme of a ΣΔ modulator. Its output, *y*, is subtracted from its input, *x*, which has been sampled at a rate much larger than the Nyquist rate. The result is filtered by *H(z)*, and passed through a quantizer, which usually has a reduced number of levels. If the gain of *H(z)* is high in the interval of the frequency of interest, and low outside of it, the quantization error is attenuated in said band due to the feedback loop.

Assuming that the quantization error (*e*) can be modeled as an additive, white noise source, the modulator in Fig.1.5.a can be viewed as in Figure 1.6. The system of Fig.1.6 is a linear model that has two inputs, *x* and *e*, and one output, *y*, which in the Z-domain can be represented by

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{1.1}$$

where *X(z)* and *E(z)* are the Z-transform of the input signal and quantization noise, respectively; *STF(Z)* and *NTF(Z)* are the respective transfer functions of the input signal and quantization noise. The exact form of both functions will depend on the architecture of the modulator. Analyzing the block diagram of Fig.1.6, yields

$$STF(z) = \frac{H(z)}{1+H(z)} \qquad NTF(z) = \frac{1}{1+H(z)} \tag{1.2}$$

In view of Eq.1.1, we can impose the following conditions to get operative modulators:

$$\left.\begin{array}{l} |STF(z)| = k \\ NTF(z) \to 0 \end{array}\right\} \text{ in the signal band} \tag{1.3}$$

with k being a constant. If $NTF(z) \to 0$ around dc, the modulator is called a *lowpass* ΣΔ modulator (LPΣΔM). Otherwise, if $NTF(z) \to 0$ in a narrow passband centered at a given frequency (usually called notch frequency and represented by f_n), the modulator is called a *bandpass* ΣΔ modulator (BPΣΔM) [Sch89]. Figure 1.5.b illustrates the filtering functions performed for both types of modulators [Ros00].

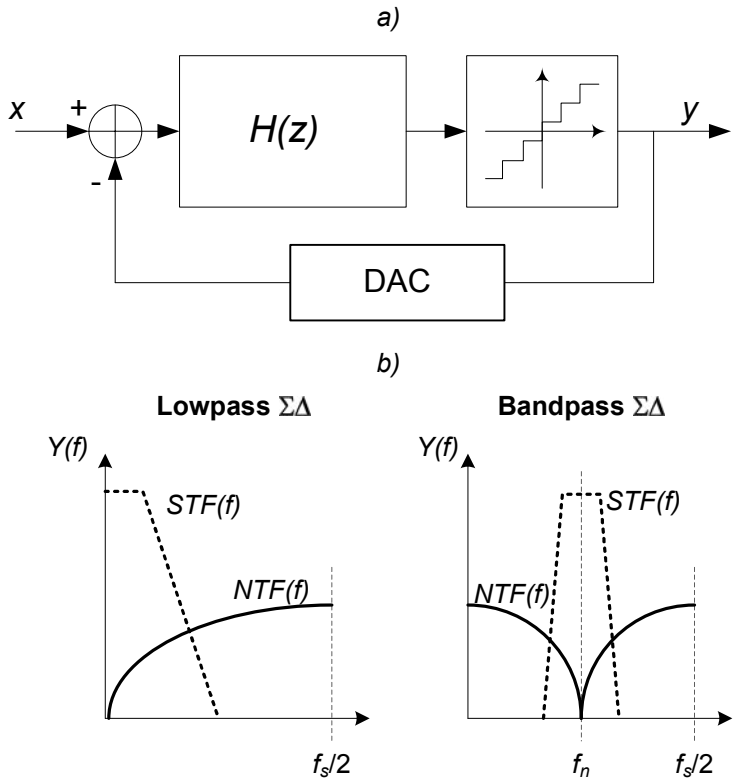

Figure 1.5: a) Basic structure of a ΣΔ modulator. b) Quantization noise filtering.

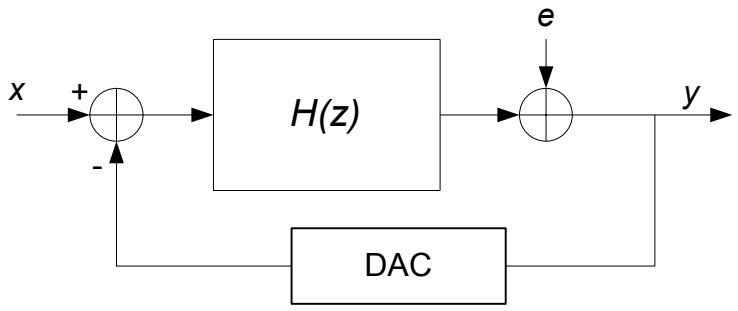

Figure 1.6. Linear model of a ΣΔ modulator.

The PSD of the *shaped* quantization noise is

$$S_Q(f) = S_E(f)\left|NTF(f)\right|^2 \tag{1.4}$$

and the shaped quantization noise in-band power is calculated as follows:

$$P_Q = \int_{SignalBand} S_Q(f)df = \begin{cases} \dfrac{\Delta^2}{6f_s}\displaystyle\int_0^{B_w} |NTF(f)|^2\, df & \text{for LP}\Sigma\Delta\text{Ms} \\ \dfrac{\Delta^2}{6f_s}\displaystyle\int_{f_n-B_w/2}^{f_n+B_w/2} |NTF(f)|^2\, df & \text{for BP}\Sigma\Delta\text{Ms} \end{cases} \tag{1.5}$$

1.3.2 Figures of merit

At this point, it is convenient to define the figures of merit cornmonly used to characterize the oversampling converters.

1.3.2.1 Signal-to-Noise Ratio (SNR)

This is the ratio between the output power at the frequency of a sinusoidal input and the in-band noise power. It is usually given in decibels:

$$SNR = 10\log_{10}\left(\frac{A^2/2}{P_Q}\right) \tag{1.6}$$

where A is the input amplitude of the sinusoide. Note that the SNR monotonously increases with A. However, beyond certain input amplitude, the quantizer input lies outside of the interval which produces the overloading of the latter and consequently a sharp drop is observed in the SNR curve. The value of the SNR at said input amplitude - the maximum value of SNR - is often called the SNR-*peak*.

As will be shown in next Chapters, besides quantization noise, there are other contributions to the in-band noise power due to non-idealities of the circuitry. To take into account all these errors, the Signal-to-(Noise plus Distortion) Ratio (*SNDR*) is normally used.

1.3.2.2 Dynamic Range (DR) and effective number of bits (ENOB)

The dynamic range is defined as the ratio between the output power of the frequency of a sinusoidal input with amplitude X_{FS}, and the output power when the input is a sinusoide of the same frequency, but of a small amplitude, so it cannot be distinguished from noise, that is, with $SNR = 0$dB.

Ideally, the full-scale range of the modulator input is approximately given by that of the quantizer, and hence,

$$DR = 10\log_{10}\left[\frac{(X_{FS}/2)^2}{2P_Q}\right] \tag{1.7}$$

On the other hand, the dynamic range of an ideal *B*-bit Nyquist ADC can be calculated from [Nor97] and Eq.1.7, yielding

$$DR = 10\log_{10}\left[\frac{(2^{B-1})^2\Delta^2}{2P_E}\right] = 10\log_{10}(3\cdot 2^{2B-1}) \tag{1.8}$$

Manipulating this expression yields the effective number of bits or *effective resolution* of an ADC as a function of its DR, expressed in dB, *DR*(dB),

$$ENOB(bits) = \frac{DR(dB) - 1.76}{6.02} \tag{1.9}$$

In general, the above expression is used to express the effective resolution of a ΣΔM in terms of *DR*(dB) if the performance of the modulator is limited by either quantization noise or by circuitry errors.

1.3.3 Bandpass ΣΔ modulators

Digitization of a signal in digital superheterodyne RF receivers (see Fig.1.3.a) can be basically accomplished using the methods represented in Fig.1.7. The first one, shown in Fig.1.7.a uses an analog quadrature mixer [Ped94] to multiply the IF signal by two carriers that are 90° out of phase. As a result, the signal is separated into its lowpass In-phase (I) and Quadrature (Q) components which are digitized by means of two lowpass ADCs.

The other method, shown in Fig.1.7.b, changes the order of the ADC and the mixer and uses only one bandpass ADC. Thus, the signal is first translated to the digital domain and then mixed to the baseband. This is advantageous for several reasons. On the one hand, the I and Q components of the signal are separated in the digital domain rather than in the analog domain as occurs in Fig.1.7.a. Hence, the problems associated with the analog mixer - mismatch between I and Q signal paths, low-frequency noise and de offset - are avoided [Nor97].

Another advantage of the scheme shown in Fig.1.7.b is that it allows channel select filtering, gain control and demodulation to be handled in the digital domain [Jan93], [Sin95]. This results in robust RF receivers with a high degree of programmability, thus allowing a

single software-controlled RF receiver to be employed for multi-standard receivers, being suitable for use in widely varying propagation environments.

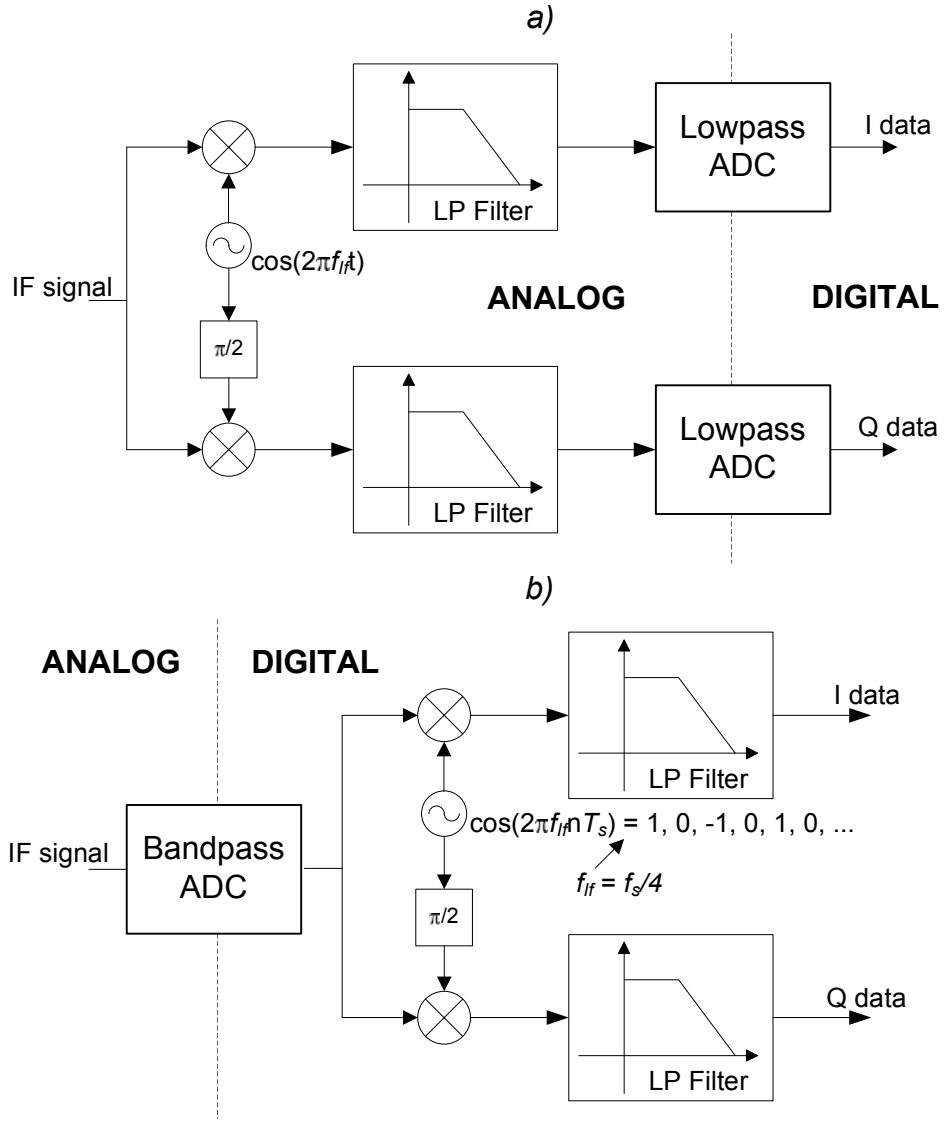

Figure 1.7. Digitizing a signal in a digital superheterodyne RF receiver using: a) Two lowpass ADCs. b) One bandpass ADC.

Digitization of an IF signal can be accomplished either with a wideband Nyquist rate ADC or a BPΣΔ ADC. The use of the latter is the optimum solution for digitizing these signals for several reasons. On the one hand, it is problematic to design high-precision Nyquist-rate converters in modem standard CMOS technologies, optimized for digital circuits, but deficiently modeled for analog interfaces which require precise components. On the other hand, as the bandwidth of IF signals is typically much smaller than the carrier frequency, reducing the quantization noise in the entire Nyquist band becomes superfluous. Instead of that, by using BPΣΔ ADCs the quantization noise power is reduced only in a narrowband around the IF

location (see Fig.1.5.b), thus taking advantage of the higher oversampling ratio[1] and hence yielding a high DR.

1.3.4 Quadrature bandpass ΣΔ modulators

As stated in Section 1.2, in IF-conversion based digital radio receivers the in-coming signal at the antenna, is first mixed down into an IF location where it is digitized and subsequently demodulated. Figure 1.8.a shows a typical block diagram of a digital receiver that employs a multiplier as a mixer.

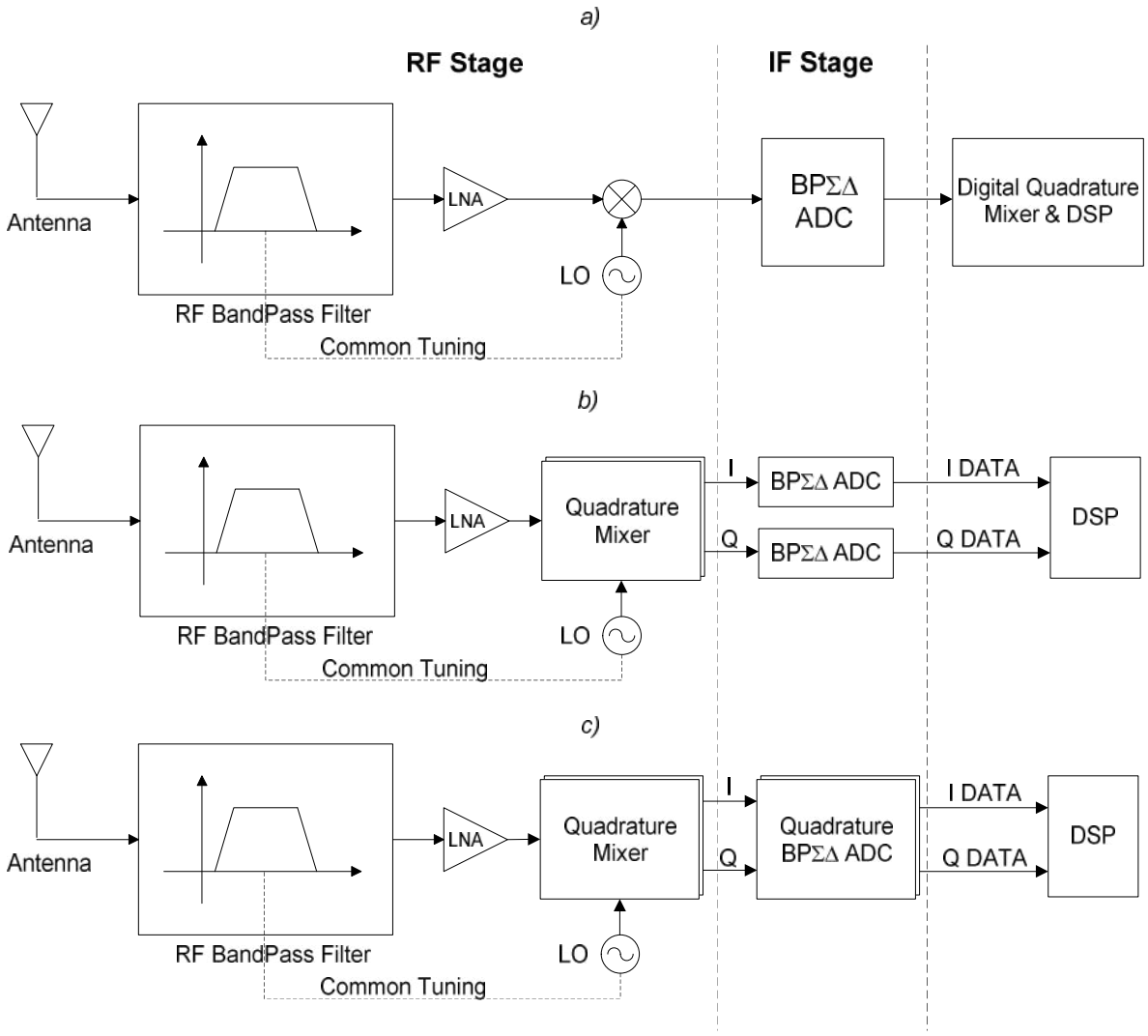

Figure 1.8. RF radio receiver schemes using BPΣΔMs. a) Typical. b) Using quadrature mixer. c) Using quadrature BPΣΔM.

The multiplication in the time domain between the LO and the antenna signal is equivalent to a convolution in the frequency domain. Because of this convolution, spectral

[1] In the case of bandpass signals, the oversampling ratio is defined as [Vau91] OSR = $f_s \lfloor (f_n+B_w/2)/B_w \rfloor / [2(f_n+B_w/2)]$, where B_w is the signal bandwidth, f_n is the centre frequency and $\lfloor x \rfloor$ represents the largest integer not exceeding x.

components at the image frequency (of the signal) are mixed down into the same IF as the desired signal is, thus corrupting the information. This can be avoided if an image-reject filter is used. However, for low-IF frequencies, narrow-band high-Q bandpass filters are required, meaning an increase of the power consumption and forcing us to use off-chip circuitry.

Image-rejection or quadrature mixers [Lee98] overcome this problem by mixing with both a cosine and a sine signal that performs a rejection of the image components. This cancellation effect is only obtained in the ideal case. In practice, a mismatch between both paths of the quadrature mixer will cause undesired image signals to appear at the IF band.

An obvious consequence of the quadrature mixing is that the IF signal is separated into two components: I and Q. Hence, two BP-ΣΔMs are required as illustrated in Figure 1.8.b, which means doubling the required hardware - two BP-ΣΔMs compared to only one BP-ΣΔM used in Fig.1.8.a. This fact motivates finding new strategies that solve the problem of the A/D conversion of both I and Q signals.

Figure 1.8.c shows a scheme that uses a complex, or quadrature, version of a BP-ΣΔM, called quadrature BP-ΣΔM [Jan97]. This type of BP-ΣΔM, which uses complex quantization noise filtering, employs only one ADC to perform directly the conversion of both I and Q mixer outputs.

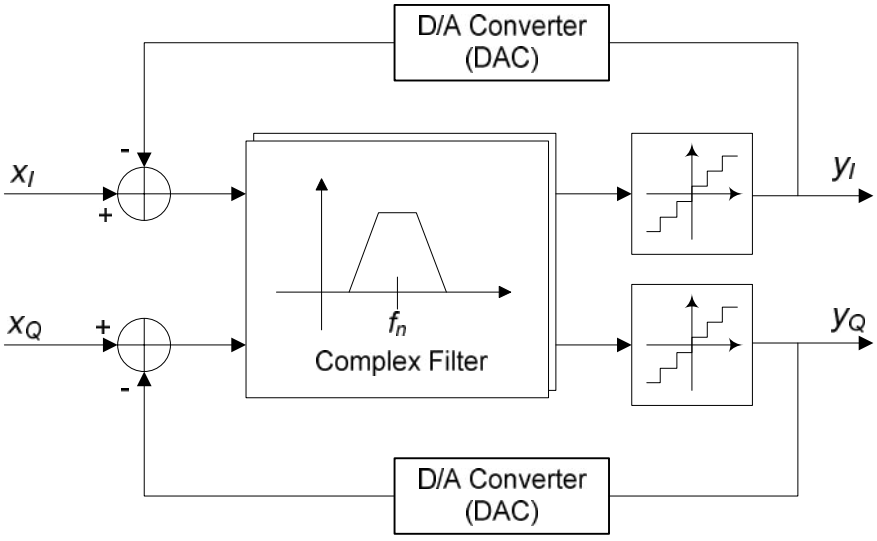

Figure 1.9. Conceptual block diagram of a quadrature BPΣΔM.

Figure 1.9 shows a conceptual block diagram of a quadrature BP-ΣΔM. The main difference with respect to conventional BP-ΣΔMs is the complex bandpass filter embedded in the loop. Thus, the modulator output consists of a pair of high-speed bit streams, one of them representing the real output and the other one the imaginary output. When combined, these

two outputs form a complex digital signal which represents the complex input signal (I and Q components coming from the mixer in an RF radio receiver) and the shaped quantization noise [Ros00].

1.3.5 Continuous-time ΣΔ modulators

The architectures described in earlier sections assumed that the loop filter is of the DT type. In recent years, the increased demand for high-speed ΣΔMs has motivated the development of CT loop filter based ΣΔMs, generically known as continuous-time ΣΔMs (CT-ΣΔMs). This approach offers several advantages. On the one hand, CT filters are much faster than their DT counterparts. On the other hand, it can be shown that CT-ΣΔMs provide an implicit anti-aliasing filter for out-of-band signals at no cost. In contrast, CT-ΣΔMs are more sensitive to clock jitter than DT-ΣΔMs. This is because the internal clock that controls the comparison instant, also controls the rising and falling edges of the DAC output. Hence, clock jitter errors are directly added to the input signal. Another important limitation of CT-ΣΔMs is the excess loop delay contributed by each building block in the modulator loop, which can severely degrade the quantization noise transfer function.

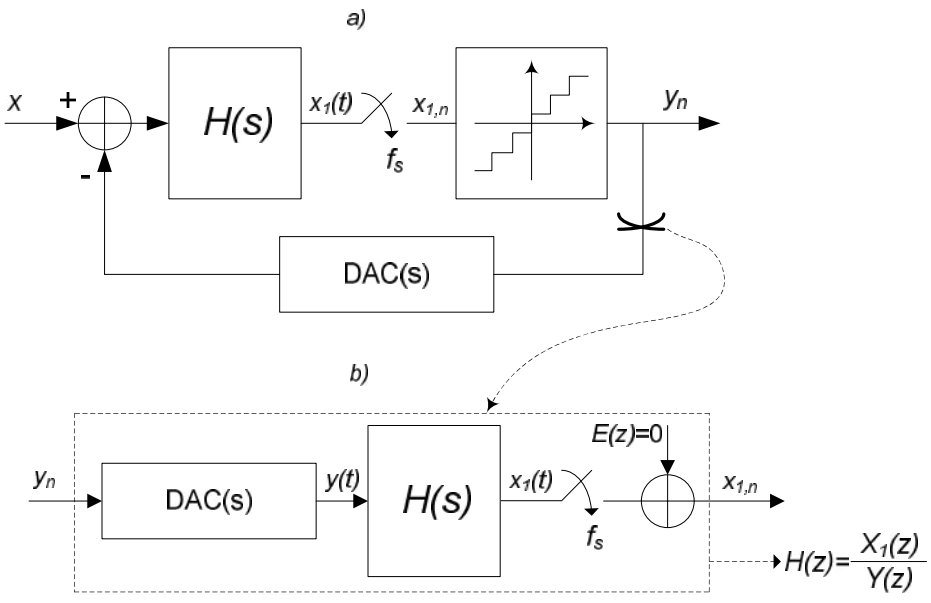

Figure 1.10: Basic architecture of a CT-ΣΔM. (a) Conceptual block diagram. (b) Open loop block diagram.

The architecture of any arbitrary CT-ΣΔM can be generated by applying a DT-to-CT transformation to an original DT-ΣΔM that meets the required specifications. Therefore, much of the knowledge available for DT-ΣΔM can be utilized for synthesizing CT-ΣΔM architectures.

There are different ways of realizing such a DT-to-CT transformation depending on the shape of the DAC impulse response [Sho94].

The block diagram of a conceptual CT-ΣΔM is shown in Figure 1.10. This modulator is internally a DT circuit since there is a S/H circuit inside the loop, just at the quantizer input. This fact makes the overall loop from the output of the quantizer back to its input have a Z-domain transfer function as illustrated in Fig.1.10.b. The equivalent DT loop filter transfer function is [Sho97]:

$$H(z) = Z\left[L^{-1}\left[DAC(s)H(s)\right]\Big|_{t=nT_s}\right] = Z\left[\int_{-\infty}^{\infty} DAC(\tau)h(t-\tau)d\tau\Big|_{t=nT_s}\right] \tag{1.10}$$

where

$$DAC(s) = \frac{e^{-sp_1T_s} - e^{-sp_2T_s}}{s} \tag{1.11}$$

is the transfer function of the DAC, which in the time domain can be expressed as:

$$DAC(t) = \begin{cases} 1 \rightarrow p_1T_s \le t \le p_2T_s \\ 0 \rightarrow otherwise \end{cases} \tag{1.12}$$

Since *DAC(t)* has a pulse waveform, the expression in (1.10) is known as the *impulse invariant transformation*. The parameters p_1 and p_2 determine the DAC pulse type, which can be: Nonreturn-to-Zero (NZ, $p_1 = 0$ and $p_2 = 1$), Return-to-Zero (RZ, $p_1 = 0$ and $p_2 = 1/2$), and Half-delay Return-to-Zero (HRZ, $p_1 = 1/2$ and $p_2 = 1$).

The impulse invariant transformation allows us to obtain an equivalent relation between DT- and CT-BPΣΔMs. Thus, the synthesis process of a CT-BPΣΔM starts from a DT loop filler that satisfies the required specifications and then it is transformed into an equivalent CT filter using Eq.1.10 [Ros00].

However, practical application of the impulse invariant transform may lead to modulators which are very sensitive to circuit impairments. Other design techniques which mix continuous time and discrete time mathematical modeling are used nowadays to design practical CT-ΣΔMs [Pat05] [Mae06].

1.4 State-of-the-art of Quadrature Bandpass ΣΔ ADCs

Considerable research effort pushes toward the realization of fully monolithic and chiefly digital RF transceivers, with the ultimate objective being the implementation of small, inexpensive, low-power communication devices. These devices should be robust, testable, and capable of handling multiple communications standards. Two-path IF architectures and single-path bandpass ΣΔM based architectures (see Fig.1.8.a, Fig.1.8.b) strive to attain these dual goals, but neither effectively achieves both. Quadrature IF receiver architectures have recently been proposed, which, with modern quadrature image-reject mixers and strategic IF placement, offer a viable solution for digital, monolithic receivers. A critical component of such a system - and indeed of any receiver that uses image-reject mixing to alleviate passive filtering requirements - is one that efficiently performs bandpass A/D conversion on quadrature signals.

A quadrature bandpass ΣΔM IC (see Fig.1.8.c) facilitates monolithic digital-radio-receiver design by allowing straightforward "*complex A/D conversion*" of an image-reject mixer's I and Q outputs. Quadrature bandpass ΣΔMs provide superior performance over pairs of real bandpass ΣΔMs in the conversion of complex input signals, using complex filtering embedded in ΣΔ loops to efficiently realize asymmetric noise-shaped spectra.

Quadrature bandpass DT-ΣΔMs with switched-capacitor (SC) architectures sample the signal at their modulator inputs. Therefore, they need *anti-aliasing filters* (AAFs) between the quadrature mixers and the modulator inputs. A quadrature bandpass modulator with continuous time architecture, however, samples the signal with the quantizer inside the modulator and uses the loop filter as an AAF. Therefore, recently, quadrature bandpass CT-ΣΔ ADCs have become very popular because of low power consumption, high-resolution A/D conversion efficiently, high speed and small area with respect to their time-discrete counterparts.

Table 1.1 and 1.2 show a summary of the main quadrature bandpass ΣΔ ADC ICs published to this day. For each of them, the most significant figures are shown, namely: Bandwidth, f_s, f_{IF}, peak SNR, IRR, the power consumption, the characteristics of the fabrication process and the modulator architecture.

The modulators in Table 1.1 and 1.2 cover multiple applications in digital wireless communications, ranging from GPS [Ste02] to digital radio receivers and modern cellular

phones [Swa96] [Jan97] [Jun00] [Oh03] [Pun06] [Bre01] [Hen02] covering commercial standards such as GSM [Ber03] [Ban06] [Esf03], WCDMA [Ber03], GPRS [Ban06], EDGE [Ban06], Bluetooth [Phi03] and WLAN [Yag05] [Ari06]. Also, covering TV tuner standards [Sch06].

As mentioned before, quadrature bandpass CT-ΣΔMs offers some advantages over DT implementations. Papers of Table 1.2 demonstrate that fully-integrated high-performance quadrature bandpass CT-ΣΔMs, with their center frequency at higher IF than DT modulators, can be implemented in standard CMOS technology and their power consumption can be reduced compared to DT implementation while increasing their bandwidth. But in order to make these CT implementations perform well, several innovations are needed.

TABLE 1.1
OVERVIEW OF QUADRATURE BANDPASS DT-ΣΔ ADCS CHIPS

ARTICLE	[Swa96]	[Jan97]	[Jun00]	[Oh03]
Type	DT	DT	DT	DT
Order	4	4	4	2
# Bits	1	1	1	3
Bandwidth (kHz)	200	200	200	200
f_s (MHz)	4	10	13	13
f_{IF} (MHz)	1 (f_s/4)	3.75 (3f_s/8)	4.875	4.875
Peak SNR (dB)	48	62	100	85
IRR (dB)				
Power (mW)	150	130	190	38
Supply (V)	5	5	5	5
Technology	0.8 µm BiCMOS	0.8 µm CMOS	0.6 µm CMOS	0.35 µm CMOS
Application	Digital Radio	Digital Radio	AM/FM radio	AM/FM radio
ARTICLE	[Ber03]	[Mau05]	[Ban06]	[Pun06]
Type	DT	DT	DT	DT
Order	8	2	2	3
# Bits	1	3	1	1
Bandwidth (kHz)	200	200	180	200
f_s (MHz)	100	13	52	6.4
f_{IF} (MHz)	7.5 (3f_s/4)	0.010		DC
Peak SNR (dB)		81	90	60
IRR (dB)		40		75
Power (mW)	36	10	19.9	13.1
Supply (V)	3.3	2.1	2.4	3.3
Technology	0.35 µm CMOS	0.25 µm CMOS	0.09 µm CMOS	0.35 µm CMOS
Application	GSM/WCDMA		GSM/GPRS	GSM

First, in [Sch06] a modification of the feedforward architecture which corrects a sensitivity problem specific to quadrature bandpass ADCs is implemented.

Second, in [Bre01] [Phi03] [Sch06] a timing calibration to ensure accurate placement of the sampling instant relative to the feedback interval is used.

Third, in [Yag05] [Ari06], a Data Weighted Averaging (DWA) algorithm is used in order to compensate the nonlinearity of the internal multibit DAC.

Fourth, [Bre01] [Sch06] employ a simple Dynamic Element Matching (DEM) technique in order to reduce the effects of path mismatch, namely aliasing in the signal band of the mirror images of the signal and of the quantization noise.

TABLE 1.2
OVERVIEW OF QUADRATURE BANDPASS CT-ΣΔ ADCS CHIPS

ARTICLE	[Bre01]	[Ste02]	[Hen02]	[Phi03]
Type	CT	CT	CT	CT
Order	?	2	2	5
# Bits	1	>1	1	1
Bandwidth (MHz)	0.2	2	1	1
f_s (MHz)	21.05	128	100	64
f_{IF} (MHz)	DC	4 (f_s/32)	1 (f_s/100)	0.5 (f_s/128)
Peak SNR (dB)	76	62	56.7	75.5
IRR (dB)	63	32	40	47
Power (mW)	10	14.2	21.8	4.4
Supply (V)	3.3	2	2.7	1.8
Technology	0.35 µm CMOS	0.25 µm CMOS	0.65 µm BiCMOS	0.18 µm CMOS
Application	QPSK-QAM	GPS	AM/FM radio	Bluetooth
ARTICLE	[Esf03]	[Yag05]	[Ari06]	[Sch06]
Type	CT	CT	CT	CT
Order	4	4	2	4
# Bits	1	4	3	4
Bandwidth (MHz)	0.27	23	20	8.5
f_s (MHz)	13	276	320	264
f_{IF} (MHz)	-0.1 (f_s/100)	11.5 (f_s/24)	DC or 10	44 (f_s/6)
Peak SNR (dB)	82	69.9	55.5	77
IRR (dB)	57	45	47.2	50
Power (mW)	4.6	42.6	32	375
Supply (V)	2	1.8	2.5	1.8
Technology	0.25 µm CMOS	0.18 µm CMOS	0.25 µm CMOS	0.18 µm CMOS
Application	GSM	WLAN	WLAN	TV tuner

Additional innovations in [Sch06] include circuit techniques that allow the use of an active-RC resonator to be high despite finite amplifier gain and bandwidth. With these techniques, the realized Q-factors of resonators exceed the design requirement by nearly a factor of 2. Finally, gain scaling is used to extend the ADC's dynamic range without increasing its power consumption.

The work in this thesis aims at designing a quadrature bandpass ΣΔM that shares some of the advantages of DT and CT implementations, using distributed resonators (Transmission Lines) in the loop filter instead of gm-C or LC resonators. For this purpose, two other designs will be studied first, a transmission line LPΣΔM and a transmission line BPΣΔM. The models and techniques described in this thesis are demonstrated through three prototypes:

- A transmission line LPΣΔM in 0.6μm CMOS technology.
- A transmission line BPΣΔM in 0.35μm BiCMOS technology.
- A transmission line Quadrature BPΣΔM in 0.35μm BiCMOS technology.

CHAPTER 2

Introduction to Retarded Linear Systems and its Application to Sigma-Delta Modulators

The classical conception of lumped linear electric networks is based into modeling them as a system of linear differential equations. Continuous time sigma delta modulators (CT-ΣΔMs) follow this approach and their loop filters are represented using the standard state variable notation. This leads to an implementation using a cascade of integrators, following closely the canonical implementation models for continuous linear systems [Hal77]. However, there are other continuous-time linear systems which cannot be fully expressed as a system of linear differential equations and that could be seized to implement a CT-ΣΔM. Specially, those systems which involve delayed versions of the output signal require the concept of retarded differential equations [Hal77]. Practical CT-ΣΔMs are in fact one of these systems when the excess loop delay effects are considered. Also, networks that produce a delay such as electrical transmission lines cannot be modeled only with linear differential equations. We will explore in this chapter the possibilities to use such retarded systems to implement a filter with the aim of replacing a discrete time sigma delta modulator (DT-ΣΔM) loop filter.

2.1 Linear Systems described by Retarded Differential Equations (RDE).

Consider a system with output y(t) described by Eq.2.1:

$$y(t) = \sum_{m=0}^{M} a_m \cdot y(t - T_m) \tag{2.1}$$

This homogeneous equation has a nontrivial solution consisting of a series of complex exponentials:

$$y_r(t) = A_r \cdot e^{k_r t} \tag{2.2}$$

Coefficients A_r and k_r can be computed by solving the following characteristic equation:

$$\sum_{m=0}^{M} a_m \cdot e^{-T_m \cdot k} - 1 = 0 \tag{2.3}$$

and imposing initial conditions. A detailed analysis of Eq.2.3 would show that this characteristic equation may have a numerable or a non numerable number of solutions depending on the delays T_m. There will be a numerable number of solutions if all the delays T_m are an integer multiply of a basic delay T:

$$T_m = m \cdot T \quad m \in N \tag{2.4}$$

The reason for this is that if Eq.2.4 holds, Eq.2.3 represents a polynomial of order M and hence has only M roots which are periodic and hence numerable. We will restrict to this case, where for every root of Eq.2.3 we have a series of periodic solutions of the form:

$$y(t) = \sum_{m=0}^{M-1} A_m \cdot \sum_{n=-\infty}^{\infty} a_{n,m} \cdot e^{j\frac{2\pi}{T}n} \tag{2.5}$$

The case where the delays T_m are related by irrational factors is a problem of complex nature because then Eq.2.3 has an countable infinite number of non-periodic solutions. We will consider this situation as a non desirable mismatch effect. The author has not found any ΣΔM with irrational delays that produces useful results. However, linear systems with infinite non

harmonic eigenvalues could also yield useful ΣΔMs if properly designed.

We are going to use the linear system represented by Eq.2.1 to implement a continuous time filter. To do so, we will modify this equation to provide an excitation by an external signal x(t):

$$y(t) = \sum_{m=1}^{M} b_m \cdot y(t - mT) + \sum_{r=0}^{R} a_r \cdot x(t - rT) \tag{2.6}$$

We prove in chapter 2 annex that y(t) may be expressed as the following series:

$$y(t) = \sum_{k=0}^{\infty} h_f[k] \cdot x_f(t - kT) \tag{2.7}$$

The solution expressed in Eq.2.7 corresponds with the conventional expression of a linear system output as the convolution sum of its impulse corresponds with the input, where such impulse response is composed of delayed Dirac delta functions.

2.2 Equivalence between continuous and discrete time linear systems

Figure 2.1 depicts two discrete time linear systems $H_{d1}(z)$ and $H_{d2}(z)$ driven by the same sequence v[n]. In Fig.2.1, system $H_{d1}(z)$ is a purely discrete time system. System $H_{d2}(z)$ is the combination of a pulse shaper p(t) that produces a pulse train weighted by sequence v[n] at a rate 1/T, a continuous time system $H_a(s)$ and a sampler S. Both systems $H_{d1}(z)$ and $H_{d2}(z)$ will be equivalent if for any input v[n], the two output sequences $u_1[n]$ and $u_2[n]$ are coincident.

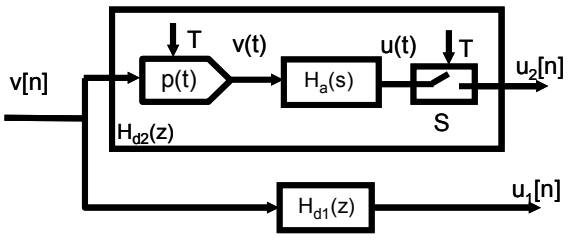

Figure 2.1. Equivalence between discrete and continuous time linear systems.

Discrete time system $H_{d1}(z)$ may be represented by its impulse response $h_{d1}[n]$. We are going to study the case where system $H_a(s)$ belongs to the class of systems represented by Eq.2.7. We may replace the value of x(t) in Eq2.7 by the pulse train v(t) at the input of $H_a(s)$ in

Fig.2.1:

$$v(t) = \sum_{m=0}^{\infty} v[m] \cdot p(t - mT)$$
$$u(t) = \sum_{k=0}^{\infty} h_a[k] \cdot v(t - kT) \tag{2.8}$$
$$u(t) = \sum_{k=0}^{\infty} \left(\sum_{m=0}^{\infty} h_a[m] \cdot v[k - m] \right) \cdot p(t - kT)$$

We may define the time instants when S samples u(t) as:

$$T[n] = nT + \Delta T \quad \Delta T < T \tag{2.9}$$

where ΔT will be a time shift smaller than T, typically $T/2$. The sequence of values at the output of the sampler will be:

$$u_2[n] = \sum_{k=0}^{\infty} \sum_{m=0}^{\infty} h_a[m] v[k - m] \cdot p((n - k)T + \Delta T) \tag{2.10}$$

On the other hand we know that the output of the discrete time system $H_{d1}(z)$ may be expressed as:

$$u_1[n] = \sum_{m=0}^{\infty} h_{d1}[m] \cdot v[k - m] \tag{2.11}$$

If we want u_1 and u_2 to be coincident, we could impose the following two conditions:

$$p(t) = \begin{cases} \neq 0 & t \in [0, T) \\ 0 & t \notin [0, T) \end{cases} \tag{2.12}$$

$$h_a[n] = \frac{1}{p(\Delta T)} \cdot h_{d1}[n] \tag{2.13}$$

Equation 2.12 defines $p(t)$ as any pulse of duration T. As a consequence of Eq.2.12, $p(t)$ in Eq.2.10 will take only two values:

$$p((n - k)T + \Delta T) = \begin{cases} p(\Delta T) & n = k \\ 0 & n \neq k \end{cases} \tag{2.14}$$

And then, Eq.2.10 may be rewritten as:

$$u_2[n] = p(\Delta T)\sum_{m=0}^{\infty} h_a[m]v[n-m] = \sum_{m=0}^{\infty} h_{d1}[m]v[n-m] \tag{2.15}$$

Condition Eq.2.15 completes the proof that $H_{d1}(z)$ and $H_{d2}(z)$ will be equivalent up to a gain factor.

In practice, it is not necessary to impose the matching of impulse responses to obtain equivalent systems. A simpler system replacement rule can be inferred by comparing Eq.2.6 with the difference equation that describes any digital IIR filter:

$$y[n] = \sum_{m=1}^{M} \beta_m \cdot y[n-m] + \sum_{r=1}^{R} \alpha_r \cdot x[n-r] \tag{2.16}$$

It is clear that the only requirement to implement equivalent discrete time systems is to use the same coefficients in Eq.2.6 and Eq.2.16:

$$b_m = \beta_m \quad a_r = \alpha_r \quad p(\Delta T) = 1 \tag{2.17}$$

This means that we may replace any unit delay z^{-1} in the flow graph that expresses a discrete time filter $H_d(z)$ by a continuous time delay T and the resulting continuous time system $H(e^{-sT})$ will be directly useable as system $H_a(s)$ in the system equivalence of Fig.2.1 except for a gain factor $p(\Delta T)$.

2.3 Properties of Retarded Linear Systems (RLS)

We will use the equations and conclusions of previous sections to define some properties of the RLS.

2.3.1 Sampling point insensitivity in Retarded Linear Systems

An interesting property of the implementation of system $H_{d2}(z)$ (see section 2.2) is that it may be made insensitive to clock jitter and time offsets in the sampling point of the clock applied to the sampler that generates *p(t)*, yet $H_a(s)$ will still be a continuous time system. We will define *p(t)* as a zero order hold pulse with a variable placement of its rise and fall edges within the n-th interval of duration *T*:

$$p(t,n)=\begin{cases}1 & t\in\left[(n-1)T+\Delta_r[n],nT-\Delta_f[n]\right)\\ 0 & t\notin\left[(n-1)T+\Delta_r[n],nT-\Delta_f[n]\right)\end{cases}$$
$$0\le\Delta_f[n]+\Delta_r[n]<T \tag{2.18}$$

With such a time varying pulse, we have tried to model the effect of a clock with period jitter but whose accumulated jitter never produces a cycle slip. The pulse defined in Eq2.18 always has a duration equal or less than T. This would be the usual situation in a CTΣΔM driven by a PLL clock with zero frequency error. We may also introduce a timing error in the sampling clock such that Eq.2.9 is transformed into:

$$T[n]=nT+\Delta T[n]\quad \Delta T[n]<T \tag{2.19}$$

With these definitions we may rewrite Eq.2.10 as follows:

$$u_2[n]=\sum_{k=0}^{\infty}\sum_{m=0}^{\infty}h_a[m]v[k-m]\cdot p\left((n-k)T+\Delta T[n],n\right) \tag{2.20}$$

The following condition will allow desensitizing the system from clock jitter:

$$\forall k\le n\begin{cases}T-\Delta_r[k]<\Delta T[n]\\ T-\Delta_f[k]>\Delta T[n]\end{cases}\Rightarrow$$
$$\Rightarrow p\left((n-k)T+\Delta T[n],n\right)=\begin{cases}1 & n=k\\ 0 & n\neq k\end{cases} \tag{2.21}$$

If Eq.2.21 is met, then we may write Eq.2.20 as:

$$u_2[n]=\sum_{m=0}^{\infty}h_a[m]v[n-m]=\sum_{m=0}^{\infty}h_{d1}[m]v[n-m] \tag{2.22}$$

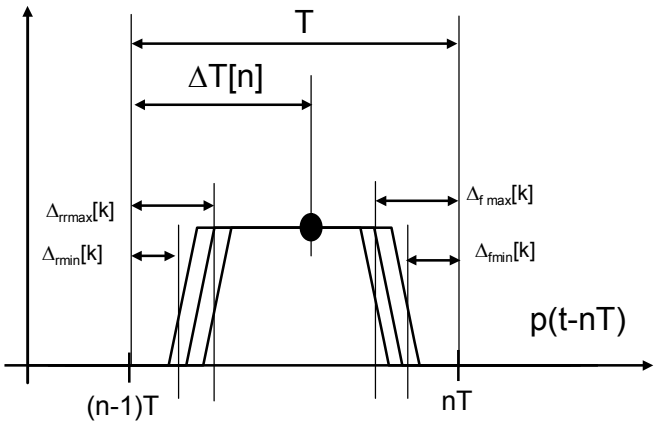

Figure 2.2. Geometric conditions for clock jitter insensitivity.

Then, Δ_r[n], Δ_f[n] and ΔT[n] do not affect the system equivalence. Thinking on a possible practical implementation of a discrete system with continuous time delays, the equivalent discrete time system would be insensitive to clock jitter or sampling time offsets as long as the timing errors were bounded as in Eq.2.21. This situation is depicted in an example in Figure 2.2.

2.3.2 Conservation of the State Variables at the sampling points

As long as Ha(s) in Fig.2.1 is composed only by equal delays and linear operators, it may be proven [Hal77] that its impulse response will be causal and composed by a number of delta functions, scaled by a sequence h[k] and shifted in time by multiples of the basic delay T:

$$h(t) = \sum_{k=0}^{\infty} h[k] \cdot \delta(t - kT) \tag{2.23}$$

The response u(t) of the system in Fig.2.1 to an input signal x(t), may be computed by the following convolution integral:

$$\begin{aligned} u(t) &= \int_0^t v(\tau) \cdot h(t-\tau) \cdot d\tau = \sum_{k=0}^{M} h[k] \cdot v(t - k \cdot T), \\ M &= Int\left(\frac{t}{T}\right) \end{aligned} \tag{2.24}$$

where Int( ) denotes the integer part. If we sample y(t) at t=nT_m, the output sequence will be:

$$u[n] = \sum_{k=0}^{n} h[k] \cdot v(nT - kT) \tag{2.25}$$

Sections 2.2 and 2.3.1 and Eq.2.25 reveal an interesting property of the RLS: the sample y[n] at t=nT_m *only* depends on the past samples of x(t) at t=0,T_m,...nT_m. Hence, we are not concerned on the actual shape of x(t), only on its values at the sampling points. This also means that the state variables of both systems of Fig.2.1 are equal in the sampling points, although at a time different than the sampling points the state variables may have different values.

2.3.3 Subsampling of the input in Retarded Linear Systems

The system $H_{d1}(z)$ of Fig.2.1 is a discrete time system, where the sampler S is placed

before the filter H[z]. Hence, if we apply a band-limited signal x(t) to its input, the discrete time system will not distinguish whether this signal is below or above the Nyquist frequency. This is what is called *"subsampling of the input"* in discrete time systems.

The continuous time system Ha(s) of Fig.2.1 is a retarded system that uses delays in its flow graph, and hence its poles are periodic. Then if we sample a signal above the Nyquist frequency, using a sampler placed after the filter, this topology is able to subsample, same as in a discrete time system. This effect is due to the periodic poles of the retarded filter. However, in a continuous time filter, where the poles are not periodic, if we sample a signal above the Nyquist frequency, using a sampler placed after the filter, this subsampling effect will not occur.

The properties of a RLS explained up to now have important consequences that will be explained in next sections, and makes the continuous time system Ha(s) of Fig.2.1 to share the properties of both discrete and continuous time system.

2.3.4 Equivalent integrators

Figure 2.3 represents the block diagram of two continuous time feedback systems that use delay elements instead of derivation or integration.

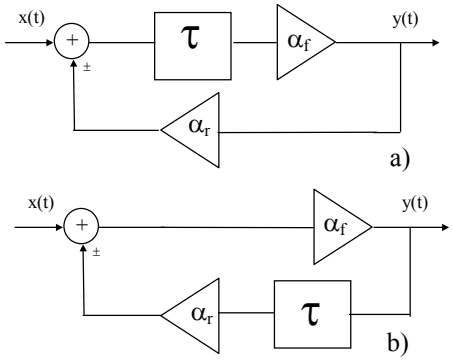

Figure 2.3. Block diagram of two possible resonator configurations based in delay elements.

In Fig.2.3.a, the input signal x(t) is applied to a delay element with delay τ. Constant α_f could model the effect of the energy dissipation in the transmission media employed in a practical implementation of the delay element. The delayed version of the input is fed back to the delay element with a gain α_r and two possible polarities. This system may be characterized by the equation:

$$y(t) = \alpha_f \left(x(t-\tau) \pm \alpha_r \cdot y(t-\tau) \right) \tag{2.26}$$

This system is linear and time invariant but its kernel is singular [Kwa91]. Hence, it does not belong to the class of systems that are fully described by its gain, pole and zero locations. As will be shown later, its transfer function has a countable infinite number of poles. The transfer function of this system resembles that of a resonator and is:

$$H_a(s) = \frac{Y(s)}{X(s)} = \frac{\alpha_f \cdot e^{-s\tau}}{1 \mp \alpha_r \cdot \alpha_f \cdot e^{-s\tau}} \tag{2.27}$$

When the feedback from the delay element is subtracted at the input we will designate the transfer function as $H_{a1}(s)$. The poles of $H_{a1}(s)$ will be the solutions of :

$$\begin{aligned} &1 + \alpha_r \cdot \alpha_f \cdot e^{-s\tau} = 0 \\ &s_p = \frac{\ln(\alpha_f \alpha_r)}{\tau} + j\frac{(2k+1)\pi}{\tau} \quad k = 0,1\cdots \end{aligned} \tag{2.28}$$

The poles are periodic and there is no pole at DC. When the feedback from the delay element is added at the input, the transfer function of the resonator will be named $H_{a2}(s)$. The poles of $H_{a2}(s)$ will be the solutions of the equation:

$$\begin{aligned} &1 - \alpha_f \cdot \alpha_r \cdot e^{-s\tau} = 0 \\ &s_p = \frac{\ln(\alpha_f \alpha_r)}{\tau} + j\frac{2k\pi}{\tau} \quad k = 0,1\cdots \end{aligned} \tag{2.29}$$

It may be seen that the poles have a periodic structure same as before, but in this configuration there is a pole at DC. To benefit from this DC pole, the delay element must be able to transmit constant input values.

Now we will consider the resonator structure shown in Figure 2.3.b, where α_r represents the loss factor in the transmission media. The input signal x(t) forms the output of the system combined with the output delayed τ seconds. The feedback path of the signal has a gain α_f and two possible polarities. This resonator may be characterized by the equation:

$$y(t) = \alpha_r \cdot \left(x(t-\tau) \pm \alpha_f y(t-\tau) \right) \tag{2.30}$$

The transfer function of the resonator will be:

$$H_b(s) = \frac{Y(s)}{X(s)} = \frac{\alpha_f}{1 \mp \alpha_r \cdot \alpha_f \cdot e^{-s\tau}} \tag{2.31}$$

Same as before, the polarity in the feedback path define two possible transfer functions. When the feedback from the delay element is subtracted at the input, the transfer function will be named $H_{b1}(s)$ and its poles will be:

$$\begin{aligned} &1 + \alpha_r \cdot \alpha_f \cdot e^{-s\tau} = 0 \\ &s_p = \frac{\ln(\alpha_f \alpha_r)}{\tau} + j\frac{(2k+1)\pi}{\tau} \quad k = 0,1\cdots \end{aligned} \tag{2.32}$$

When the feedback from the delay element is added at the input, the transfer function will be $H_{b2}(s)$, and its poles will be:

$$\begin{aligned} &1 - \alpha_f \cdot \alpha_r \cdot e^{-s\tau} = 0 \\ &s_p = \frac{\ln(\alpha_f \alpha_r)}{\tau} + j\frac{2k\pi}{\tau} \quad k = 0,1\cdots \end{aligned} \tag{2.33}$$

Again, the DC pole will require the delay element to transmit constant input values.

To clarify the concepts of this section, we are going to analyze a simple example that will provide a graphical intuition of the system equivalence proposed in Fig.2.1. Figure 2.4 shows three equivalent linear systems which represent a discrete time integrator. Fig.2.4.a shows the standard representation of a delaying discrete time integrator, together with is response to a discrete time step function. Fig.2.4.b shows and equivalent system implemented with a pulse shaper *p(t)*, a continuous time integrator and a sampler. Fig.2.4.c represents an equivalent system implemented with the pulse shaper and sampler as in Fig.2.4.b but using a continuous time integrator based on a delay.

Although formally they are equivalent, systems 2.4.b and 2.4.c have a different behavior against misalignment of the pulses generated by the pulse shapers or sampling errors in the samplers. The reason is that the output of the continuous time integrator in 2.4.b is a ramp and any error in the sampling point will lead to an error in the sampled value, however the output of system 2.4.c is a staircase signal whose slope near the sampling point is zero. Also, if the pulses generated by *p(t)* in system 2.4.b are not uniformly distributed in time, the ramp at the output of the integrator will be broken into misaligned pieces, whereas in the case of system 2.4.c the steps of the staircase will be misplaced but its value will not be affected

close to the sampling points.

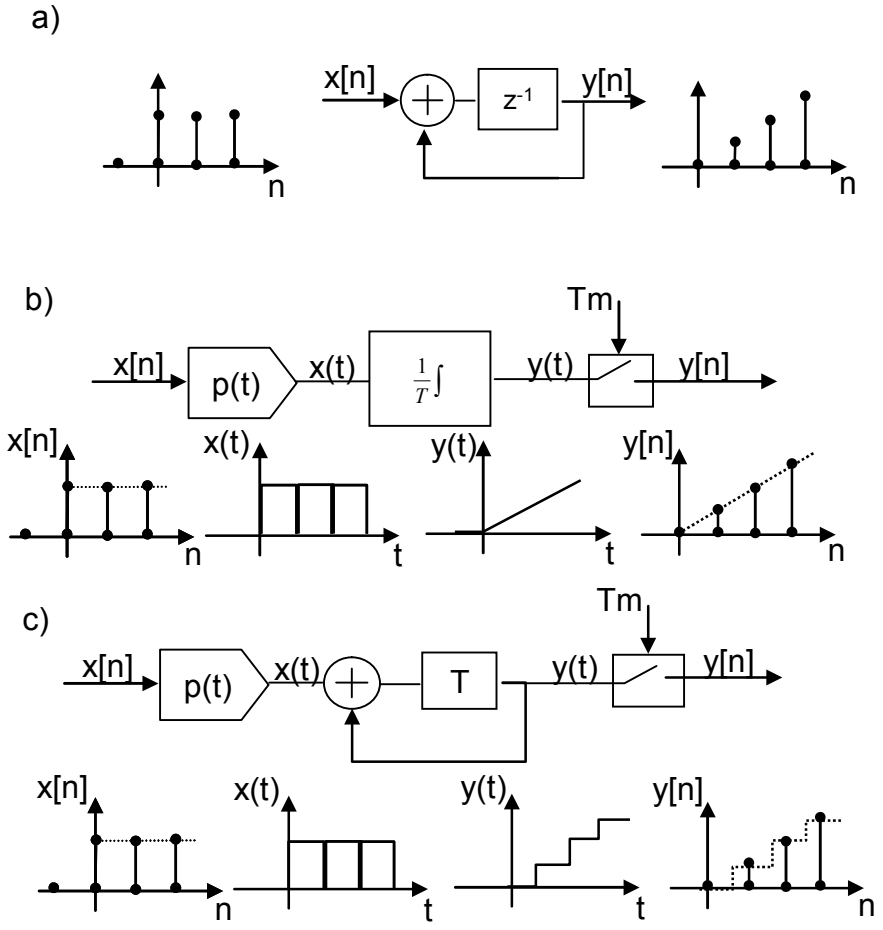

Figure 2.4. Block diagram of three equivalent integrators.

2.4 Synthesis of ΣΔ Modulators using continuous time Delays

The system replacement mentioned before may be applied to any discrete time filter. In the particular case of a sigma delta modulator loop filter, this transformation may be of a special interest due to the properties of the retarded linear systems analyzed in the previous section.

Figure 2.5.a depicts a general model of a CT-ΣΔM, whose loop filter belongs to the class of filters expressed by Eq.2.8. Figure 2.5.b shows the equivalent DT-ΣΔM, where the input sampling clock has also been marked.

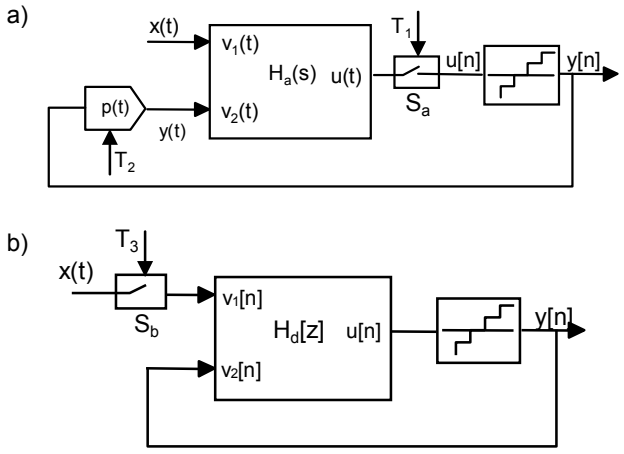

Figure 2.5. General model of a) CTΣΔ modulator and b) DTΣΔ modulator.

If we want the CT-ΣΔM in Fig 2.5.a to be equivalent to the DT-ΣΔM in Fig. 2.5.b, we may use the *impulse invariance condition* [Che99] (see also chapter 1). In the design of a conventional CT-ΣΔM, the condition of impulse invariance requires the computation of an inverse Laplace transform of some complexity. However, in our case it suffices to apply the condition of Eq.2.17 to accomplish this task. By using the same signal flow graph and replacing the unit delays of the filter $H_d[z]$ on Fig. 2.5.b by continuous time delays of T in the filter $H_a(s)$ of Fig. 2.5.a, both modulators will have the same NTF. This will happen regardless of the shape of $p(t)$ because of Eq.2.16. Assuming that all clock signals T_1 and T_2 operate at points $t=nT$ without timing errors, the behavior of the CT-ΣΔM of Fig.2.5.a may be described by the following equation:

$$\begin{aligned} u[n] &= \sum_{m=0}^{\infty} h_{a1}[m] \cdot y[n-m] + \sum_{m=0}^{\infty} h_{a2}[m] \cdot x(nT - mT) \\ h_{a1}[0] &= 0 \\ y[n] &= Q(u[n]) \end{aligned} \tag{2.34}$$

where Q(*u[n]*) are the samples of the quantizer at $t=nT$.

In Eq.2.34, sequences h_{a1} and h_{a2} represent the impulse responses of the loop filter, evaluated from inputs v_1 and v_2 respectively up to the output u(t). These sequences match with the impulse responses of the equivalent discrete time modulator. The impulse invariance condition to transform discrete into continuous time modulators [Che99], is implicit in this architecture [Her03].

An important property of delay based CT-ΣΔM may be observed in Eq.2.34: the behavior of the modulator depends only on the values of the input signal and the quantizer output at specific time instants, as a difference with conventional CT-ΣΔMs that depend on averages over a time range produced by integrators (see section 2.3). Hence, only the values of *p(t)* at the sampling points are relevant. In the foregoing, we will choose a DAC pulse *p(t)* which is constant over *T*, i.e. the typical zero-order-hold pulse:

$$p(t) = u(t) - u(t-T) \tag{2.35}$$

We could take as a start point in the design, a known DT-ΣΔM with loop filter $H_d[z]$, which would be implemented with continuous time delays by replicating its impulse response into $H_a(s)$. As an example, we will try to synthesize and simulate the equivalent of the standard single-bit, low-pass, second order DT-ΣΔM shown in Figure 2.6.a [Nor96]. Although in next sections we will show a more efficient hardware implementation of this system, we may simply replace the unit delays represented by z^{-1} by a continuous time delay *T* and rearrange the input sampler and feedback DAC. The resulting system is shown in Figure 2.6.b. To simplify the analysis it has been assumed that the resonators are ideal, hence $\alpha=1$. The quantizer carries out both the sampling operation and the amplitude discretization. Assuming the conventional white noise model for the quantization error introduced at the quantizer, and applying the *pulse invariant transformation* (see chapter 1, section 1.3.5), we may define the equivalent NTF and STF of the structure of Fig.2.6.b as follows:

$$NTF(z) = \left(1 - z^{-1}\right)^2 \quad STF(z) = z^{-1} \tag{2.36}$$

The alias components generated by the sampling operation may be feedback to the modulator loop filter, causing instabilities or degrading the SNR due to its periodic pole structure. A possible solution is to use a sampling clock with a period that is an integer multiply of *T*, the resonator delay. Assuming a proper band limitation of the input signal, this choice may avoid any undersampling problem because the alias components have the same periodicity in frequency than the loop filter function.

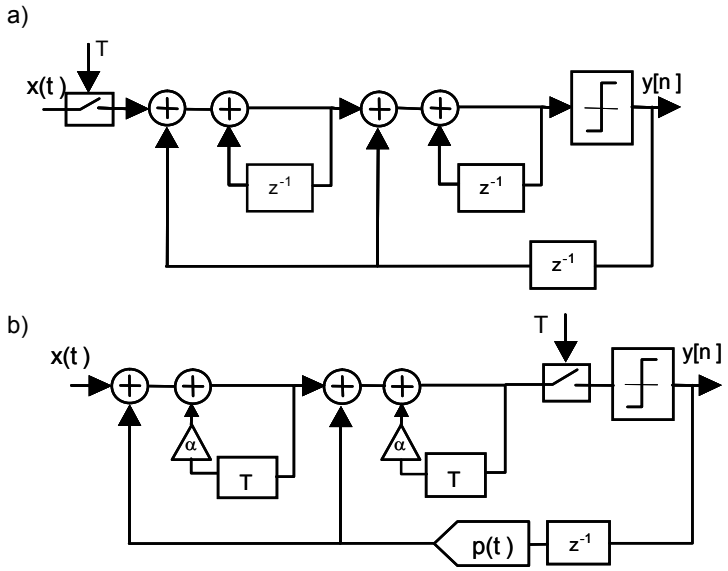

Figure 2.6. Two realizations of a second order single bit ΣΔ modulator. a) discrete time. b) continuous time with delays.

We will show a measurement to validate the synthesis of delay based ΣΔMs using the proposed method in this chapter. For such purpose, the loop filter of the modulator in Fig.2.6.b has been designed with an open loop gain of 120dB at DC.

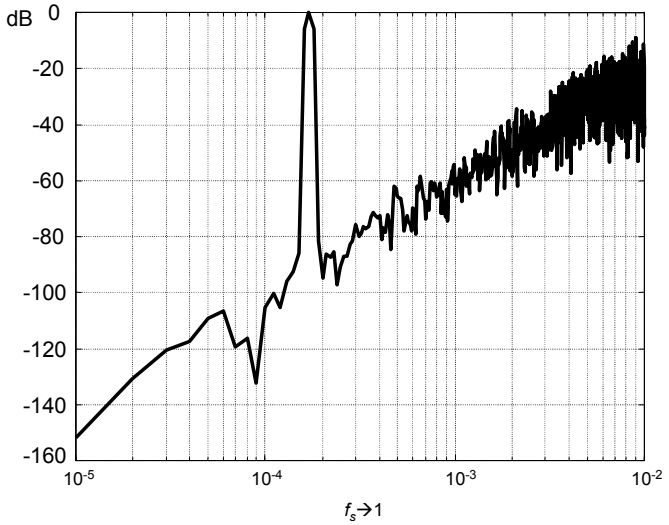

Figure 2.7. FFT of simulated output from delay based CTΣΔ modulator of Fig.2.6.b.

This value has been calculated using a non ideal resonator (α=0.999). Considering OSR=256, we will simulate the modulator in Fig.2.6.b with a full scale tone in the middle of the signal band. Figure 2.7 shows the modulus of the FFT of the simulated output of the delay based CT-ΣΔM of Fig.2.6.b using a single bit quantizer and applying a -3dB low frequency sine wave at the input. The sampling clock (f_s) was set to $1/T$ to place the first NTF zero at DC and to match the following zero with the sampling frequency. The output sequence shows a noise spectrum that closely matches that of the second order ΣΔM in Fig.2.6.a [Nor96].

2.5 Implementation Advantages of Delayed CTΣΔ Modulators

The main differences at system level between this new type of delayed CT-ΣΔM, when compared to standard CT-ΣΔM and DT-ΣΔM, may be inferred by observing Fig.2.5. First, in this new architecture, the sampler is located in front of the quantizer, seizing its error shaping properties, same as in a CT-ΣΔM. However, if the conditions in Eq.2.17 are met, the equivalent system would be insensitive to timing errors in the generation of the feedback pulse *p(t)* and the area and rising and falling times of this pulse would be no longer relevant (see section 2.3.1). Finally, we would not need the initial sample and hold function inherent to switched capacitor implementations of DT-ΣΔMs. Hence, this new architecture seizes many of the advantages of both CT-ΣΔMs and DT-ΣΔMs.

These properties provide several implementation advantages over conventional CT-ΣΔMs, which will be analyzed in the following chapters:

a) The modulators are partially desensitized from clock jitter and code dependencies in the feedback signal.

b) There may be an arbitrary delay between the sampling at the quantizer and the update of the feedback DACs. This allows a varying loop delay. This loop delay may be added as part of the loop filter in the design, if required.

c) The modulators may be designed using the tools of discrete time modulators.

d) The modulators may allow sub-sampling of the input as in discrete time modulators, but using a continuous time loop filter.

Chapter 2 Annex

Although we know that a solution of Eq.2.7 may be obtained by an equivalent of the variation of constants formula, we are going to use a simpler method to solve this equation for a generic causal input x(t). We will try to prove that in a system expressed by the following equation:

$$y(t) = \sum_{m=1}^{M} b_m \cdot y(t - mT) + x_f(t) \tag{A.1}$$

y(t) may be expressed as the following series:

$$y(t) = \sum_{k=0}^{\infty} h_f[k] \cdot x_f(t - kT) \tag{A.2}$$

After substituting (A.2) into (A.1) and changing the summation orders we obtain:

$$\sum_{k=0}^{\infty} \left(h_f[k] - \sum_{m=1}^{M} b_m \cdot h_f[k-m] \right) \cdot x_f(t - kT) = x_f(t) \tag{A.3}$$

The values of $h_f[k]$ can be computed recursively as follows if we consider the system causal:

$$\begin{aligned} h_f[0] &= 1 \\ h_f[k] &= \sum_{m=1}^{M} b_m \cdot h_f[k-m], \; k \neq 0 \end{aligned} \tag{A.4}$$

To make this linear system more general, we may replace x_f by a linear combination of delayed input signals:

$$x_f(t) = \sum_{r=0}^{R} a_r \cdot x(t - rT) \tag{A.5}$$

With this modification, the nature of the output signal will still be a series but with different coefficients h[k]:

$$\begin{aligned} y(t) &= \sum_{m=1}^{M} b_m \cdot y(t - mT) + \sum_{r=1}^{R} a_r \cdot x(t - rT) \\ h[k] &= \sum_{r=0}^{R} a_r \cdot h_f[k - r] \\ y(t) &= \sum_{k=-\infty}^{\infty} h[k] \cdot x(t - kT) \end{aligned} \tag{A.6}$$

This completes the proof.

CHAPTER 3

Continuous Time Implementation of Delay Elements for ΣΔ Modulators

According to the results of chapter 2, we could replace any unit delay element in an already designed discrete-time sigma-delta modulator by a continuous time delay equal to the sampling clock period and rearrange the position of the sampler and feedback DAC to obtain a continuous time implementation.

In this chapter we will study the physical implementation options for these continuous time delays, as well as the mapping of discrete time systems using delay elements with special emphasis on Transmission Lines.

Some passive components taken from the field of RF circuits can be candidates to implement a continuous time delay. They can be divided into two groups depending on the kind of propagation media use to store the signal. We will study devices which use electrical or mechanical media:

a) Transmission Lines (electrical propagation).

b) RF MEMS and SAW (mechanical or electromechanical propagation).

3.1 Implementation of a delay element

Our purpose is to implement an electronic circuit where a physical magnitude like a voltage or a current is available in the circuit delayed by a certain amount of time T. There are two possible options to accomplish this.

In Figure 3.1.a, $v_1(t)$ is applied to the input port of a fourpole and appears in the load at the output port delayed. This would require that the signal is stored in some distributed energy storage device, such as transmission media where a waveform propagates.

In Figure 3.1.b we have an impedance connected to a current or voltage driving source, being the output signal of the circuit the reciprocal voltage or current magnitude which represents a voltage-to-current or a current-to-voltage conversion with a delay. To accomplish this, the signal must travel through a transmission media and be reflected back to the source.

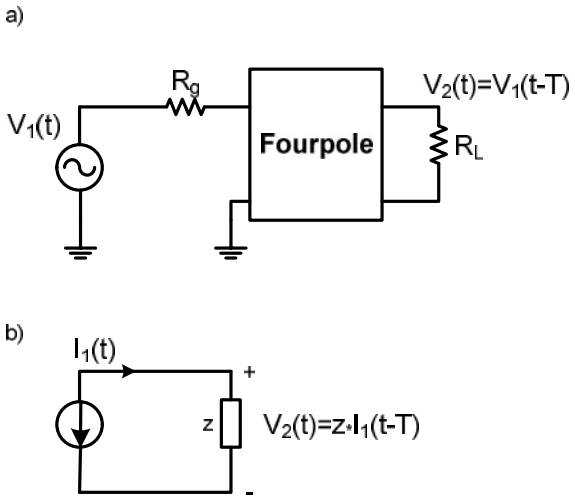

Figure 3.1. Electrical implementation of a delay element.

The signal is available in the circuit in the form of an electromagnetic field. It is known that electromagnetic fields can propagate through a longitudinal structure forming what is referred as a transmission line. This would suffice to achieve our purpose; however the propagation speed in conventional transmission lines leads to very short delays when compared with the resonant frequency of LC resonators of similar physical magnitudes. For instance, a LC resonator whose inductor and capacitor values are in the order of nH and pF would resonate at hundreds of megahertz and still could be integrated on a chip. However, a transmission line which resonates at hundreds of megahertz has a length in the order of a meter.

The propagation speed of mechanical waves in solids is usually much lower than the propagation speed of electromagnetic fields. For this reason, it may be helpful to implement a delay in a circuit, to convert the electrical energy into a mechanical energy, feed it to a solid and convert the mechanical energy back to electrical energy after propagation. This principle has been used extensively in RF electronics with piezoelectric resonators such as SAW filters, quartz crystals, etc.

In this chapter we will make a brief survey of the theoretical aspects and the physical principles of the available devices to implement a delay.

3.2 Transmission Lines (electrical propagation)

3.2.1 Introduction

An electrical transmission line can be seen as a continuous time delay. This property of transmission lines is commonly used in RF applications to build resonators when the transmission line is properly loaded. When used in such a way, two main characteristics must be described: the characteristic impedance Z_0 and the unloaded Q_0 factor of the transmission line.

A transmission line can be modeled as a two-port network (also called a fourpole network), as in Figure 3.2:

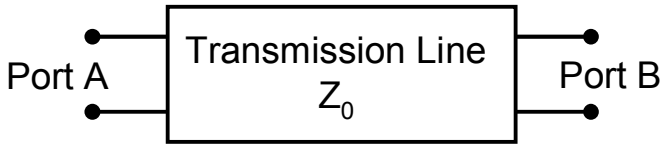

Figure 3.2. Transmission Line model as a two-port network.

In the simplest case, the network is assumed to be linear (i.e. the complex voltage across either port is proportional to the complex current flowing into it when there are no reflections), and the two ports are assumed to be interchangeable. If the transmission line is uniform along its length, then its behavior is largely described by a single parameter called the characteristic impedance, symbol Z_0. This is the ratio of the complex voltage of a given wave to the complex current of the same wave at any point on the line. The characteristic impedance of a lossless transmission line is purely real, that is, there is no imaginary component ($Z_0=|Z_0|+j0$).

Characteristic impedance appears like a resistance in this case, such that power generated by a source on one end of an infinitely long lossless transmission line is dissipated *through* the line but is not dissipated *in* the line itself.

A transmission line of finite length (lossless or lossy) that is terminated at one end with a resistor equal to the characteristic impedance ($Z_L = Z_0$) appears like an infinitely long transmission line to the source. Figure 3.3 shows the schematic representation of a transmission line, showing the characteristic impedance Z_0. Typical values of Z_0 are 50 or 75 ohms for a coaxial cable, about 100 ohms for a twisted pair of wires, and about 300 ohms for a common type of untwisted pair used in radio transmission.

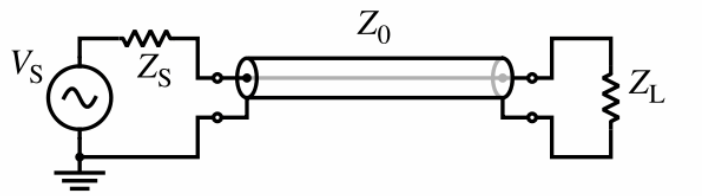

Figure 3.3. Schematic representation of a transmission line, showing the characteristic impedance Z_0.

Some of the power that is fed into a transmission line is lost because of its resistance. This effect is called *ohmic* or *resistive* loss. At high frequencies, another effect called *dielectric loss* becomes significant, adding to the losses caused by resistance. Dielectric loss is caused when the insulating material inside the transmission line absorbs energy from the alternating electric field and converts it to heat.

3.2.2 Telegrapher's equations

The Telegrapher's Equations (or just Telegraph Equations) [Var02] are a pair of linear differential equations which describe the voltage and current on an electrical transmission line with distance and time. They were developed by Oliver Heaviside who created the *transmission line model*, and are based on Maxwell's Equations.

Figure 3.4 shows the transmission line model. This model represents the transmission line as an infinite series of two-port elementary components, each representing an infinitesimally short segment of the transmission line:

- The distributed resistance *R* of the conductors is represented by a series resistor (expressed in ohms per unit length).

- The distributed inductance *L* (due to the magnetic field around the wires, self-inductance, etc.) is represented by a series inductor (henries per unit length).

- The capacitance *C* between the two conductors is represented by a shunt capacitor C (farads per unit length).

- The conductance *G* of the dielectric material separating the two conductors is represented by a conductance G shunted between the signal wire and the return wire (siemens per unit length).

The model consists of an *infinite series* of the elements shown in Fig.3.4, and that the values of the components are specified *per unit length* so the picture of the component can be misleading. *R*, *L*, *C*, and *G* may also be functions of frequency. An alternative notation is to use *R*', *L*', *C*' and *G*' to emphasize that the values are derivatives with respect to length.

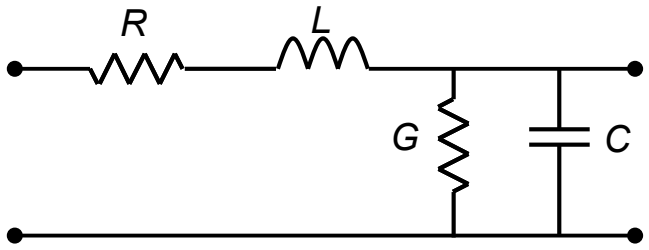

Figure 3.4. Schematic representation of the elementary components of a transmission line.

When the *elements R* and *G* are very small, their effects can be neglected, and the transmission line is considered as an idealized, lossless, structure. In this case, the model depends only on the *L* and *C* elements, and we obtain a pair of first-order partial differential equations, one function describing the voltage *V* along the line and the other the current *I*, both function of position *x* and time *t*:

$$\begin{aligned} \frac{\partial}{\partial x}V(x,t) &= -L\frac{\partial}{\partial t}I(x,t) \\ \frac{\partial}{\partial x}I(x,t) &= -C\frac{\partial}{\partial t}V(x,t) \end{aligned} \tag{3.1}$$

These equations may be combined to form either of two exact wave equations:

$$\frac{\partial^2}{\partial t^2}V = \frac{1}{LC}\frac{\partial^2}{\partial x^2}V$$
$$\frac{\partial^2}{\partial t^2}I = \frac{1}{LC}\frac{\partial^2}{\partial x^2}I \tag{3.2}$$

In the steady-state case (assuming a sinusoidal wave), these reduce to

$$\frac{\partial^2 V(x)}{\partial x^2} + \omega^2 LC \cdot V(x) = 0$$
$$\frac{\partial^2 I(x)}{\partial x^2} + \omega^2 LC \cdot I(x) = 0 \tag{3.3}$$

where ω is the frequency of the steady-state wave.

If the line has infinite length or when it is terminated with its characteristic impedance, these equations indicate the presence of a wave, traveling with a speed:

$$v = \frac{1}{\sqrt{LC}} \tag{3.4}$$

Note that this propagation speed, Eq.3.4, applies to the wave phenomenon on the line and has nothing to do with the electron drift velocity. In other words, the electrical impulse travels very close to the speed of light, although the electrons themselves travel only a few centimeters per second. For a coaxial transmission line, made of perfect conductors with vacuum between them, it can be shown that this speed is equal to the speed of light.

Applying the transmission line model based on the telegrapher's equations, the general expression for the characteristic impedance of a transmission line is:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{3.5}$$

For a lossless line R and G are zero and the equation for characteristic impedance reduces to:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{3.6}$$

3.2.3 Input Impedance, resonant frequency and Q_0 factor of a Transmission Line

The characteristic impedance Z_0 of a transmission line is the ratio of the amplitude of a single voltage wave to its current wave. Since most transmission lines also have a reflected wave, the characteristic impedance is generally not the impedance that is measured on the line.

For a lossless transmission line, it can be shown that the impedance measured at a given position l from the load impedance Z_L is:

$$Z_{in} = Z_0 \frac{Z_l \cos(\beta l) + jZ_0 \sin(\beta l)}{Z_0 \cos(\beta l) + jZ_l \sin(\beta l)} \tag{3.7}$$

where $\beta = \frac{2\pi}{\lambda}$ is the propagation constant in the medium.

In calculating β, the wavelength is generally different inside the transmission line to what it would be in free-space. The velocity constant of the material of the transmission line is made of needs to be taken into account when doing such a calculation.

When the transmission line is of finite length, a short circuited quarter wavelength behaves as a parallel resonant circuit. To analyze this, the input impedance of a transmission line is defined as in Eq.3.7. If this line is terminated in a short circuit, the input impedance Z_{in} is written as:

$$Z_{in} = Z_0 \frac{\sinh(\alpha l)\cos(\beta l) + j\cosh(\alpha l)\sin(\beta l)}{\cosh(\alpha l)\cos(\beta l) + j\sinh(\alpha l)\sin(\beta l)} \tag{3.8}$$

where α is the attenuation constant in the medium.

Applying boundary conditions, the resonant frequency is such that

$$\beta l = \frac{n\pi}{2}, \qquad n \text{ is a odd integer} \tag{3.9}$$

The corresponding resonant frequency is

$$f_0 = \frac{nv}{2} \tag{3.10}$$

where v is the is the velocity of electromagnetic waves in the medium (see Eq.3.4) between the conductors of the transmission line. Using the resonant condition in Eq.3.9, Eq.3.8 reduces to:

$$Z_{in} = Z_0 \frac{\cosh(\alpha l)}{\sinh(\alpha l)} = \frac{Z_0}{\tan(\alpha l)} \approx \frac{Z_0}{\alpha l} \tag{3.11}$$

At this point it is also possible to derive expressions for the Q factor of such a resonating segment. At frequencies close to the resonant frequency f_0,

$$\beta l = \frac{2\pi f}{v} l = \frac{2\pi(f_0 + \delta f)}{v} l = \frac{n\pi}{2} + \frac{2\pi\delta f l}{v} \tag{3.12}$$

Substituting these into Eq.3.8, after simple trigonometric transformations, the input impedance becomes:

$$Z_{in} = Z_0 \frac{-\sinh(\alpha l)\sin(2\pi\delta f l / v) + j\cosh(\alpha l)\cos(2\pi\delta f l / v)}{-\cosh(\alpha l)\sin(2\pi\delta f l / v) + j\sinh(\alpha l)\cos(2\pi\delta f l / v)} \tag{3.13}$$

Substituting simplifications for small arguments of these trigonometric functions:

$$Z_{in} = Z_0 \left(\alpha l + j \frac{2\pi\delta f l}{v} \right)^{-1} \tag{3.14}$$

Comparing this with Eq.3.11, it is clear that if the imaginary term in the denominator of Eq.3.14 is made equal to its real term, the input impedance is half that at the resonant frequency. The corresponding frequency deviation is:

$$\delta f = \frac{\alpha v}{2\pi} = \frac{\alpha f_0}{\beta} \tag{3.15}$$

The corresponding Q_0 factor is therefore:

$$Q_0 = \frac{f_0}{2\delta f} = \frac{\beta}{2\alpha} \tag{3.16}$$

3.2.4 Types of electrical Transmission Lines

a) Coaxial transmission lines:

Figure 3.5.a shows a typical coaxial transmission line. This kind of transmission lines confines the electromagnetic wave to the area inside the transmission line, between the center conductor and the shield.

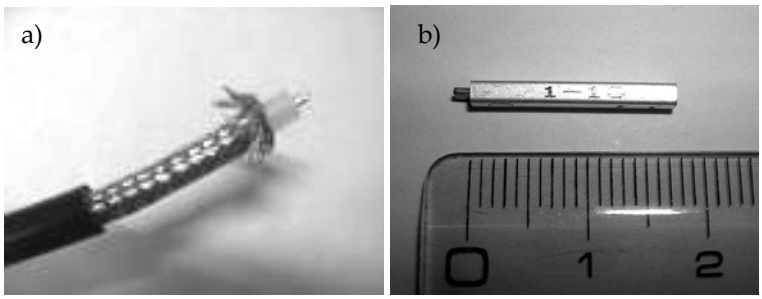

Figure 3.5. Coaxial transmission lines.

The transmission of energy in the line occurs totally through the dielectric inside the cable between the conductors. We can use them as continuous time delays to implement resonators when properly loaded. When implemented in such a way the resonator benefits from the high unloaded Q_0 factor of the coaxial transmission line (Q_0>100). The standard characteristic impedance of this coaxial transmission lines is around Z_0=50Ω. The propagation speed in a coaxial transmission line depends on the properties of the dielectric inside of the transmission line. To reduce the size of the transmission line while keeping its delay properties, a material with a high dielectric constant is used, for example the ceramic material used for capacitors. An example of this kind of ceramic coaxial transmission line is shown in Figure 3.5.b.

b) Microstrip:

A microstrip circuit when implemented as a transmission line uses a thin flat conductor which is parallel to a ground plane. Microstrip can be made by having a strip of copper on one side of a printed circuit board (PCB) or ceramic substrate while the other side is a continuous ground plane. The width of the strip, the thickness of the insulating layer (PCB or ceramic) and the dielectric constant of the insulating layer determine the characteristic impedance of the strip which is a transmission line.

In the literature also some examples of integrated *Microstrip Tubs* used as a

transmission line structure are shown. The microstrip tub structure shown in Figure 3.6 is used throughout the CMOS chip in [Kom06] [Kom05] for matching 50Ω transmission lines. The presence of the side shields increases isolation between adjacent lines, allowing a compact layout. The lines are implemented using the top three metals of the process. The lower two metals are left for routing of low frequency signals.

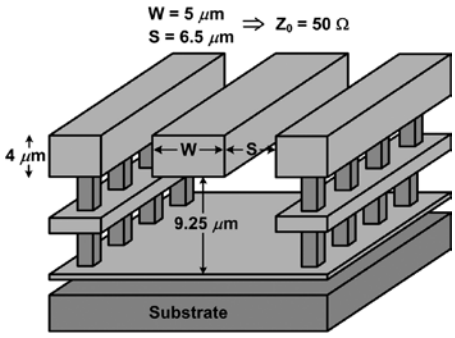

Figure 3.6. Conductor-backed coplanar waveguide microstrip tub transmission line structure used for impedance matching in [Kom06] [Kom05].

c) Integrated Lines

It is also possible to integrate a transmission line in silicon using *L* and *C*. However, the resonance frequencies are constrained to values above the tenths of gigahertz due to the dimension of the chips and the dielectric constant of silicon. Also, these transmission lines are subjected to the same loss problems that affect to integrated inductors.

In the recent literature two approaches have been used to overcome the loss problem and to achieve transmission line resonators in gigahertz range.

In [Ana03] an integrated transmission line structure is described whose resonance frequency is in the order of 5 GHz. It is consists of a constant-k *LC* ladder structure. The ladder is a lumped approximation of a transmission line and hence, can be used as a delay line. But this approximation still suffers from the low Q factor of its integrated *L* and *C* components.

A second approach that has been published in recent years uses distributed Microelectromechanical System (MEMS) transmission line for making RF filters. In this way, distributed MEMS transmission lines (DMTLs) are used in implementation of phase shifters [Reb03] [Bar00] [Bar98] [Bor00], resonators [Mul00] and filters [Lak03], which are the key components in phased arrays, radars, wireless communication systems and measurement instrumentation. The implementation of DMTLs employs the idea of periodically loading a

high-impedance coplanar waveguide (CPW) with reactive loading elements. Generally, the loading elements are tunable RF MEMS bridges, forming a transmission line with adjustable parameters [Reb03] [Bar00] [Bor00] [Bar98]. Figure 3.7 shows a simplified schematic of this structure.

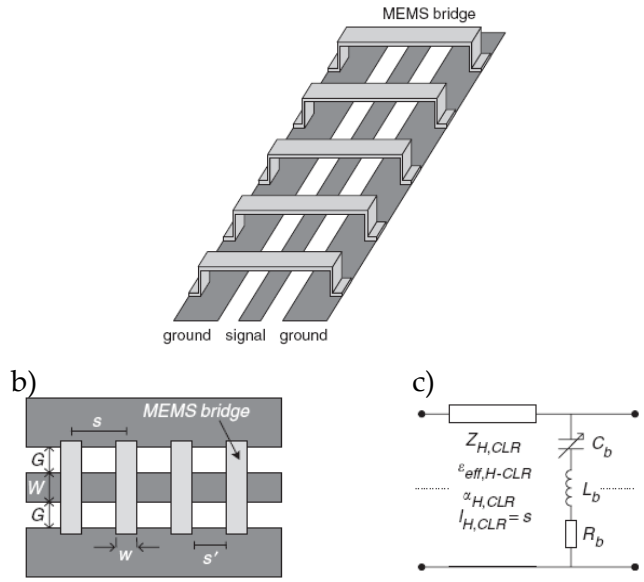

Figure 3.7. General view of DMTL structure and model from [Bar00]. a) General view of a DMTL structure. b) Top view of a DMTL structure. c) Lumped-element CLR model of the unit section of DMTL.

Simulations and measurement results of fabricated devices in 1–20GHz band verify that these DMTL structures provides good results, even with bridge widths in the range of 50μm. The Q factor of these transmission lines can be one order of magnitude higher than that of the *LC* ladder structures.

A second option is to use the RF-MEMS as a mechanical transmission line where a mechanical propagation is used to build a transmission line instead of an electrical propagation. In next section we describe this kind of integrated transmission line resonators using mechanical propagation.

3.3 RF MEMS transmission lines (mechanical propagation)

Mechanical resonance characteristics of coupling components such as bar, string and beam have been studied in the context of conventional mechanical filters [Var02]. Although their micro size RF-MEMS counterparts may not behave identically as the larger ones, an analysis of these would give an insight into the performance of these systems. For these components, we first endeavor to develop an equivalent circuit model, treating them as an

ideal transmission line. These equivalent circuits are developed based on electromechanical mobility analogies. Their wave propagation characteristics for specified boundary conditions are used to obtain their resonance characteristics.

In the recent literature some works have shown that using sound waveguides as delay lines for RF signals is desirable since much smaller group velocities can be reached than with electromagnetic waveguides. Also high-Q values of microelectromechanical resonators suggest that, at least for narrow bandwidths below 100 MHz, mechanical impedance transformation can enable efficient acoustic waveguide operation with capacitive coupling [Ala03]. Figure 3.8 shows an example of a mechanical RF-MEMS transmission line.

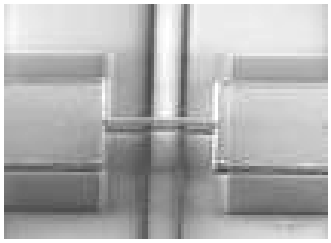

Figure 3.8. Mechanical RF-MEMS transmission line.

Also, other kinds of resonators that use mechanical propagation are common used in RF applications. They are called Surface Acoustic Wave (SAW) resonators. These resonators are normally used to place only one resonance frequency [Yu07]. Therefore, we will not consider them for our applications, as they don't behave as a continuous time delay with multiple resonance frequencies as transmission lines do.

3.3.1 Assumptions and theorems for mechanical modeling of RF-MEMS transmission lines

For a simple straight forward analysis the present discussion is restricted to homogeneous, isotropic, continuous, elastic, lossless solids. Even for micro size systems, these assumptions are valid if the grain size of the crystalline materials is much smaller than the wavelength. It is also assumed that disturbances that travel along these solids are continuous motions around their rest positions with a relatively small magnitude of variation. The elasticity law defines the normal stress σ_x, due to deformation in the direction of propagation x as

$$\sigma_x = E_l \varepsilon_x \tag{3.17}$$

where E_l is the longitudinal modulus of elasticity and ε_x is the fractional variation in thickness (strain). The longitudinal modulus of elasticity is

$$E_l = E\frac{(1-\mu)}{(1+\mu)(1-2\mu)} \tag{3.18}$$

where E is the modulus of elasticity of the material and μ is the Poisson ratio.

The deformations in the transverse directions on a rectangular element make it a parallelogram:

$$\tau_{xy} = \tau_{yx} = G\gamma_{xy} \tag{3.19}$$

where τ_{xy} and τ_{yx} are the tangential stresses on the element, γ_{xy} is the shear angle and G is the shear modulus. For long thin bars, Hooke's and Poisson's laws are also relevant:

$$F = SE\frac{\delta l}{l} \tag{3.20}$$

$$\frac{\delta a}{a} = -\mu\frac{\delta l}{l} \tag{3.21}$$

where F is the force applied, S is the cross-sectional area, $\delta l/l$ is the strain and $\delta a/a$ is the relative variation in the lateral dimension.

Consider a long thin solid bar of length l and a uniform cross-sectional area S placed along the x-axis. A small longitudinal deformation traveling in the x direction causes a force $F(x)$. The resultant displacement at x is $\xi(x)$. For a section of length dx on the bar, Newton's law can be applied to equate the force to mass of the section and the acceleration

$$-F(x+dx)+F(x) = \rho S dx\frac{d^2\xi(x)}{dt^2} \tag{3.22}$$

After rearranging terms, this becomes:

$$\frac{\partial F}{\partial x} = \rho S\frac{dv}{dt} \tag{3.23}$$

Hooke's law in Eq.3.20 is used to express the force at a location in terms of displacement as

$$F(x) = SE\frac{\xi(x+dx)-\xi(x)}{dx} = SE\frac{\xi(x)}{\partial x} \tag{3.24}$$

Taking the derivative with respect to time and rearranging terms:

$$\frac{\partial v}{\partial x} = \frac{1}{SE}\frac{dF}{dt} \tag{3.25}$$

Assuming sinusoidal variations for these disturbances, phasor notation can be employed to remove the time dependencies of Eq.3.23 and Eq.3.25. These then become:

$$\frac{d\tilde{F}}{dx} = -j\omega\rho S\tilde{v} \tag{3.26}$$

$$\frac{d\tilde{v}}{dx} = -\frac{j\omega}{SE}\tilde{F} \tag{3.27}$$

Comparing Eq.3.26 and Eq.3.27 with the characteristic equations of lossless transmission lines in Eq.3.3 (after making R = G = O), the similarities are striking. Now, using electromechanical mobility analogies, an equivalent circuit representation can be obtained for the transmission line equivalent circuit of the bar, as shown in Figure 3.9.

It would also be of interest to obtain the propagation constant and the velocity of propagation on this transmission line equivalent of the bar. Comparing with Eq.3.4, the velocity of waves in the bar v_b is

$$v_b = \left(\frac{E}{\rho}\right)^{1/2} \tag{3.28}$$

The propagation constant is

$$\beta = \omega\left(\frac{\rho}{E}\right)^{1/2} \tag{3.29}$$

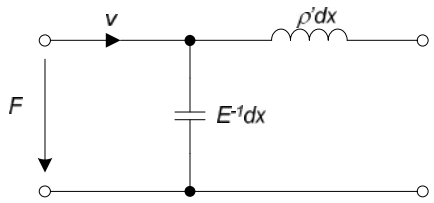

Figure 3.9. Equivalent circuit for a string modeled as a transmission line.

3.4 Implementation issues for continuous time delays using transmission lines

As we have explained in the previous two sections, there are different kinds of possible practical implementations for continuous time delays modeled as transmission lines. They can be off-chip transmission lines: coaxial resonators or microstrips implemented on PCB, or integrated transmission lines: integrated microstrips, *LC* ladder structures [Ana03], electrical distributed RF-MEMS transmission lines (DMTLs) [Bar00] or mechanical RF-MEMS transmission lines [Ala03].

In the case of off-chip transmission lines we can build resonators that have the advantage of the unloaded high-Q_0 factor of the coaxial transmission lines (up to 5000) and wide and accurate resonant frequency range (from tenth of megahertz to gigahertz). In the other hand, these transmission lines have the disadvantage of the parasitics in the connections with the integrated circuit and the low value of the characteristic impedance that is around Z_0=50Ω. As the g_m of the transconductors of the modulator is inversely proportional to the value of Z_0, as we will explain in next section, an increase in the value of Z_0 will reduce the power consumption of the transconductors.

Then, to fully seize the properties of transmission line ΣΔMs we would need to integrate the transmission lines together with the associated active elements in a single chip. In this way we can reduce power by increasing the value of Z_0 and we are also able to reduce the parasitics in the connection between the transmission lines and the active elements. However, the integrated transmission lines have a lower unloaded Q_0 factor (Q_0<100) than coaxial transmission lines and they are in the range of gigahertz. Only the unloaded Q_0 factor of the mechanical RF-MEMS transmission lines is comparable to that of the coaxial transmission lines. Table 3.1 shows a comparison between different types of transmission lines.

Although off-chip transmission lines could be a problem, depending on the

application, could be accepted as a solution. In [Yu07] a bandpass CT-ΣΔM employing off-chip SAW resonators as loop filters is presented. Compared with the loop filters realized with *gm-C* and *LC* resonators, the SAW resonator has the advantage of high-*Q* factor, wide resonant frequency range and accurate resonant frequency without the need for automatic tuning.

	Implementation	**Propagation**	**Freq. range (GHz.)**	**Z_0 (Ω)**	**Q_0**
Coaxial TLs	Off-chip	Electrical	0.01-3	50-75	100-5000
Microsrtips	Off-Chip/Integrated	Electrical	0.5-10	50-100	20-100
***LC* ladders**	Integrated [Ana03]	Electrical	1-30	50-300	5-50
DMTLs	Integrated [Bar00]	Electrical	1-20	50-350	5-100
Mechanical RF-MEMS SAW resonators	Integrated [Ala03] [Yu07]	Mechanical	0.5-40	50-300	10-1000

Table 3.1. Transmission lines implementation options.

The demonstration circuits that we present in this thesis operate at a sampling rate of hundreds of megahertz and therefore they require off-chip coaxial transmission lines. However, we believe that the advantages of transmission line ΣΔMs to implement data converters at very high frequencies may motivate more research on the field. As it has been shown in this chapter, a fully integrated solution would require that, apart from tackling the theoretical aspects of transmission line ΣΔMs, we would need to implement RF-MEMS devices which are still a field under research. This would exceed the scope of the thesis.

3.5 Mapping of ΣΔMs with Transmission Lines

3.5.1 Replacement of a continuous time integrator

A delay element may be implemented electronically by using a transmission line, as has been discussed in previous sections, with proper loads. If we consider that the signals traveling through the transmission line are going to be well below its cutoff frequency, the delay line behaves as a linear phase four pole with nearly constant attenuation. However, replacing the delays of a discrete time filter by transmission lines is not very practical as long as the transmission line should be embedded in the feedback loop of an amplifier, as for example, in an integrator (see section 2.4). There is a more convenient way to implement a modulator with transmission lines but it requires rearranging the modulator structure to fit with some basic building blocks that will be defined next.

The building blocks proposed in this chapter, implement an integrator seizing the impedance poles and zeroes of a transmission line with proper termination, and are shown in Figure 3.10. We will analyze a transmission line terminated with an open (Fig.3.10.a) or short (Fig.3.10.b) circuit, driven by a transconductor in series with a resistor and producing an electrical delay of T/2.

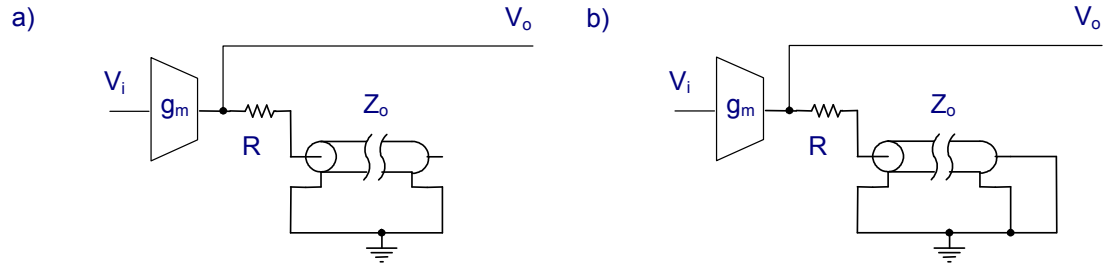

Figure 3.10. Integrators using transmission lines.

The input-output relationships for these two circuits are:

$$H_a(s)=\frac{V_o(s)}{V_i(s)}=g_m\left(R+Z_o\frac{1+e^{-sT}}{1-e^{-sT}}\right)$$
$$H_b(s)=\frac{V_o(s)}{V_i(s)}=g_m\left(R+Z_o\frac{1-e^{-sT}}{1+e^{-sT}}\right) \qquad (3.30)$$

A special case is when Z_0=R, gm*R=gm*Z_0=1/2:

$$H_a(s)=\frac{1}{1-e^{-sT}} \quad H_b(s)=\frac{1}{1+e^{-sT}} \quad f_s=1/T \qquad (3.31)$$

If we use sampling frequency f_s as defined in Eq.3.31, the circuit in Fig.3.10.a may replace a non delaying integrator in conventional discrete-time systems. Hence, these two building blocks allow the implementation of many of the existing ΣΔM topologies by moving all delays in the forward path of the signal after the quantizer, where they can be implemented with digital hardware. Also, the circuit in Fig.3.10.a allows building resonators that place poles at different frequencies than DC by cascading two integrators and adding negative feedback. This enables this architecture to implement band pass modulators as well. The circuit in Fig.3.10.b has its poles at multiplies of f_s/2 rather than at DC. It may find use to build bandpass CTΣΔ modulators as well.

As a practical example, we may observe in Figure 3.11 transconductor loaded with an open ideal transmission line and a resistor. If the input to the transconductor is a zero-order-

hold pulse train, this system may be shown to be equivalent to a discrete time integrator, if we sample the voltage in the transmission line.

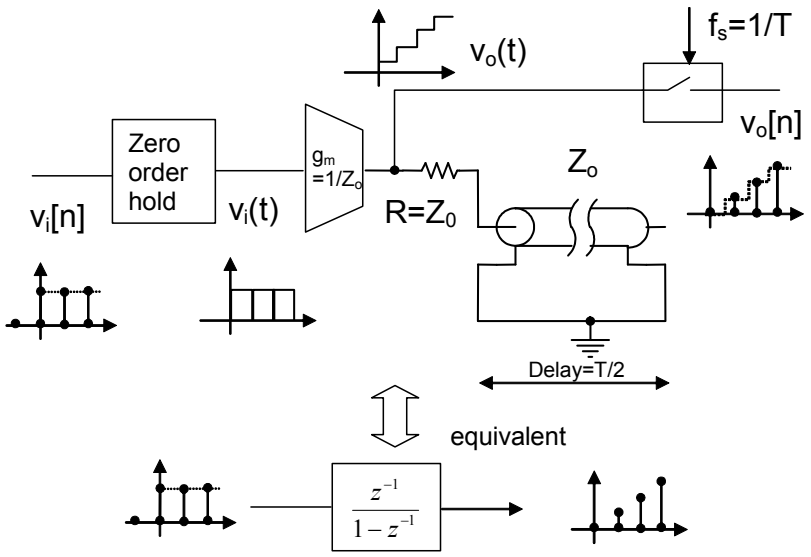

Figure 3.11. Equivalence between a discrete time integrator and a delayed continuous time integrator.

This formal equivalence is established in Eq.3.32, where L^{-1} represents the inverse Laplace transform:

$$V_o(s) = V_i(s) \cdot g_m \cdot \left(Z_0 + Z_0 \frac{1+e^{-sT}}{1-e^{-sT}} \right)$$
$$v_o[n] = L^{-1}\left(V_o(s)\right)\Big|_{t=nT} = 2g_m Z_0 \sum_{k=1}^{\infty} v_i[n-k] \tag{3.32}$$

Obviously, a practical implementation of Fig.3.11 will behave in a different manner if we consider real elements with finite bandwidth. However, the properties that make this circuit interesting for ΣΔMs with transmission lines will still be valid for feasible bandwidths. As we explain in section 2.3.5, some of the advantages of implementing a discrete system using a delayed continuous time system may be visualized by observing the time domain waveforms in Fig.3.11, where a unit step has been applied to the integrator. The sampler at the output of the transmission line would sample a stair case waveform with flat top steps. Hence, any uncertainties in the sampling point would yield the same output data if they are restricted to one clock period. Also, this property holds for uncertainties in the position of the zero order hold pulses in the input signal. In the case of a conventional continuous time integrator, (for instance a gm-C integrator), the output of the integrator would be a straight line and the timing uncertainties in the sampling clock would be reflected at the output as erroneous amplitude

levels.

3.5.2 Example: Design of a Second Order Low Pass ΣΔM

We will design a modulator which has the same NTF as the standard low-pass single-bit second order delta-sigma modulator [Nor96] but implemented as described in chapter 2. Figure 3.12 shows the block diagram of the proposed modulator, where the blocks named H, d_1 and d_2 represent the resonator of Fig.3.10. This architecture uses local feedforward coefficients d_1 and d_2 instead of multiple feedbacks from the quantizer. The reason for this is that the circuit to implement such coefficients is only a series resistor between the transconductor and the coaxial resonator, simplifying the converter architecture.

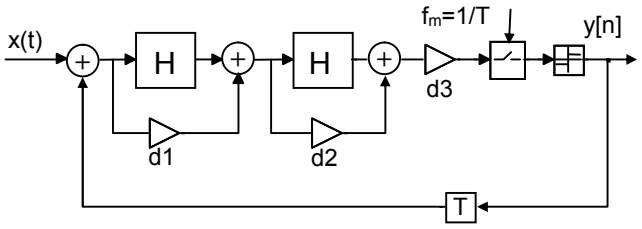

Figure 3.12. Model of a 2nd order 1-bit low pass transmission line ΣΔM.

It may be seen that a full clock cycle delay has been inserted in the feedback path as part of the loop filter. This delay may comprise the excess loop delay imposed by the hardware. To compute coefficients d_1, d_2 and d_3 we may apply the impulse invariance condition, but it is easier to solve the following equation between the Z and the Laplace transform representations of the NTF functions:

$$\begin{aligned} &NTF(z)\Big|_{z^{-1}=e^{-sT}} = NTF(s) \quad , \quad NTF(z) = \left(1-z^{-1}\right)^2 \\ &NTF(s) = \left(e^{-sT}\left(d_3H^2 + d_3(d_1+d_2)H + d_1d_1d_3\right)-1\right)^{-1} \end{aligned} \tag{3.33}$$

This equation yields d_1=1, d_2=3, d_3=-1/4. A simplified circuit that implements the system of Fig.3.12 is shown in Figure 3.13.

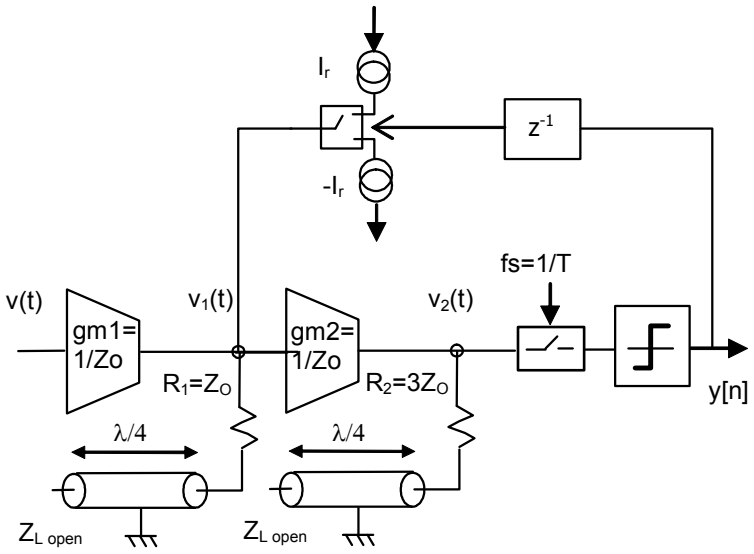

Figure 3.13. Schematic of the Second-order single-bit low-pass transmission line ΣΔM.

For an ideal transmission line, the input-output relationships of the circuit in Fig.3.13 will be:

$$v_y(t) - v_y(t-T) = g_m(R_1 + Z_0)\cdot v_x(t) + g_m(R_1 - Z_0)\cdot v_x(t-T) \tag{3.34}$$

A special case is when Z_o=R_1 and g_m=$1/Z_0$, as the circuit may replace the integrators in conventional discrete-time systems. This building block allows the implementation of most of the existing ΣΔM topologies, even bandpass modulators if configured as a resonator or with the line end shorted.

We will show two simulated measurements to demonstrate the properties of the transmission line ΣΔM proposed in Fig.3.13. Considering OSR=256, we will simulate the modulator in Fig.3.13 with a full scale tone in the middle of the signal band.

First, Figure 3.14 shows the modulus of the FFT of the simulated output of the transmission line ΣΔM of Fig.3.13 applying a -3dB low frequency sine wave at the input. The sampling clock (f_s) was set to $1/T$ to place the first NTF zero at DC and to match the following zero with the sampling frequency. The output sequence shows a noise spectrum that closely matches that of the second order ΣΔM in [Nor96]. Also if we compare this result with Fig.2.8, we may end up with the conclusion that the mapping mechanism that we propose in this chapter for transmission line ΣΔM is valid.

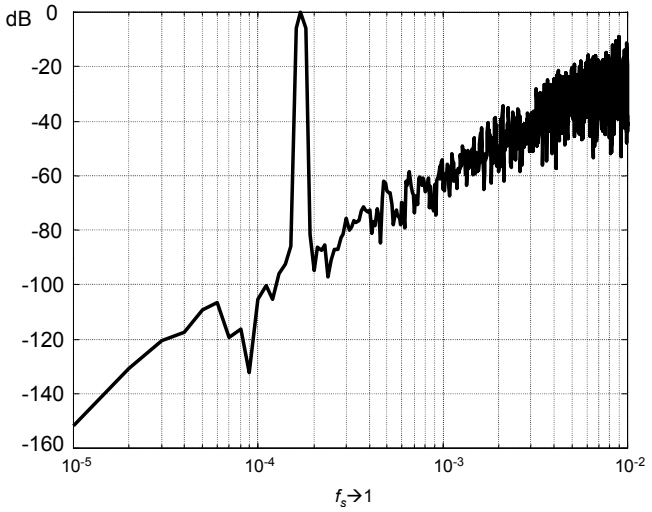

Figure 3.14. FFT of simulated output from the transmission line ΣΔM of Fig.3.13.

Second, we have measured the behavior of the transmission line ΣΔM of Fig.3.13 against jitter. The solid trace of Figure 3.15 represents the SNR of modulator of Fig.3.13 and the dashed trace represents the SNR of the standard second order CT-ΣΔM of Figure 3.16, for various jitter variances. The dotted line represents the SNR obtained by sampling the input signal without any quantization but using a clock with jitter, which is the performance limit of a discrete time modulator. As we may see, the delay based modulator reaches a maximum SNR of 85dB with a jitter $\sigma=3x10^{-3}T$ while the conventional integrator-based CT-ΣΔM requires a more stringent jitter specification of $\sigma=10^{-5}T$ to achieve the same SNR. In this simulation, the clock has independent random timing uncertainties with a uniform PDF. This result was predicted in chapter 2, and is one of the advantages that transmission line ΣΔMs has over existing CT-ΣΔMs.

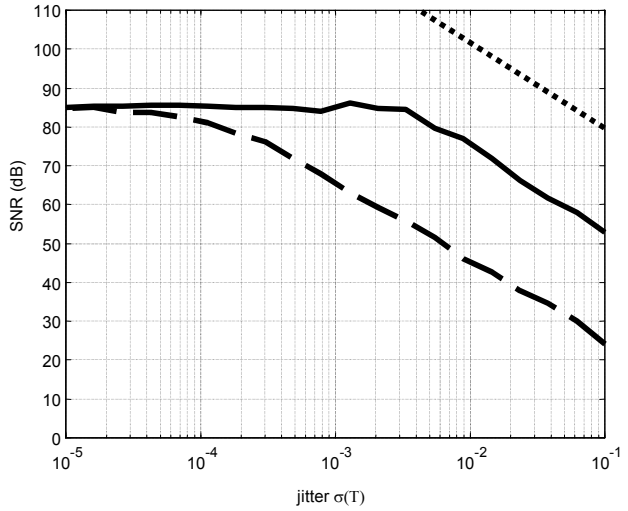

Figure 3.15. Simulation of three ΣΔMs under different jitter conditions. (···) discrete time, (—) continuous time with transmission lines (Fig.3.13) and (- - -) continuous time with integrators.

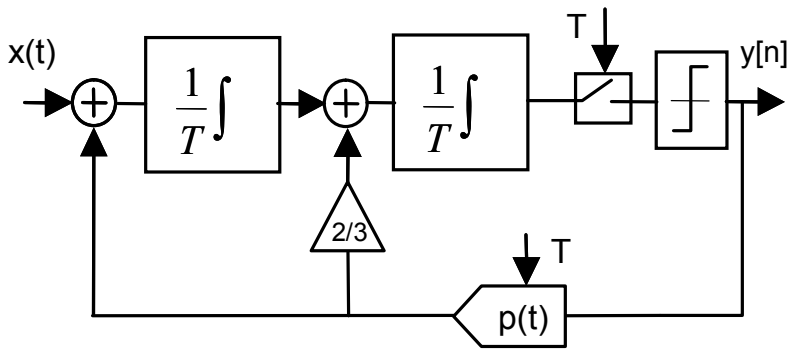

Figure 3.16. Standard second-order CT-ΣΔM.

3.5.3 Example: Design of a Second Order Band Pass ΣΔM

The structure of Fig.3.13 may be modified to have a band-pass noise transfer function. By replacing the transmission line resonators of Fig.3.13 by the same transmission line resonators with their end shorted to ground and changing the polarity of the feedback DAC signal y(t), the NTF obtained has zeroes at $(n+1)f_s/2$ Hz with n=0,1,2... The resonators require a transmission line with an electrical length equivalent to half a wavelength of the first desired NTF zero frequency. A single bit quantizer and a digital delay that matches the delay of the transmission line, complete the feedback loop.

This modulator structure has been simulated using a -6dB sine wave whose frequency is slightly shifted from the first NTF zero. Figure 3.17 shows the FFT of the output of the digital sampler. A detailed analysis of the simulation results reveals that the spectral noise density has a slope similar to that of a second order zero.

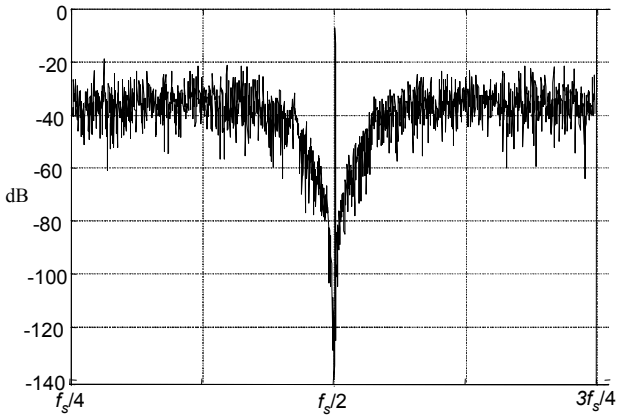

Figure 3.17. FFT of a 2nd order bandpass transmission line ΣΔM.

Figure 3.18 shows the NTF (solid) and STF (dotted) of the circuit.

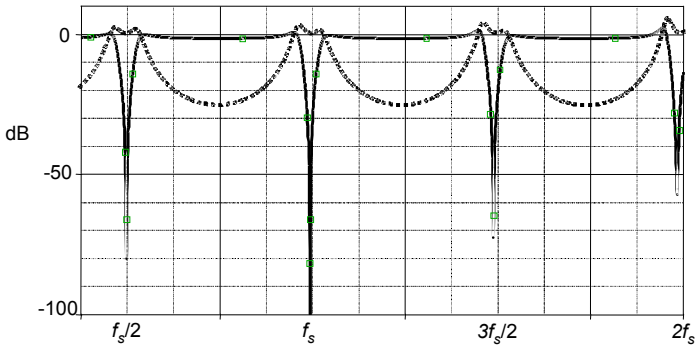

Figure 3.18. NTF and STF of a 2nd order bandpass transmission line ΣΔM.

CHAPTER 4

Non-Ideal Effects in ΣΔ Modulators Implemented with Transmission Lines

In this chapter we will describe some of the implementation problems and practical limitations of transmission lines ΣΔMs as well as the advantages of this new architecture.

In chapter 2 we have concluded that the main property of a transmission line ΣΔM is that its loop filter may be written as a Laplace domain transfer function which only depends on complex exponentials, $H(e^{-sT})$. This would require that a physical implementation is only realized with distributed energy storage elements. The presence of any lumped element such a concentrated capacitor or inductor will include in the loop transfer function a dependence on variable *s* in addition to complex exponentials. Then the eigenfunctions of the system will no longer have periods harmonically related, which is the basic property that equips transmission line ΣΔMs with advantageous features against conventional CT-ΣΔMs. These lumped capacitors or inductors are inherent to the physical dimensions of the wiring of the circuit and the parasitics that affect the semiconductors. In this chapter we will analyze these effects with the purpose of finding the right trade-offs between a feasible circuit and a modulator that benefits from using transmission lines.

As the main advantages of using a transmission line ΣΔM instead of a conventional CT-ΣΔM we may highlight the following:

- *Loop delay tolerance*

A common problem in standard CT-ΣΔMs is undesired loop delay [Che99], which is caused by delays in the feedback path, inherent to the hardware implementation. In most designs, this represents a deviation form the desired NTF which is compensated by increasing the order of the modulator or, if it does not cause instabilities, tolerated causing a SNR loss. However, in a transmission line ΣΔM, this delay may be included as part of the NTF as explained in chapter 2 and 3. Hence, this effect may be turned from a problem into a necessity of the design.

- *NRZ DAC pulse distortion*

Using a continuous time delay based loop filter also alleviates the problems caused by time-varying changes in the area of the feedback DAC pulses *p(t)*. One of such problems is DAC pulse distortion [Che99]. Time varying pulse distortion is due to unequal pulse areas for same DAC codes among different sampling periods. The unequal pulse areas are caused by ringing and non ideal rise and fall times in the feedback DAC when NRZ codes are used. If the implementation of the transmission line ΣΔM proposed in this thesis is used, the actual area of the pulses is not relevant, only the pulse value in the proximity of the sampling point, as explained also in chapter 2.

- *Clock jitter insensitivity in the DAC*

Another source of SNR degradation in a conventional CT-ΣΔM is jitter in the feedback DAC clock. The main reason for that is the same as before, jitter causes unequal pulse areas in the feedback DAC. Jitter in the sampling clock may also be considered. The noise introduced at the quantizer is spectrally shaped by the modulator in a standard CT-ΣΔM. However, [Her05] shows that in a transmission line modulator, jitter affects mainly at the quantizer, due to a different coupling mechanism. This will be studied in section 4.1, where we will show that in a transmission line ΣΔM, the shape of the DAC pulses *p(t)* may be time varying without SNR degradation, as long as the time domain waveform of each of the pulses takes always the same value at the sampling points.

- *Design parameters independence*

Due to the properties of transmission line modulators, the design parameters are independent of the sampling clock, only the length of the transmission lines determines the clock frequency and signal band location. In the case of a standard CT-ΣΔM modulator, most of the architecture coefficients are related to the sampling period, which forces to define such parameters in the design process. In transmission line ΣΔMs, only the bandwidth requirements of the transconductors and the maximum operating frequency of the sampler and DACs set the bounds for the clock rate.

On the other hand, a ΣΔM implemented with transmission lines has several circuit limitations that influence the design and performance of the modulator. These limitations are discussed in this chapter:

- *Effect of clock jitter in the quantizer.*
- *Bandwidth limitations of the active elements.*
- *Mismatch among the resonators of the loop filter.*
- *Parasitic capacitance and inductance on the resonator connections.*
- *Finite Q factor of resonators and transconductor load.*
- *Non-linear distortion due to:*
    - *Dynamic range of the State Variables.*
    - *Transconductor saturation.*

4.1 Clock jitter performance of transmission line ΣΔ modulators

As explained in chapter 2, section 2.4, the system replacement proposed in this thesis may be applied to any digital filter. In the particular case of a ΣΔM loop filter, this transformation may be of a special interest due to the timing error desensitization property analyzed in the previous chapters. The block diagram of such a ΣΔM using a continuous time filter with delays is shown in Figure 4.1.a, where all points that require a clock signal have been explicitly marked. Figure 4.1.b shows the equivalent DT-ΣΔM, where the input sampling clock has also been marked. The retarded linear system H_a will have two inputs $v_1(t)$ and $v_2(t)$, and one output u(t). For every input, a pulse shaper is required to transform a discrete time sequence into a pulse train. This is obviously required in the feedback path from the quantizer as y[n] is a sequence of quantized values. However x(t) is a continuous time signal and the usual practice in CT-ΣΔMs is to remove the input sampler and pulse shaper S_1. We will propose to remove this input block (marked in dashed line) as well in the foregoing explanations, but to formally analyze the block diagram of Fig.4.1.a we will keep it for the moment. Assuming that all clock signals T_1, T_2 and T_3 operate at points $t=nT$ without timing errors, the behavior of the ΣΔM using delays may be described as in section 2.4 (see Eq.2.34).

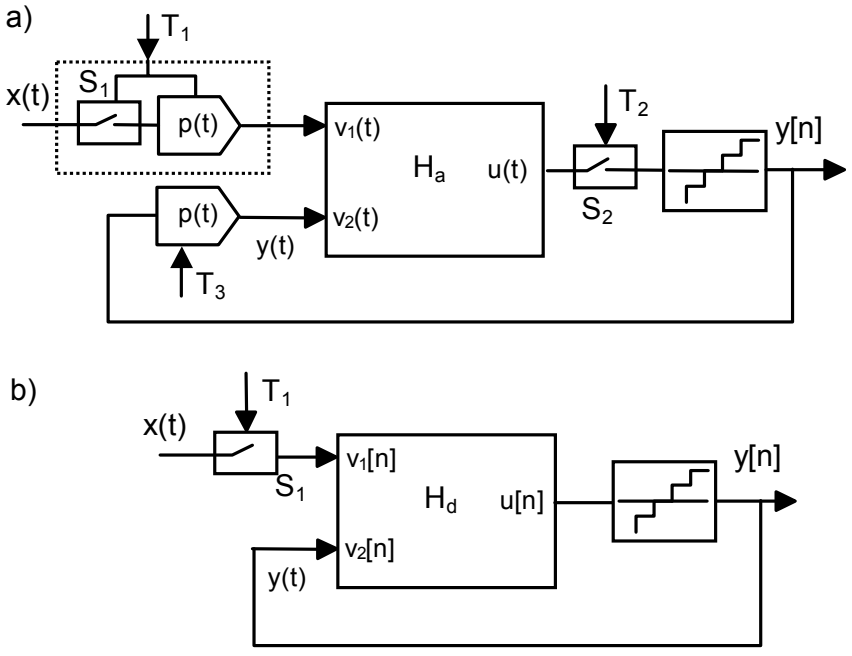

Figure 4.1. Block diagram of a) a ΣΔM with delays and an input sampler and b) a DT-ΣΔM.

The models of Fig. 4.1.a and 4.1.b may be made completely equivalent even when

some of the clocks are subjected to clock jitter. In both models, the clock jitter of T_1 will degrade the resulting SNR as samplers S_1 introduce some error at the input of both modulators that cannot be distinguished from the signal itself. However, as a difference with an integrator-based CT-ΣΔM, the system of Fig. 4.1.a is not affected by clock jitter in T_2 and T_3 if some conditions equivalent to Eq.2.21 are accomplished.

For instance, this fact can be observed in a time domain simulation of the modulator of Figure 4.2 (second order lowpass ΣΔM implemented with delays and input sampler). We are going to simulate the behavior with a sinusoidal input signal when the DAC clock and the quantizer clock (T_2 and T_3 of Fig.4.2) have jitter, but the input sampler (T_1) is ideal. Figure 4.3.a represents the input to the quantizer without jitter. Figure 4.3.b represents the input to the quantizer when the clock jitter of T_2 and T_3 have a rms value of σ=0.1%T.

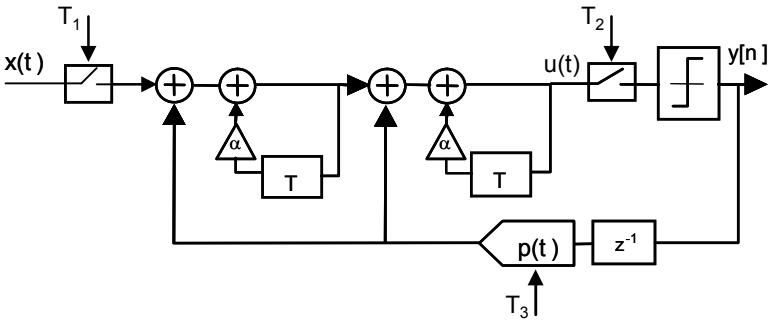

Figure 4.2. Second order lowpass ΣΔM with delays an input sampler.

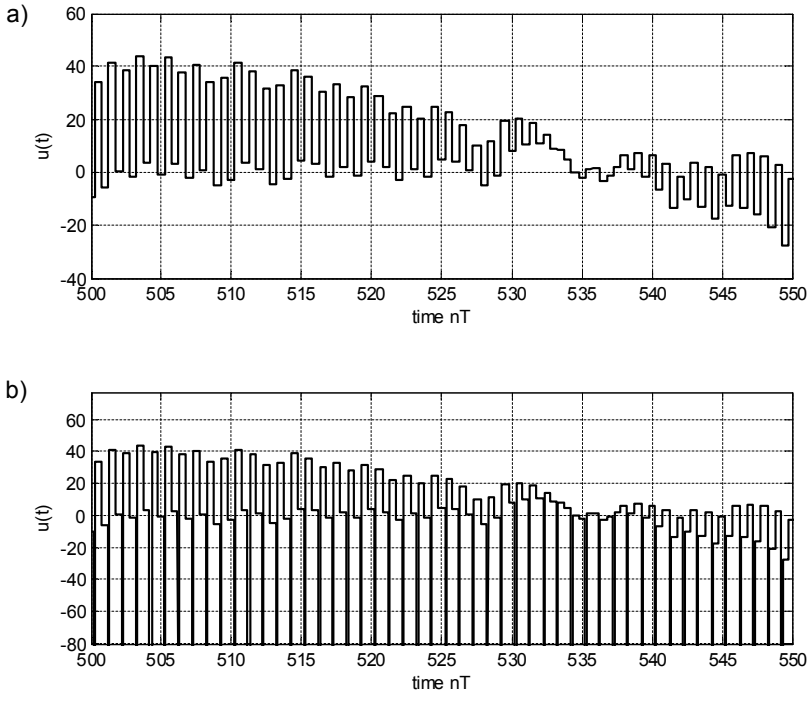

Figure 4.3. Input to the quantizer with jitter in the DAC and the quantizer clocks of Fig.4.2.

As can be seen jitter is accumulated by the integrators in the edges of the signal whereas in the hold phase of the input sampler and DAC, the signal exhibits a flat top which would make any jitter in sampler T_2 irrelevant. If the jitter in T_3 is constrained to a moderated value its effect in the sampled signal could also be neglected.

If the block diagram of Fig. 4.1.a were used in a practical CT-ΣΔM, there would be no advantage in using the proposed architecture. One of the motivations to use a CT-ΣΔM is to avoid using the input sampler S_1. We may remove this sampler but then the influence of clock jitter will be different.

In this new situation, there will be no sampling error directly introduced into the input signal, as sampling will take place at the quantizer input in S_2. This is a favorable situation because the errors produced by clock jitter in sampler S_2 will be spectrally shaped by the sigma-delta loop. On the other hand, we will show that the power of the error signal introduced by clock jitter at S_2 depends on the clock source and also on the open loop filter gain, which may be very large within the band of interest of the modulator. The proposed architecture may be an advantageous replacement of conventional CT-ΣΔMs if there is a compromise between the open loop response and the clock jitter variance. As we will see, this compromise can be found without difficulty for most modulators.

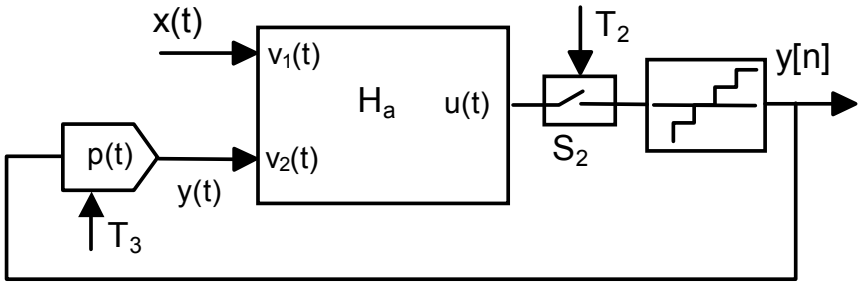

Figure 4.4. Block diagram of a ΣΔM with delays and without input sampler.

We are going to quantify the effect of clock jitter in the model of Fig. 4.1.a when S_1 is removed. Figure 4.4 represents the same system as Fig. 4.1.a with this input sampler removed. With this figure we may rewrite the system equations as follows:

$$u[n] = \sum_{m=0}^{\infty} h_{a1}[m] \cdot x((n-m)T + \Delta T_2[n]) + \\ + \sum_{m=0}^{\infty} h_{a2}[m] \sum_{k=0}^{n} y[k] \cdot p((n-m-k)T + \Delta T_2[n], n) \tag{4.1}$$

In this equation, we may impose some conditions to the shaping pulse *p(t)* operated by clock T_3 to avoid the influence of clock jitter in the feedback pulse (see chapter 2):

$$\forall k \le n \begin{cases} T - \Delta_{r3}[k] < \Delta T_2[n] \\ T - \Delta_{f3}[k] > \Delta T_2[n] \end{cases} \tag{4.2}$$

Using the definition of *p(t)* in Eq.2.18 we may write Eq.4.1 as:

$$\begin{aligned} u[n] &= \sum_{m=0}^{\infty} h_{a1}[m] \cdot x((n-m)T + \Delta T_2[n]) + \\ &+ \sum_{m=0}^{\infty} h_{a2}[m] \cdot y[n-m] \end{aligned} \tag{4.3}$$

We can see that clock jitter only influences the samples of x(t) but in a different manner as in the block diagrams of Fig. 4.1, because the sampling error $\Delta T_2[n]$ is simultaneously applied to all the samples memorized in the delays of the filter. We can make an approximated analysis of the sampling error using the derivative of x(t):

$$\begin{aligned} u[n] \approx u_{ideal}[n] + e[n] &= \left(\sum_{m=0}^{\infty} h_{a1}[m] \cdot x((n-m)T) + \right. \\ &\left. + \sum_{m=0}^{\infty} h_{a2}[m] \cdot y[n-m] \right) + \Delta T_2[n] \sum_{k=0}^{n} h_{a1}[k] x'(nT - kT) \end{aligned} \tag{4.4}$$

The term $e[n]$ in Eq.4.4 represents a random variable $\Delta T_2[n]$ multiplied by the samples of the derivative of the input x(t) filtered by the loop filter. This error is applied along with the ideal input to the quantizer; hence its spectra will be shaped by the sigma-delta loop provided that this error signal has a finite power.

We may decompose the error term as:

$$e[n] = \Delta T_2[n] \sum_{k=0}^{n} h_{a1}[k] x'(nT - kT) = e_T[n] \cdot e_{dx}[n] \tag{4.5}$$

where $e_T[n]$ is a random sequence and $x'[nT]$ is a deterministic sequence which may be considered uncorrelated with $e_T[n]$ and of finite power. Hence, the only requirement is that the output of the open loop filter is stable. A loop filter made up of a cascade of ideal integrators would have an output with infinitely growing amplitude and the jitter errors would be accumulated.

As practical circuits never have an infinite gain, we only need that the gain in the band of interest and the expected jitter power are properly adjusted to yield the required SNR when the jitter error is shaped by the loop filter. To quantify the relation between jitter variance σ_T^2 of the clock signal T_2 and the in-band gain of the loop filter, we will analyze the case of a generic sigma-delta modulator when a tone of amplitude A and frequency ω_o is applied to the input:

$$\sigma_e^2 = \sigma_{dx}^2 \cdot \sigma_T^2 = \sigma_T^2 \cdot \frac{A^2 \omega_0^2}{2} \cdot \left| H_{a1}(j\omega_0) \right|^2 \tag{4.6}$$

The graph of Figure 4.5 represents the relation between the clock jitter sigma and the open loop gain such that the quantization noise power equals the power of e[n] given by Eq.4.5 in a single-bit modulator, using a full scale test tone shifted $f_s/128$ from the center of the signal band. It must be noticed that both quantization and jitter noises are assumed white and shaped by the same NTF. The solid line represents a low pass modulator, the dashed line a band pass modulator with the signal band located at π/4 and the dotted line a band pass modulator at π/2.

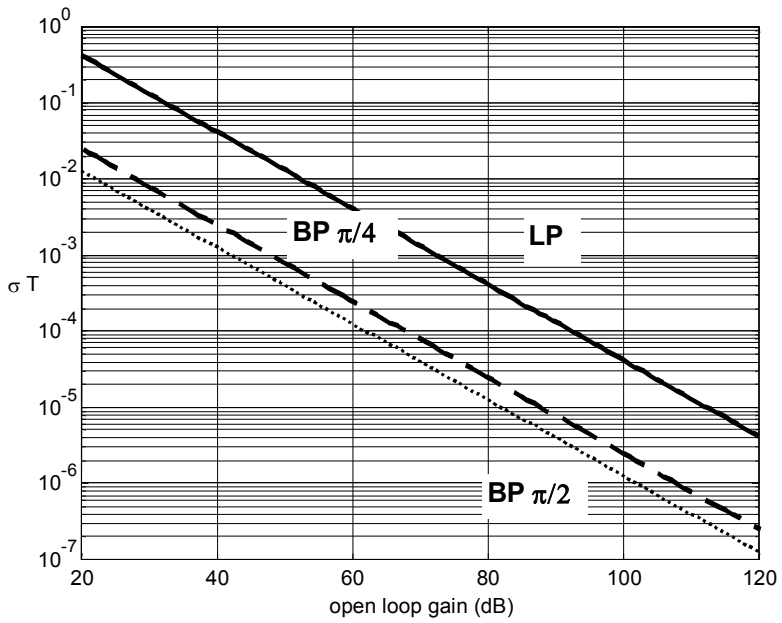

Figure 4.5. Maximum jitter σ (ref. to T) as a function of the open loop gain (dB).

The predictions of Eq.4.6 are conservative if we consider the SNR degradation due to jitter which is a more relevant figure of merit. A better estimation of the jitter sigma may be achieved by simulation of an integrator based CT-ΣΔM and the equivalent delayed-based ΣΔM operated by the same clock.

To validate practically the theory exposed in this section, we are going to apply its results to the second order ΣΔM implemented with transmission lines from chapter 3 (see Fig.3.12 and Fig.3.13).

We will analyze the clock jitter sensitivity of the modulator assuming infinite bandwidth but finite output resistance of the transconductors and using the prediction of Eq.4.6. This will be done by a time domain simulation of a behavioral model of the block diagram of the modulator of Fig. 3.13, simulated with jitter and without jitter, but injecting a white noise source with the power predicted by Eq.4.6 at the quantizer.

Figure 4.6 shows a plot of the SNR achieved with a -4dBfs tone considering an OSR of 128. The solid trace represents the predictions of Eq.4.6 and the dashed trace represents the simulations using a clock with jitter. In both cases the modulator has a finite open loop DC gain of 80dB.

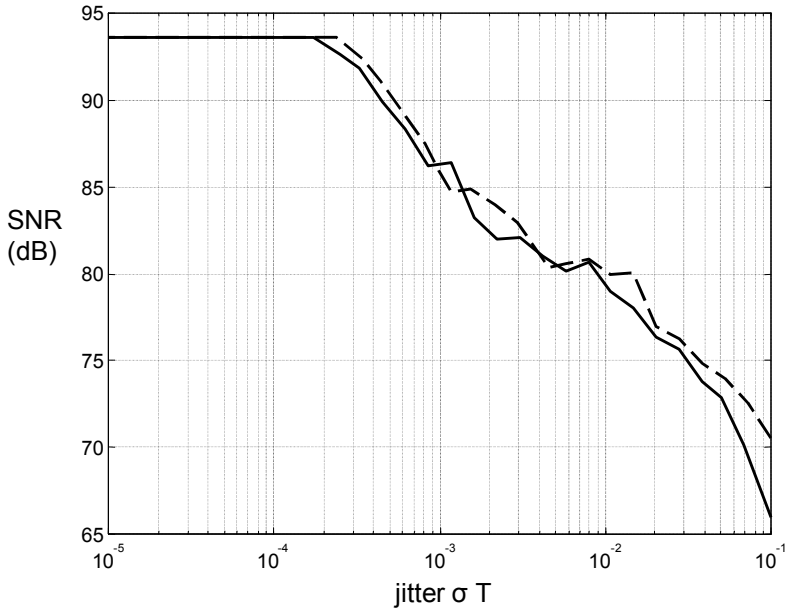

Figure 4.6. Predicted and simulated effect of jitter in a second order TL-ΣΔM.

It may be seen that the simulation and the theoretic prediction match except for high jitter variances. For jitter variances smaller than $2x10^{-4}T$, the SNR of the modulator is dominated by the quantization noise instead of jitter, as predicted by Fig.4.5.

4.2 Effect of finite bandwidth in active elements

The systems studied so far rely on the principle that they produce linear combinations of delayed signals. In essence, this means that a pulse train weighted by a sequence will be processed into another pulse train whose shaping pulse has the same shape as in the original sequence if the pulse is of a finite duration equal to the basic delay. If we investigate this fact further, we would require that all signal processing elements such as adders, delays and gains operate with signals which are not band limited (for instance, a zero order hold pulse train). As long as practical circuits always have a finite bandwidth, any of such implementations will have a deviation from its ideal behavior which is related to this bandwidth limitation. As a consequence, the jitter insensitivity property that we have discussed in previous sections will also be restricted by the finite bandwidth effects. In this section we will try to quantify the trade off between the performance of a practical delay based ΣΔM and the bandwidth of its active components.

A linear system that requires both, delays and derivatives to be modeled, is complex to handle. A simpler approach can be applied if we restrict the analysis to a system where the finite bandwidth effects can be separated from the delays allowing the whole system to be expressed as a cascade of a purely retarded linear system and a linear system expressed by differential equations only. This separation will be possible if there are no feedback loops involving both delays and finite bandwidth elements. As we have seen in chapter 2 and 3, there are practical ways to implement integrators using a delay element without the need of a loop with a summing amplifier of finite bandwidth, as it would be required in Fig.2.6.b. Hence, the case which will be analyzed here is really meaningful in practice.

Figure 4.7 depicts a practical system to synthesize a discrete time filter using the system equivalence of Fig.2.1. The finite bandwidth effects of all components have been separated in a transfer function H(s) from the delay transfer function $H(e^{sT})$. If we make the block arrangement of Fig.4.7, the pulse train v(t) will be filtered by H(s) so, we may consider that this system behaves as the original one where the shaping pulse p(t) has been replaced by another pulse $p_h(t)$ (bottom graph of Fig.4.7). This new pulse is the convolution of p(t) with the impulse response of H(s). The effect that we may expect is that the pulse $p_h(t)$ is no longer of

finite duration, so we cannot exactly accomplish condition of Eq.2.18 and we will have an inter-symbol interference effect among the successive samples of v[n].

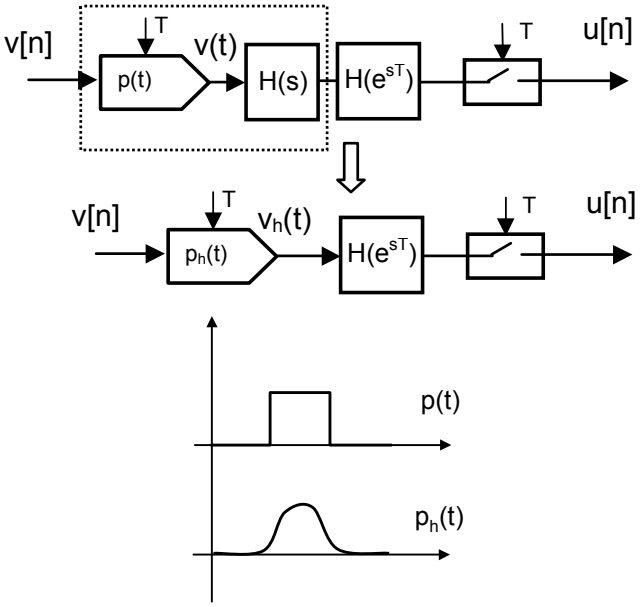

Figure 4.7. Separation of the delay transfer function.

This by itself is not a problem and it would suffice that we compensate $H(e^{-sT})$ such that the impulse response of the overall system matches again with the desired discrete time system. However, the clock jitter insensitivity property will be affected because it completely relies in the fact that the pulses p(t) are of finite duration. It may be expected that clock jitter influence is progressive with bandwidth decrease, so we could try to establish the trade off between the overall system bandwidth expressed by H(s) and the clock jitter influence.

We may rewrite Eq.4.1, assuming that pulses *p(t)* are generated with some timing uncertainty $\Delta T[n]$:

$$u[n] = \sum_{k=0}^{\infty}\left(\sum_{m=0}^{\infty} h_a[m]\cdot v[k-m]\right)\cdot p_h(nT - kT - \Delta T[k]) = \\ = \sum_{k=0}^{\infty} u_i[k]\cdot p_h(nT - kT - \Delta T[k]) \tag{4.7}$$

Sequence $u_i[n]$ is what could be expected from the equivalent ideal discrete time system. We may decompose u[n] into a term representing the ideal system output without clock jitter and an additive jitter error term. This decomposition may be accomplished by approximating the effect of the timing uncertainties $\Delta T[n]$ using the derivative of $p_h(t)$:

$$p_h[n] = p_h(t)\big|_{t=nT} \qquad p'_h[n] = \left.\frac{dp_h(t)}{dt}\right|_{t=nT}$$
$$u[n] = u_i[n] * p_h[n] + ((v[n]\cdot \Delta T[n]) * p'_h[n]) * h_a[n] \tag{4.8}$$

We have represented a discrete time convolution by *. Eq.4.8 allows to estimate the trade off between the loop bandwidth and the noise power that is injected in the feedback loop of a CT-ΣΔM modulator, as well as to define a block diagram of the delay-based modulator, considering clock jitter with a band-limited loop. This model is depicted in Figure 4.8.

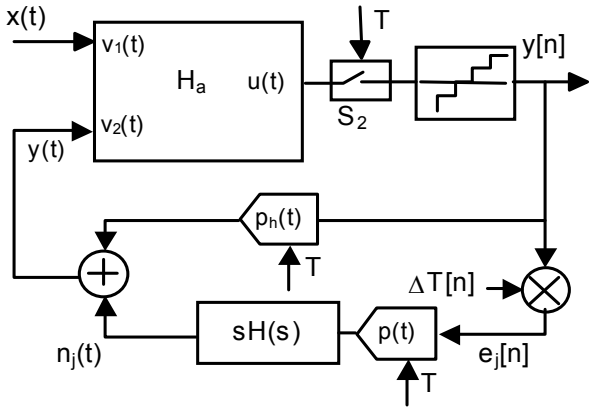

Figure 4.8. Clock jitter noise model of a delay based ΣΔM with finite bandwidth components.

The error component $n_j(t)$ will be indistinguishable from the input signal x(t). As the errors introduced by S_2 are spectrally shaped by the modulator loop under the conditions expressed in previous section, error $n_j(t)$ will be the dominant source of SNR degradation in a practical ΣΔM modulator constructed with delays. To estimate the variance of $n_j(t)$, we may assume that sequence $e_j[n]$ is a white noise and that $y[n]$ is uncorrelated with $\Delta T[n]$. Then, using the Fourier transform of $p'_h[n]$ we have:

$$P_{dh}\left(e^{j\omega}\right) = \Im\left(p'_h[n]\right)$$
$$\sigma_{nj}^2 = \frac{T^2\cdot\sigma_{\Delta T}^2\cdot\sigma_y^2}{2\pi}\cdot\int_0^{2\pi}\left|P_{dh}\left(e^{j\omega}\right)\right|^2 d\omega \tag{4.9}$$

The power of $y[n]$ will be one for single bit modulators and smaller than one and close to the power of the input signal for multibit modulators. Considering σ_y=1, a bound of the jitter noise power in the band of interest may be approximated by the following formula:

$$\sigma_{nj}^2 \le \eta_j \cdot Eb_j$$
$$\eta_j = \frac{1}{2\pi}\left(\frac{\sigma_{\Delta T}^2}{T^2}\right),\ Eb = T^2\int_{-\pi/R}^{\pi/R}\left|P_{dh}\left(e^{j\omega}\right)\right|^2 d\omega \tag{4.10}$$

We have decomposed Eq.4.10 into two terms. One is η_j which represents the spectral density of the clock jitter noise referred to the clock period and Eb_j which may be considered an equivalent jitter noise bandwidth. The jitter noise bandwidth depends on the over sampling ratio R, the order of the modulator and the bandwidth of the active elements.

As an example, we have evaluated numerically Eb_j for the case of an m-th order, low-pass modulator using a cascade of integrators similar to the one depicted in Fig.3.16. We will consider that each integrator has a bandwidth ω_0 , which is k times larger than the sampling frequency. Then, we may group the transfer functions of every integrator in the loop and the zero order hold pulse into a single transfer function as follows:

$$\omega_0 = k\omega_m = \frac{2\pi}{T}$$
$$H(s) = \left(\frac{\omega_0}{s+\omega_0}\right)^m \cdot \left(\frac{1-e^{-sT}}{s}\right) \tag{4.11}$$

Figure 4.9 shows the numerical evaluation of Eq.4.10 assuming the feedback pulse and amplifier bandwidth expressed by Eq.4.11, considering the cases m=2 and 3 and an over sampling ratio OSR=128.

Fig. 4.9 allows to estimate the bandwidth required for the active circuitry in this CT-ΣΔM, such that the SNR of the modulator is dominated by quantization noise rather than by clock jitter noise. Fig.4.9 may be tailored to different over sampling ratios, modulator orders and location of the band of interest.

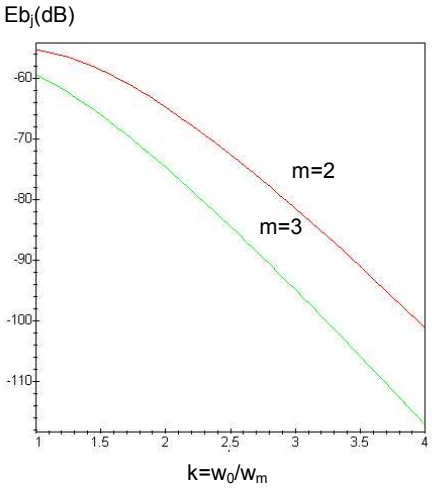

Figure 4.9. Clock jitter attenuation factor for a second and third order modulator with open loop amplifiers and NRZ feedback as a function of the amplifier bandwidth.

As a consequence of the previous discussion about jitter and limited bandwidth effects, making analytical calculations in a design may be a complicated task and we will prefer to do an estimation of the design parameters by time domain simulations.

In order to address the problem of finite bandwidth in the resonators and jitter of the modulator, we will do transient simulations using the second order transmission line ΣΔM of Fig.3.11. We may model finite bandwidth by placing a first order low pass function after every resonator in Fig.3.13. The low pass functions will convolve with the pulse *p(t)* making it loose its finite duration. This will degrade the SNR of the modulator, although the proposed structure may still be used compromising jitter sensitivity with resonator bandwidth.

Figure 4.10.b shows the output spectra of the second order transmission line ΣΔM in Fig.3.13 for a random jitter with $\sigma=0.01T$ and whose resonators are restricted by a dominant pole at 3.5 times the sampling frequency (f_s). This is comparable to the gain-bandwidth product required for opamps in a conventional CT-ΣΔM [Che99]. Figure 4.10.a shows the behavior of modulator in Fig.3.13 with an ideal clock. In all previous simulations, transconductor saturation has been included and the delay between the quantizer and the DAC has been reduced to compensate the phase shift in the transconductor low pass functions.

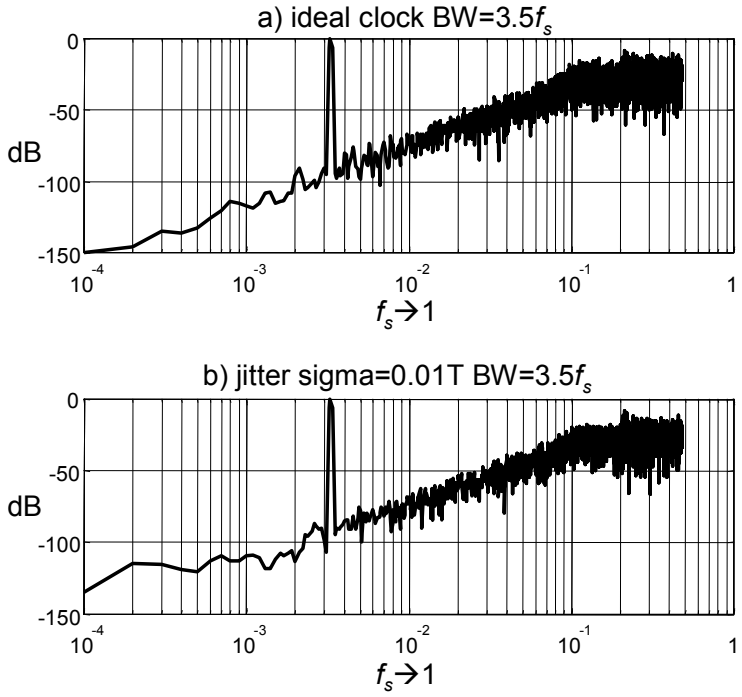

Figure 4.10. Effect of finite bandwidth on jitter sensitivity.

We may conclude from Fig.4.10 that in this case, finite bandwidth of transconductors and resonators should not be more restrictive than in a conventional CT-ΣΔM. Although, in the transmission line ΣΔM jitter of the clock can be relaxed.

As an example of this jitter performance, Figure 4.11.a shows variable $v_2(t)$ of the modulator in Fig. 3.13 with a null input and a clock with a jitter variance of $0.01T$.

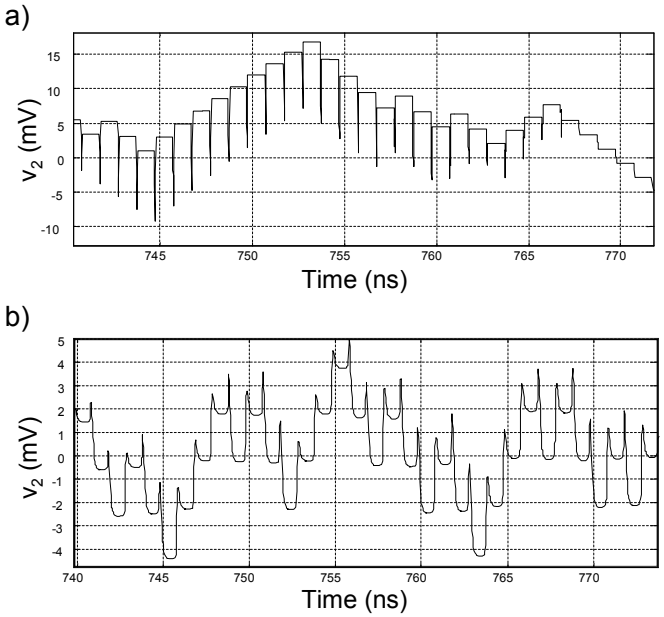

Figure 4.11. State variables in a transmission line ΣΔM. a) Ideal. b) Transconductors with finite bandwidth.

Clock jitter insensitivity is degraded when we consider that circuit elements have a finite bandwidth. Then, the zero order hold pulses of the feedback are smeared in time and occupy more than a single clock cycle producing an effect similar to the intersymbol interference in a communication system. Figure 4.9.b reproduces the same situation as Fig.4.9.a but the transconductors have a bandwidth of 3.5 times the sampling frequency. As we can see, active element bandwidths in the range of those of conventional CT-ΣΔMs still provide a qualitative advantage, as the feedback signal is still flat close to the sampling point.

4.3 Mismatch and parasitic effects in the resonators

Parasitics at the connection of the transmission line and the circuit also present design challenges. There is parasitic inductance to the resonator and parasitic capacitance in parallel with the resonator, which is exacerbated when using an external transmission line. When we examine the parasitic model of a resonator, the parasitic capacitance and inductance are caused by the pads and bonding wires. These alter the frequency-dependent impedance of the

transmission line, and affect the resonant frequencies. The poles of the input impedance of the transmission line are a function of the parasitic capacitance and inductance of the transmission line, and have terms in s, as well as in e^{-sT}, destroying the ideal locations of the loop filter poles.

Mismatch between the different resonators of a transmission line ΣΔM is another effect that must be taken into account. Transmission lines are fabricated with a tolerance in its electrical length that can be very tight. However, even transmission lines with tolerances of 1% may need some kind of trimming if they are used to implement narrowband bandpass converters. The attenuation of the quantization noise is proportional to the product of the gains of all resonators in the band of interest. Hence, any detuning among the resonance frequencies diminishes the average attenuation and worsens the SNR.

These two problems can be solved by placing a parallel trimming capacitor in the transmission line and correcting the nominal electrical length of the transmission line to match with the desired resonance frequency, at least in the band of interest of the modulator.

Assume that we chose an electrical length of the transmission line slightly shorter than required by the nominal resonance frequency. The total capacity resulting from the parallel of the parasitic capacitor and the trimming capacitor (C_P) may correct the phase of the resonator impedance increasing the effective transmission line delay [Her05].

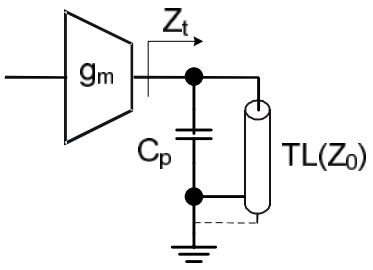

Figure 4.12. Transmission line resonator with parasitic/trimming capacitance.

If we calculate the impedance seen by transconductor of Figure 4.12 loaded with a transmission line in parallel with a capacitor we obtain:

$$Z_t = \frac{Z_0\left(1-e^{-sT}\right)}{\left(C_p Z_0 s+1\right)+e^{-sT}\left(1-C_p Z_0 s\right)} \tag{4.12}$$

The poles of Eq.4.12 are no longer evenly spaced and the resonance frequencies no longer match with the ideal ones. This effect is shown in Figure 4.13.

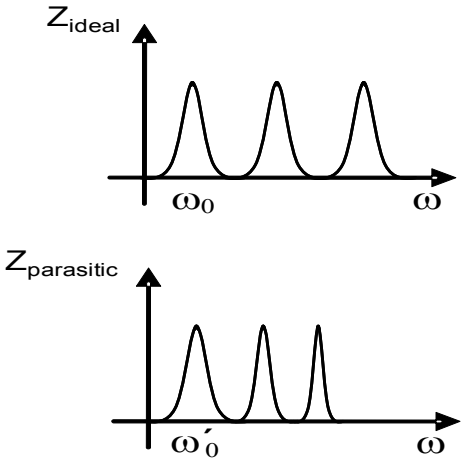

Figure 4.13. Transmission line impedance w/o and with parasitics.

We can correct approximately the total delay time by an amount T_c by giving the proper value to C_P. This can be accomplished using the following expression:

$$T_c = \frac{\tan^{-1}(2\pi f_s Z_0 C_p)}{2\pi f_s} \tag{4.13}$$

Figure 4.13 shows the electrical model of the assembly of a transmission line together with the parasitic capacity of a pad and a trimming capacitor. The lower plot in Fig.4.14 shows the impulse response of the resonator and the effect of the trimming capacitor. The frequency domain equivalent of this trimming is to adjust the first pole of the resonator to its nominal frequency.

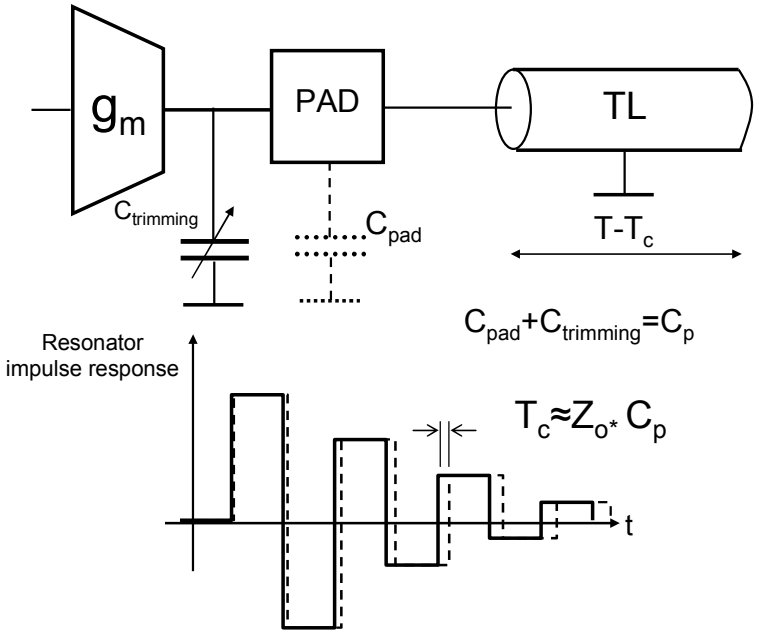

Figure 4.14. Compensation of parasitic and mismatch effects in a transmission line.

This way, the mismatch between the transmission line lengths of the different resonators could be ideally adjusted to zero. For 50Ω transmission lines, circuit simulations and measurements in [Her06] [Pre07] have shown that an estimated capacitor of C_P=2pF do not severely degrade the SNR and clock jitter properties, if resonant frequency of the transmission line is around hundreds of MHz, while allowing to trim-off the mismatches and compensate the parasitic capacity of the pads.

Moreover, in transmission line ΣΔMs, the resonator length is designed such that the multiple resonance frequencies fold into the fundamental frequency after sampling. Deviations from the ideal resonator length perturbate the pole and zero locations of the NTF, not only due to the detuning but also due to incorrect aliases. This results in a degradation of the modulator performance, which cannot be corrected with the method described before. The lowpass implementation is far more immune to non-idealities than the bandpass implementation. In the lowpass implementation, the fundamental resonant frequency is always 0, regardless of the transmission line length. In the bandpass implementation, the resonant frequency shifts around of the designed notch frequency, thus affecting both the STF and NTF.

The effect of resonant frequency on the STF is exacerbated for signals in higher Nyquist zones [Kap05]. The SNR is more sensitive to mismatch among the resonators when the signal is in the second and consecutive Nyquist zones. With a non-ideal length, the multiple resonator harmonics no longer alias into the fundamental harmonic after sampling. The harmonics play a large role in the STF, and the first harmonic largely determines the NTF, especially when the NTF has RC time constants that attenuate DAC harmonics. Thus, the STF and NTF have misaligned center frequencies and resonator lengths which mean that an optimal NTF may lead to low STF values.

4.4 Finite Q factor of resonators

A well known limitation of standard bandpass CT-ΣΔM is the Q factor of the loaded resonators of the loop filter [Sch06]. One of the main motivations of this thesis was the advantage in replacing a LC resonator with a transmission line due to its better Q factor. The author has found experimentally that the SNR limiting factor is the output impedance of the transconductor that drives the transmission line rather than the loss in the transmission line itself.

In a practical situation, the transconductor will have finite output impedance. This finite output impedance can degrade the performance of the modulator. The transfer function TF realized by Figure 4.15 looks like:

$$TF = R_{OUT} // Z_0 \frac{1 + Ae^{-sT}}{1 - Ae^{-sT}} + R \tag{4.14}$$

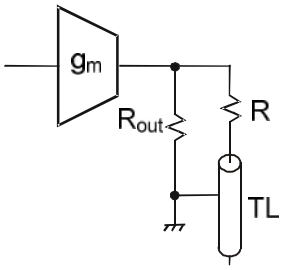

Figure 4.15. Transconductor with output impedance followed by transmission line resonator.

If R = Z_0, then Eq.4.14 can be simplified as follows:

$$TF = \frac{2Z_0}{\left(1 + \frac{2Z_0}{Rout}\right) - Ae^{sT}} \tag{4.15}$$

We assume that the position of the poles of TF will have the largest influence on the performance of the modulator and not the gain of TF or the position of the NTF poles. As a result, we can model the finite output impedance with the loss parameter A.

$$A = \frac{R_{OUT}}{R_{OUT} + 2Z_0} \text{ if R = } Z_0 \tag{4.16}$$

Considering typical values, the transmission lines can achieve a maximal Q-factor associated to the first resonance frequency of 5000. Since the Q-factor in terms of the loss parameter A is about:

$$Q \approx \frac{2}{1 - A} \tag{4.17}$$

This means that:

$$A \approx 1 - \frac{2}{Q} \leq 0.9996 \tag{4.18}$$

The loss parameter A has an influence on the SNR performance as well as on the jitter performance. Jitter will introduce an upper limit for A, the SNR requirement a lower limit.

Also, in a standard CT-ΣΔM, another problem associated with subsampling operation is the dependence of the loop filter H(s) with the subsampling ratio to obtain a modulator H(z) equivalent to the Nyquist rate modulator, when finite Q of resonators is considered. As an advantage of transmission line ΣΔMs the frequencies of the notches of the NTF of a bandpass modulator are not affected by the subsampling ratio when finite Q values are considered [Her08].

4.5 Non-linear distortion

The feedback loop of the transmission line ΣΔM is essentially designed so the DAC cancels the input at the transmission line node (see v_1 and v_2 in Fig.3.13). However, the input is designed to be narrowband, while the DAC output has a wide bandwidth. While the DAC can cancel the input at one frequency, it does not at the harmonics of the DAC signal. These harmonics can feed into the resonator higher pole locations and create very large voltage swings.

In [Pre07] a simulation of a bandpass transmission line ΣΔM is realized in order to estimate the dynamic range of the state variables. The difference between the peak of state variables in continuous time and the maximum values in the sampling instants is produced by the mismatch between the feedback DAC spectrum, which has sync shaped aliases, and the input signal with no aliases.

As shown in Figure 4.16, the DAC aliases would be suppressed by the loop filter of a conventional CT-ΣΔM, but with a transmission line loop filter, the DAC aliases are amplified by the higher resonances of the transmission lines, which create large instantaneous voltage values in the transconductors, far from the sampling points.

To prevent this effect, the Q_0 of the resonators and the transconductor bandwidth can be deliberately lowered. While this reduces the peak SNR, it also prevents high resonances values which may lead to saturation. Also a voltage clamp can be placed at the output of each transconductor [Kap05].

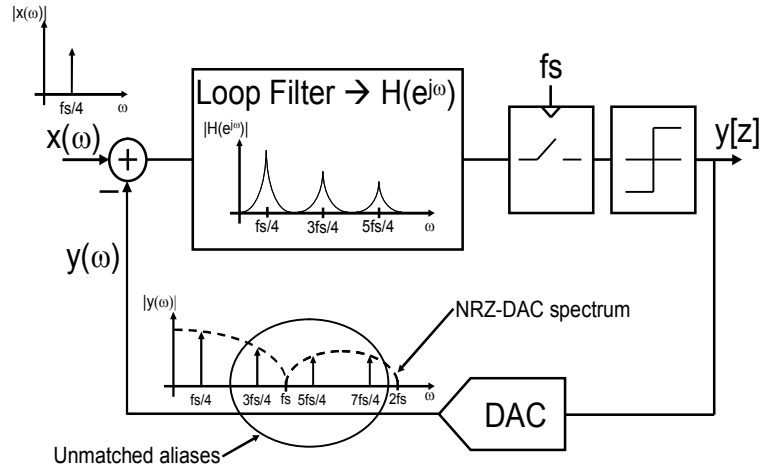

Figure 4.16. Effect of DAC aliases in the state variables in a transmission line ΣΔM.

There should be a trade off between the SNR achievable due to the Q_0 factor, the dynamic range of the state variables and the minimum voltage that needs to be resolved by the quantizer. To evaluate this problem, in [Pre07] a simulation of a bandpass ΣΔM has been made including a saturation model for the transconductors. The result of this simulation shows that there is no significant degradation compared with the ideal performance of the modulator.

The main problem encountered in the implementation of bandpass transmission line ΣΔMs is distortion [Pre07] [Her06], which is responsible of the reduction in the performance of the modulators. This effect is due to the large state variables outside the sampling points, as explained in this section.

Although in simulations it was shown that this effect would ideally not affect to the behavior of the modulator, the output stage of the implemented transconductors may not be fast enough to recover from the large peak level of the state variables. This may require some kind of compensation method, such modulation of the transconductor gains with the clock signal or low pass filtering the DAC signal to attenuate high-frequency components.

CHAPTER 5

Low-pass transmission line ΣΔ Modulator in 0.6μm CMOS

5.1 Introduction

In this chapter, we discuss the practical implementation and measurements of the second order low-pass single-bit transmission line ΣΔM proposed in chapter 3, Fig.3.13, using off-chip passive resonators constructed with transmission lines and terminated as an open circuit.

This chapter includes the architecture design, the circuit design and the layout of the chip in a 0.6μm CMOS technology, together with the chip measurements that prove the validity of the design.

5.2 System level design

Figure 5.1 shows the system level diagram of the transmission line ΣΔM proposed in chapter 3. The blocks named H implement the following transfer function:

$$H(s) = \frac{1 + e^{-sT}}{1 - e^{-sT}} \tag{5.1}$$

This transfer function is proportional to the impedance of an open circuit transmission line (see chapter 3), where T corresponds to the delay of the transmission line. If this delay T is equal to the period of the sampling clock, this diagram can be used to implement a transmission line ΣΔM that has nearly identical properties as a discrete time counterpart [Her03].

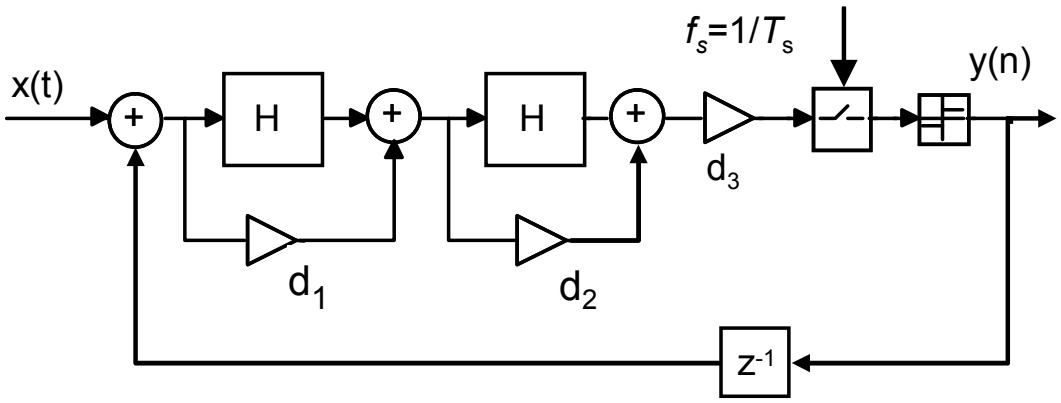

Figure 5.1. System level diagram of a 2nd order low-pass single-bit transmission line ΣΔM.

In this design, d_i coefficients are chosen such that the transmission line ΣΔM is equivalent to the ideal second-order lowpass discrete time modulator in [Nor96]. Mathematically this can be written as (see section 3.4.2):

$$\begin{aligned} &NTF(z)\big|_{z^{-1}=e^{-sT}} = NTF(s) \quad , \quad NTF(z) = \left(1 - z^{-1}\right)^2 \\ &NTF(s) = \left(e^{-sT}\left(d_3 H^2 + d_3(d_1 + d_2)H + d_1 d_1 d_3\right) - 1\right)^{-1} \end{aligned} \tag{5.2}$$

This yields the values d_1=1, d_2=3, d_3=1/4. Coefficient d_3 may be neglected in our single-bit design.

In order to accomplish the design of the modulator, in this section we will show some simulations of the proposed modulator of Fig.5.1. We will introduce some non-ideal parameters in order to have a more realistic response. Those parameters are:

- Finite bandwidth.

- Transconductors saturation.
- Loop delay.
- Clock jitter.
- Transmission line delay mismatch.

We will show the modulator behavior against such non-idealities using the SNR as a figure of merit. We will also show the dynamic range of state variables, gm_1 and gm_2 values, voltage swing at V_1 and V_2 and maximum value of the transconductors current I_1 and I_2.

5.2.1 Maximum Ideal SNR

We have used a simulation model of Fig.5.1 to simulate the behavior of the second order low-pas transmission line ΣΔM.

In the Simulink model of Fig.5.1, the previously defined d_i coefficients are implemented by adding series resistors to the transmission lines. The resonator block H is implemented as explained in sections 2 and 3. Also, we have included the gm_i values for the transconductors, a sample and hold block, a one-bit quantizer and a delay block that represents the loop delay of the feedback DAC.

Figure 5.2 shows a simplified circuit implementation of the modulator of Fig.5.1. In this case we have used the same conceptual circuit as in section 3.4.2.

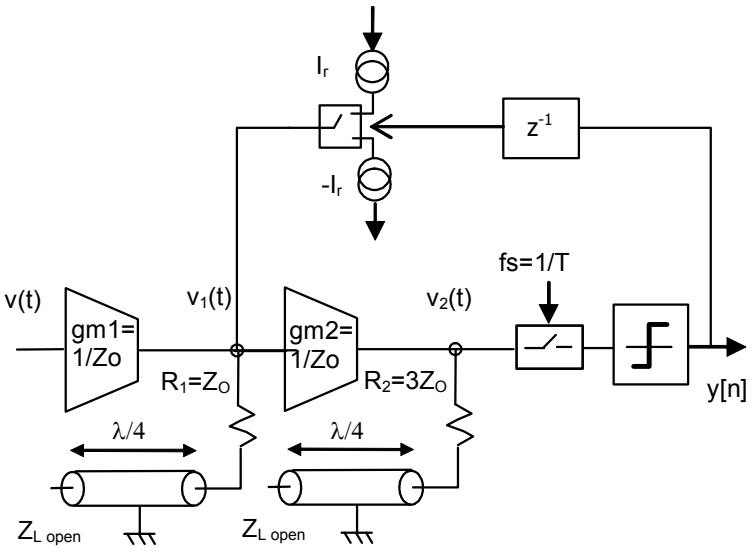

Figure 5.2. Schematic of the Second-order single-bit low-pass transmission line ΣΔM.

Matching equations from circuit in Fig5.2 and Fig.5.1 and Eq.5.2 we conclude:

$$gm_i = \frac{1}{Z_0}$$
$$R_i = d_i Z_0 \tag{5.3}$$

If we assume Z_0 (transmission line impedance) as 50Ω, gm_1 and gm_2 will have a value of 20 mA/V. This value for gm_1 and gm_2 may be too large to keep a low power design. In the simulations we have scaled the gm_i down to 2 mA/V. This factor has not a significant influence in the maximum SNR value, as long as the absolute value of transconductances is only a gain factor and only defines the full-scale of the input. Equation 5.4 and 5.5 show this point. These equations are extracted from section 3.4.2 and Eq.3.41.

$$V_2 = A(s) \cdot \left[gm_1 * gm_2 * V_i + gm_2 * I_{DAC} \right] \tag{5.4}$$

$$A(S) = (R_2 + Z_0 \cdot H(s)) \cdot (R_1 + Z_0 \cdot H(s)) \Rightarrow H(s) = \frac{1 + e^{-sT}}{1 - e^{-sT}} \tag{5.5}$$

The appropriate values of these resistors and the transconductors are expressed in Table 5.1. Here f_s corresponds to the sampling frequency, Z_0 to the characteristic impedance of the line and V_{iMAX} to the maximum input level.

gm_1	$1/(10*Z_0)$
gm_2	$1/(10*Z_0)$
R_1	Z_0
R_2	$3Z_0$
I_r	$V_{iMAX}/(10*Z_0)$
Electrical length	$v/2f_s$

Table 5.1. Design values of the lowpass 2nd order transmission line ΣΔM of Fig.5.2.

Figure 5.3 shows the ideal output spectrum of the model in Fig.5.1. In this simulation we have used an OSR=128, and an input tone at half of the signal bandwidth (BW=f_s/2/OSR).

The FFT of Fig.5.2 shows a second order low pass function, corresponding with the behavior of the equivalent 2nd order low pass DT-ΣΔM in [Nor96], as explained in section 3.4.

The SNR in this simulation is 69.7 dB with an input of -10dBFs.

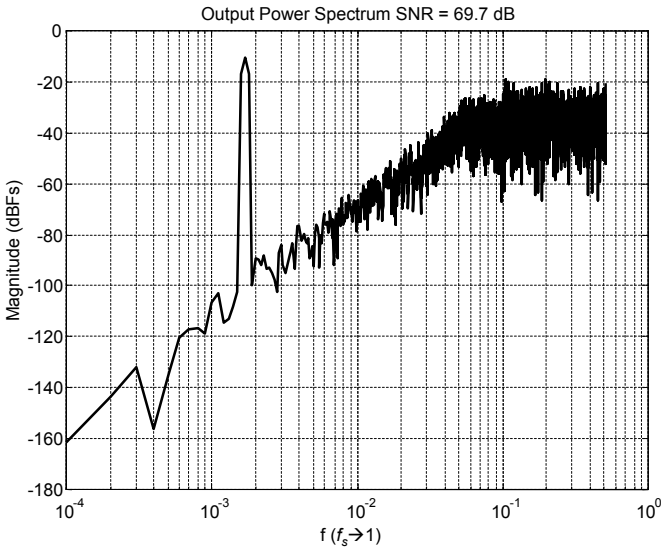

Figure 5.3. Output spectrum of the low-pass 2nd order transmission line ΣΔM of Fig.5.2.

5.2.2 Finite bandwidth of transconductors

As explained in section 4.2, the finite bandwidth (Bw) of the active elements in the modulator limits its performance. In this design we have two transconductors. We have to estimate what is the minimum bandwidth of the two transconductors in order to design them properly. As we target a low voltage and low power design, this parameter is one of the limitation for this task. Also, in [Her03] and in section 4.2 was shown that transconductors require a minimum unity gain bandwidth in excess of $2.5f_s$ to ensure that the intersymbol interference between the feedback DAC pulses will produce a noise power below the quantization noise, when moderate jitter ($\sigma \leq 0.1\%T$) is present.

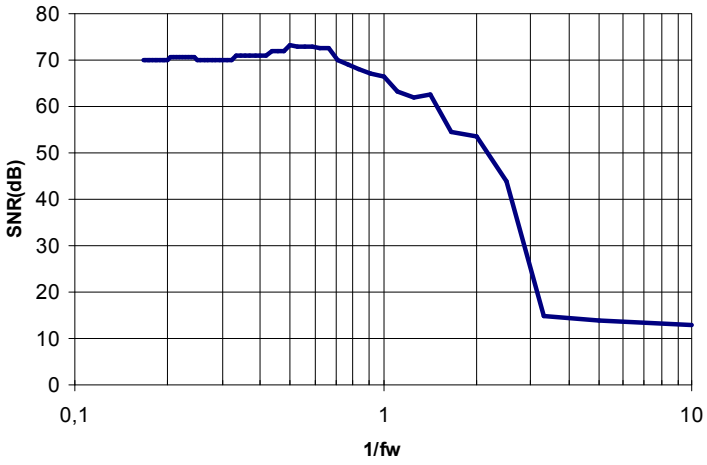

Figure 5.4. SNR of the low-pass transmission line ΣΔM of Fig.5.2 vs. 1/fw.

Figure 5.4 shows a plot where we have used different values for the transconductors bandwidth of Fig.5.2. For this simulation a one pole model has been used to estimate the finite

bandwidth of each transconductor. In Fig.5.4 we represent 1/fw, where fw=Bw/f_s, in log scale against the SNR of the modulator, using for this simulation the same parameters as in section 5.2.1.

In the simulation of Fig.5.4 the clock had no jitter. In next sections we will also introduce a clock jitter to compute the trade off between finite bandwidth of active elements and open loop gain of the loop filter.

5.2.3 Dynamic range of state variables

We have done a time domain simulations of the dynamic range of the state variables of Fig.5.2 to define the saturation values for the transconductors. These values are shown in Figure 5.5, considering an ideal transconductor and an open loop gain limited to 120dB at DC to account for transmission line losses.

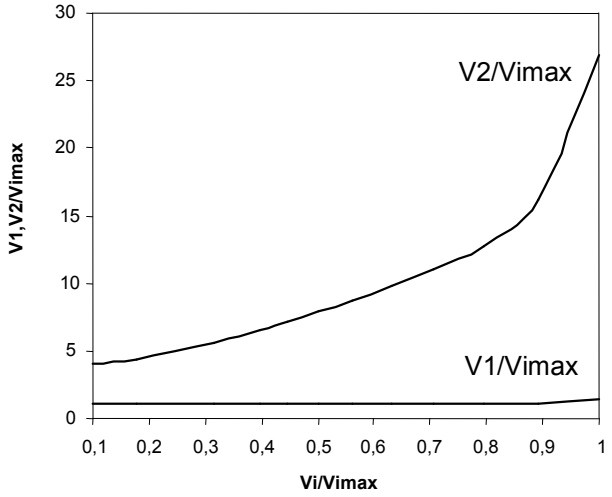

Figure 5.5. Dynamic range of state variables of the low-pass 2nd order transmission line ΣΔM of Fig.5.2.

Using the graph of Fig.5.5, we may estimate the maximum current provided by transconductor gm_2 and its maximum input voltage. For an input tone of –4dBFs, the maximum current delivered by gm_2 is 1.74Ir (see Fig.5.2) and the maximum amplitude at the transmission line $V_1(t)$ is $1.1V_{iMAX}$. We can also note that the value of $V_2(t)$ peaks at $9.7V_{iMAX}$ for the same input level. To compare this value with a standard second order sigma-delta modulator we should multiply $V_2(t)$ by d_3.

5.2.4 Clock jitter

As discussed in sections 4.1 and 4.2, the noise induced by jitter into the output sequence of a transmission line ΣΔM is composed of two terms. The equation that expresses such noise decomposition is Eq.4.10 of section 4.2.

One noise term represents the jitter component that is signal dependant and appears at the sampler in front of the quantizer. This noise term is spectrally shaped by the loop provided that its power is finite. This power is proportional to the derivative of the input signal and the open loop gain of the modulator. Hence in a practical implementation it is always a shaped component, although its variance may be enough to be a significant source of SNR loss, as a difference with conventional CT-ΣΔMs. Due to the derivative dependence, DC inputs or idle channel noise (DC=0) produce a null noise component.

The second component is due to the DAC pulses which may have a time varying area due to jitter. In the ideal case, the DAC pulses should be of finite duration and the signal processing elements of infinite bandwidth. Under such ideal conditions this noise component should be null if the jitter variance is constrained to some limits. However, in a real implementation, finite bandwidth of transconductors will affect the duration of the DAC pulses and this jitter term will depend on the loop bandwidth and the jitter noise power. This is the noise component that is inherent to the modulator implementation.

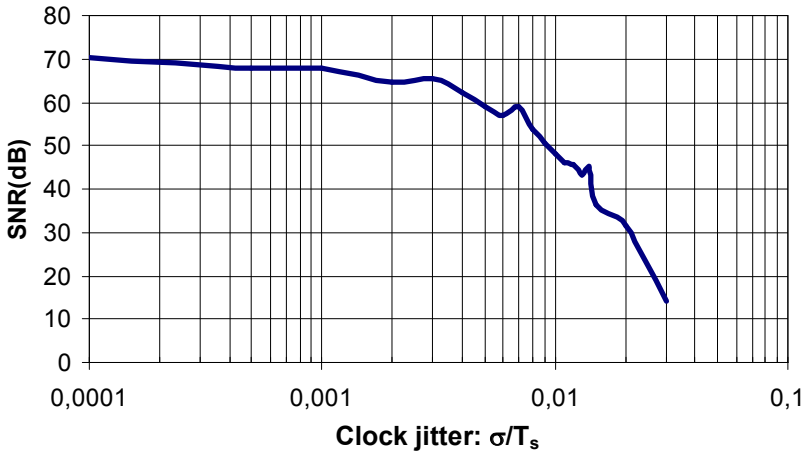

Figure 5.6. Clock jitter performance of the low-pass 2nd order TL-ΣΔM of Fig.5.2.

To compute this effect first we will run a simulation including jitter in the clock. For this simulation, the transconductors have a finite bandwidth of Bw=2.5f_s. Figure 5.6 shows the jitter performance of the low-pass 2nd order transmission line ΣΔM of Fig.5.2. Also in this simulation we have include a loop delay of 0.4T_s for the feedback path of the DAC.

Second, we can simulate the modulator with a fixed clock jitter and vary the loop delay to calculate the maximum delay that we can tolerate in the feedback path of the DAC. This is explained in next section.

5.2.5 Loop Delay

As explained in chapter 2 and 4, in a low-pass 2nd order transmission line ΣΔM, with ideal transconductors, the loop delay may vary between 0 to one full clock cycle without any theoretical degradation, if a NRZ feedback pulse is used in the DAC. However, in chapter 4 we explain that if the transconductors of the modulator have finite bandwidth and clock is jittered, we should reduce the loop delay in order to keep the ideal performance of the modulator.

Figure 5.7 shows a simulation of the low-pass 2nd order transmission line ΣΔM of Fig.5.2 where we plot the SNR against the loop delay of the feedback path of the DAC. The loop delay has been simulated as a function of the clock period T_s. We have defined parameter mld=*loopdelay*/T_s to compute de loop delay.

In the simulation of Fig.5.7 transconductors gm_1 and gm_2 have a finite bandwidth of BW=2.5f_s. The clock has jitter of $\sigma=10^{-3}T_s$. This simulation shows that the loop delay should be approximately smaller than $0.5T_s$ to keep the ideal performance of the modulator.

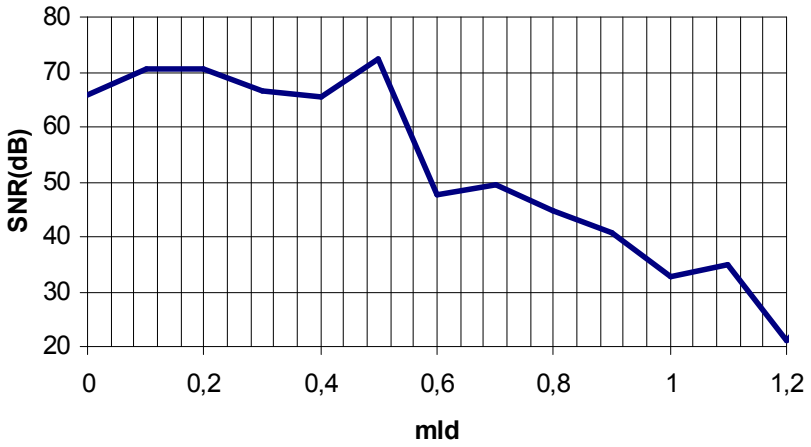

Figure 5.7. SNR vs. loop delay with finite bandwidth of transconductors of the LP 2nd order TL-ΣΔM.

5.2.6 Mismatch among the resonance frequencies

One of the limiting factors in the design of a transmission line ΣΔM is the mismatch among the resonance frequencies of the resonators, as explained in section 4.3.1. Figure 5.8 shows the relation between the resonance frequency of the transmission line connected to the

second transconductor gm_2 of Fig.5.2, expressed as a function of the period of this frequency (T_d), and the SNR. We have kept the first transmission line with a delay equal to the sampling period in order to compute the mismatch among the resonance frequencies of the transmission lines.

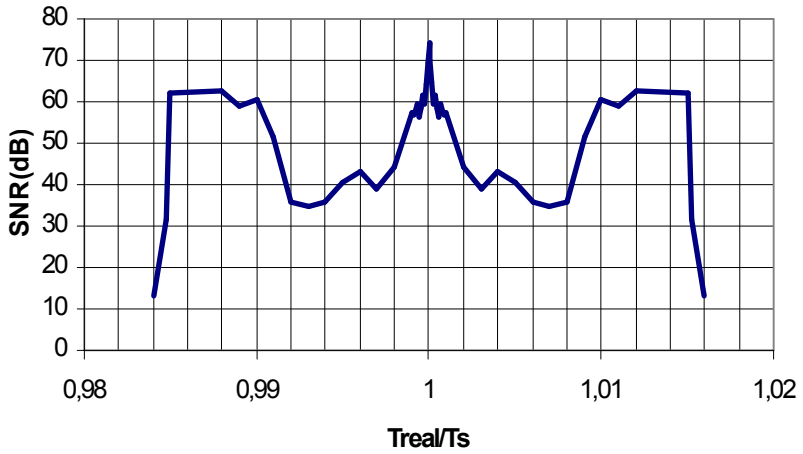

Figure 5.8. Mismatch among the resonators frequencies of the low-pass 2nd order TL-ΣΔM of Fig.5.2.

As predicted in [Kap05] the mismatch of the resonance frequency of the transmission lines perturbate the poles and zeros of the NTF of the modulator. This perturbation degrades the performance of the modulator as it can be seen in Fig.5.8.

5.3 Circuit Design

The system block diagram (see Fig.5.2) and parameters defined in the previous section were used as the start point of a CMOS circuit design. For this proof-of-concept circuit, a conservative 0.6μm standard CMOS process and a power supply of 3.3 V were selected. A clock frequency of f_s = 50MHz was targeted.

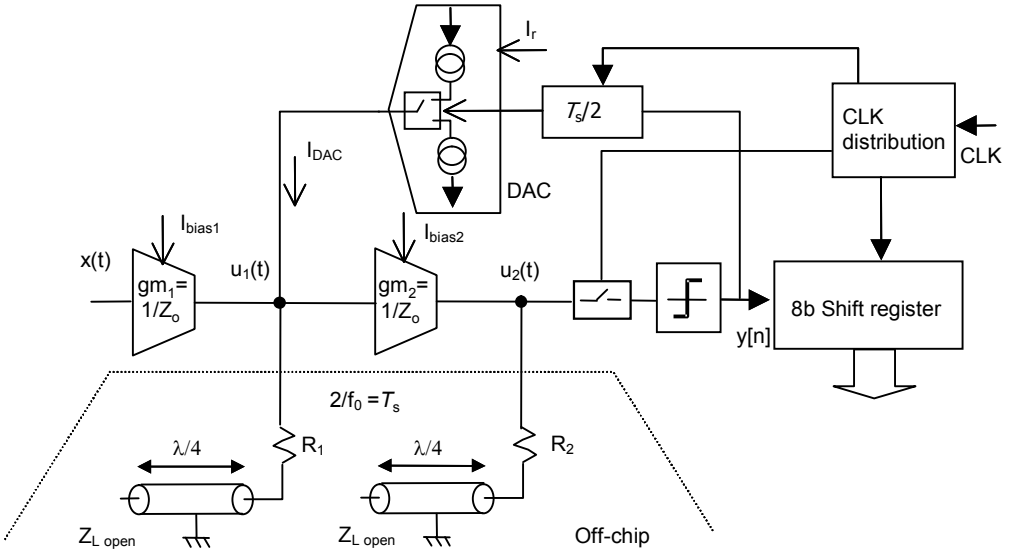

Figure 5.9. Block diagram of the low-pass 2nd order TL-ΣΔM CMOS chip.

A block diagram of the chip is shown on Figure 5.9. It consists of a first input transconductor, a second transconductor, a comparator, a synchronization latch, a 1bit DAC and a digital interface block. Essentially it is the same block diagram as in Fig.5.2 but including the digital block to generate the output data and the clock distribution.

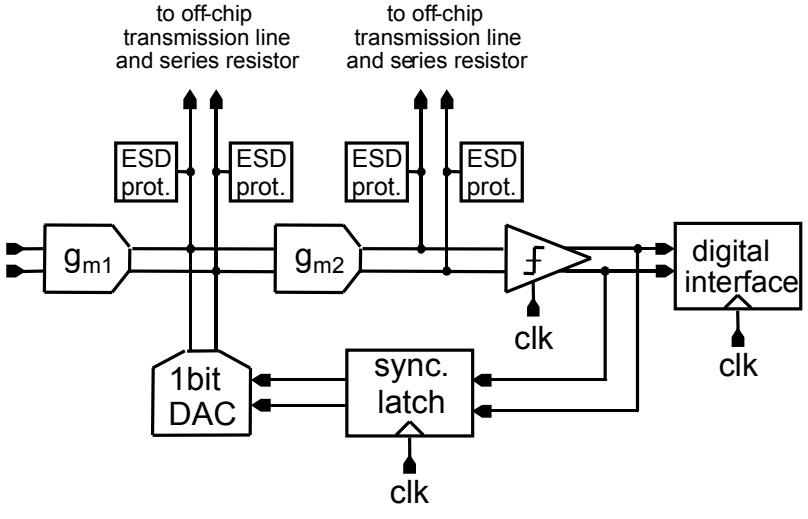

Figure 5.10. Differential block diagram of the low-pass 2nd order transmission line ΣΔM CMOS chip.

A fully differential implementation of the modulator shown on Fig.5.9 is shown in Figure 5.10. The transmission lines and their series resistors are not implemented on-chip. This way, the output of each transconductor is connected to an ESD-protected bond pad.

5.3.1 First transconductor (gm_1)

The most demanding building block of the entire circuit is the input transconductor. This block should be at least as linear as the linearity of the overall modulator. The reason for this is that this transconductor performs the voltage-to-current conversion of the input signal prior to entering the feedback loop. Hence, non-linearity of this transconductor is not attenuated by the operation of the loop. For the same reason, this input transconductor does only require the bandwidth of the input signal instead of 2.5 times the sampling frequency, as stated in the previous section, which only applies to transconductor g_{m2}.

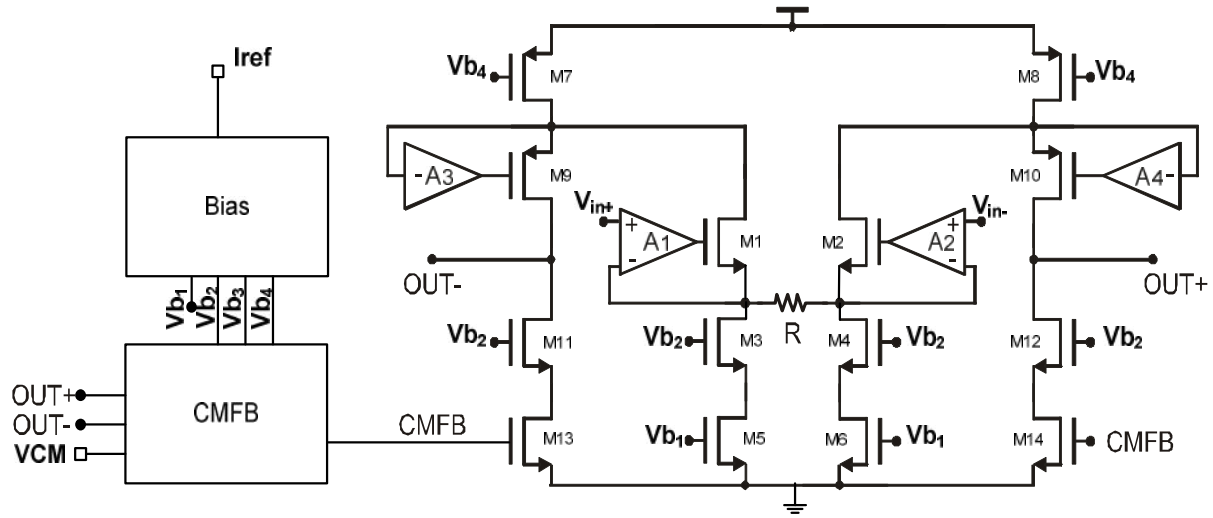

Figure 5.11. Simplified schematic of the first transconductor of the lowpass TL-ΣΔM.

Table 5.2 shows the sizes of the main CMOS transistors of the first transconductor.

Figure 5.11 depicts the simplified schematic of this first transconductor. It is based on source degeneration of the input differential pair transistors similar to what was used in [Cha95]. Also, Fig.5.11 shows the connections with the Common Mode Feedback Circuit (CMFB) and the biasing circuit (Bias).

For enhanced linearity, the operational amplifiers A_1 and A_2 are added at the inputs. These amplifiers are implemented as simple NMOS differential pairs with active loads.

The resistor R is a 1kΩ linear resistor which is available in the target process. This value was a compromise between noise and power consumption. Note that this does not correspond

to the value of Table 5.1. However, as explained above, the first transconductor is outside the loop and hence this deviation from the theory only results in a gain error of the overall modulator.

Amplifiers A_3-A_4 are added to achieve an adequate output impedance [Sac90]. It turned out that the equivalent amplifiers for the NMOS cascodes could be removed. This is due to the fact that relatively long channels were used for these current source transistors that are outside the main signal path.

CMOS trts.	W/L [μm]
M1,M2	400/0.6
M3,M4	400/0.6
M5,M6	800/1.2
M7,M8	600/0.6
M9,M10	300/0.6
M11,M12	200/0.6
M13,M14	800/1.2

Table 5.2. CMOS transistors of transconductor gm_1 of the lowpass TL-ΣΔM.

CMFB circuit

Since the circuit is differential, it requires a common mode feedback circuit (CMFB) to stabilize the output common mode voltage.

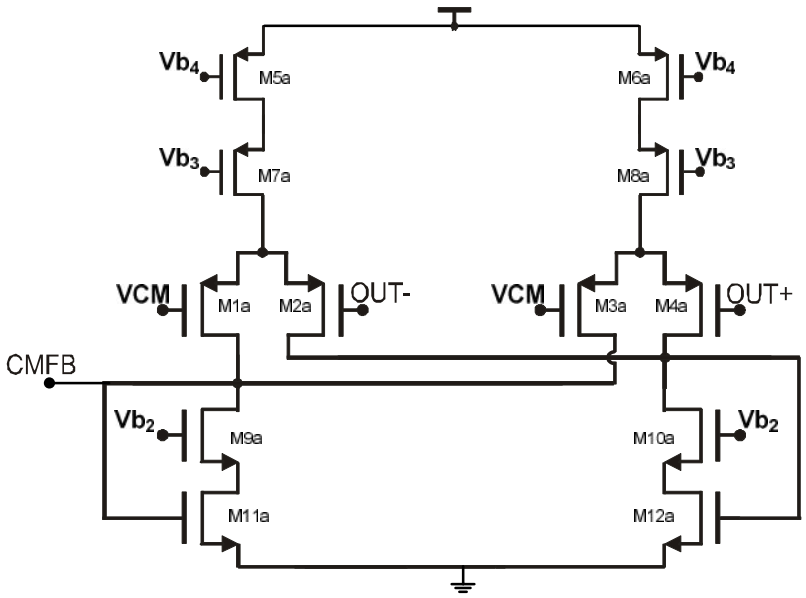

Figure 5.12. Simplified schematic of the first transconductor of the lowpass TL-ΣΔM common mode feedback circuit (CMFB).

The circuit [Joh97], shown on Figure 5.12, was used to set the common mode level. It consists in two cross-coupled PMOS differential amplifiers (M1a, M2a, M3a, M4a) that compare

the differential output of the transconductor with the desired common mode voltage of the output of the transconductor. This circuit then compensates the differences respect to the common mode voltage and sets the new gate voltage of transistors M13 and M14 of Fig.5.11, acting as a control loop of the current of the output stage of the transconductor.

One important issue to design the CMFB circuit of Fig.5.12 is its bandwidth. This bandwidth should be enough to ensure:

- The stability of the control loop between the CMFB circuit and the output of the transconductor.
- Enough phase margin of the circuit itself, as it can be seen as an opamp.
- That the circuit is fast enough to follow the input signal.

For this reason the input transistors of circuit of Fig.5.12 (M1a, M2a, M3a, M4a) have been designed such the bandwidth and phase margin of the CMFB circuit make the loop control stable and make the differential pair fast enough to follow the input signal. Table 5.3 shows the sizes of these CMOS transistors.

CMOS trts.	W/L [μm]
M1a,M2a,M3a,M4a	60/0.6
M5a,M6a,M7a,M8a	30/0.6
M9a,M10a	20/0.6
M11a,M12a	80/1.2

Table 5.3. CMOS transistors of the CMFB circuit of transconductor gm_1 of the lowpass TL-ΣΔM.

5.3.2 Second transconductor (gm_2)

The second transconductor (gm_2 on fig.5.10) is implemented as a simple differential pair without source degeneration nor auxiliary amplifiers. This is possible because non-linearity of this block is attenuated by the operation of the loop. Due to the simplicity of this block, it also achieves high bandwidth.

Figure 5.13 shows a simplified schematic of the second transconductor of Fig.5.10, including the CMFB circuit and the bias circuit. To achieve the proper bandwidth for the second transconductor gm_2, we have designed the sizes of the input NMOS transistors (M1, M2) such their *gm* fit with the value of table 5.1.

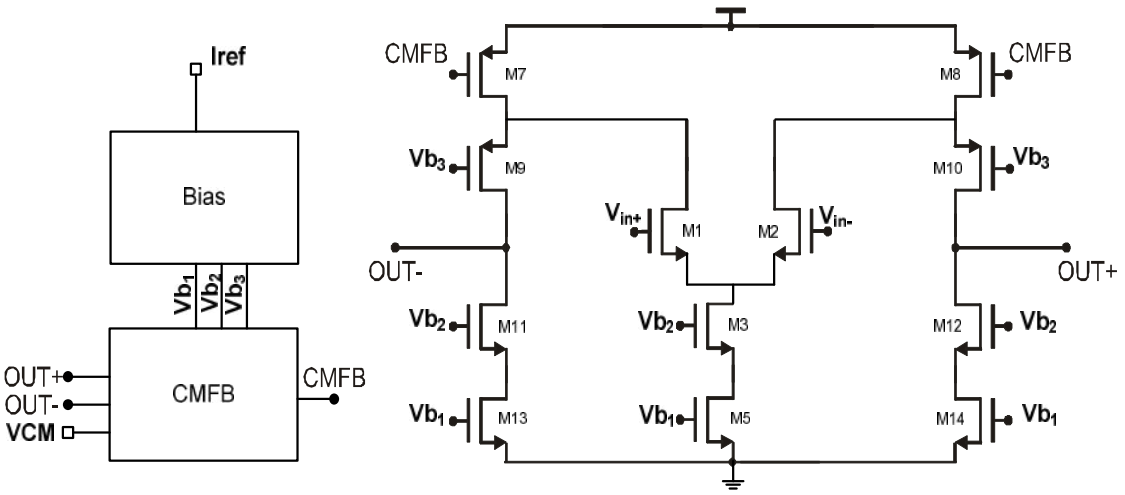

Figure 5.13. Simplified schematic of the second transconductor of the lowpass TL-ΣΔM.

In the other hand, as far as the linearity of this block is not critical for the performance of the modulator, we can also achieve high bandwidth by increasing gm_{M1} and gm_{M2}. This change in the value of the transconductance of the input differential pair will only be a gain error, as predicted by Eq.5.4 and section 5.2.1, but will increase the power consumption of the transconductor.

To properly design transconductor gm_2 we should have a trade off between bandwidth and power consumption. But as far as this design was only a proof-of-concept, the implementation was not power optimized. Therefore, the final value of the transconductance of the input differential pair of the second transconductor was selected in order to achieve a bandwidth of 3 times the sampling frequency. This bandwidth was Bw=3*f_s=150MHz, which may exceed the minimum bandwidth needed.

Table 5.4 shows the final values of the MOS transistors of the second transconductor.

CMOS trts.	W/L [μm]
M1,M2	80/0.8
M3	800/0.6
M5	1600/1.2
M7,M8	600/0.6
M9,M10	300/0.6
M11,M12	200/0.6
M13,M14	800/1.2

Table 5.4. CMOS transistors of transconductor gm_2 of the lowpass TL-ΣΔM.

CMFB circuit

Since the circuit is differential, it requires a common mode feedback circuit to stabilize the output common mode voltage. The circuit [Joh97], shown on Figure 5.14, was used to set the common mode level of the second transconductor. It consists in two NMOS cross-coupled differential amplifiers (M1a, M2a, M3a, M4a) that compare the differential output of the transconductor with the desired common mode voltage of the output of the transconductor.

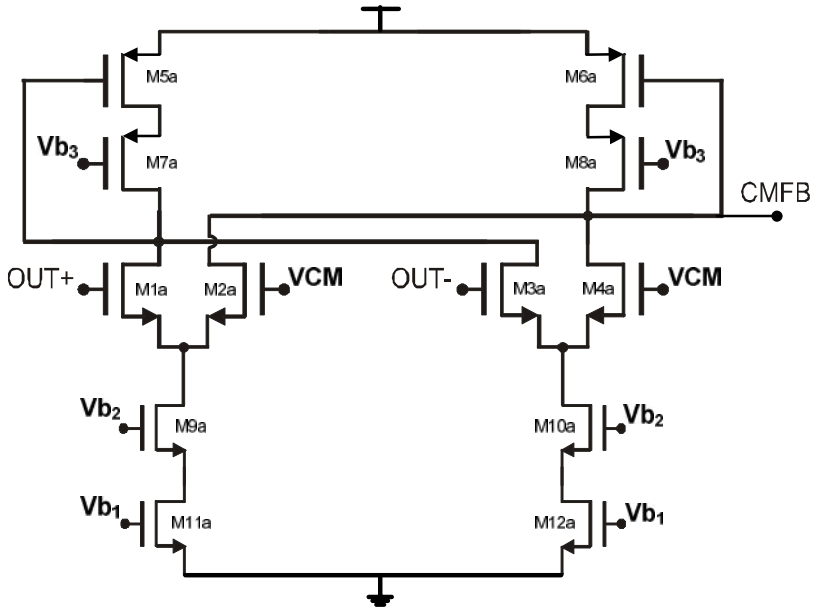

Figure 5.14. Simplified schematic of the second transconductor of the lowpass TL-ΣΔM common mode feedback circuit (CMFB).

As a difference with the CMFB circuit (see Fig.5.12) of transconductor gm_1, the CMFB circuit of transconductor gm_2 uses NMOS transistors instead of PMOS transistors for its input stage. Therefore, we are able to increase the bandwidth of the CMFB circuit of Fig.5.14, compared with the CMFB circuit of Fig.5.12. This bandwidth increase is needed due to the fact that the bandwidth of the transconductor itself has been increased. Table 5.5 shows the sizes of the CMOS transistors of the CMFB circuit of gm_2.

CMOS trts.	W/L [μm]
M1a,M2a,M3a,M4a	100/0.6
M5a,M6a,M7a,M8a	30/0.6
M9a,M10a	20/0.6
M11a,M12a	80/1.2

Table 5.5. CMOS transistors of the CMFB circuit of transconductor gm_2 of the lowpass TL-ΣΔM.

5.3.3 DAC

Next we will describe the 1-bit DAC (see Fig.5.10) implemented for this design. This DAC can be implemented as NRZ DAC which simplifies the implementation. Use of NRZ or RZ DACs has no impact in this type of ΣΔMs in the sensitivity to non-idealities in the switching points, such as clock jitter or code dependent distortion of the DAC pulses, as has been explained in chapter 4 [Pre07].

Figure 5.15 shows a simplified schematic of the 1-bit DAC. It is composed of one synchronization latch (Gigalatch of Fig.5.15 [Van01]) that drives the switches of a 1-bit current cell.

The dynamic performance degradation of a current-steering D/A converter can be caused by several reasons [Van01]. Some important issues that have been identified to cause dynamic limitations are:

1) imperfect synchronization of the control signals at the switches;

2) drain-voltage variation of the current-source transistors;

3) coupling of the control signals through the G_{GD} of the switches to the output.

To minimize these three effects, a well-designed and carefully laid out synchronized driver is used. A major function of this driver is shifting the crossing point of the switch transistor's differential control signals, in such a way that these transistors are never simultaneously in the off state. The driver also performs the final synchronization. By placing it in front of the switches and by paying much attention to symmetrical interconnections in the layout, the difference in delay between the different digital decoder outputs is minimized. Furthermore, the dynamic error caused by the parasitic gate–drain feedthrough capacitance is significantly lowered by the use of a reduced voltage swing at the input of the switches. This reduced voltage swing is achieved by lowering the power supply of the digital driver.

In this way the synchronization latch, and therefore the DAC, is strobed slightly after the comparator latch [Joh97] by adjusting a chain of inverters. This chain of inverters can be programmed to adjust the loop delay to the correct value.

The full-scale current of the DAC (I_F) is calculated from table 5.1. As explained in section 5.2 the input full-scale should be a trade-off between the dynamic range of the state variables, the power consumption and the input to the quantizer. For this design we have

selected an input full-scale of V_{iMAX}=100mV. Using this value, the full-scale of the DAC is I_r=300μA.

Figure 5.16 shows a simplified schematic of the 1-bit NRZ current cell. In this schematic transistors M1 and M2 are the PMOS current source of the DAC, and transistors M7 and M8 are the NMOS current source of the DAC. Transistors M3, M4, M5 and M6 are the switches driven by the Gigalatch.

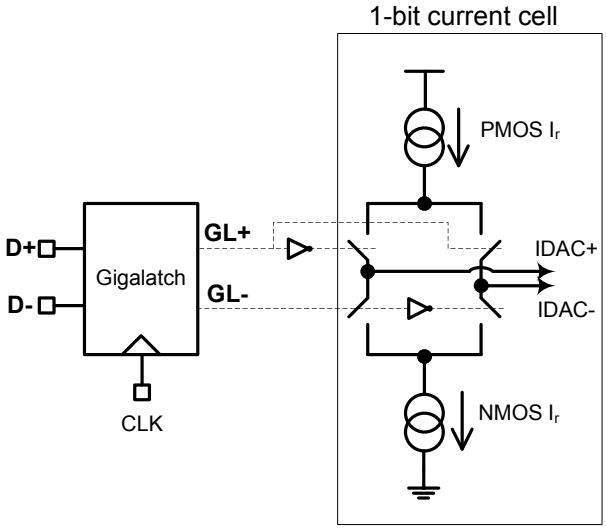

Figure 5.15. Simplified schematic of the NRZ 1-bit DAC of the lowpass TL-ΣΔM.

Table 5.6 shows the sizes of the CMOS transistors of the 1-bit current cell of Fig.5.16.

CMOS trts.	W/L [μm]
M1	240/2
M2	90/0.6
M3,M4	30/0.6
M5,M6	10/0.6
M7	30/0.6
M8	80/2

Table 5.6. CMOS transistors of the 1-bit current cell of the lowpass TL-ΣΔM.

One restriction in the design of the DAC is its output impedance. The output impedance of the DAC should be large enough to avoid a reduction of the loaded Q factor of the associated transmission line. For this reason a NMOS and PMOS wide-swing current mirrors [Joh97] are designed to implement the NMOS and PMOS current sources of the DAC. In this case the output impedance of the DAC is similar to a CMOS cascode mirror:

$$Rout_{NMOS\_CURRENT\_SOURCE} = gm_{M7} rds_{M7} rds_{M8} \tag{5.6}$$

$$Rout_{PMOS\_CURRENT\_SOURCE} = gm_{M2} rds_{M2} rds_{M1} \tag{5.7}$$

Equation 5.6 and 5.7 represents the output impedance at nodes *x* and *y* of Fig.5.16 respectively.

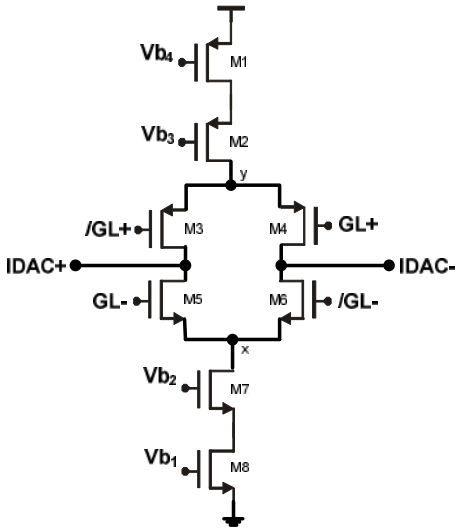

Figure 5.16. Simplified schematic of the NRZ 1-bit current cell of the lowpass TL-ΣΔM.

5.3.4 Comparator

The 1-bit comparator of the modulator is implemented as shown in Figure 5.17. It consists of a pre-amplifier and a two stage regenerative latch [Gee99].

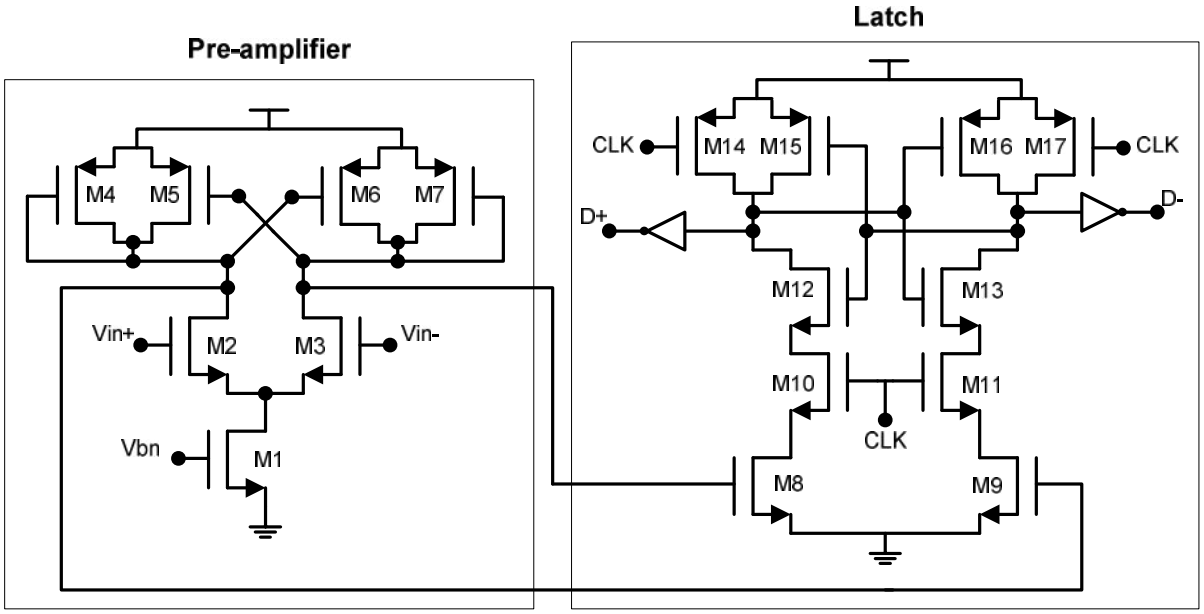

Figure 5.17. Simplified schematic of the comparator of the lowpass TL-ΣΔM.

In the comparator of Fig.5.17 we have used a pre-amplifier in order to avoid kickback of the latch in the sampling instant of the clock (CLK). However, this pre-amplifier is also used

to amplify the input to the comparator ($u_2(t)$ in Fig.5.9) in order to reduce the metastability of the latch. This effect can be seen as a delay between the sampling instant and the "decision" instant. This means that ideally, when a rise edge of the clock arrives, the comparator must decide whether its output is a "1" or a "0" without any delay. In the real circuit this is not possible. Even with a very carefully design, this delay gets larger as the input gets smaller. For this reason, we have placed a re-synchronization latch after the comparator to avoid as much as possible this variable delay from the feedback loop. If we do not do so, distortion from the feedback path would appear into our modulator.

Then the gain stage of the latch of Fig.5.10 (transistors M8 and M9) can be relaxed due to the pre-amplifier. This latch has two phases. In the first phase, when the clock is positive, the latch decides whether the input signal is negative or positive. The transistors involve in this stage are M8 and M9. Transistors M10 and M11 act as a switch. Then when the clock is negative, the latch gets into the hold phase. In this phase, transistors M12, M13, M15 and M16 act like strong inverters, holding the decision taken in the previous stage.

Table 5.7 shows the transistors sizes of the comparator of Fig.5.17.

CMOS trts.	W/L [μm]
M1	120/1.2
M2,M3	10/0.6
M4,M7	6/0.6
M5,M6	3/0.6
M8,M9	15/0.6
M10,M11,M12,M13,M15,M16	7.6/0.6
M14,M17	3/0.6

Table 5.7.CMOS transistors of the comparator of the lowpass TL-ΣΔM.

5.3.5 Digital interface

The digital interface, shown in Figure 5.18, groups 8 consecutive output bits in a single 8-bit word (DataOut<7:0>) to reduce the clock rate of the output digital pads. Also a direct digital output (TestOut) is provided for testing at low clock rates.

The digital block is composed of a shift register (ShiftReg) that makes the serial to parallel conversion, a parallel loadable register (Register8) that captures every 8-bit word, and a ring counter (ShiftCount1) that controls the block and generates the output signals. This output

signals have a clock rate of 1/8 the sampling frequency, and they are synchronize by an auxiliary clock signal (Latch Enable).

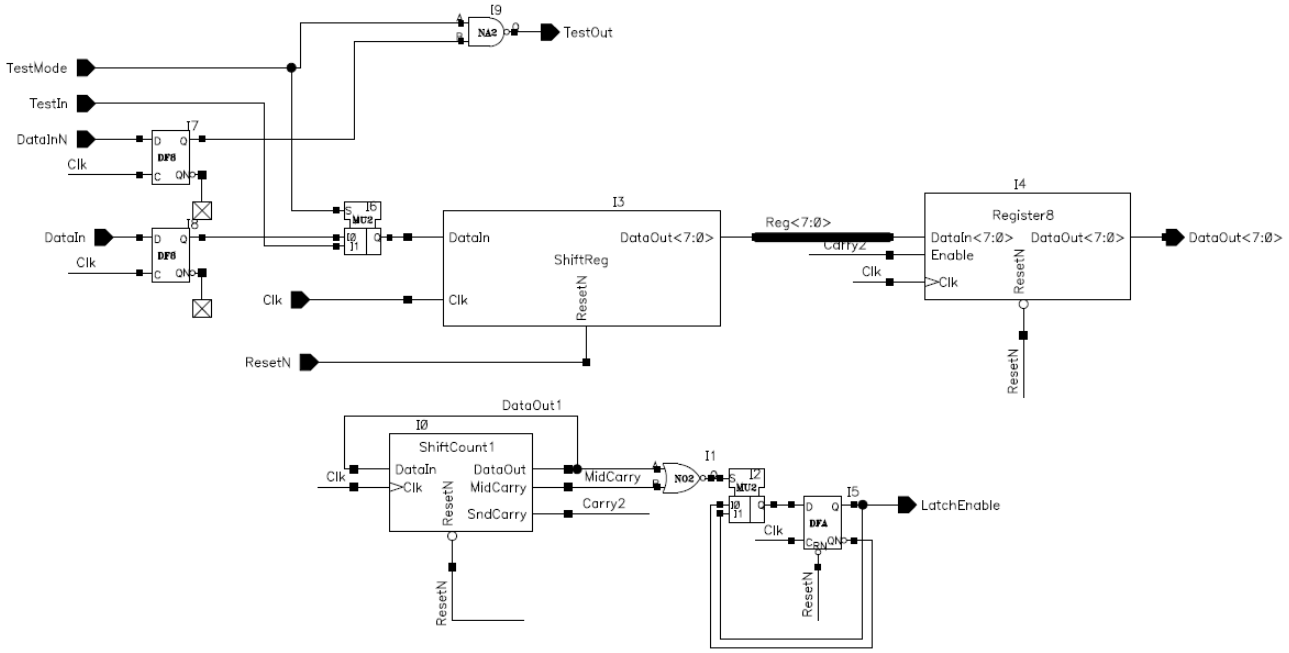

Figure 5.18. Simplified schematic of the digital interface of the lowpass TL-ΣΔM.

The digital interface has been designed using the standard cells of the technology. However, as the target sampling frequency is 50MHz, and therefore the clock rate of the digital output is 6.25MHz, no optimization of this block was needed.

5.3.6 Power estimation

Once all the main blocks of the modulator are designed, we can estimate the power consumption of the chip. For this purpose we have run a transient simulation in Spectre, with a full spice transistor-level model of the modulator. For this calculation we have taken into account only the next blocks from Fig.5.10:

- gm_1
- gm_2
- comparator
- 1-bit DAC

Table 5.8 shows the rms value of an equivalent current source, connected to the power supply of each block of the modulator.

Block	Irms [mA]	Pwr [mW]
gm_1	1.15	3.8
gm_2	1.8	5.94
comparator	0.95	3.13
1-bit DAC	5.1	16.8

Table 5.8. Power estimation of the low-pass 2nd order transmission line ΣΔM.

5.3.7 Transistor-level simulation

Finally, we have made a full SPICE transistor-level simulation of the chip in Spectre. We have used an OSR=128, and an input tone at half of the analog bandwidth (ABW=f_s/2/OSR). The amplitude of the tone was 0dFs in order to estimate the distortion contributions of each block of the modulator.

Figure 5.19 shows the FFT of the modulator output computed with a transistor level simulation of 8K points, same as in section 5.2.1. The simulation produces a SNDR of 77dB. As it can be seen in Fig.5.19, the behavior of the modulator is not limited by distortion, and it is close to the ideal simulation of section 5.2.1.

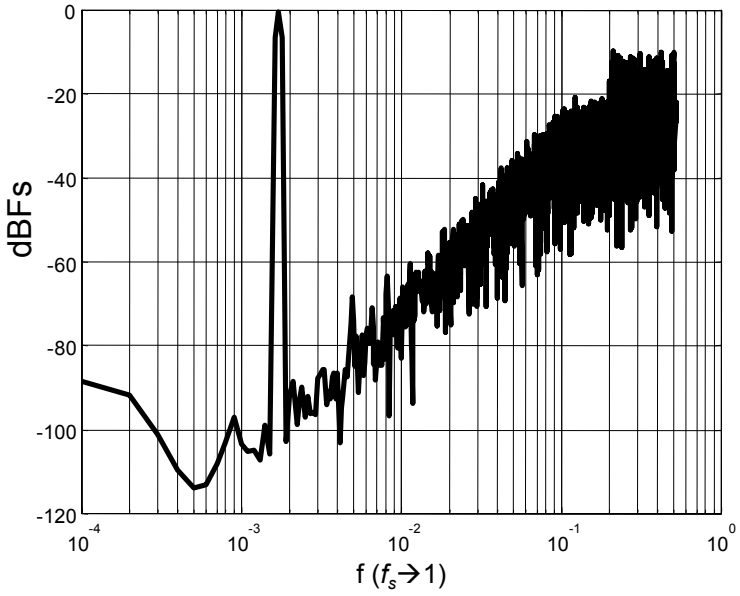

Figure 5.19. FFT of the low-pass 2nd order TL-ΣΔM output computed with a full spice transistor level simulation of 8K points.

5.4 Implementation and measurements

5.4.1 Layout considerations

The operation of an electronic circuit may be severely degraded as a consequence of the fabrication process. This fact is extremely important in analog circuits in which technology parameter variations may fully destroy their ideal performance. This degradation can be partially avoided by following some practical recommendations during the layout synthesis process.

On the other hand, when both analog and digital circuits are integrated on the same chip, the high-speed switching signals provided by the digital circuitry create interferences on the sensitive analog nodes. This interference is often referred to as "switching noise" or simply digital noise. This noise is mainly coupled to the analog circuitry via the power supplies and the substrate.

For the design of the chips in this work, the following precautions were taken into account, when possible, during the layout process.

1. *Separate digital and analog power supplies*.
2. *Partitioning of the circuit*. It is critical to avoid the proximity of analog and digital circuitry. When this is not possible, it is very important to place well and substrate contacts between the corresponding analog and digital interfaces.
3. *Shielding of sensitive circuits*. These guard rings are composed of two parts. One part is of the p^+-well type and the other one is of the *n*-well type. The former is placed closer to the circuit it guards than the latter.
4. *Basic analog layout recommendations*. In addition to the mentioned precautions, we have applied the basic analog layout recommendations for those parts of the circuit that have to be matched. Among others, the most important rules are: the use of unit transistors, making all transistors matched in order to drive the drain current in the same direction, placing them as close as possible, using common-centroid techniques or similar techniques, etc.

A photograph of the prototype chip described in this chapter is shown in Figure 5.20. The layout of each block and the final floor planning has been completed taking into consideration the pad routing to minimize the parasitic capacitance at the transmission line connections. The chip measures 4 mm^2 including the pad ring.

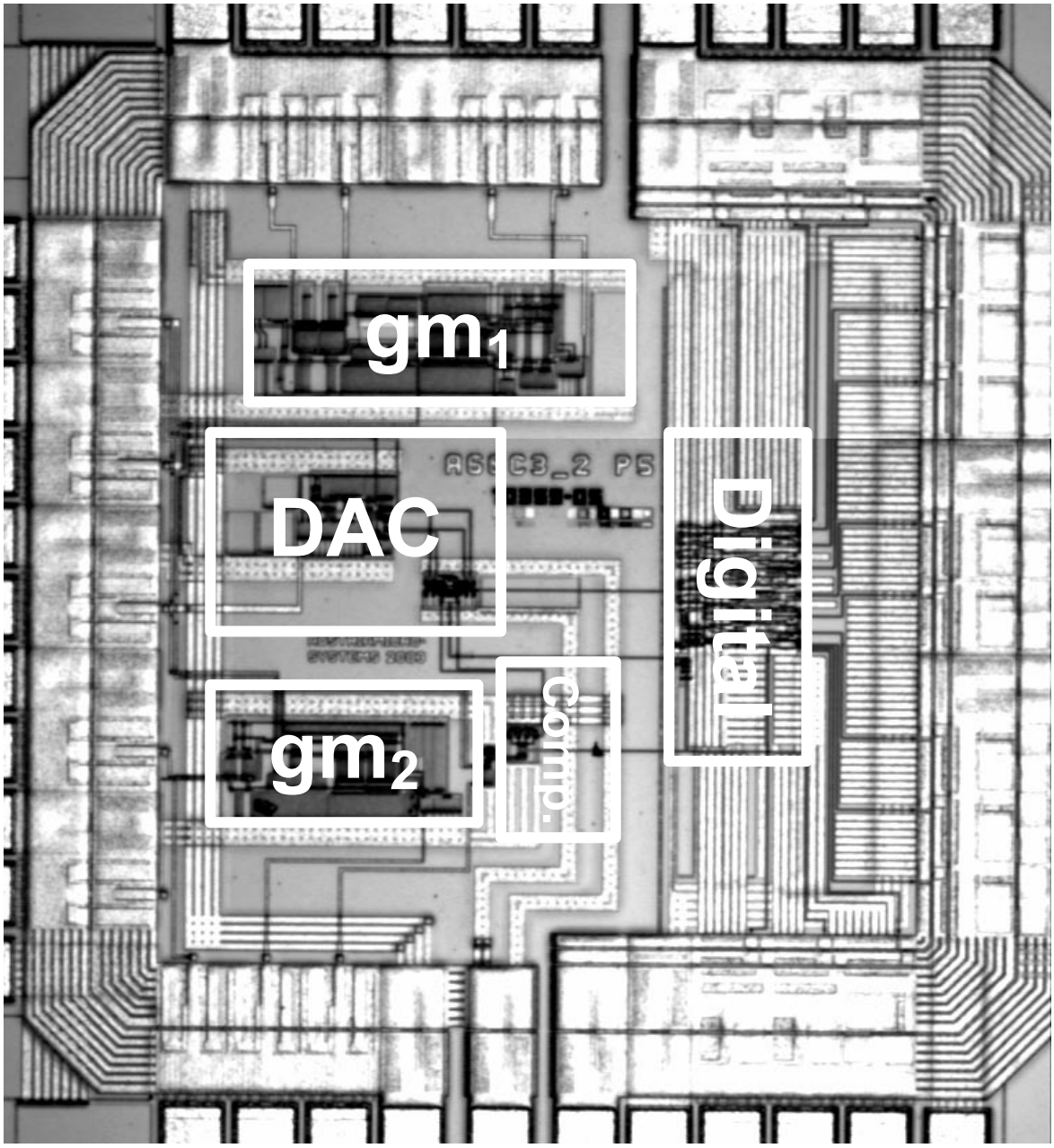

Figure 5.20. Chip microphotograph of the low-pass 2nd order TL-ΣΔM.

5.4.2 Chip measurements

To test the chip, four pieces of RG-178 coaxial cable were used as off chip resonators, trimmed to the clock frequency. The test setup consisted of a PCB board with current references, analog single ended to differential drivers and an interface to a logic analyzer.

The values of the off-chip circuit parameters that have been chosen for the design are in Table 5.9.

Z_0	50Ω
R1	50Ω
R2	150Ω

Table 5.9. Off-chip circuit parameters of the lowpass 2nd order TL-ΣΔM.

Figure 5.21 shows the block diagram of the test board used to measure the chip of this chapter. The single-ended to differential input stage has been made with two Opamps (AD8041). The digital buffer is a 74LVC244A and provides a 3.3V to 5V logic level translation. The clock circuit has been made with a 74LVCU04 and a circuitry that allows to introduce a jitter noise in the clock signal. The bias circuit has been made with four matched transistor pairs SSM2220. Tp+ and Tp- are the input signal points of the chip.

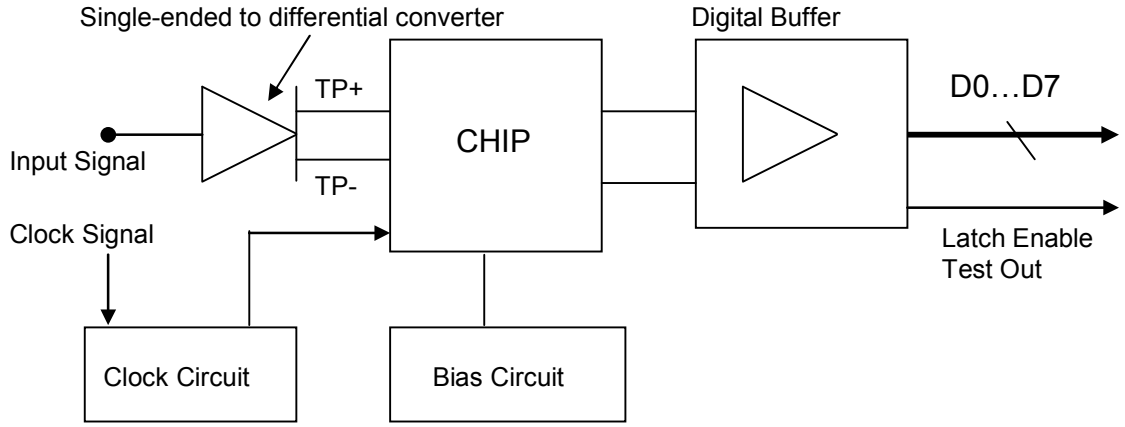

Figure 5.21. Block diagram of the test board of the low-pass 2nd order TL-ΣΔM.

In order to capture the data and make all the necessary measurements in this section, we have used the test bench shown in Figure 5.22.

The instrumentation used for the measurements is the next:

* Signal Generator and Clock Generator: Hameg HM8134-2 1Hz.-1,2 GHz.

* Power Supply: Programmable Power Supply HM7044 (Hameg).

* Spectrum Analyzer: Anritsu Spectrum Analyzer MS2661C 9kHz-3GHz.

* Digital oscilloscope: Yokogawa DL1720 1GS/s 500MHz digital oscilloscope.

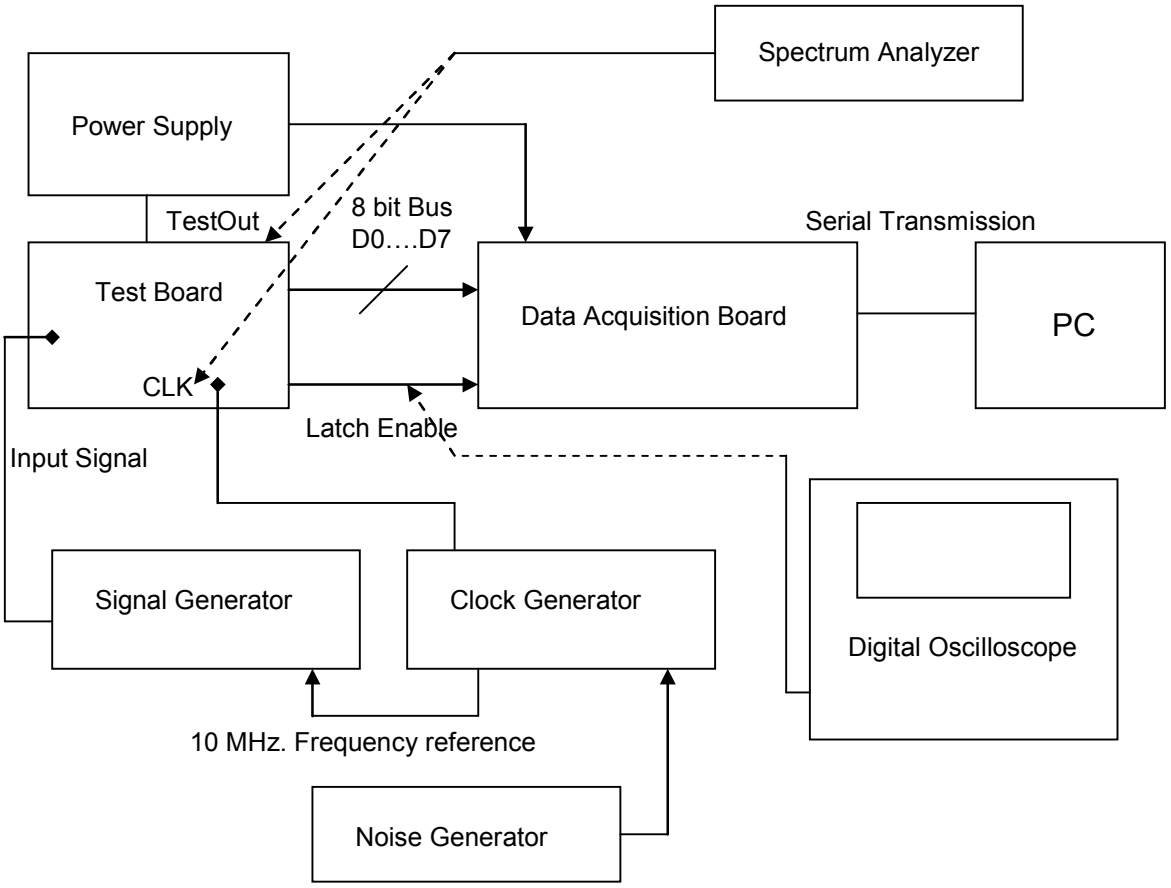

Figure 5.22. Block diagram of the test bench used to measure the chip.

Nominal measurements

The modulator was tested by applying sinusoidal signals at its input. In order to calculate the FFT of the output signal we have used a set of Matlab programs. We have captured for every measurement a record length of 64k samples of 1 bit with the data capture board of Fig.5.22, and then the FFT plots have been obtained by the average of 8 FFT with 8K samples. The Y axis is in dBFs referred to the input tone, and the X axis is scaled logarithmically and expressed as function of the sampling frequency f_s.

In figure 5.23 we show the windowed FFT of a data capture when using an input signal at half of the analog bandwidth f_{in}=ABW/2=f_s/2/OSR/2=104.883kHz, using a sampling frequency f_s=53.7MHz, and the OSR=128. The input amplitude was -3dBFs. The DC component has been removed. The nominal jitter of the clock is $\sigma = 0.1\%T_s$.

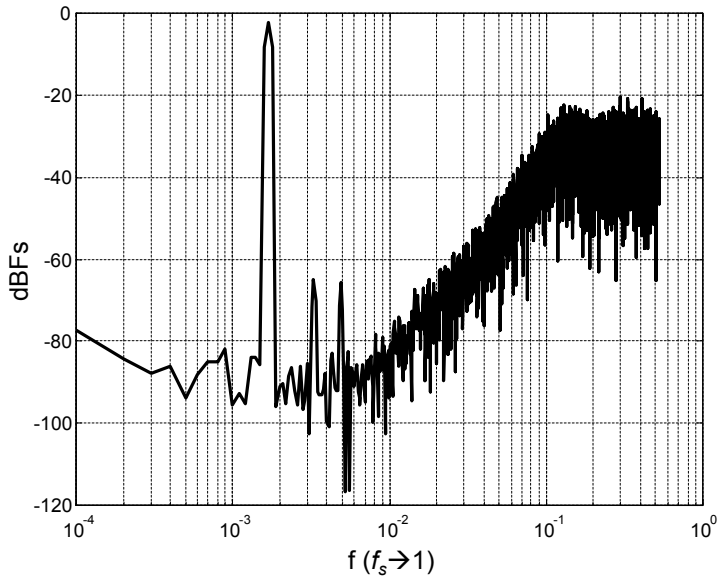

Figure 5.23. Measured 8k FFT of the low-pass 2nd order TL-ΣΔM at ABW/2.

We obtain a maximum SNDR value of 63 dB with an input signal of –3 dBFs. This value is the average of the SNDR of 10 data captures with different input phases.

Figure 5.24 shows a dynamic range of the modulator DR=62dB at f_s=53.7MHz, using an input signal at 104.883KHz.

The SNDR loss against the simulated behavior is mainly due to:

1. *1/f noise in the first transconductor*.
2. *Frequency mismatch among the resonators*. Although a trimming capacitor has been added, as suggested in chapter 4 at the connection between the transmission lines and the pads, this does not correct perfectly the mismatch among the resonance.
3. *Finite output impedance of the DAC and transconductors*. Although we have designed them using a special circuit (CMOS cascode mirror) to increase their output impedance, this is yet not enough to keep the Q factor of the resonators close to the nominal unloaded Q_0 factor of the transmission lines.
4. *Distortion of the transconductors*. As explained in chapter 4, the large state variables out of the sampling instants, can severally degrade the performance of the modulator. This is because, although in simulations this is not a problem, in the real circuit the output cascode of the transconductors is not fast enough to recover from these large swings in their outputs nodes. In Fig.5.23 we can see two

distortion tones. These tones are not cause by the linearity of the transconductors, but by the slow cascodes at the output stages of the transconductors.

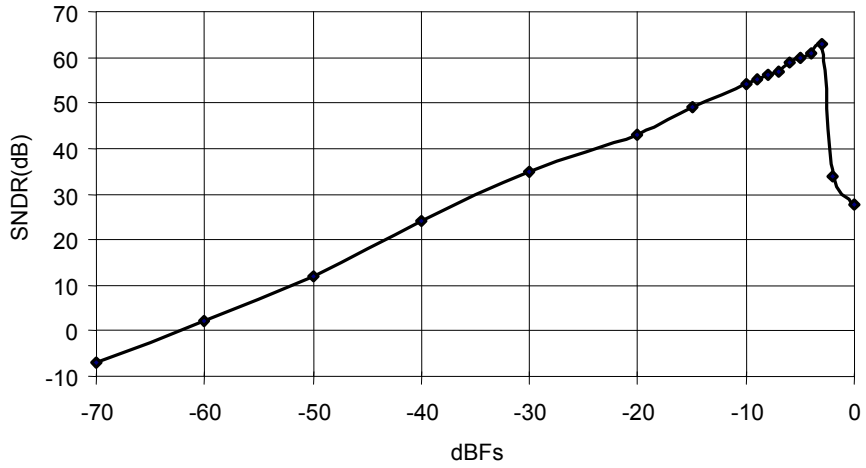

Figure 5.24. Dynamic Range of the low-pass 2nd order TL-ΣΔM.

In Figure 5.25 we show the spectrum analyzer screen hardcopy of the digital output of the chip (pin Test Out) using the TTL level output gate as a single-bit reconstruction D/A converter. For this measurement we have lowered the sampling frequency up to 9MHz. The frequency span goes from 0 Hz. to 15 MHz. We can see the noise shaping effect at DC and also the first alias around the sampling frequency.

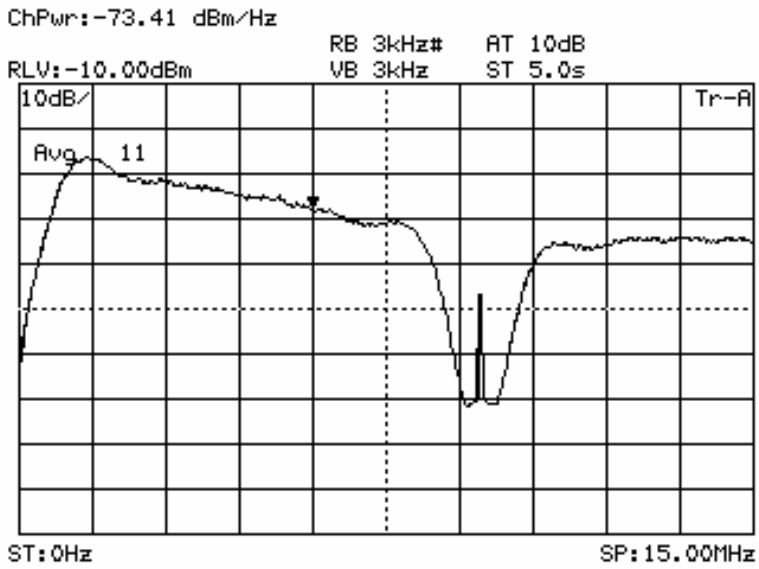

Figure 5.25. Spectrum analyzer screen hardcopy of the digital output of the low-pass 2nd order TL-ΣΔM.

At 3.3 Volt supply voltage, the power consumption of the chip was measured to be 32.4 mW analog and 16.5 mW digital. Since the circuit's goal was to demonstrate the feasibility and the jitter insensitivity of transmission line ΣΔMs, no attempt was done to obtain a power efficient design. Table 5.10 shows the power measurements of the modulator.

	I [mA]	Pwr [mW]
Analog core (VDDA)	9.8	32.4
Digital Core (VDD)	5	16.5

Table 5.10. Power measurement of the low-pass 2nd order TL-ΣΔM.

Jitter measurements

To generate the clock jitter in the test bench we will use a 74ACT04 digital inverter as clock driver whose input is the combination of a DC level, a 0dBm sine wave of the clock frequency and a gaussian noise source with programmable rms level. This jitter generation method has been preferred to a clock synthesizer modulated in phase with a noise source, because it can be modeled in Simulink in a more precise way and produces faster simulations. This clock driver guarantees that statistically the average period of the clock is constant and equal to the nominal clock (there is no cycle slip) but the clock edges are randomly placed producing time varying pulse widths in the DAC.

To demonstrate the robustness against clock jitter of the architecture, the clock jitter was increased until it was the dominant source of the in-band noise.

As jitter measurement technique we will compare the FFT of the measured data against simulations of a Simulink model of the transmission line ΣΔM and as a comparison with prior art, a second order modulator based on integrators. In these simulations we will use a clock modeled with the equivalent jitter variance.

The FFT of the measured data has been plotted in Figure 5.26 when the modulator is clocked at f_s=53.7MHz and a test tone of –15dBFs is applied. A small amplitude value for the input signal has been selected to avoid distortion in the inband spectrum. The dotted trace shows the FFT of the measured data using the nominal jitter of the clock generator (18ps rms, 0.1% of the clock period T_s). The solid trace shows the FFT of the captured data with a clock jitter variance of 186ps rms (1% of T_s), which produces only 5dB below the nominal case. For comparison purposes, the dashed trace shows the simulated output of an equivalent CT-ΣΔM implemented with ideal integrators using the same test signal and clock jitter variance of 1% of T_s. In this case, the SNDR is 15 dB below the nominal case.

As it can be seen, the spectral density of the in band noise caused by this level of jitter variance is larger in the integrator-based modulator than in the case of the transmission line modulator.

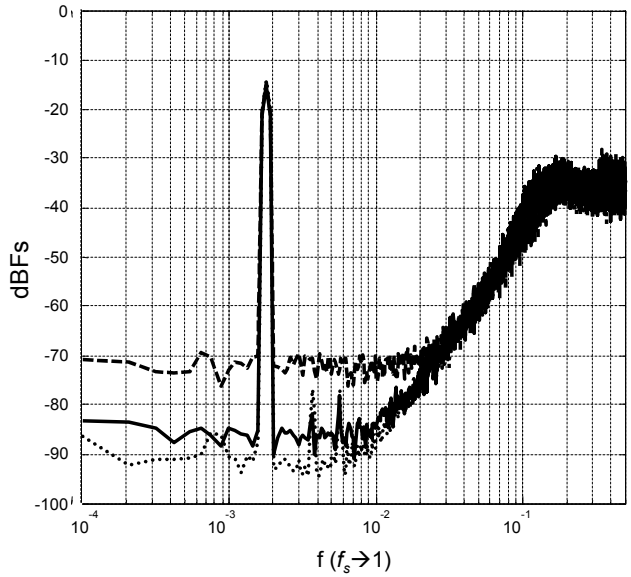

Figure 5.26. Measured output spectrum for the low-pass 2nd order TL-ΣΔM and simulated output spectrum for an equivalent integrator based CT-ΣΔM for a clock jitter of σ=1%Ts.

Idle channel measurements

The pads of the external transmission lines allow to observe the time domain waveform at the transmission line connection. The feedback DAC signal in the transmission line has a staircase shape with flat top pulses, which is the reason for a lesser jitter sensitivity.

This situation is depicted in Figure 5.27 which shows the measured voltage across gm_1 (v1(t)) in the upper trace and the clock in the lower trace. In this measurement, the modulator input was grounded (idle channel).

As may be seen, this signal is composed of staircase-like ramps corresponding to accumulated square DAC pulses. This measurement is not differential and is partially contaminated by digital ground noise.

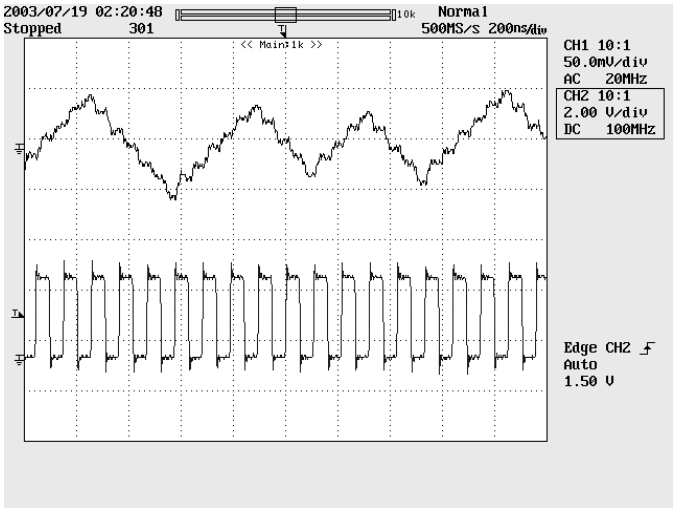

Figure 5.27. Oscilloscope capture of the first transconductor output voltage of the low-pass 2nd order TL-ΣΔM.

5.5 Conclusions

In this chapter we have demonstrated the feasibility of sigma-delta modulation with transmission lines as resonators in its loop filter.

The prototype second-order modulator was clocked at 53.7 MHz and achieves 63dB peak SNDR at an oversampling ratio of 128.

When an excessive clock jitter of 1% of the clock period is applied, the modulator SNDR is degraded by 5dB only. This is 15dB better than a conventional CT-ΣΔM with capacitive integrators.

The next two chapters will focus on two possible applications of this new architecture. The first one is a 6^{th} order bandpass transmission line ΣΔM with programmable bandwidth. The second one is a subsampling quadrature transmission line ΣΔM for use in radio receivers.

CHAPTER 6
Programmable Subsampling Bandpass Transmission Line ΣΔ Modulator in 0.35μm BiCMOS

6.1 Introduction

In this chapter we present the design and implementation of a band-pass sigma-delta modulator. This modulator is based on similar principles as the low-pass modulator described in the previous chapter and also uses transmission lines as delay elements; however it is implemented in BiCMOS technology which is more suited for RF applications.

The novelty of the modulator presented here compared to the low-pass modulator of chapter 5 is the use in the design of its equivalent discrete time NTF of a z^{-1} to z^{-2} transformation, known as 2-path transformation [Ong97]. This allows to trade off analog signal bandwidth by resolution with a single tuning coefficient.

As an additional benefit, the modulator tolerates two full clock periods of loop delay and a higher clock jitter level than conventional continuous time band pass modulators. Note that a N-path transformation is feasible in a delay-based ΣΔM due to its formal similarity with discrete time modulators (see chapter 2). An equivalent approach is not easily feasible in continuous time modulators based on lumped elements.

6.2 System level design

To design a band-pass ΣΔM with transmission lines it is better to start form a discrete time design and apply a similar transformation to the one of chapter 3 to translate a discrete time block diagram into a delayed continuous time system which permits an implementation with transmission lines. This approach allows implementing modulators that for instance, can subsample a signal due to the higher resonances of the transmission lines.

As stated before, the first step is to choose a discrete time prototype that can be transformed using the equivalence that we have describe in this thesis between a discrete time resonator and a transmission line resonator. Figure 6.1 depicts the block diagram of the proposed modulator in the Z domain:

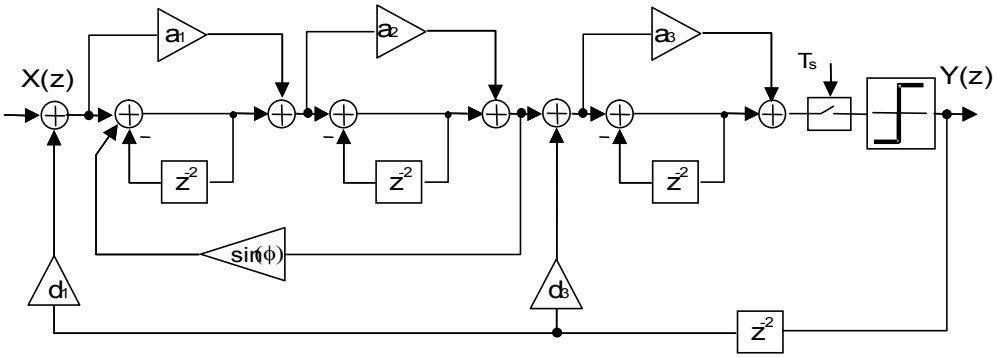

Figure 6.1. Discrete time prototype of the 6th order bandpass TL-ΣΔM.

This modulator structure is based on a cascade of resonators with local feed forward coefficients a_i and multiple feedback coefficients d_i that provide stability to the modulator. An interesting feature is that the loop includes a delay of two samples which permits to account for the delay of the quantizer at high speed.

Figure 6.2.a depicts the pole-zero plot of the NTF(z) prototype that will be used in the design. This transfer function has two complex conjugate zeroes located in the unit circle close to a real zero at z=-1. The phase $\pm\phi$ of the two complex conjugate zeroes will define the bandwidth of interest of the modulator and will be selected according to the desired oversampling ratio OSR.

The NTF has also been equipped with three poles p_0, p_1 and p^*_1 to provide stability in a single bit design. If we replace z^{-1} by z^{-2} in the NTF, the zeroes and poles are shifted around

$z=e^{\pm j\pi/2}$ and the order is doubled, as shown in Figure 6.2.b, without increase on the resonator count.

The input signal can be placed at $f_s/4$ or, if the modulator is used as a subsampling converter, at any odd integer multiply of $f_s/4$.

The expression of the NTF(z) represented in Fig. 6.2 is as follows:

$$NTF(z)=\frac{(z^2+1)\cdot(z^4-2\cos(\phi)z^2+1)}{(z^4+az^2+b)\cdot(z^2-c)} \tag{6.1}$$

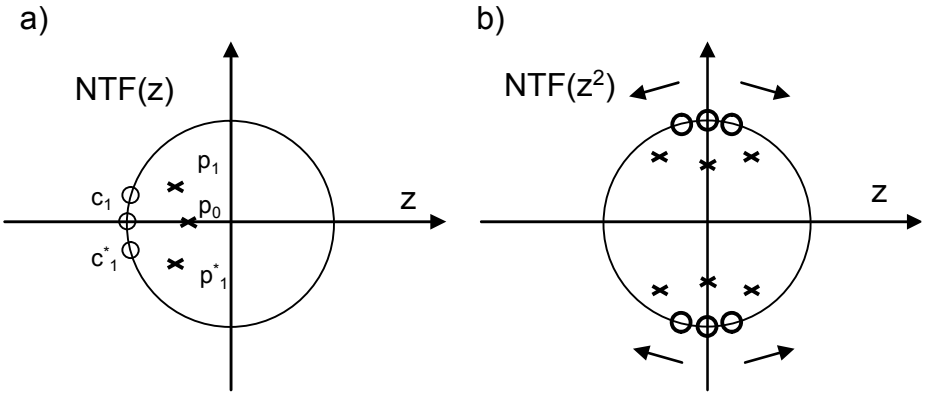

Figure 6.2. Prototype NTF pole-zero plot of the 6th order bandpass TL-ΣΔM. a) Pole-zero plot of NTF(z) prototype used in the design. b) Effect of replacing z^{-1} by z^{-2} in the NTF.

Figure 6.3 shows the modulus of the discrete noise transfer function (NTF(z)) and the discrete signal transfer function (STF(z)) of the bandpass modulator.

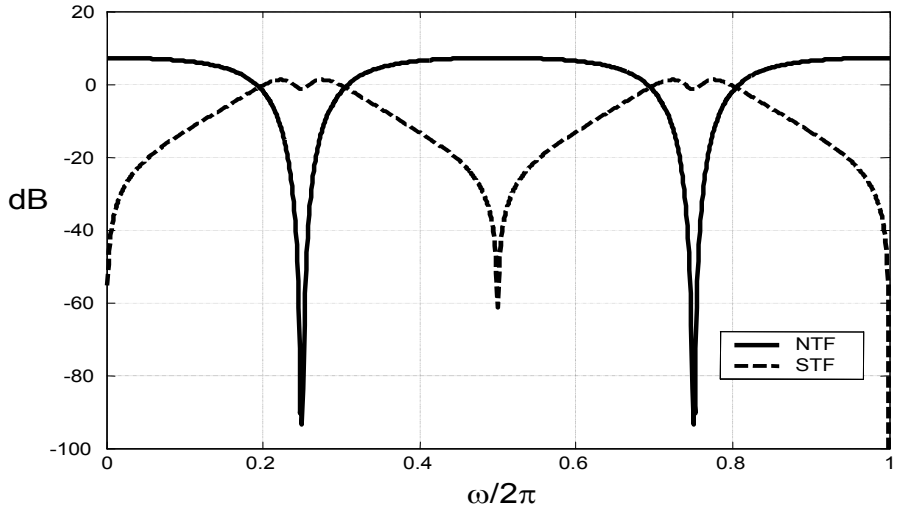

Figure 6.3. Prototype discrete NTF(z) and STF(z) plot of the 6th order bandpass TL-ΣΔM.

The next step in the design is to accomplish the block diagram of a delayed system with an equivalent behavior to the proposed discrete time modulator. We may implement such

retarded system by means of transconductors, transmission lines, a sampler and quantizer and two current feedback DACs.

The proposed system is shown in Figure 6.4, where all transmission lines are identical, have a characteristic impedance Z_0, an electrical delay T corresponding to the sampling frequency period $f_s=1/T$ and a loss parameter $A\leq 1$.

The feedforward coefficients a_i have been implemented by means of resistors in series with the transmission lines and the feedback coefficients d_i are two single bit current DACs. It must be noted that the subsampling property of the discrete time equivalent system still holds for the system of Fig.6.4 despite of the lack of an input sampler, due to the periodic frequency response of the transmission lines.

It may be shown that any of the state variables u_i complies with the following relationship:

$$U_i(s)=\left(R_i+Z_0\frac{1-A\cdot e^{-s2T}}{1+A\cdot e^{-s2T}}\right)\cdot I_i(s)$$
$$A=1-\frac{1}{Q_0} \qquad (6.2)$$

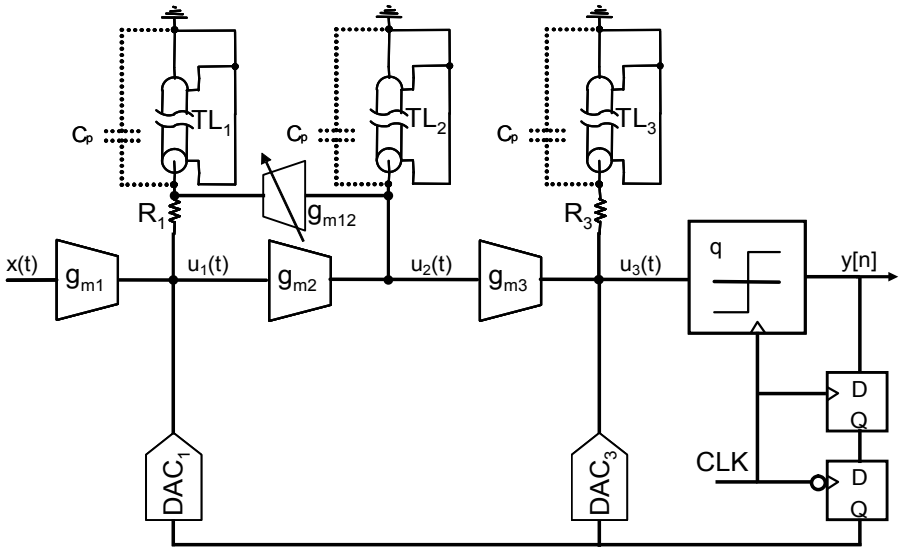

Figure 6.4. Block diagram of the bandpass 6th order TL-ΣΔM.

where Q_0 is the unloaded Q factor of the TL [Kuh94].

Considering the system equivalence defined in this thesis, we may replace e^{-s2T} by z^{-2} in Eq.6.2 and compute the corresponding NTF and STF of the modulator as if it was a discrete time system. Note that this equivalence holds for any DAC pulse shape of finite duration T, because the value of the DAC pulse in the sampling instant is what is relevant instead of the

pulse area, as a difference with a conventional CT-ΣΔM, as explained in chapter 4. Due to the same practical considerations, we will select a NRZ zero-order-hold pulse as in the design of chapter 5.

To complete the design, it suffices to equate the coefficients of Eq.6.1 with the NTF(z) obtained using Fig.6.4, Eq.6.2 (assuming A=1) and the proposed replacement. Transconductances gm_1, gm_2 and gm_3 may be considered design parameters to scale the state variables $u_i(t)$ and the STF gain. Table 6.1 shows the resulting design equations.

$dac_1 = \frac{1-b+ac-2\cos^2(\phi)+(bc-a+c)\cos(\phi)}{2Z_0^3 gm_2 gm_3\left(2\cos(\phi)-1-\cos^2(\phi)\right)}$	
$dac_3 = \frac{3-a-b+c+bc+ac-4\cos(\phi)}{4Z_0(\cos(\phi)-1)}$	
$R_1 = Z_0 \frac{(2\cos(\phi)-c+bc+a)(\cos(\phi)-1)}{1-b+ac-2\cos^2(\phi)+(bc-a+c)\cos(\phi)}$	
$R_2 = 0$	$R_3 = Z_0$
$gm_{12} = -\frac{1+\cos(\phi)}{Z_0^2 gm_2(1-\cos(\phi))}$	

Table 6.1. Design equations for the bandpass 6th order TL-ΣΔM.

The signal bandwidth of the modulator depends on angle ϕ and can be modified by transconductance gm_{12}, which moves four of the zeroes of Fig.6.2.b all together, as shown by the arrows. Setting constant values for dac_1, dac_3 and R_1 and changing only gm_{12} shifts also the location of the NTF poles. However, as ϕ approaches π, this pole shift is small enough for the modulator to remain stable, as will be verified by simulation in the next section.

The NTF expressed in Eq.6.1 requires a loop with a z^{-2} delay block. This is equivalent to delaying the quantizer data by two clock cycles before reaching the feedback DAC. The feedback path in Fig.6.4 contains a quantizer and two D flip-flops triggered in the rising and falling edges of the sampling clock respectively. For a symmetric clock signal, this configuration would update the DAC output with the data captured in the quantizer 1.5 clock cycles before. The next sampling operation in the quantizer would happen 0.5 clock cycles after the DAC update. Hence, this circuit provides the two clock cycles of delay required by the NTF and forces the sampler to sample in the middle of the zero order hold feedback DAC pulse. By doing so, the modulator is desensitized from clock jitter or code dependent distortion of the DAC pulses, which will accumulate in the DAC pulse edges, as explained in chapter 4.

In the following sub-sections we will first specify the values for the circuit parameters such as transconductance values and bandwidths, resonator Q factor or clock jitter requirements for an implementation in a 0.35u 3.3V BiCMOS technology. Afterwards we will discuss the circuit details and the measurements.

6.2.1 Loop Filter Design

To prove the validity of this design we have used the model of Fig.6.4 to simulate the system along with some circuit non-idealities.

The design has been realized with the aid of a software tool specifically designed for this type of modulators. This software tool assumes the implementation described in this section. For the implemented case, the outcome of this tool is in Figure 6.5, showing the STF, the NTF, the circuit design parameters, the FFT of a discrete time domain simulation and a plot of the state variables.

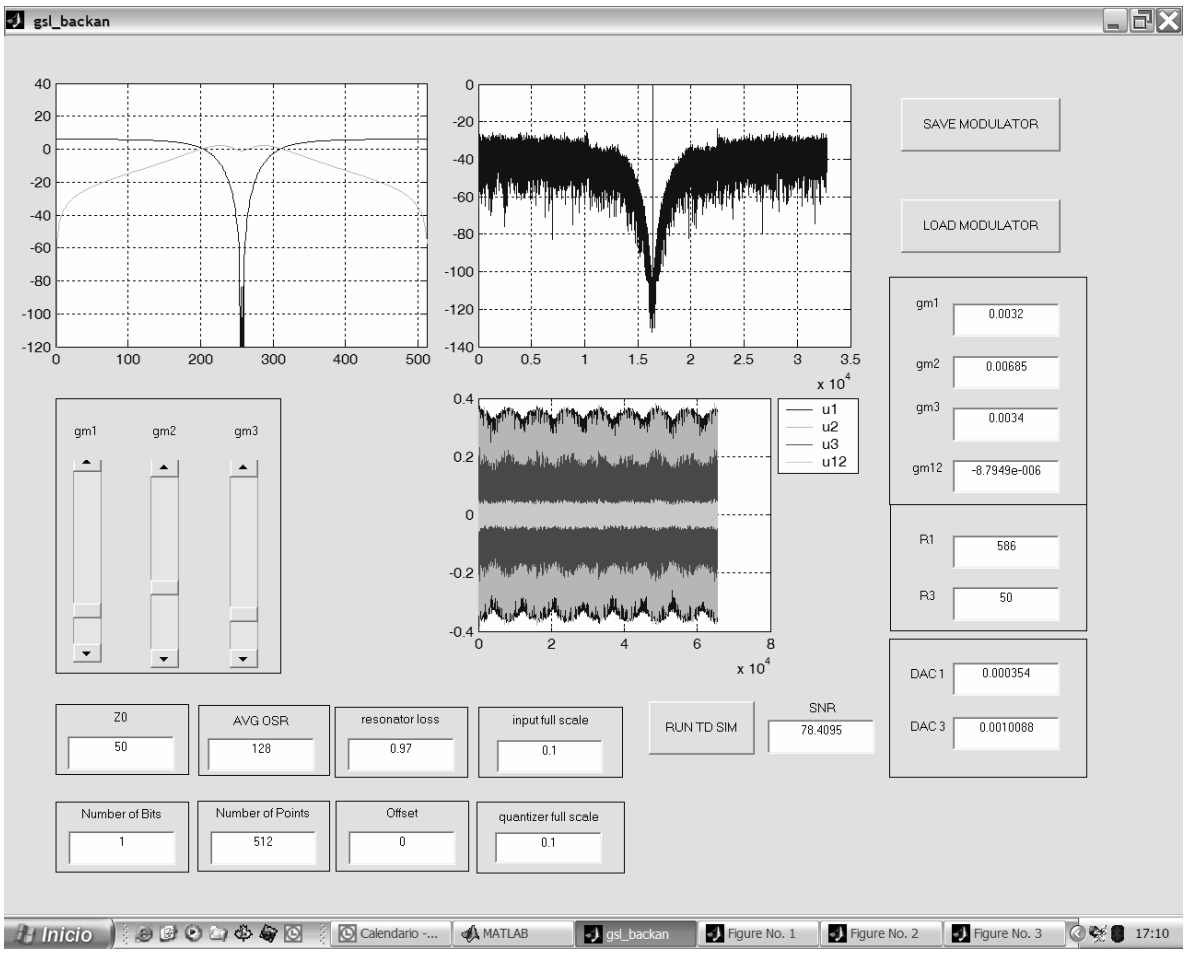

Figure 6.5. Design tool output for the bandpass 6th order TL-ΣΔM.

To define a practical case, we will use the circuit parameters expressed in Table 6.2, a line impedance of 50Ω, an input full scale 0dBFs=-10dBm and a sampling frequency f_s=200MHz.

In this way we can digitize an IF signal at $f_s/4$ or, if the modulator is used as a subsampling converter, at any odd integer multiply of $f_s/4$.

gm_1 =3.4mA/V	gm_2 =6.8mA/V	gm_3 =3.4mA/V
R_1 =586Ω	R_2 =0	R_3=50Ω
DAC_1 =±367μA		DAC_3 =±1.05mA

Table 6.2. Circuit parameters of the bandpass 6th order TL-ΣΔM.

Figure 6.6 shows the FFT of three time domain simulation of the modulator of Fig.6.4 using transmission lines with a loss parameter A=0.99 (see Eq. 6.2). The simulations use three values of gm_{12}, computed by optimizing the NTF for oversampling ratios OSR=16, OSR=128 and OSR=256 respectively.

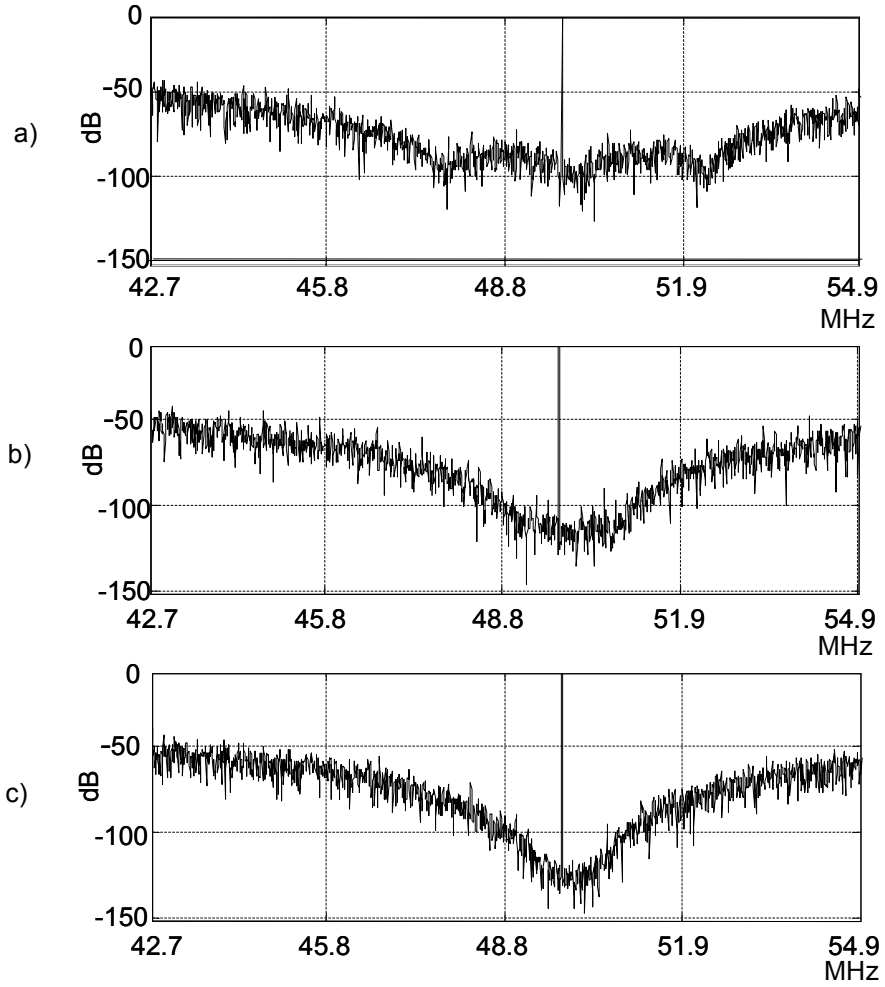

Figure 6.6. FFT of time domain simulations of the bandpass modulator of Fig.6.4 with different values of gm_{12}. a) OSR=16. b) OSR=128. c) OSR=256.

Due to the properties of transmission line modulators, the parameters in Table 6.2 are independent of the sampling clock, only the length of the transmission lines determines the clock frequency and signal band location. In the case of a standard CT-ΣΔM modulator, most of

the architecture coefficients are related to the sampling period, which forces to define such parameters in the design process. In this case, only the bandwidth requirements of the transconductors and the maximum operating frequency of the sampler and DACs set the bounds for the clock rate.

6.2.2 Finite Bandwidth of transconductors

In a practical implementation, the loop filter of the modulator will not have a perfectly periodic frequency response, as suggested by Eq.6.2, due to finite bandwidth (*BW*) of transconductors. The finite *BW* limits the performance of the modulator and sets the maximum bound for the sampling frequency f_s. To prove the feasibility of the modulator we have simulated the bandpass 6th order transmission line ΣΔM of Fig.6.4 using a first order model for the transconductors bandwidth with a dominant pole at *BW*. For this simulation we have used the conditions of Fig.6.6.c (OSR=256).

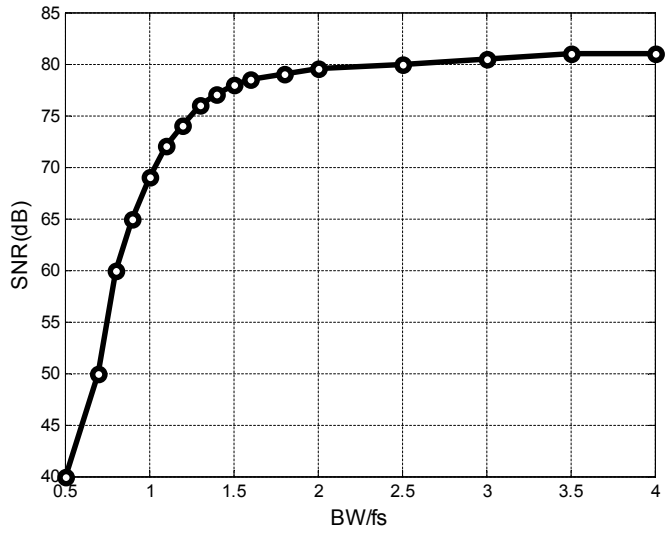

Figure 6.7. Simulated SNR vs. transconductors BW in the bandpass 6th order TL-ΣΔM.

The plot of Figure 6.7 shows the SNR of the modulator of Fig.6.4 as a function of the BW of the transconductors g_{m2} and g_{m3}. In this architecture, transconductor g_{m1} will only affect the linearity of the modulator as it is outside the loop and for this reason is not considered in this simulation. After the results of Fig.6.7, we have considered that a BW=2.5f_s for transconductors g_{m2} and g_{m3} is an adequate compromise between performance and power consumption.

6.2.3 Q factor of Transmission Lines

Another effect that limits the performance of a standard bandpass CT-ΣΔM is the Q factor of the loaded resonators of the loop filter [Sch06]. As stated before, one of the reasons because we use transmission lines is to increase the performance of the modulator due to the high Q factor that can be achieved. A usual value for the unloaded Q of a low loss transmission line is around 500. To estimate the required Q_0 of the transmission lines, we have obtained the plot of Figure 6.8 by simulation, which shows the SNR as a function of the Q_0 factor.

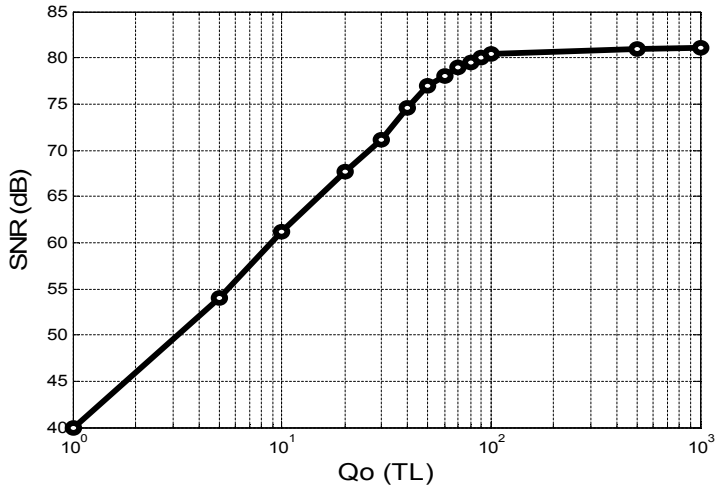

Figure 6.8. Simulated SNR vs. Q_0 factor of transmission lines in the bandpass 6th order TL-ΣΔM.

For the simulation of Fig.6.8 we have used the conditions of Fig.6.6.c (OSR=256) and a ratio BW/f_s=2.5 for g_{m2} and g_{m3}. A Q_0 of the transmission lines around 150 would be enough to ensure that our modulator achieves a performance close to the results of section 6.2.1.

6.2.4 Feedback DAC

For the block diagram of Fig.6.4 to be associated to the NTF expressed in Eq.6.1, a delay of two samples in the feedback loop is required, as shown in Fig.6.1. This is equivalent to delaying the quantizer data by two clock cycles before reaching the feedback DAC. The feedback path in Fig.6.4 contains two D flip-flops triggered in the rising and falling edges of the sampling clock respectively. For a symmetric clock signal, this configuration would update the DAC output with the data captured in the quantizer 1.5 clock cycles before. The next sampling operation in the quantizer would happen 0.5 clock cycles after the DAC update, completing the required condition, as shown in Figure 6.9.

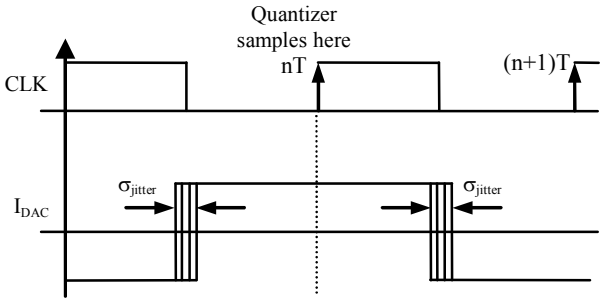

Figure 6.9. NRZ feedback DAC pulse used in the bandpass 6th order TL-ΣΔM.

6.2.5 Dynamic Range of State Variables

Once the circuit parameters of Table 6.2 are defined, we need to estimate the level of the state variables to see if they represent a feasible dynamic range for a transconductor in a BiCMOS 3.3V technology. Table 6.3 shows the peak values of the 3 state variables of Fig.6.4, u_1, u_2 and u_3. The values are computed as a function of the input voltage, both in continuous time and in the sampling instants. Table 6.3 shows two input conditions, the nominal one with a full-scale tone at $f_s/4$ and a subsampling case, with the same input tone at $3f_s/4$.

Input at $f_s/4$		**Input at $3f_s/4$**	
$u_1(t)/x(t)=2$	$u_1[nT]/x[nT]=1$	$u_1(t)/x(t)=2$	$u_1[nT]/x[nT]=1$
$u_2(t)/x(t)=2$	$u_2[nT]/x[nT]=0.72$	$u_2(t)/x(t)=4$	$u_2[nT]/x[nT]=0.72$
$u_3(t)/x(t)=48$	$u_3[nT]/x[nT]=0.48$	$u_3(t)/x(t)=160$	$u_3[nT]/x[nT]=0.48$

Table 6.3. Simulated peak values of the state variables of the bandpass 6th order TL-ΣΔM.

The difference between the peak state variables in continuous time and the maximum values in the sampling instants is produced by the mismatch between the feedback DAC spectrum, which has sync shaped aliases, and the input signal with no aliases.

As shown in Figure 6.10, the DAC aliases would be suppressed by the loop filter of a conventional CT modulator, but with a transmission line loop filter, the DAC aliases are amplified by the higher resonances of the transmission lines, which create large instantaneous voltage values in the transconductors, far from the sampling points. To prevent this effect, the Q_0 of the resonators and the transconductor bandwidth can be deliberately lowered. While this reduces the peak SNR, it also prevents high resonances values. Also a voltage clamp can be placed at the output of each transconductor [Kap05].

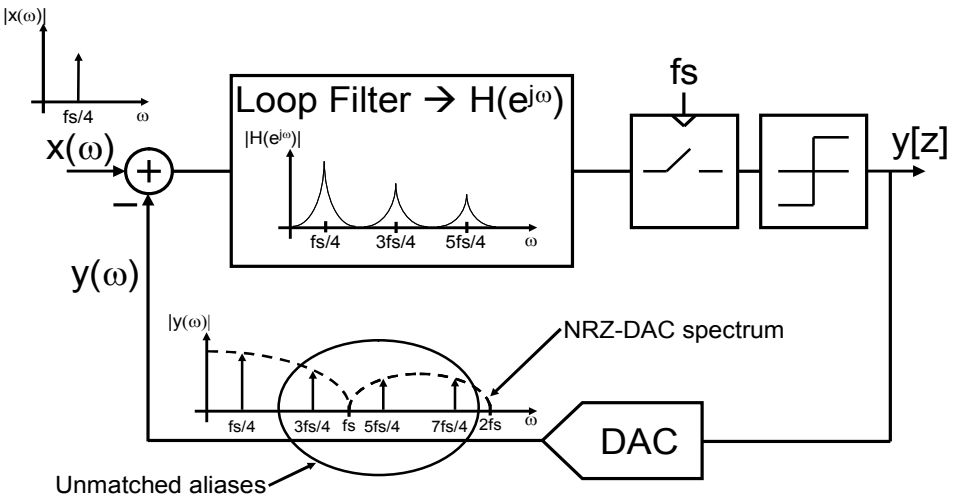

Figure 6.10. Effect of DAC aliases in the state variables of a bandpass TL-ΣΔM.

There should be a trade off between the SNR achievable due to the Q_0 factor, the dynamic range of the state variables and the minimum voltage that needs to be resolved by the quantizer (see u_3 in Table 6.3).

To evaluate this problem, a simulation of the modulator in Fig.6.4 has been made including some non-idealities. We have used a saturation model in transconductors g_{m1}, g_{m2} and g_{m3}. The saturation voltage of this model was set to 3V, while the full scale input level was set to 100mV. We have also lowered the Q_0 of transmission lines up to 100 and used a ratio BW/f_s=2.5 for gm_2 and gm_3. The result of this simulation shows that there is no significant degradation compared with the results of the modulator in section 6.2.1.

6.2.6 Clock Jitter performance

The performance of band-pass CT-ΣΔM can be limited also by clock jitter, as explained in chapter 2 and 4 of this work. Figure 6.11 shows the variation of the overall SNR of the modulator against the standard deviation of the clock jitter. Fig.6.11 shows two simulations of the transmission line band-pass ΣΔM of Fig.6.4 with an input tone of -6dBFs at $f_s/4$ and $3f_s/4$. These two simulations were made using the same parameters as in Table 6.2, a ratio BW/f_s=2.5 for g_{m2} and g_{m3} and a Q_0(TLs)=150.

We will compare the proposed transmission line band-pass ΣΔM with the results predicted in [Hai99] for conventional ΣΔ modulators. Fig.6.11 also shows the SNR considering only the noise introduced by jitter for three conventional single-bit modulators: a band-pass DT-ΣΔM with an input tone at $f_s/4$, a band-pass DT-ΣΔM with an input tone at $3f_s/4$ and a band-pass CT-ΣΔM with an input tone of -6dBFs at $f_s/4$.

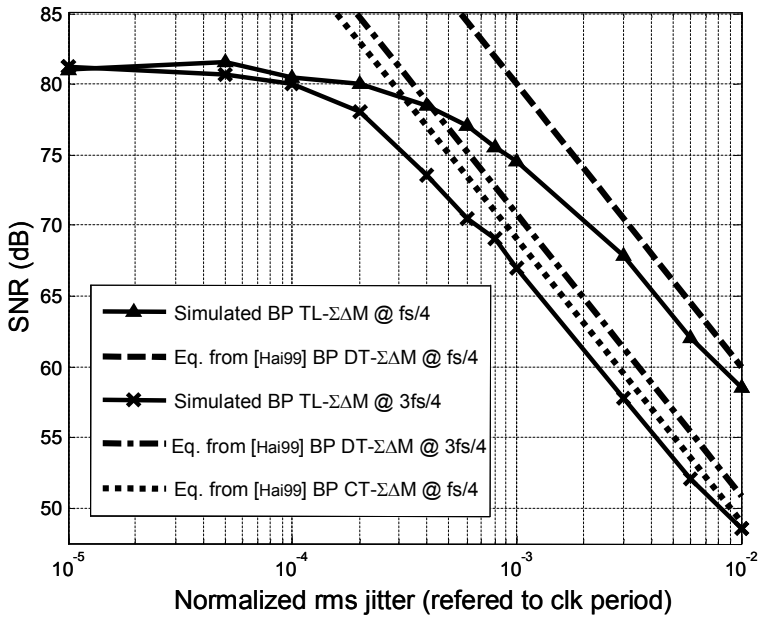

Figure 6.11. Jitter performance of the bandpass 6th order TL-ΣΔM compared to conventional BP-ΣΔMs.

When jitter noise dominates the SNR, the simulated behavior of the transmission line band-pass ΣΔM is close to that of a conventional band-pass DT-ΣΔM calculated using the equations in [Hai99], both for inputs at $f_s/4$ and $3f_s/4$.

This behavior indicates that the performance with a jittered clock in the transmission line band-pass ΣΔM approaches what could be achieved with an ideal discrete time implementation. Furthermore, if we compare the behavior of the transmission line band-pass ΣΔM with an input tone at $f_s/4$ against the calculated results of a band-pass CT-ΣΔM using equations from [Hai99], we can see that, when jitter dominates over quantization noise, the transmission line band-pass ΣΔM achieves better performance.

In conventional CT-ΣΔMs noise induced by the clock jitter at the quantizer is shaped by the loop and the relevant jitter source is the feedback DAC clock. However, [Her05] shows that in a transmission line band-pass ΣΔM modulator, jitter affects mainly at the quantizer, due to a different coupling mechanism. Observing Fig.6.11 it may be concluded that the jitter sensitivity of this transmission line modulator is between that of a discrete time modulator and a continuous time modulator.

6.2.7 Resonators Frequency Mismatch

The resonators length is designed such that the multiple resonance frequencies fold into the fundamental frequency after sampling. Deviations from the ideal resonators length

perturbate the pole and zero locations of the NTF. This results in a degradation of the modulator performance [Kap05].

However, this problem can be solved by placing a parallel trimming capacitor C_P (see Fig.6.4), as we have explained in chapter 4 and 5. Capacitor C_P corrects the phase of the resonator impedance reducing the effective transmission line delay by $T_c=Z_0C_p$ within the transconductor bandwidth [Her05]. This way, the mismatch between the transmission line length of the different resonators could be ideally adjusted to zero. Circuit simulations have shown that an estimated capacitor of C_P=2pF do not severely degrade the SNR and clock jitter properties, while allows trimming of the transmission line mismatches and may include the parasitic capacity of the pads.

6.3 Circuit Design

The system block diagram and parameters defined in the previous section were used as the start point of a BiCMOS circuit design. For this circuit, a 0.35μm SiGe process and a power supply of 3.3 Volt were selected.

The block diagram of the demonstration bandpass 6th order transmission line ΣΔM chip is shown in Figure 6.12 which is a fully differential implementation of the modulator structure in Fig.6.4. It consists of four transconductors, g_{m1}, g_{m2}, g_{m3} and g_{m12}, a single bit quantizer, two 1-bit feedback DACs, an auxiliary DAC and a digital interface block.

The 50Ω transmission lines are not implemented on-chip. This way, ESD-protected bond pads were used to connect the output of each transconductor to the transmission lines.

A clock frequency of f_s = 200MHz was targeted for this design, as explained in previous section. Also, setting the input full-scale level at 100mV, with a 50Ohm source, results in a thermal noise 10dB below the quantization noise. A smaller value of the input full scale would optimize the power consumption of the modulator but could produce quantizer metastability due to the low level of state variable u_3 in the sampling points (see section 6.2.5). Also, there must be a trade off between the input full scale and the peak values of the state variables to ease the recovery from saturation in the transconductors.

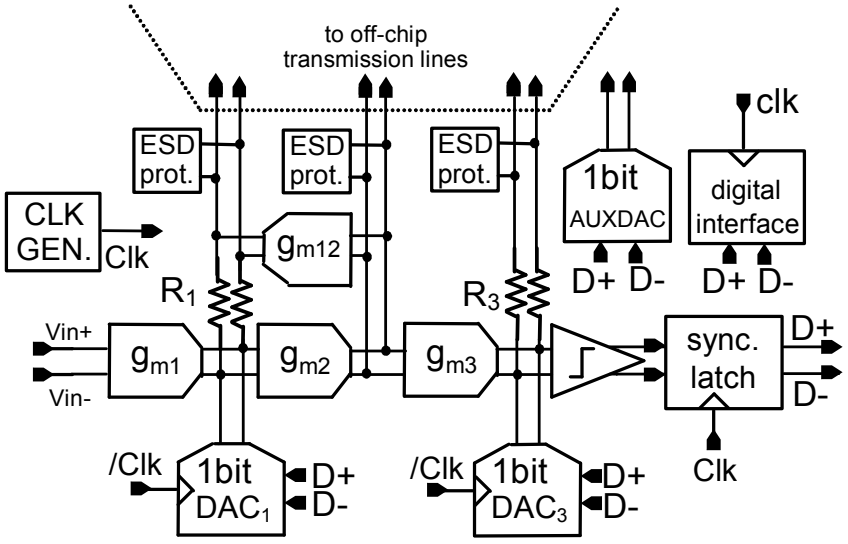

Figure 6.12. Block diagram of the bandpass 6th order TL-ΣΔM chip.

6.3.1 First transconductor (g_{m1})

The most demanding building block of the entire circuit is the input transconductor. This block should be at least as linear as the linearity of the overall modulator, as explained in the previous chapter. The reason for this is that this transconductor performs the voltage-to-current conversion of the input signal prior to entering the feedback loop. Hence, non-linearity of this transconductor is not attenuated by the operation of the loop.

Figure 6.13 shows a simplified schematic of g_{m1} (see Fig.6.12). This transconductor is based on a source degenerated differential pair with two operational amplifiers A1 and A2 added at the inputs to enhance the linearity. These amplifiers are implemented as simple PMOS differential pairs with active loads.

Transconductor g_{m1} has been designed for a BW=300MHz, to allow subsampling of inputs beyond the sampling frequency. This input transconductor does only require the bandwidth of the input signal instead of 2.5 times the sampling frequency, as stated in the previous section, which only applies to transconductors g_{m2} and g_{m3} (see Fig.6.12).

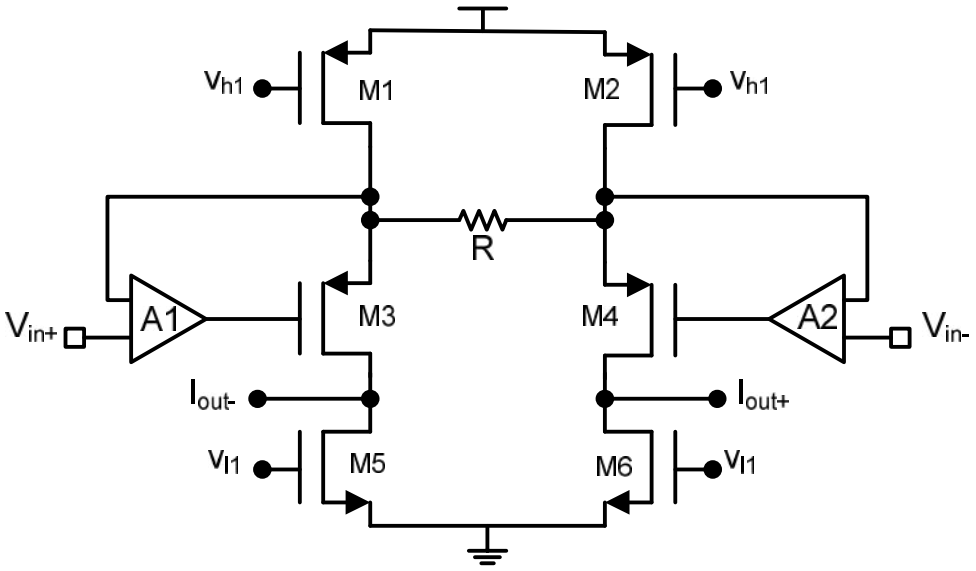

Figure 6.13. Simplified schematic of the input transconductor g_{m1} of the bandpass 6th order TL-ΣΔM.

The resistor R is a linear resistor which is available in the target process. The value of R is calculated using the value of g_{m1} in Table 6.2. Then, using an approximated relation between the input voltage and the output current through the resistor, its value is $R = 2/g_{m1} = 590\Omega$. This value was a compromise between noise and power consumption.

In this design we have not used a current cascode for the output of the transconductor. Instead, we have designed transistors M5 and M6 with relatively long channels to keep the high

output impedance needed to avoid a reduction of the loaded Q factor of the resonators. Also, in this way we can save area and power because the bias circuit is simpler than the circuit used in chapter 5 for the input transconductor. Table 6.4 shows the sizes of these CMOS transistors of the first transconductor.

CMOS trts.	W/L [μm]
M1,M2	156/0.35
M3,M4	80/0.35
M5,M6	200/1.2

Table 6.4. CMOS transistors of the input transconductor of the bandpass 6th order TL-ΣΔM.

Another point that was modified in this design compared with the circuit of chapter 5 is the CMFB circuit. In this case the transmission lines are DC coupled and used as supply points of the transconductors common mode voltage. Also, this helps to reduce the power consumption and simplifies the design.

6.3.2 Second and third transconductors (g_{m2} and g_{m3})

The second and third transconductors (g_{m2} and g_{m3} in fig.6.12) are implemented as a simple bipolar differential pair with emitter degeneration and a poly resistor (R) that sets the transconductance. This simple implementation is possible because non-linearity of these blocks is attenuated by the operation of the loop. Also, due to the simplicity of these blocks, they can achieve high bandwidth.

Using the results of section 6.2.2, a bandwidth of $2.5f_s$=500MHz was selected to achieve a compromise between clock jitter desensitization, feasibility and power consumption.

Figure 6.14 shows a simplified schematic of the second (g_{m2}) and third (g_{m3}) transconductors of the bandpass 6th order TL-ΣΔM of Fig.6.12. To achieve the proper bandwidth for the second and third transconductors, we have used bipolar transistors to realize the voltage-to-current conversion (B1 and B2 in Fig.6.14). These transistors are available in the targeted process. This way, we can increase the bandwidth of the implemented transconductors without increasing their power consumption due to the high cutoff frequency (ft) of such transistors.

As explained in section 6.3.1 for the input transconductor, we have used the transmission lines also as supply points for the common mode voltages of g_{m2} and g_{m3}. This way we save area and power because we don't need a CMFB circuit.

Another important point in the design of these transconductors is the output impedance at node *y* of Fig.6.14. We need transconductors with a high output impedance to avoid a reduction in the loaded Q factor of the resonators.

One possible solution is to increase the output impedance by using a current cascode PMOS transistor in the output of the transconductors. This will increase the area and the power consumption of the bias circuit.

In the other hand we can increase this output impedance by using relatively long channels in transistors M1 and M2 of Fig.6.14. This way we can save area and power as well.

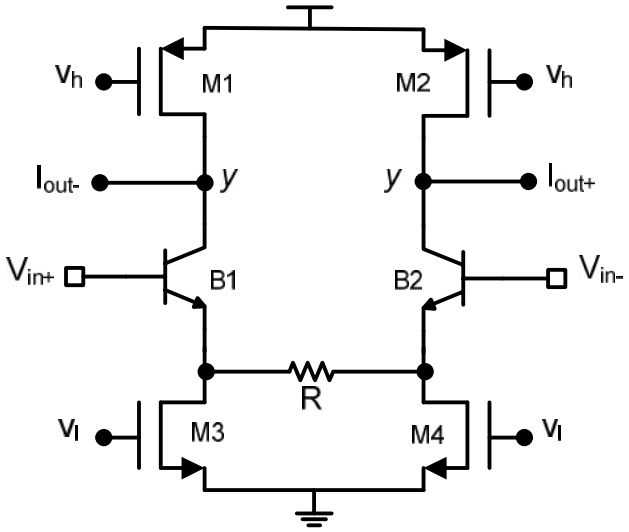

Figure 6.14. Simplified schematic of the second (g_{m2}) and third (g_{m3}) transconductors of the bandpass 6th order TL-ΣΔM.

Table 6.5 shows the sizes of the transistors of transconductors g_{m2} and g_{m3} of the bandpass 6th order TL-ΣΔM. Also in Table 6.5 we show the value of the resistor R that fits the transconductance of each transconductor.

g_{m2}		**g_{m3}**	
CMOS trts.	**W/L [μm]**	**CMOS trts.**	**W/L [μm]**
M1,M2	200/1	M1,M2	300/1
M3,M4	200/1	M3,M4	300/1
Bipolar trts.	**Ratio**	**Bipolar trts.**	**Ratio**
B1,B2	4	B1,B2	4
R	150 Ω	**R**	300 Ω

Table 6.5. Design parameters of the second and third transconductors of the bandpass 6th order TL-ΣΔM.

Transconductor g_{m12} is similar to g_{m2} and g_{m3} but with a programmable transconductance.

6.3.3 Single bit Quantizer

The 1-bit quantizer of the modulator is implemented as shown in Figure 6.15. It consists of a pre-amplifier and a two stage regenerative latch. Due to the architecture of the modulator, which includes a two clock cycle delay in its feedback path, the synchronization latch and the clock drivers provide a delay of 1.5 clock cycles between the comparator sampling and the update of the DAC outputs. For this reason a D-flip-flop (DFF) has been included in Fig.6.15 to provide a complete full cycle of delay between the latch and DACs. The other half cycle is realized by updating the DACs with the inverse clock (/CLK) compare with the latch and the DFF.

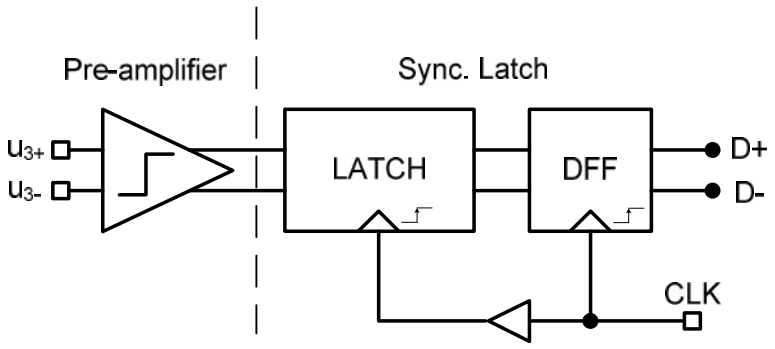

Figure 6.15. 1-bit quantizer simplified schematic of the bandpass 6th order TL-ΣΔM.

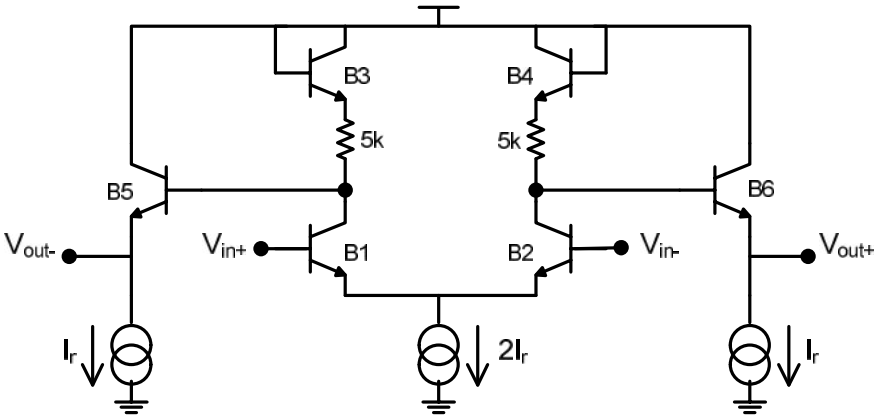

Figure 6.16. Pre-amplifier simplified schematic of the bandpass 6th order TL-ΣΔM.

In the quantizer of Fig.6.15 we have used a pre-amplifier in order to avoid kickback of the latch in the sampling instant of the clock (CLK). However, this pre-amplifier is also used to amplify the input to the latch ($u_3(t)$ in Fig.6.4) in order to reduce the metastability of the quantizer. Also, the pre-amplifier helps to ease the design of the input stage of the latch,

reducing its power consumption. Figure 6.16 shows a simplified schematic of the pre-amplifier. We have used bipolar transistors in order to have more gain and bandwidth compared with a pure CMOS design.

The pre-amplifier of Fig.6.16 has two stages. The input stage (B1 and B2) is used to fix its gain. The second stage is a voltage follower (B5 and B6) to decouple the pre-amplifier from the latch.

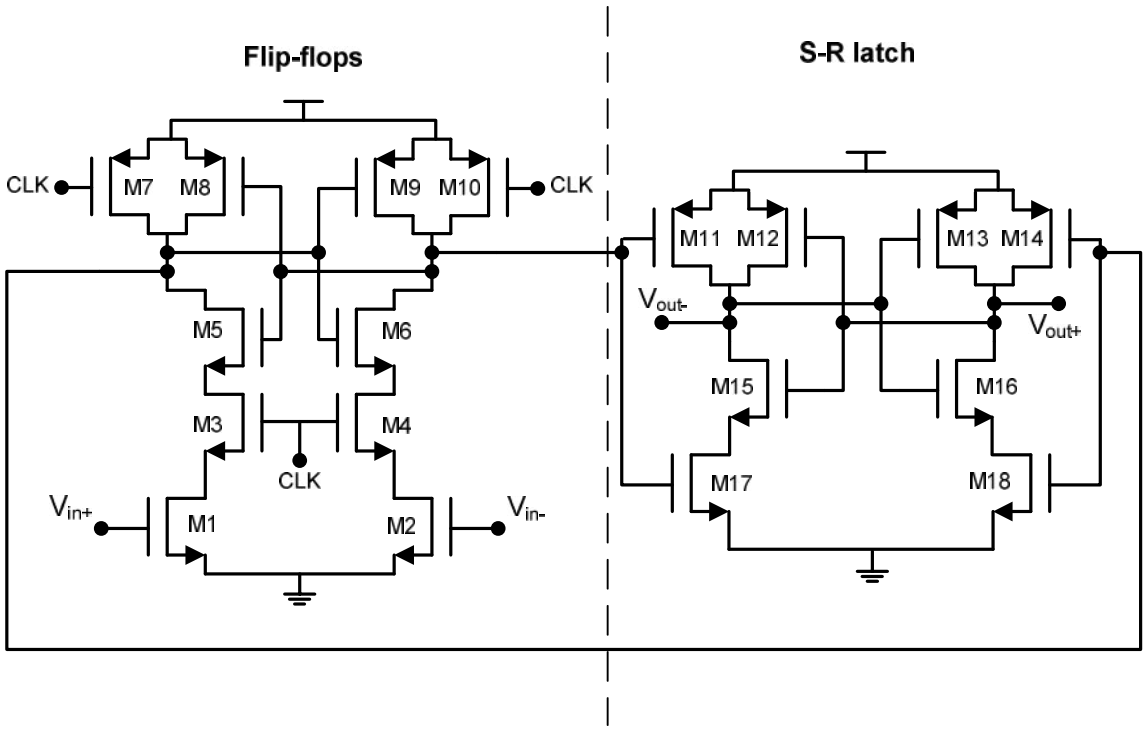

Figure 6.17. Simplified schematic of the two-stage regenerative latch of the bandpass 6th order TL-ΣΔM.

Table 6.6 shows the transistors sizes of the latch of Fig.6.17.

CMOS trts.	W/L [μm]
M1,M2	8/0.35
M3,M4	2/0.35
M5,M6,M7,M8,M9,M10	2/0.35
M11,M12,M13,M14	1/0.35
M15,M16,M17,M18	0.4/0.35

Table 6.6. CMOS transistors of the latch of Fig.6.17.

Figure 6.17 shows a simplified schematic of the two-stage regenerative latch of Fig.6.15. This is a version of the latch described in [Gee99]. It consists of a top and bottom regeneration loop divided into two stages. The first one is a flip-flop stage similar to what was used in chapter 5 (see section 5.3.4 and Fig.5.17). The second stage is an S-R latch that stores and regenerates the data captured in the first stage. As far as the output of this latch is connected to

a DFF, no extra logic is needed to adequate the output signals to the correct value. Only a carefully layout is needed to place together these two blocks and make sure that the DFF does not load the latch.

6.3.4 DACs

Next we will describe the implementation of the two 1-bit DACs, DAC_1 and DAC_3 in Fig.6.12. Figure 6.18 shows a simplified schematic of the 1-bit DAC scheme used for both DACs. It is composed of a synchronization latch (Gigalatch) that drives the switches of a 1-bit NRZ current cell [Van01].

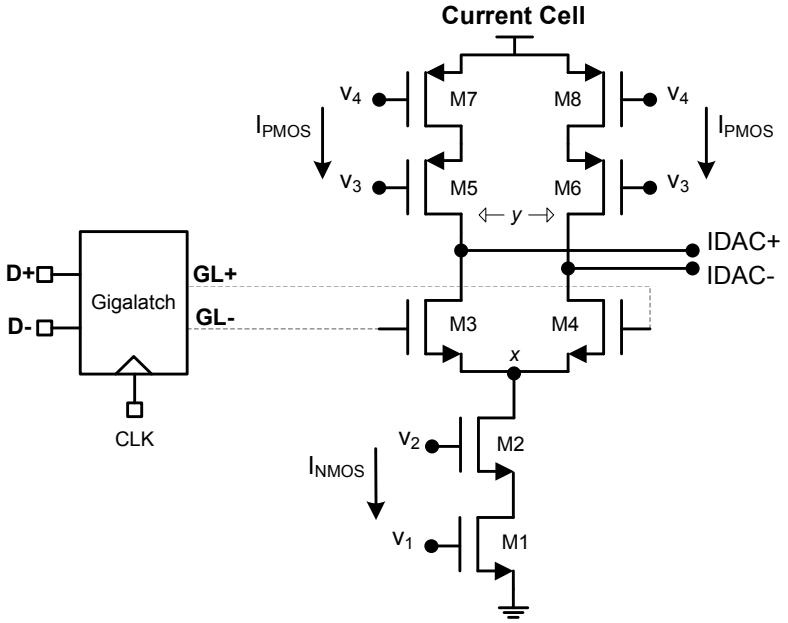

Figure 6.18. NRZ 1-bit DAC simplified schematic of the bandpass 6th order TL-ΣΔM.

The dynamic performance degradation of a current-steering D/A converter can be caused by several reasons [Van01]. Some important issues that have been identified to cause dynamic limitations have been explained in previous chapter (section 5.3.3) and in this design are also considered. To minimize these effects, a well-designed and carefully laid out synchronized driver (Gigalatch) is used as explained in section 5.3.3. A major function of this driver is shifting the crossing point of the switch transistor's differential control signals, in such a way that these transistors are never simultaneously in the off state. The driver also performs the final synchronization. By placing it in front of the switches and by paying attention to symmetrical interconnections in the layout, the difference in delay between the different digital decoder outputs is minimized.

The 1-bit NRZ current cell of Fig.6.18 is similar to what was designed in [Van01], but with some changes. In this schematic, transistor M1 is the NMOS current source of the DAC, and transistors M7 and M8 are the PMOS current source of the DAC. In his design we have implemented also wide-swing current mirrors [Joh97] by placing NMOS and PMOS cascodes in each current source (transistor M2 for the NMOS cascode and transistors M5 and M6 for the PMOS cascode). Transistors M3 and M4 are the switches driven by the Gigalatch.

The full-scale current of each DAC is calculated from Table 6.2. In this design this value is composed by the difference between the NMOS and the PMOS current sources.

One restriction in the design of the DAC is the output impedance at nodes *x* and *y* of Fig.6.18. The output impedance of the DAC should be large enough to avoid a reduction of the loaded Q factor of the associated resonator through the frequency of interest [Van01]. This high-frequency output impedance design specification is one of the critical elements to size the high-frequency Q factor behavior of the resonators. For this reason a NMOS and PMOS wide-swing current mirrors have been designed to implement the NMOS and PMOS current sources of the DACs.

Table 6.7 shows the sizes of the CMOS transistors and the current sources of the two NRZ 1-bit DACs of this design.

DAC_1		**DAC_3**	
CMOS trts.	**W/L [μm]**	**CMOS trts.**	**W/L [μm]**
M1	70/2	M1	200/2
M2	28/0.6	M2	80/0.6
M3,M4	3.5/0.35	M3,M4	10/0.35
M5,M6	70/0.35	M5,M6	200/0.35
M7,M8	168/1	M7,M8	480/1
Current sources	**μA**	**Current sources**	**μA**
I_{NMOS}	367	I_{NMOS}	1050
I_{PMOS}	525	I_{PMOS}	525

Table 6.7. CMOS transistors and current sources of the two NRZ DACs of the bandpass 6th order TL-ΣΔM.

6.3.5 Clock generator

The internal clock signals are generated using an input clock buffer (block CLKGEN in Fig.6.12). This block produces a digital level clock signal to drive the quantizer and DACs from a low level external sinusoidal source. It is composed of a cascade of low noise amplifiers (LNA) and a differential to single-ended circuit that produce the CMOS clock signal. Figure 6.19 shows a simplified schematic of the input clock buffer.

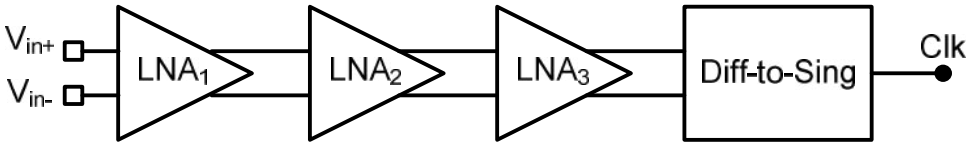

Figure 6.19. Input clock buffer simplified schematic of the bandpass 6th order TL-ΣΔM.

The CMOS clock signal must followed by a clock tree made of buffering inverters to drive all the clock paths of the chip.

Figure 6.20.a shows a simplified schematic of the LNAs used in the input clock buffer. They consist in a degenerated bipolar differential pair with active loads to enhance their gain and bandwidth.

Figure 6.20.b shows a simplified schematic of the differential to single-ended circuit used in the input clock buffer. This circuit transforms the differential signal that comes from the LNAs to a two opposite single-ended CMOS signals that can be used to drive the different clocks of the chip.

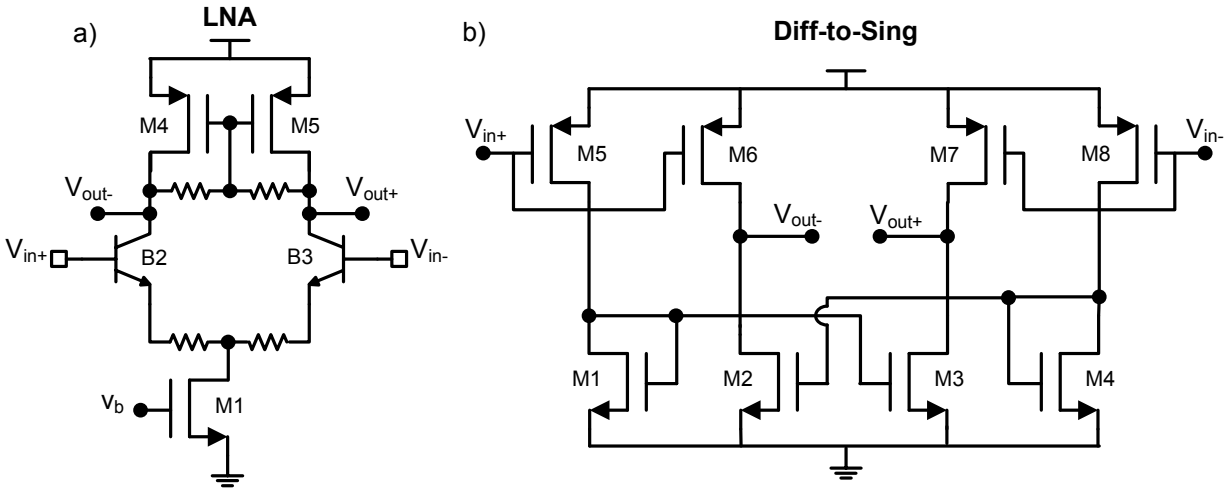

Figure 6.20. a) Simplified schematic of a LNA of the input clock buffer. b) Simplified schematic of the differential to single-ended circuit.

6.3.6 Output interface

To measure the performance of the chip we have implemented two circuits to capture the output data of the chip.

The first one is the digital block (see Fig.6.12) that groups 16 consecutive output bits in a single 16-bit word to reduce the clock rate of the output digital pads. This block has been designed using the same architecture as in section 5.3.5. The only difference is that we use a single 16-bit word instead of a single 8-bit word.

The digital interface has been designed using the standard cells of the technology. However, as the target sampling frequency is 200MHz, and therefore the clock rate of the digital output is 12.5MHz, no optimization of this block was needed.

The second one is a dedicated single bit DAC (AUXDAC in Fig.6.12) that is used to represent in real time the spectrum of the output data in an analog spectrum analyzer to perform online trimmings. It must be noted that this auxiliary DAC reproduces the same data as the DACs used in the feedback path and will differ from the digital capture. Also, the architecture of this auxiliary DAC is the same as we have used for the feedback path DACs (see Fig.6.18).

6.3.7 Power estimation

Once all the main blocks of the modulator are designed, we can estimate the power consumption of the chip. For this purpose we have run a transient simulation in Spectre, with a full spice transistor-level model of the modulator. For this calculation we have taken into account only the next blocks from Fig.6.12:

- g_{m1}, g_{m2}, g_{m3}, g_{m12}, 1-bit quantizer, 1-bit DAC_1 and 1-bit DAC_3

Table 6.8 shows the rms value of an equivalent current source, connected to the power supply of each block of the modulator.

Block	Irms [mA]	Pwr [mW]
g_{m1}	4.1	13.53
g_{m2}	2.9	9.57
g_{m3}	2.5	8.25
g_{m12}	0.9	2.97
1-bit Quantizer	1.9	6.27
1-bit DAC_1	2.3	7.59
1-bit DAC_3	3.4	11.22
Total	18	**59.4**

Table 6.8.Power estimation of the lowpass 2nd order transmission line ΣΔM of Fig.5.10.

6.3.8 Transistor-level simulation

Finally, we have made a full SPICE transistor-level simulation of the chip in Spectre. We have used an input tone at $f_s/4$-$ABW/4$=49.8MHz, with an analog bandwidth $ABW=f_s/2/OSR$=782kHz. The analog bandwidth of the modulator depends on angle ϕ of Eq.6.1 that can be modified by transconductance g_{m12}, which moves four of the zeroes of the NTF. For this simulation we have used an OSR=128. The sampling frequency of this simulation was f_s=200MHz and the amplitude of the tone was -3dFs, where we have defined the full-scale of the modulator to be Fs=100mV, as discussed in section 6.2.5.

The parasitic capacity of the pad that connects the transmission lines perturbates the pole and zero locations of the NTF. Circuit simulations have shown that an estimated parasitic capacitor of the output pad is around 1.8pF. This parasitic capacity has been increased intentionally by a trimming capacitor C_p (see section 6.2.7), in parallel with the transmission lines, in spite of degrading the clock jitter robustness [Her05] to allow trimming of the transmission line mismatches. We have placed a parallel capacitor C_p=2pF.

The transmission line delay has to be corrected by the time constant: $\tau=Z_0 \cdot C_p$, as explained in section 6.2.7. In this case, the characteristic impedance of the transmission line was set to 50Ω and the Q_0 factor of the transmission line was simulated by a parallel resistor of 1Ω at the far end of the transmission line to introduce loss in the reflection.

Figure 6.21 shows the FFT of the modulator output computed with a transistor level simulation of 8K points. The simulation produces a SNDR of 70dB. As it can be seen in Fig.6.21, the behavior of the modulator is limited by distortion, which is responsible of the spurs seen in Fig.6.21. This effect is due to the large state variables outside the sampling points, as explained in section 6.2.5.

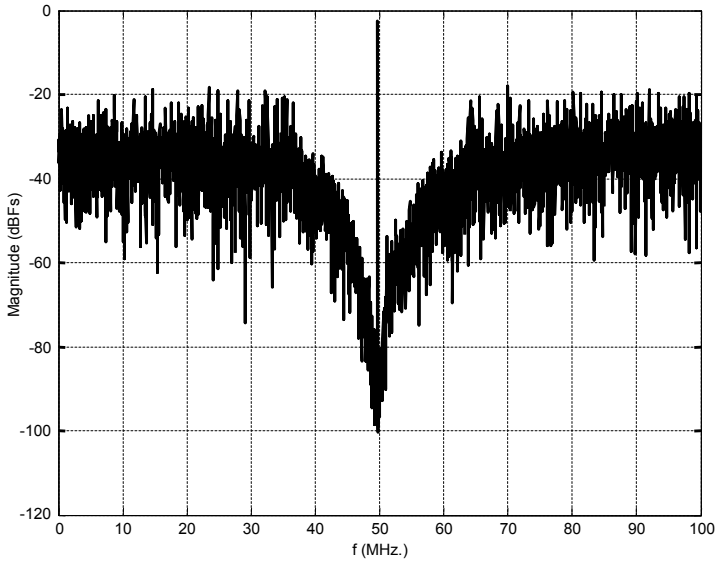

Figure 6.21. FFT (8k points) of a transistor level simulation of the bandpass 6th order TL-ΣΔM.

6.4 Implementation and measurements

6.4.1 Layout considerations

A photograph of the prototype chip is shown in Figure 6.22. The layout of each block and the final floor planning has been completed taking into consideration the pad routing to minimize the parasitic capacity at the transmission line connections. Also we have taken into account the same precautions as in section 5.4.1. The chip measures 6 mm^2 due to the pad ring requirements.

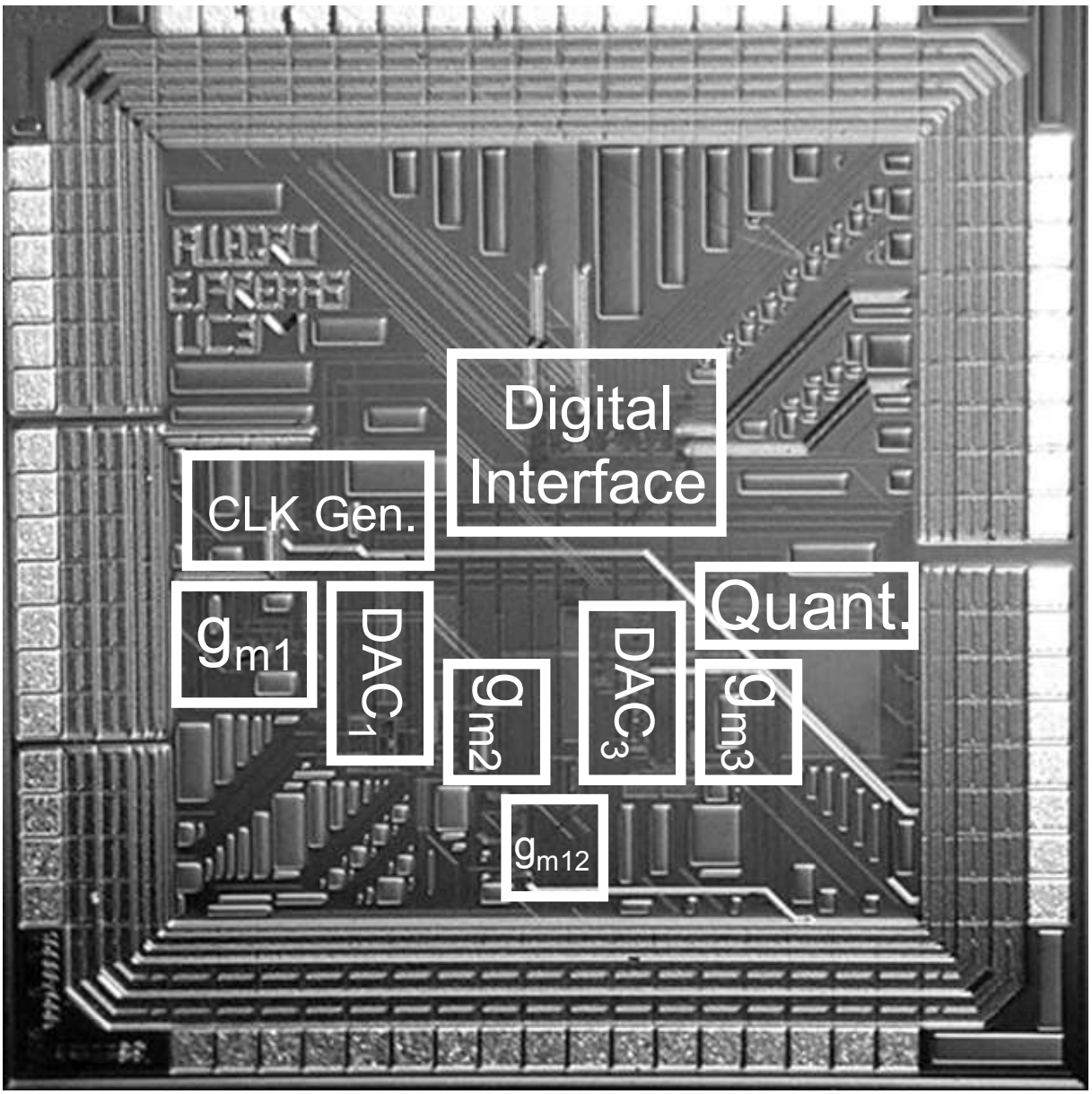

Figure 6.22. Chip microphotograph of the bandpass 6th order TL-ΣΔM.

6.4.2 Chip measurements

The test setup consisted of a PCB with current references, single ended to differential transformers to couple the input signal sources (input sine wave and input clock sine wave), an interface to a spectrum analyzer to represent the output of the auxiliary DAC and an interface to a logic analyzer connected to the digital test interface of the chip. Figure 6.23.a shows a simplified schematic of the PCB used to test the chip. Figure 6.23.b shows a picture of the fabricated PCB, showing the ceramic coaxial transmission lines.

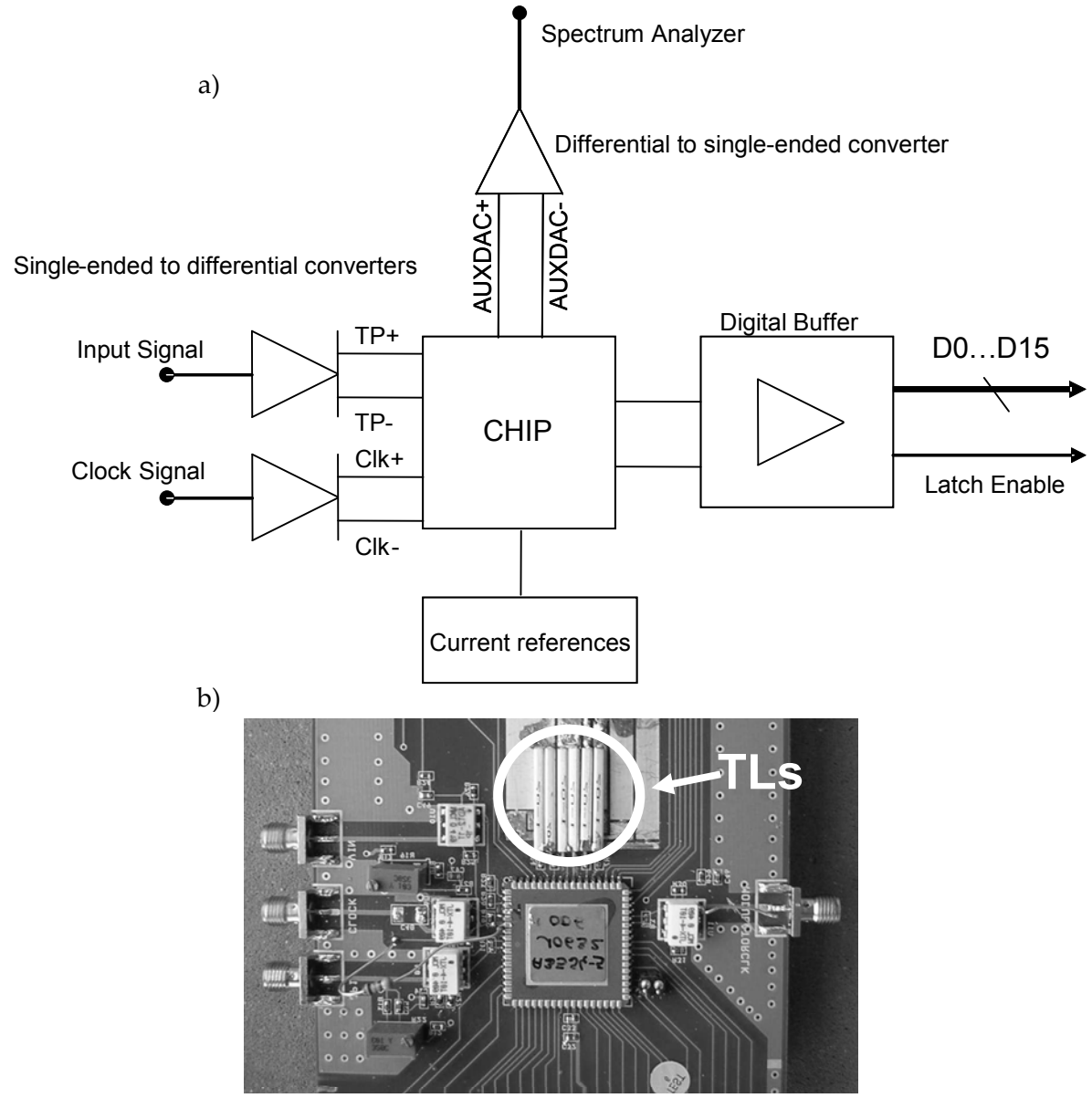

Figure 6.23. a) PCB simplified schematic used to test the bandpass 6th order TL-ΣΔM chip. b) Photograph of the PCB.

Also, to test the chip, six 50Ohm off-chip ceramic coaxial resonators were used as transmissio lines with a frequency tolerance of 1%. Detuning of the resonators was compensated using external trimming capacitors, as explained in previous sections.

In order to capture the data and make all the measurements that we will propose in this section, we have used the same test bench as in section 5.4.2 that is represented in Fig.5.22.

Nyquist measurements

The chip was tested using a clock frequency of 184MHz. The difference with the targeted frequency of the system (200MHz.) design was due to the commercial availability of ceramic coaxial resonators.

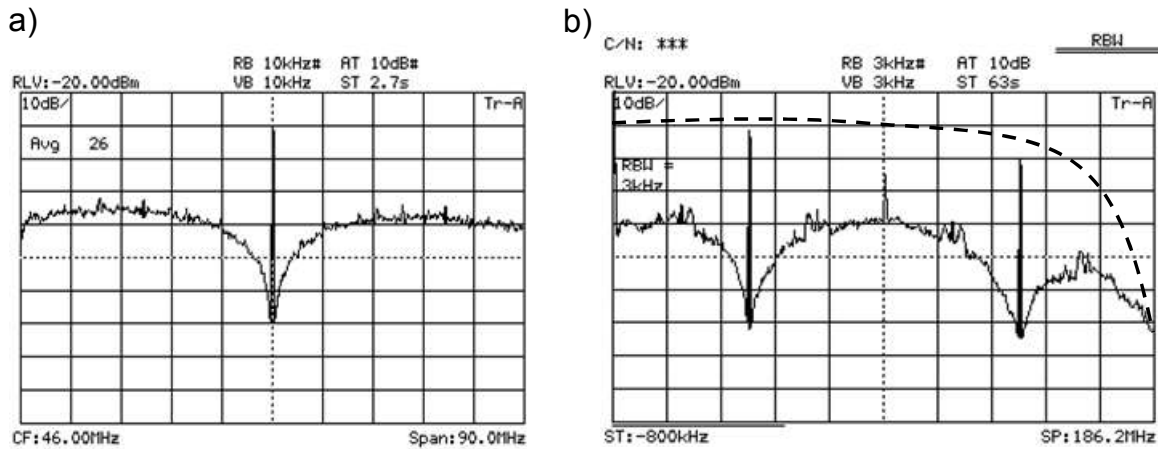

Figure 6.24. Output spectrum of the bandpass 6th order TL-ΣΔM.

The first measurement that we realized was to trim the modulator to obtain the desired NTF. For this purpose we used an input tone of -6dBFs at 46.02MHz. Figure 6.24 shows two spectrum analyzer captures taken at the AUXDAC output, showing the expected shape for the modulator output.

Fig.6.24.a shows a capture of the spectrum analyzer where the frequency span goes from 0 to $f_s/2$=92MHz. In this plot we can see the expected NTF of the modulator with the notch at $f_s/4$.

Fig.6.24.b shows a capture of the spectrum analyzer with a frequency span from 0 to f_s=184MHZ. Also, in this plot we have superimposed the feedback DAC transfer function (dashed line) which is represented by a sinc function with a cero at f_s. Fig.6.24.b shows the expected behavior of the modulator, where the input tone at $f_s/4$ also appears at $3f_s/4$ due to periodic poles of the NTF. The notches of the NTF are at odd multiples of $f_s/4$.

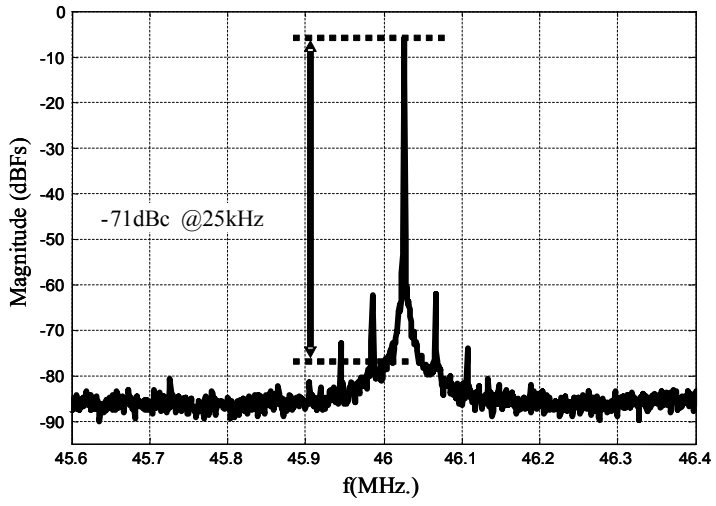

Figure 6.25. FFT plot of a digital capture within the signal band (input at $f_s/4$) of the bandpass 6th order TL-ΣΔM.

Figure 6.25 shows a close up view of a 512K point FFT of the same data as in Fig.6.24, taken from the digital interface, which allows to estimate a peak SNDR of 58dB with an OSR=256. The dynamic range of the modulator was limited to 40dB. As no DC regulation loop was implemented, the limited dynamic range is assumed to be due to the offset produced by the loop filter at the comparator, which stops the operation of the modulator for small inputs. Adding a dither signal at the external connections of g_{m3} extended the dynamic range but at the expense of altering the load of the transmission line and its Q factor.

Operation as a sub-sampling ADC

Next, we will show the ability to perform subsampling of the input signal. To test the subsampling capability of this modulator, a signal located at $3f_s/4$ was used. We repeated the data capture in Fig.6.25 in Figure 6.26 with a signal located at 137.98MHz and equivalent amplitude. In this case, the peak SNDR obtained was 53dB, thus proving the down conversion capabilities by subsampling of this architecture.

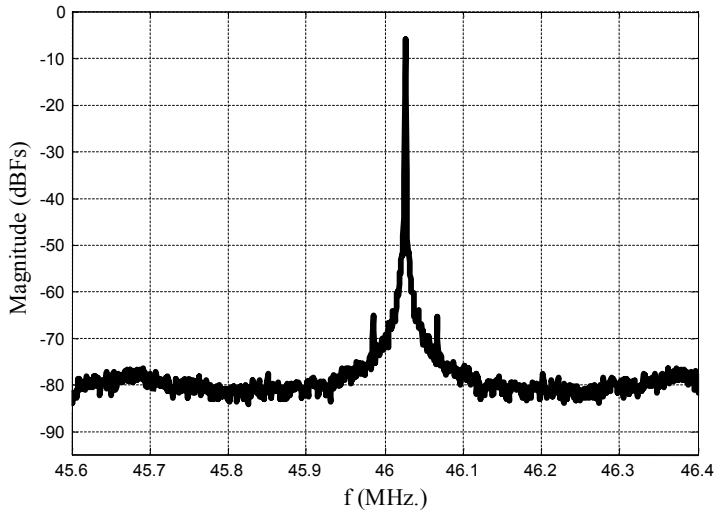

Figure 6.26. FFT plot of a digital capture within the signal band (input at $3f_s/4$) of the bandpass 6th order TL-ΣΔM.

This reduction in the performance of the modulator is due to two factors. First, when the modulator is used as a subsampling ADC and the clock has jitter, there is a reduction in the SNR achievable by the modulator, as we have explained in section 6.2.6.

Second, in the subsampling mode the dynamic range of the state variables is increased, as pointed out in section 6.2.5. Therefore the distortion produced by the transconductor due to the voltage swing also gets larger and may increase the inband noise floor as seen in Fig.6.26.

Clock jitter sensitivity

The sensitivity to clock jitter was evaluated using the phase noise spectral densities at 25kHz from the carrier of the clock input sine wave and the input signal compared to the noise floor in the digital capture of the modulator. Figure 6.27 shows the measured spectra of the clock signal superimposed to the input tone, using a resolution bandwidth approximately equivalent to the FFT bin spacing in Fig.6.25.

We will use Fig.6.27 to estimate the phase noise spectral densities of the clock and the input, assuming signal generators with negligible AM noise. In the data capture of Fig.6.25, a signal generator with a phase noise spectral density of -90dBc/Hz (upper trace in Fig.6.27) was used to drive the clock signal, whereas a generator with -110dBc/Hz (lower trace in Fig.6.27) was used as input signal, to be well below the phase noise of the clock. If we would sample an ideal tone located at ft=f_s/4 with a clock with -90dBc/Hz phase noise, the sampled tone would have a noise density of:

$$-90dBc/Hz + 10\log(ft/fs) = -96dBc/Hz \tag{6.3}$$

By observing the FFT of Fig.6.25, we may see that each FFT bin represents a bandwidth of 350Hz and hence, the phase noise at 25 kHz from the carrier would be approximately:

$$-71dBc - 10\log(350Hz) = -96dBc/Hz \tag{6.4}$$

Comparing Eq.6.3 and Eq.6.4, we may conclude that the spectral density of the acquired signal is similar to what could be achieved by a sampler at the input of a discrete time modulator.

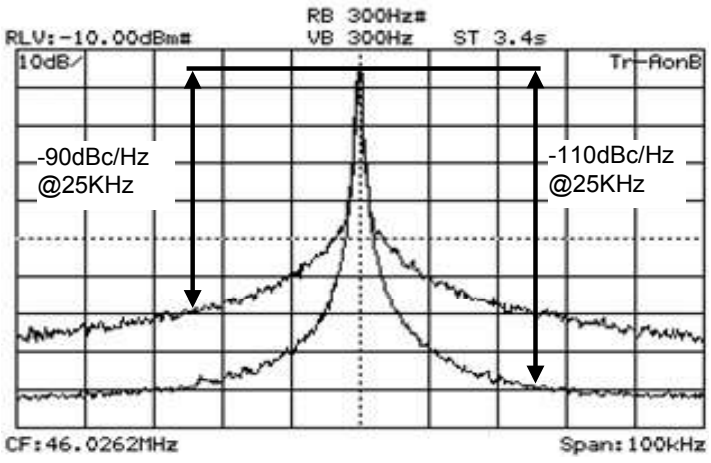

Figure 6.27. Clock and input tone spectra used in the measurements of the bandpass 6th order TL-ΣΔM.

Resonators frequency mismatch

Another effect that was measured was the detuning between the sampling clock and the transmission line resonant frequency. By trimming the external capacitor C_P we can adjust this frequency offset within a certain range. Figure 6.28 shows the effect in the output spectrum of a detuned resonator. An increase of the noise floor at the frequency offset is observed in Figure 6.28, marked with an arrow.

Detuning is more problematic when the frequency offset is within the signal band. For this reason and to tune the mismatches among the transmission lines of the different stages, an on chip capacity tuning circuit should be implemented.

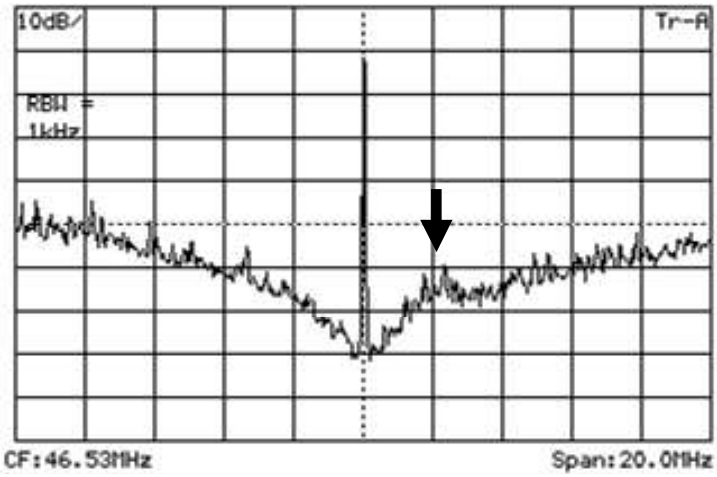

Figure 6.28. Effect of mismatch between the sampling clock and the resonance frequency of the transmission lines.

Distortion

The main problem encountered in this design is distortion, which is responsible of the spurs seen in Fig.6.24, Fig,6.25 and Fig.6.26. This effect is due to the large state variables outside the sampling points, as explained in section 6.2.5. Although in simulations it was shown that this effect would ideally not affect the behavior of the modulator, the output stage of transconductors may not be fast enough to recover from the large peak level of the state variables. This may require some kind of compensation method, such as modulation of the transconductor gain with the clock signal or low pass filtering of the DAC signal to attenuate high-frequency components. However, this would have negative impact in the jitter sensitivity and its subsampling capabilities.

Power measurements and FOM

At 3.3 V supply voltage, the power consumption of the chip was measured as 62.7 mW. Table 6.9 shows the power measurements of the modulator.

	I [mA]	**Pwr [mW]**
Analog core (VDDA)	19	62.7

Table 6.9. Power measurement of the bandpass 6th order TL-ΣΔM.

The measured performance is summarized in the first column of Table 6.10 and compared with the previously published 0.35μm CMOS/BiCMOS single-bit high order (>4) band-pass CT-ΣΔMs and DT-ΣΔMs. A figure of merit (FOM) similar to that proposed in [Sch05] is also used for comparison. The FOM is defined as:

$$FOM = SNDR_{dB} + 10\log\left(\frac{BW}{P}\right) \tag{6.5}$$

where BW is the signal bandwidth and P is the power consumption.

The measured SNDR and FOM using an OSR=256 are comparable with that of band-pass CT-ΣΔMs and DT-ΣΔMs previously published.

	This Work	[Yu07]	[Mau00]	[Tao99]	[Cus01]	[Sal03]
Technology	**0.35um SiGe BiCMOS(3.3V)**	0.35um CMOS(3.3V)	SiGe BiCMOS(3V)	0.35um CMOS(3.3V)	0.35um CMOS(3.3V)	0.35um CMOS(3V)
Type	**TL**	SAW	Gm-C	LC,SC	SC	SC
Modulator order	**6**	4	4	4	6	4
Power	**62mW**	45mW	64mW	330mW	76mW	24mW
f_s	**184MHz**	189.2MHz	800MHz	400MHz	42.8MHz	80MHz
Center Frequency	**46MHz / 138MHz**	47.3MHz	200MHz	100MHz	10.7MHz	20MHz
Bandwidth	**360kHz**	200kHz	200kHz	200kHz	200kHz	270kHz
OSR	**256**	473	2000	1000	107	148.15
Peak SNDR	**58dB / 53dB**	66dB	68dB	45dB	61dB	78dB
FOM	**125.6 / 120.6**	132.48	132.95	102.83	125.2	148.51

Table 6.10. Performance comparison of the bandpass 6th order TL-ΣΔM with previously published designs.

6.5 Conclusions

This chapter discusses the theory behind the design of a band-pass ΣΔM using transmission lines as delay elements. The theory is illustrated with the design and implementation of an experimental modulator using a 3.3V 0.35μm BiCMOS technology.

As we have seen in this chapter, modulators implemented with this architecture have the drawbacks of requiring a special circuit to limit the distortion, the lack of inherent antialiasing filtering in the STF and the mismatch of the resonators. The mismatch would require not only off-chip tuning capacitors but on-chip tuning capacitors as well.

Despite of this, building a bandpass transmission line ΣΔM with this approach benefits from the high Q_0 factor of transmission lines, allows down conversion by subsampling of the input, behaves close to a discrete time modulator at high clock jitter levels and tolerates loop delay. With a careful design, this modulator potentially allows for efficient sampling of narrow-band signals at very high frequencies with simple circuitry that does not require either a mixer or high-precision sampler.

To summarize the results, the ADC operates at a f_s=184 MHz, consumes 62mW and is able to convert narrow-band signals centered both at 46 MHz and 138 MHz respectively, with a maximum SNDR of 58dB assuming an analog bandwidth of ABW=360kHz.

CHAPTER 7

Subsampling Quadrature Receiver using a Transmission Line ΣΔM in 0.35μm BiCMOS

The receiver architecture proposed in this chapter seizes the subsampling properties of continuous time ΣΔ modulators based on distributed resonators presented in this thesis to construct a quadrature receiver.

As we have already explained, such kinds of modulators employ continuous time circuitry, which makes them suitable for high frequency operation. Yet they have some of the advantages of discrete time modulators, such as allowing subsampling of the input signal.

The proposed receiver in this chapter is based on a lowpass ΣΔ modulator, similar to that of chapter 5, that subsamples an IF signal around the sampling frequency. Therefore the modulator may be feasible for the typical IF frequencies used in cellular base stations.

The modulator employs transmission lines and transconductors as main components and does not require any switches. Two circuit architectures are going to be proposed to do the practical implementation. The first one uses separate circuitry for the I and Q paths. The second architecture introduces an innovative way to produce the I and Q outputs that is immune to path mismatch due to the sharing of all the analog circuitry for both paths. We will implement these two modulators in only one integrated circuit. The system level design, the implementation of the proposed architecture in a 3.3V 0.35μm BiCMOS technology and the experimental results will be also presented in this chapter.

7.1 System level design

A simplified block diagram of a subsampling superheterodyne quadrature receiver is shown in Figure 7.1.a. A pre-select filter attenuates the out-of-band signals and performs image rejection of the received signal. A low-noise amplifier (LNA) follows the pre-select filter. After the LNA, the desired RF signal is downconverted to a fixed IF using a single mixer and tunable LO.

An IF filter rejects the unwanted images and selects the desired signal bandwidth. After the IF filter there is an IF amplifier with gain G that performs part of the amplification of the IF stage, another part can be supplied by the signal transfer function of the modulator.

Instead of an image rejection mixer to perform the I and Q decomposition and baseband demodulation, the receiver in Fig.7.1.a demodulates by subsampling. The I and Q decomposition is accomplished by a delay $\Delta T = 1/4f_s$ in the sampling instants between the I and Q paths. This corresponds to a frequency dependent phase difference instead of the desired constant phase shift of $\pi/2$.

Then, the dedicated image rejection mixer is traded off by two samplers at the cost of limiting the image rejection to a narrow bandwidth [Val04]. Such architecture would map into the baseband a desired alias of any signal located around the sampling clock frequency. Therefore, the sampling clock frequency is chosen equal to the IF value ($f_s=f_{IF}$). Afterwards, the signal is digitized by two discrete time (DT) interpolative lowpass ΣΔMs.

Finally, part of the automatic gain control (AGC) of the receiver can be accomplished by digitally trimming the reference of the feedback DACs [Sch02].

Considering that, typical IF values for base station receivers are situated around a few hundreds of MHz, a practical implementation of this receiver, with switched capacitor circuits, would be difficult to achieve. Furthermore, it would not be competitive in terms of power consumption against a classical receiver with an analog image rejection mixer.

Also, the required gain for the IF and the rejection of out of band signals would rely on the ΣΔM loop, which would be limited by its operational amplifiers, yielding a very poor rejection to blocking interferers.

7.1.1 Loop Filter Design (Quadrature Lowpass)

To overcome these problems, we introduce the architecture of Fig.7.1.b where a CT-ΣΔM based on TLs is used. One of the properties of TL- ΣΔMs is the ability to convert signals located at any multiple of the sampling frequency f_s, due to the periodic frequency response of their loop filter [Her06], [Kap05]. This property permits to directly demodulate to baseband a bandpass modulated signal *x(t)* located around the clock frequency by subsampling with a low-pass ΣΔM.

Note that the quadrature modulator of Fig.7.1.b does not require the high precision sample-and-hold circuits of Fig.7.1.a. Now, the samplers are replaced by clocked comparators, seizing the error shaping properties of the loop, just as in a conventional CT-ΣΔM. With regard to the linearity and noise requirements of the remaining building blocks, the requirements are expected to be very similar to the conventional structures.

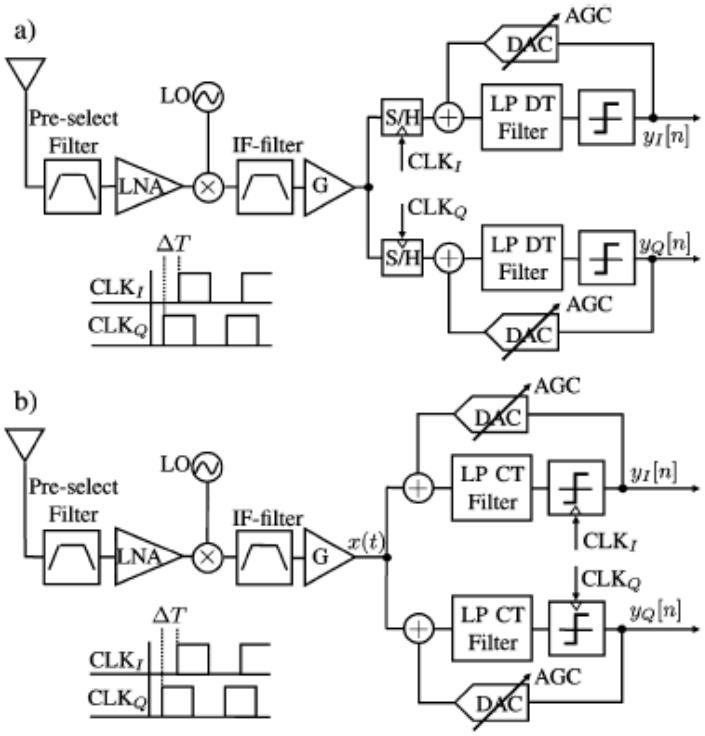

Figure 7.1. Superheterodyne quadrature receiver (a) using a DT quadrature ΣΔM, and (b) using a CT quadrature TL-ΣΔM. [Ree07]

Moreover, TLs permit to implement resonators close to the gigahertz range with low power and reduced complexity. In this case, the resonator frequency can be close to the GHz range and would only be limited by the speed of the active elements in the loop.

Figure 7.2 represents the block diagram of a possible quadrature ΣΔM based on TLs, which can be used in the receiver of Fig.7.1.b. This structure is the complex equivalent of the lowpass TL modulator of chapter 5.

It is clear that the structure does not require a quadrature mixer. A circuit implementation would require six transconductors, four open circuit TLs, two single bit sampled quantizers and two current feedback DACs. For robust circuit design, we select a nonreturn-to-zero (NRZ) zeroth-order-hold DAC pulse.

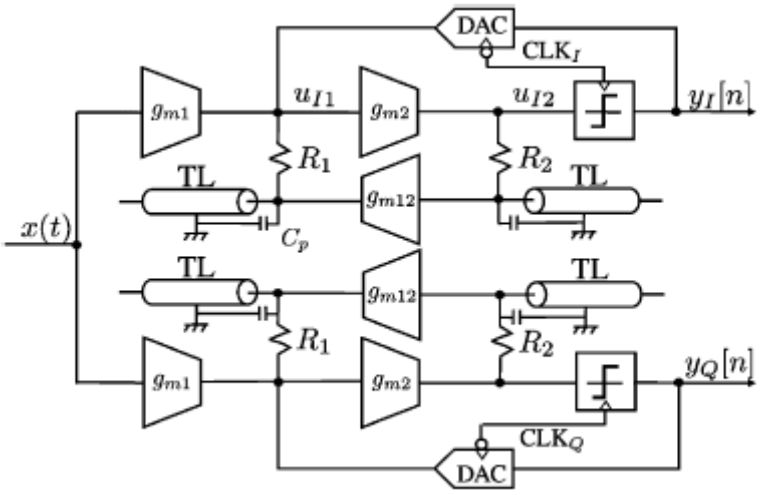

Figure 7.2. Block diagram of the quadrature modulator with TLs. [Ree07]

In the quadrature modulator of Fig.7.2, all the TLs are identical, have a characteristic impedance Z_0, an electrical delay of $T/2$, corresponding to half the sampling period and a loss parameter $A \leq 1$. The TLs are used as part of the load of a transconductor g_m. For instance, in Fig.7.2, if we neglect the parallel capacitors C_P for the moment, we could define the following transfer function:

$$\frac{U_{I2}(s)}{U_{I1}(s)} = g_{m2}\left(Z_0 \frac{1+Ae^{-sT}}{1-Ae^{-sT}} + R_2\right) \tag{7.1}$$

In this case, the frequency dependency of the loop transfer function only depends on delays (terms in e^{-sT}). Thus, we may apply the system equivalence of chapter 2 with a DT-ΣΔM: i.e., we may replace e^{-sT} by z^{-1} and compute the corresponding noise transfer function (NTF) and signal transfer function (STF) of both branches of the modulator as if it was a DT system. By doing so, the proposed circuit has an NTF that can be mapped to the following transfer function of a second-order lowpass DT-ΣΔM, assuming A = 1:

$$NTF(z) = (e^{j\phi} - z^{-1}) \cdot (e^{-j\phi} - z^{-1}) = z^{-2} + 2\cos(\phi)z^{-1} + 1 \tag{7.2}$$

The transfer function NTF(z) is the same for both branches: NTF(z) = $NTF_I(z)$ = $NTF_Q(z)$.

The phase ϕ defines the location of two complex conjugated zeros. These zeros will determine the bandwidth of interest of the modulator and will be selected according to the desired oversampling ratio (OSR).

Furthermore, the NTF with real coefficients of Eq.7.2 is preferred instead of one with complex coefficients to avoid cross-couplings between the I- and Q-path. These cross-couplings would require extra sample-and-hold circuits if the quadrature modulator is implemented with TLs. Mapping the NTF obtained with the circuit of Fig.7.2 and Eq.7.1 with Eq.7.2, results in the following design equations for a single-bit modulator:

$$\begin{aligned} R_1 &= Z_0 \\ R_2 &= Z_0 \frac{2\cos(\phi)+1}{2\cos(\phi)-1} \approx 3Z_0 \text{ if } \phi \approx 0 \\ g_{m12} &= -\frac{1-\cos(\phi)}{Z_0^2 g_{m2}(1+\cos(\phi))} \end{aligned} \tag{7.3}$$

The transconductors g_{m1}, g_{m2}, and the DAC current occur as scale factors in the expression for the loop gain. Due to the presence of the quantizer in the loop, their value is irrelevant. In practice, they may be used to scale the state variables and the STF gain, as we have discussed in the implementation of the circuits of chapters 5 and 6. If necessary, a voltage clamp could be used to ensure that the state variables are bounded [Kap05].

Note that the design parameters in Eq.7.3 are independent of the sampling period, due to the properties of the TL modulators. Only the length of the TLs is determined by the clock frequency. To implement the NTF expressed in Eq.7.2, the CT-ΣΔM requires a loop with a delay of one clock cycle, same as in the lowpass design of chapter 5.

In the schematic of Fig.7.2, the feedback loop contains a quantizer and a DAC triggered in the rising edges and falling edges of the sampling clock, respectively. This results in a delay of 0.5 clock cycles between the data capture in the quantizer and the update of the DAC output. The next sampling operation in the quantizer occurs 0.5 clock cycles after the DAC update, resulting in the required delay of one clock cycle.

Moreover, the quantizer samples in the middle of the zeroth-order-hold feedback DAC pulse. This has the potential to desensitize the modulator against clock jitter in the DAC because the value of the DAC pulse in the sampling instant is what is relevant instead of the pulse area,

as would be the case with conventional CT-ΣΔMs. For the same reason, the loop delay may vary between zero and one clock cycle without any performance degradation.

Application issues

The coexistence of different communication standards in wireless systems demands flexible data converter architectures that allow reconfiguration to exchange bandwidth by resolution. As can be seen from Eq.7.3, the signal bandwidth of the modulator mainly depends on one transconductor, namely g_{m12}. Setting a constant value for R_2 and changing only g_{m12} will produce the desired change of the zeros of the NTF.

To analyze a practical example we will explore the application of this receiver to a WCDMA UMTS signal. The same receiver could be used in a narrow bandwidth GSM application by setting g_{m12} equal to zero.

In Fig. 7.3.a and 7.3.b, the simulated output spectra of the proposed quadrature modulator without nonidealities are plotted for two different OSRs: OSR=128 and OSR=64, respectively. For the plot, a sinusoidal input has been preferred against a WCDMA modulated signal to better show the quantization noise spectra and the image rejection ratio (IRR).

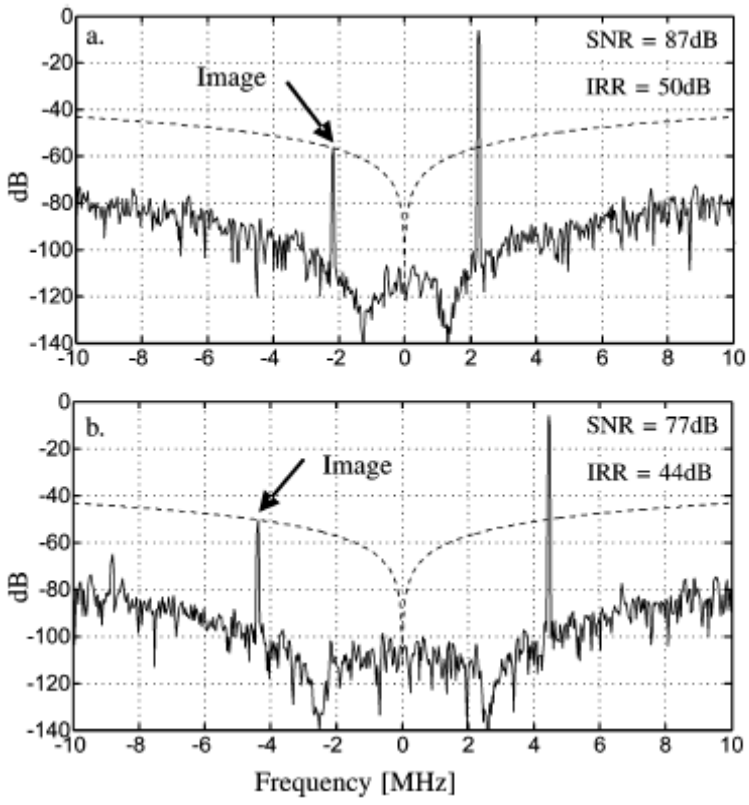

Figure 7.3. Ideal output spectrum of the quadrature modulator. a) OSR = 128. b) OSR = 64. Both modulators have an -6 dBFs input tone at f_s+BW/2. The dashed line shows the frequency dependence of the IRR.[Ree07]

The signal bandwidth (BW) in Fig.7.3.a was set to 3.84 MHz, which is the bandwidth occupied by a WCDMA UMTS channel. For an OSR of 128, the sampling frequency equals 491.52 MHz, which is in the range of feasible sampling frequencies for the given architecture when implemented in a standard RF BiCMOS technology [Her06]. For an -6dBFs input tone $x(t)$ located at f_s+BW/2, the signal-to-noise ratio (SNR) is equal to 87 dB and the IRR is about 50 dB. Note that the IRR in our structure is limited due to the fact that the decomposition is implicitly approximated by delayed sampling. This effect is known [Val04] and the corresponding calculated frequency dependence of the IRR is represented by the dashed line in Fig.7.3, which is consistent with the simulation. Still, this IRR is more than good enough to attenuate the self-image so that the received signal could be demodulated correctly [Fdd05]. Note, the IRR improves for input signals closer to the sampling frequency.

In Fig.7.3.b, a bandwidth of 8.84 MHz is chosen. To achieve a feasible sampling frequency, the OSR is lowered to 64, resulting in a 565.76-MHz clock. In this case, the receiver architecture could be used to digitize two WCDMA UMTS channels with a channel spacing of 5 MHz. One channel is located at positive frequencies and the other at negative frequencies. As a result, the dc component resulting for e.g., clock feedthrough lies in the gap between the two channels. This way, it can be removed digitally without harming any UMTS signal. The required IRR is now higher and equals the adjacent channel rejection ratio (40 dB) as specified in [Fdd05].

Simulations show that in this case the SNR is 77 dB and the IRR is about 44 dB which should be sufficient. However, if a higher IRR is desired, the IRR can be improved by means of a simple digital compensation technique suitable for delayed sampling [Val04].

Feasibility Analysis

In a practical implementation, the loop filter does not have a perfectly periodic frequency response due to finite bandwidth effects. To prove the feasibility of the ΣΔM in the examples of this section, we have used the model of Fig.7.2 to simulate the configuration used for Fig.7.3.a, assuming typical circuit nonidealities.

Figure 7.4 shows the output spectrum of the modulator including finite bandwidth transconductors, parasitic capacitance, loss in the TLs and clock jitter. We have used a first order model for the transconductors with a pole at $3f_s$, as a compromise between feasibility and power consumption, assuming an implementation in a 0.35μm BiCMOS process [Her06].

The TLs have a loss parameter A=0.99 (see Eq.7.1) which will limit the dc loop gain. Furthermore, a clock source with a random period jitter with a constant standard deviation of σ=0.1%T is used. The combination of these nonidealities results in a SNR loss of only 5 dB, while maintaining the IRR performance.

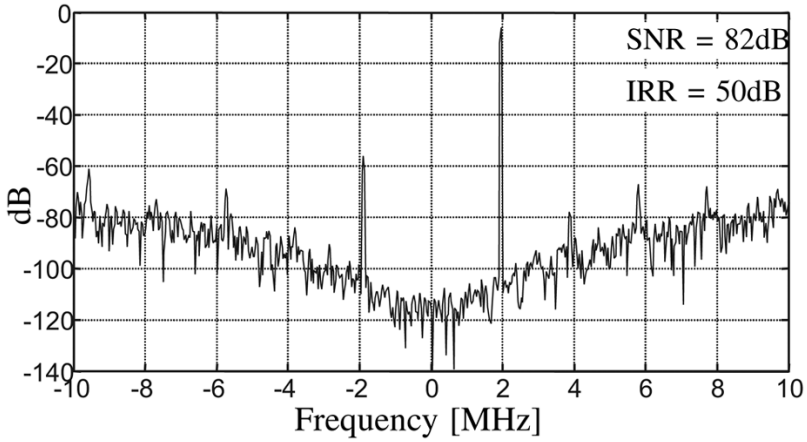

Figure 7.4. Output spectrum of the nonideal quadrature modulator.

Figure 7.5, shows the dependence of the SNR of the modulator against the standard deviation of the clock jitter. The solid line represents the SNR in the case of the presented modulator, assuming A=0.99 and a transconductor with a dominant pole at BW=3f_s. The dashed line has been included as reference and represents the SNR obtained in the case that an ideal delay-based quadrature subsampling circuit would be used for the same input around f_s. The asymptotic behavior of the solid line for high jitter values is close to the ideal dashed line indicating that the performance with a jittered clock in this type of ΣΔM approaches what could be achieved with an ideal switched capacitor implementation.

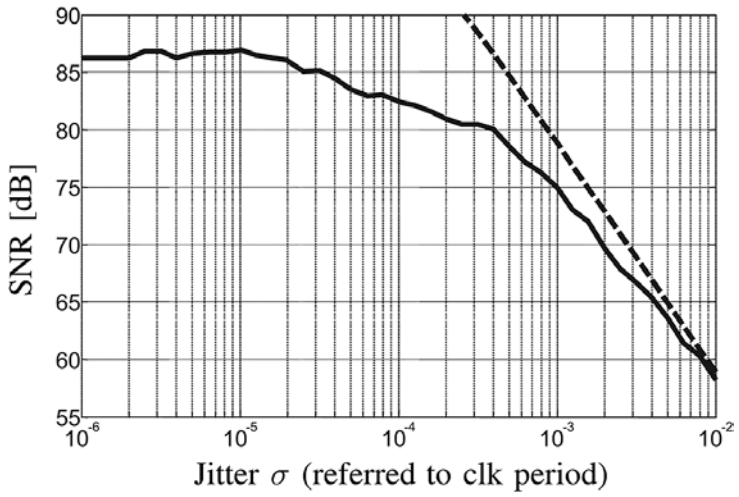

Figure 7.5. Jitter sensitivity comparison between the CT-ΣΔM with TLs (solid line) and an ideal delay based quadrature subsampling circuit without quantizer (dashed line).[Ree07]

Furthermore, due to mismatch between the TL length of the different resonators, the exact location of the NTF zeros will deviate from the desired ones. This has the effect that there could be a mismatch between clock and resonate frequency and also that the resonate frequency of the different resonators are mismatched. This results in a deterioration of the performance. However, this problem can be solved by placing a small parallel trimming capacitor C_P (see Fig.7.2), as it was shown in chapter 4.

Alternative Implementation

The main problem still remaining in the structure of Fig.7.2 is mismatch between the I and Q path, which causes an undesired alias between positive and negative signal bands. For a symmetric NTF, the alias of quantization noise is of no importance, however, the IRR will be degraded. For example, if we perform the simulations of Fig.7.3.a and Fig.7.4 with a path mismatch of 2% between the I and Q branches the SNR remains unaffected but the IRR is degraded to 34 dB. This problem of path mismatch for quadrature modulators is well known and various partial solutions have been proposed [Mau05], [Ree06].

A novel implementation that is insensitive to path mismatch is shown in Figure 7.6. The idea is to share the loop filter and feedback DAC for both the I and Q paths. At the bottom of Fig.7.6, the required clock phases are shown. Here, the arrows on the clock edges indicate a sampling operation. A black arrow means the I-value is updated at the output of the block driven by that clock phase and gray stands for an update of the Q-value. If the time axis is black (gray), the I-value (Q-value) is available at its output.

The quantizer is sampled at both the rising and the falling edge of CLKs. On edge (1) (rising edge), it captures the new I-sample and on edge (6) (falling edge) the Q-sample. The deinterleaving between the I- and Q-paths is done digitally by means of two D flip-flops. At edge (2) the new I-sample is available at the upper output of the modulator and at edge (7) the new Q-sample at the lower output. Note that the upper (lower) flip-flop should update during the time that the I–sample (Q-sample) is available at the output of the quantizer. The exact moment of the update is of minor importance as long as the order is preserved and as long as it is feasible at circuit level.

Before the DAC, a multiplexer interleaves the I and Q paths again, resulting into only one feedback DAC. When CLK_M is high, the I-value is passed through to the DAC and at edge (4) it becomes available at the output of the DAC and remains at least until a new I sample is

taken at edge (5). When CLK_M is low, the Q value is passed through to the DAC and at edge (9) it becomes available at the output of the DAC and remains at least until a new sample is taken at edge (10).

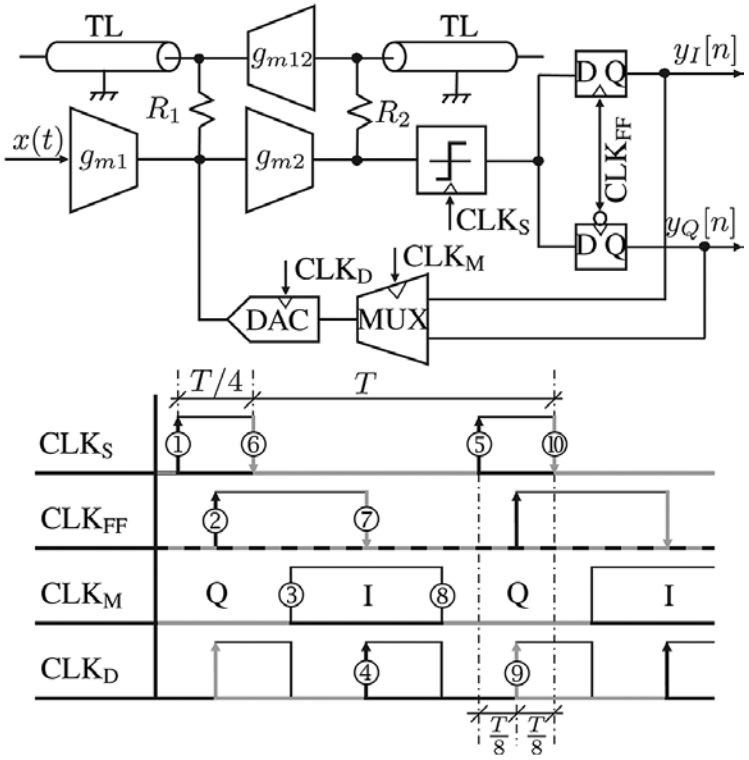

Figure 7.6. One path quadrature modulator with TLs. [Ree07]

To understand the influence of timing errors, let us first assume that all clocks phases with the exception of CLK_D are free of timing error and jitter. By spreading the sampling instants of the quantizer (edge (5) and edge (10)) equally around edge (9), a timing-error of $\pm T/8$ on CLK_D without performance degradation can be afforded in case there are no bandwidth limitations. Since, no other timing schedules result in a higher allowable timing error, the clock signals of Fig.7.6 are optimized such that the modulator has the best jitter performance.

As a result of the finite bandwidth effects, the zeroth-orderhold DAC pulses are smeared in time, resulting in a slightly different DAC gain between the I- and Q-path at the sampling instants due to the asymmetric timing of CLK_S. Additionally, this also results in a kind of inter-symbol interference between the feedback DAC pulses, mostly from the I-path to Q-path. This will degrade the IRR. The effect of the bandwidth on the IRR is quantified in Figure 7.7, where the solid line shows the IRR degradation in the case that the clocks are optimized for the best jitter performance, corresponding to the clocks signals shown in Fig.7.6.

By advancing CLK_D by a time equal to $T/8$, the IRR performance could be optimized in case of finite transconductor bandwidth. In this case, the DAC pulses have more time to settle before the quantizer goes off. The dashed line of Fig.7.7 shows the reduction of the required bandwidth if such a clocking scheme is used. However, this optimization limits the jitter performance. So, for a given clock jitter and transconductor bandwidth, the sampling instants of the quantizer may be adjusted to achieve the best overall performance.

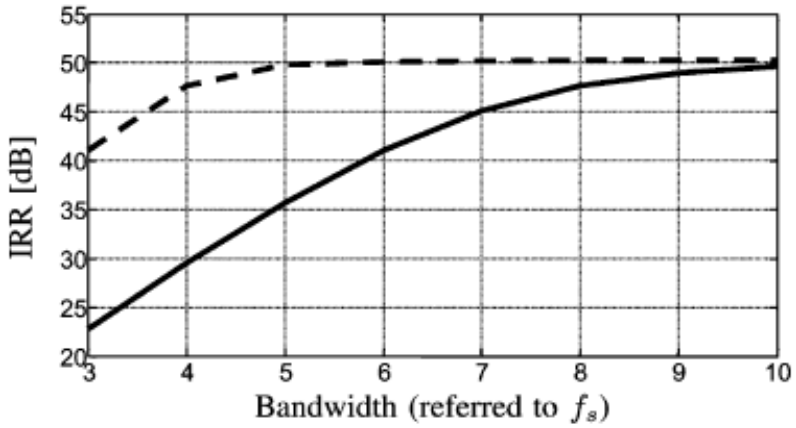

Figure 7.7. IRR versus bandwidth of the transconductors: Solid line: clocks optimized for best jitter performance. Dashed line: clocks optimized for best finite bandwidth performance.[Ree07]

7.1.2 Quadrature Bandpass at $f_s/2$

Another possible mode for the quadrature implementation of this section is to place the first notch of the NTF at $f_s/2$, transforming the modulator from lowpass to bandpass. In this way we could be able to digitize signals above the sampling frequency, for instance at $3f_s/2$. Then, if we target the same specifications as in the lowpass mode, we are able to reduce the sampling frequency as well as the bandwidth requirements of the active elements of the modulator.

To go from the lowpass mode to the bandpass one, some changes should be made. First of all, the NTF needs to be altered from a notch at DC to a notch at $f_s/2$. This can be accomplished by altering in the NTF(z) every z by −z. For the circuit implementation this means that all the transmission line ends should be a short instead of an open line. Furthermore, since the feedback introduces one delay, also the sign of the feedback needs to be altered.

Secondly, the phase shift among the I/Q sampling clocks should now be 180 degrees instead of 90. We know that the attenuation of the image is given by

$$L(f) = \left| \frac{1+\cos(2\pi f \Delta T)}{\sin(2\pi f \Delta T)} \right|^2 \tag{7.5}$$

where ΔT stands for the time delay between the two paths [Val04]. When ΔT is equal to

$$\Delta T = \frac{1}{4 f_s} \tag{7.6}$$

the image rejection is very high around DC. On the other hand when ΔT is equal to

$$\Delta T = \frac{1}{2 f_s} \tag{7.7}$$

the image rejection is very high around fs/2. Which proves why the phase shift among the I/Q sampling clocks should now be 180 degrees instead of 90.

7.1.3 Real Bandpass at $f_s/4$

Finally, a third mode can be implemented in this modulator. In this third mode, the output samples of the I and Q path are no longer interpreted as the I and Q part of a complex signal. The outputs of the I part are the even samples of a real output and the outputs of the Q part are the odd samples.

Since the two quantizers work at alternated clock, a two path transformation (every z is altered into a z^2) occurs and we achieve a real bandpass modulator at $f_s/4$ running at twice the speed.

With the three modes presented in this section we show the possibilities of our architecture to be implemented in a multi-standard digital receiver, where different types of A/D converters are needed.

Next, we will show the nominal simulations along with some circuit impairments.

7.1.4 Design specifications and circuit impairments

Definition and operation modes

On the chip we will make two modulator-loops which means that we can process one input signal in basic mode or two different input signals in multiplexed mode. When the modulator is used in its basic mode, it means that I/Q channels are processed by two separated lowpass modulators. If the modulator is used in its multiplexed mode, then the I/Q channels are processed by the same loop. The analog part of the loop can be reused in both modes. The digital parts will be different for both modes and will be discussed in detailed.

- Nominal sampling frequency: fs = 433 MHz.
- Input bandwidth:

  BW_1 = 3.84 MHz (one UMTS channel), OSR_1 = 112.76.

  BW_2 = 8.84 MHz (two UMTS channels), OSR_2 = 48.98.
- Required resolution: above 10 bits.
- STF gain: about 0 dB.
- Required image rejection ratio:

  BW_1: IRR_1 > 20 dB.

  BW_2: IRR_2 > 40 dB.

The following modes are included in the design:

1. Basic mode, poles at DC.
2. Basic mode, poles optimized for one UMTS channel.
3. Basic mode, poles optimized for two UMTS channels.
4. Multiplexed mode, poles at DC.
5. Multiplexed mode, poles optimized for one UMTS channel.
6. Multiplexed mode, poles optimized for two UMTS channels.

All these modes can be also been implemented using the bandpass configuration. To fix the nominal modes for the quadrature receiver we need design equations Eq.7.3 and Eq.7.4. As mentioned before, the transconductors g_{m1} and g_{m2} and the DAC current will be used to scale the state variables and the STF gain.

gm-cell: finite bandwidth

- Basic Mode:

The influence of finite bandwidth of g_{m2} has the same influence on the performance of the modulator as in the case of the lowpass modulator of chapter 5. The SNR as well as the IRR remains almost the same, as in the ideal case, for a BW larger than two times the sampling frequency.

Furthermore, also the performance of the modulator in combination with the digital compensation algorithm does not change significantly.

- Multiplexed Mode:

The influence of finite bandwidth of g_{m2} has the same influence on the SNR as in the basic mode. However, as shown in Figure 7.7, the IRR degrades strongly if the BW lowers.

gm-cell: finite Q

The transmission lines are used as part of the load of a transconductor. In a practical situation, the transconductor will have finite output impedance. And as we have seen in the practical implementations of the lowpass and bandpass modulators, this finite output impedance can degrade the performance of the modulator. The transfer function TF realized by Figure 7.8 looks like:

$$TF = R_{OUT} // Z_0 \frac{1 + Ae^{-sT}}{1 - Ae^{-sT}} + R \tag{7.8}$$

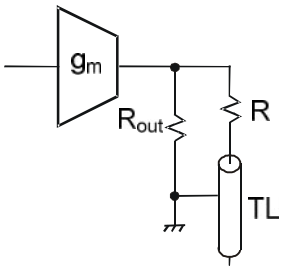

Figure 7.8. Transconductor with output impedance followed by transmission line resonator.

If R = Z_0, then Eq.7.8 can be simplified as follow:

$$TF_1 = \frac{2Z_0}{\left(1 + \frac{2Z_0}{Rout}\right) - Ae^{sT}} \tag{7.9}$$

If R = $3Z_0$, then:

$$TF_2 = \frac{2Z_0\left(2 - Ae^{sT}\right)}{\left(1 + \frac{4Z_0}{Rout}\right) - \left(1 + \frac{2Z_0}{Rout}\right)Ae^{sT}} \tag{7.10}$$

We assume that the position of the poles of TF_1 and TF_2 will have the largest influence on the performance of the modulator and not the gain of TF_1 and TF_2 or the position of the NTF poles. As a result, we can model the finite output impedance with the loss parameter A.

$$A = \frac{R_{OUT}}{R_{OUT} + 2Z_0} \text{ if } R = Z_0 \tag{7.11}$$

$$A = \frac{R_{OUT} + 2Z_0}{R_{OUT} + 4Z_0} \text{ if } R = 3Z_0 \tag{7.12}$$

With the transmission lines we can achieve a maximal Q-factor associated to the first resonance frequency of 5000. This means that:

$$A \approx 1 - \frac{2}{Q} \leq 0.9996 \tag{7.13}$$

since the Q-factor in terms of the loss parameter A is about:

$$Q \approx \frac{2}{1 - A} \tag{7.14}$$

The loss parameter A has an influence on the SNR performance as well as on the jitter performance. Jitter will introduce an upper limit for A, the SNR requirement a lower limit.

Due to the fact that simulation results always show limit cycles if A < 1, the performance of the modulator can be hardly simulated, even with finite bandwidth. Therefore, we decided to perform no time based simulations, but to research the influence of A on the frequency response of the NTF. As a result, the results will be the same for the basic and multiplexed mode.

For zeros at DC, the NTF in function of A = [0.9996 0.99 0.98] looks like Figure 7.9. In Figure 7.10 on the left axis, we see the SNR degradation in function of A. On the right, the necessary R_{OUT} is plotted to achieve this A.

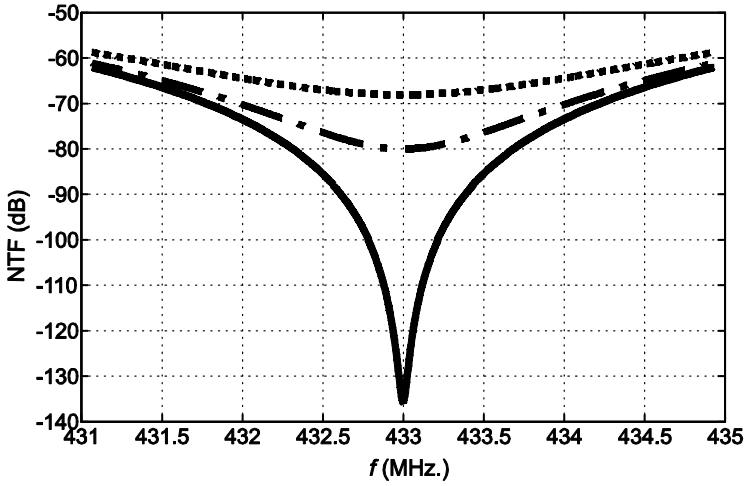

Figure 7.9. Amplitude response of the NTF with the zeros at DC, (__): A = 0.9996, (_._._): A = 0.99 and (……): A=0.98.

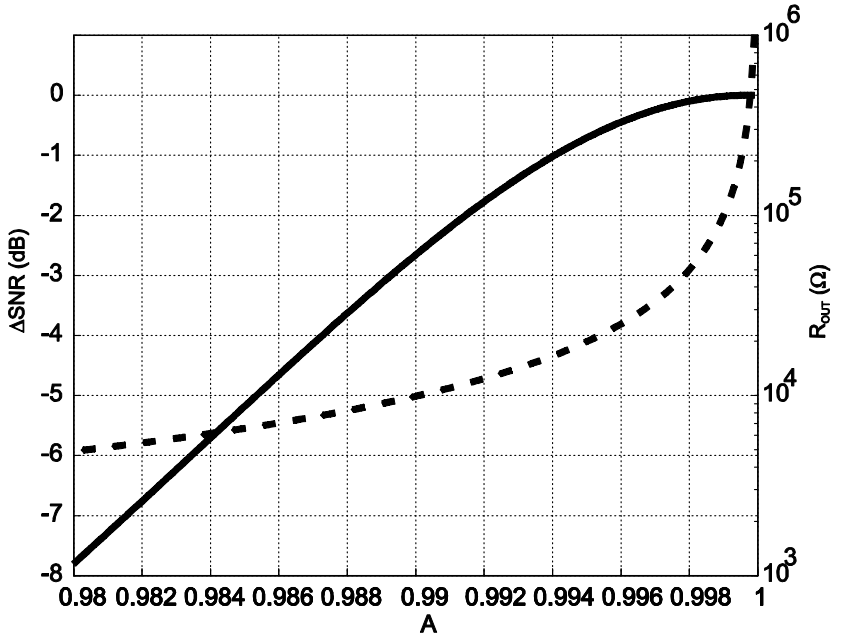

Figure 7.10. (___): ΔSNR and (- - -): ROUT in function of A for the quadrature TL-ΣΔM with the zeros at DC.

Resistor mismatch

As long as this design can suffer from I/Q mismatch, we have simulated the influence of the resistor mismatch in two cases. First in case of homopolaire mismatch (R1 and R2 evolve in the same direction) and secondly when there was a differential mismatch. The simulations show that the influence of resistor mismatch is small for feasible mismatch values. We have used a standard value of the resistor mismatch of 20% taken from the technology. We can draw these conclusions for every mode and pole locations.

Parasitic capacitor after trimming

With a non-zero pad capacitance, the resonant frequency is shifted as shown in Figure 7.11 (dashed line in the ideal case, solid line is with parasitic capacitance). This frequency shift can be compensated by changing the transmission line length with Eq.4.13.

With this compensation the NTF is shown in Figure 7.12 for two cases. The dashed line indicates the NTF in the band of interest with a finite transconductor output resistor of 10k. The solid line shows the NTF for a R_{OUT} = 10k and a pad capacitance C_p of 4pF. We can conclude from Fig.7.12 that the in-band spectrum is higher in the case with C_p than in the case without pad capacitance. Hence, we can also conclude from system level simulations that there is SNR degradation. The SNR degradation also depends on the fact that the STF gain drops for higher C_p. We can compensate this effect with a higher g_{m1} gain.

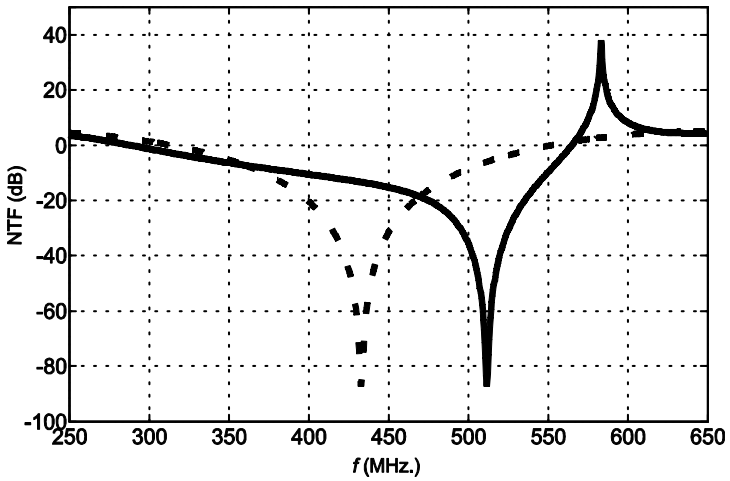

Figure 7.11. NTF of the quadrature TL-ΣΔM in ideal case (- - -) and with parasitic capacitance: (___).

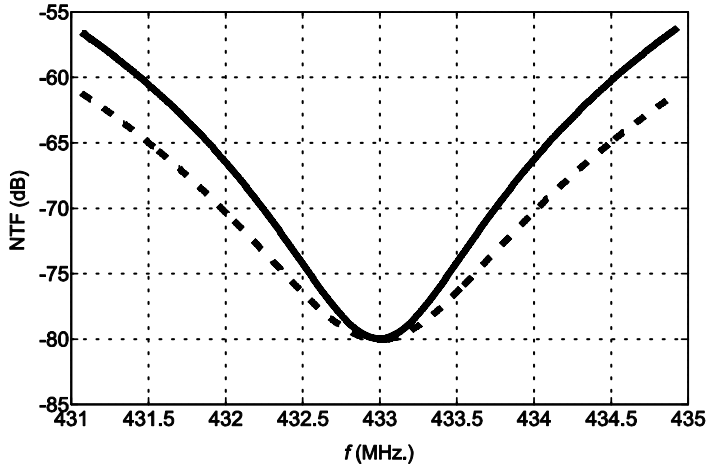

Fig. 7.12. NTF of the quadrature TL-ΣΔM in ideal case (- - -) and with parasitic capacitance (___) using the compensation Eq.7.4.

State Variables

Table 7.1 shows the scaled coefficients of the modulator so that the amplitude of the state variables is limited to 500mV and that the input reference value is 100mV. For A = 0.99 this values results in bounded state variables.

MODE	R_1 [Ω]	R_2 [Ω]	g_{m12} [μA/V]	g_{m1} [mA/V]	g_{m2} [μA/V]	I_{DAC} [μA]
mode 1	50	150	0	1	250	100
mode 2	50	150	105	1	250	100
mode 3	50	150	572	1	250	100
mode 4	50	150	0	1	250	100
mode 5	50	150	105	1	250	100
mode 6	50	150	572	1	250	100

Table 7.1. Scaled coefficients for the quadrature TL-ΣΔM.

In this case the input to the quantizer in the sampling instants is around 2mV when we apply 50mV at the input. As we have shown in this thesis, the amplitude of the state variables

outside the sampling instants is much higher than in the sampling instants. In this case there is a maximum value of 600mV at the input of the quantizer outside the sampling instants when a 50mV input is applied.

7.2 Circuit Design

The system block diagram and parameters defined in the previous section were used as the start point of a circuit design using a 0.35μm SiGe BiCMOS technology with a supply voltage of 3.3V from AMS.

The differential block diagram of the quadrature transmission line ΣΔM chip is shown in Figure 7.13. The analog part is composed of the following elements: a differential first gm cell, a differential second gm cell, a differential feedback gm cell, a differential two level current DAC, a comparator configured as sign detector, an analog test buffer with an input multiplexer that allows to observe different quantizer outputs (the power supply of this circuit will be separated form the rest of the analog circuits to avoid wrong power consumption estimation), a clock generator and a CMFB circuit. The off-chip elements are: transmission lines with characteristic impedance $Z_0 = 50\Omega$ and a trimming capacitors C_P to compensate the transmission line variance.

Design specifications

- Required bandwidth for every transconductor. We have decided that all the transconductor in the loop must have a bandwidth of 1.5 GHz.
- For the first transconductor, a bandwidth of 500 MHz should be sufficient as long as it is matched for the two loops. The first transconductor only introduce a gain loss which can be compensated by a higher gain.
- Minimum output impedance for every transconductor must be R_{OUT} = 10k. In this point we have to be carefully with the specification. We need this minimum output impedance at least at the first and second resonant frequency; this means, that the output impedance of the transconductor must have frequency dependency that feet with this requirement.

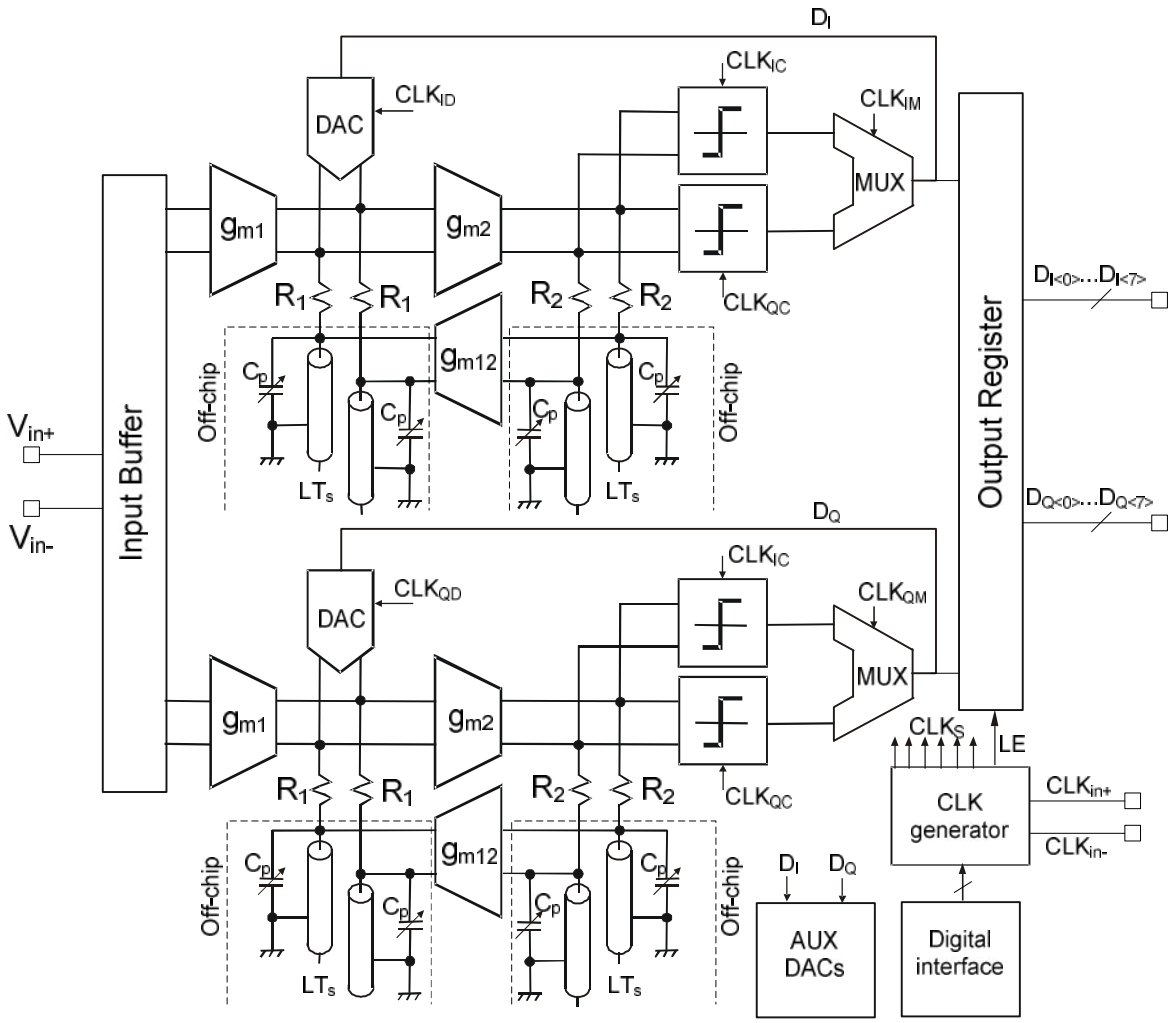

Figure 7.13. Block diagram of the quadrature TL-ΣΔM.

- Estimation trimming capacitor to compensate transmission line mismatch should match with next equation:

$$C_p = \frac{T}{Z_0}\varepsilon = 46.18pF \cdot \varepsilon \tag{7.15}$$

with ε the transmission line mismatch normalized to the nominal transmission line length.

7.2.1 First transconductor (g_{m1})

As we have discussed in the previous section the first transconductor should have a bandwidth of 500MHz and should be at least as linear as the linearity of the overall modulator. Also this transconductor should meet the output impedance requirements discussed in the previous section. Figure 7.14 depicts the simplified schematic of the first transconductor. It is a two stage transconductor.

The first stage it is composed of transistors M1-M6. It is based on source degeneration of the input differential pair transistors (PMOS M3-M4) similar to what was used in [Cha95]. The resistor R is a 1.2kΩ linear resistor which is available in the target process. This value was a compromise between noise and power consumption. Note that this value can introduce a mismatch in the value of g_{m1} compare to the value of Table 7.1. However, the first transconductor is outside the loop and hence this deviation from the theory only results in a gain error of the overall modulator. Transistors M1 and M2 are the current source of the first stage, and transistors M5 and M6 are the active load of the input stage.

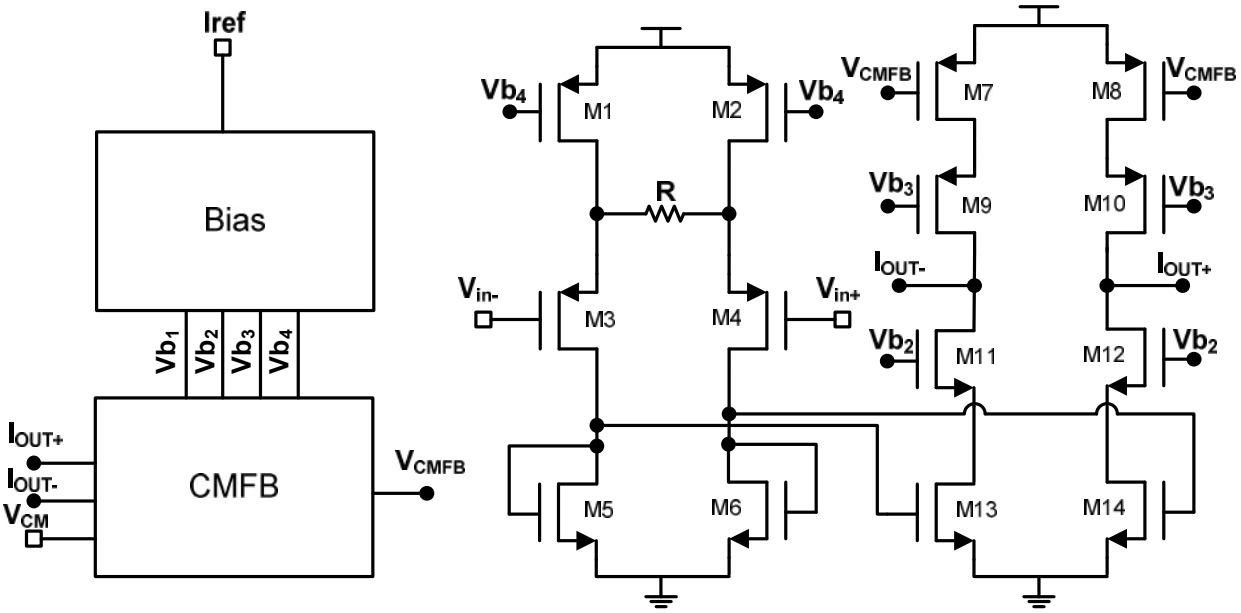

Figure 7.14. First transconductor g_{m1} simplified schematic of the quadrature TL-ΣΔM.

Then, the current across transistors M5-M6 is copied in the second stage using transistors M13 and M14. This second stage is composed of wide swing PMOS and NMOS cascodes (M9-M10 and M11-M12 respectively) and a current source controlled by a CMFB circuit (M7-M8). In this way the output impedance of the first transconductor has been increased to meet the requirements specified in previous section and also the output stage of the transconductor allows more voltage swing than previous solutions implemented in this thesis.

Fig.7.14 also shows the connections with the CMFB and the biasing circuit (Bias). Table 7.2 shows the sizes of the main CMOS transistors of the first transconductor.

CMOS trts.	W/L [μm]
M1,M2	150/0.35
M3,M4	150/0.35
M5,M6	150/0.7
M7,M8	480/0.35
M9,M10,M11,M12	500/0.35
M13,M14	280/0.7

Table 7.2. CMOS transistors of transconductor g_{m1} of the quadrature TL-ΣΔM.

CMFB circuit

Since the circuit is differential, it requires a CMFB circuit to stabilize the output common mode voltage. The proposed continuous-time CMFB circuit [Luh00] is shown in Figure 7.15. It is composed of transistors M3-M9 and current sources M1-M2. Long channel (small aspect ratio) NMOS transistors are used for the input stage (M3-M6) to minimize the differential pair nonlinearity and to accommodate more input voltage swing. They also minimize the common mode error voltage (V_{ERR}) caused by the transistor mismatch among M3-M6. The transistor sizes are listed in Table 7.3.

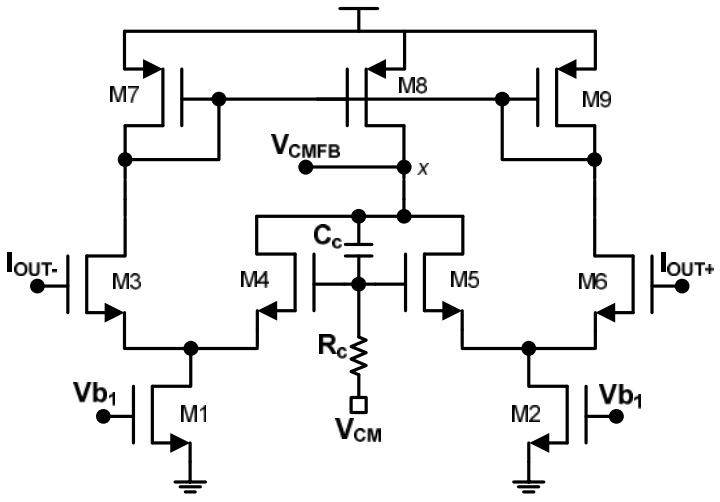

Figure 7.15. Simplified schematic of g_{m1} CMFB circuit of the quadrature TL-ΣΔM.

A high-impedance place, node *x* in Fig.7.15, introduce a low frequency pole and causes a stability problem. Frequency compensation is achieved by adding R_C and C_C. With C_C shunted to the input and output of the CMFB circuit, an extra pole and zero are introduced to attenuate the high frequency gain of this stage. Therefore, the proposed CMFB circuit has a large low-frequency gain to minimize V_{ERR} and a moderate high-frequency gain to keep the system stable.

CMOS trts.	W/L [μm]
M1,M2	40/1
M3,M4,M5,M6	5/1
M7,M9	20/0.35
M8	40/0.35

Table 7.3. CMOS transistors of the g_{m1} CMFB circuit of the quadrature TL-ΣΔM.

7.2.2 Second transconductor (g_{m2})

As we have discussed in the previous section the second transconductor should have a bandwidth of 1.5GHz and moderated non-linear distortion produced by this transconductor can be tolerated due to the fact that it is inside the loop. Figure 7.16 depicts the simplified schematic of the second transconductor. It is a two stage transconductor similar to the first transconductor.

The first stage it is composed of CMOS transistors M1-M4 and bipolar transistors B5-B6. It is based on source degeneration of the input differential pair transistors (PMOS M3-M4) similar to what was used in g_{m1}. The resistor R is a 1.8kΩ linear resistor which is available in the target process. Note that this value can introduce a mismatch in the value of g_{m2} compare to the value of Table 7.1. However, the second transconductor can be used also to scale the modulator, as explained in previous section, and hence deviation from its nominal value can be tolerated and only results in a gain error of the overall modulator. Transistors M1 and M2 are the current source of the first stage, and transistors B5 and B6 are the active load of the input stage.

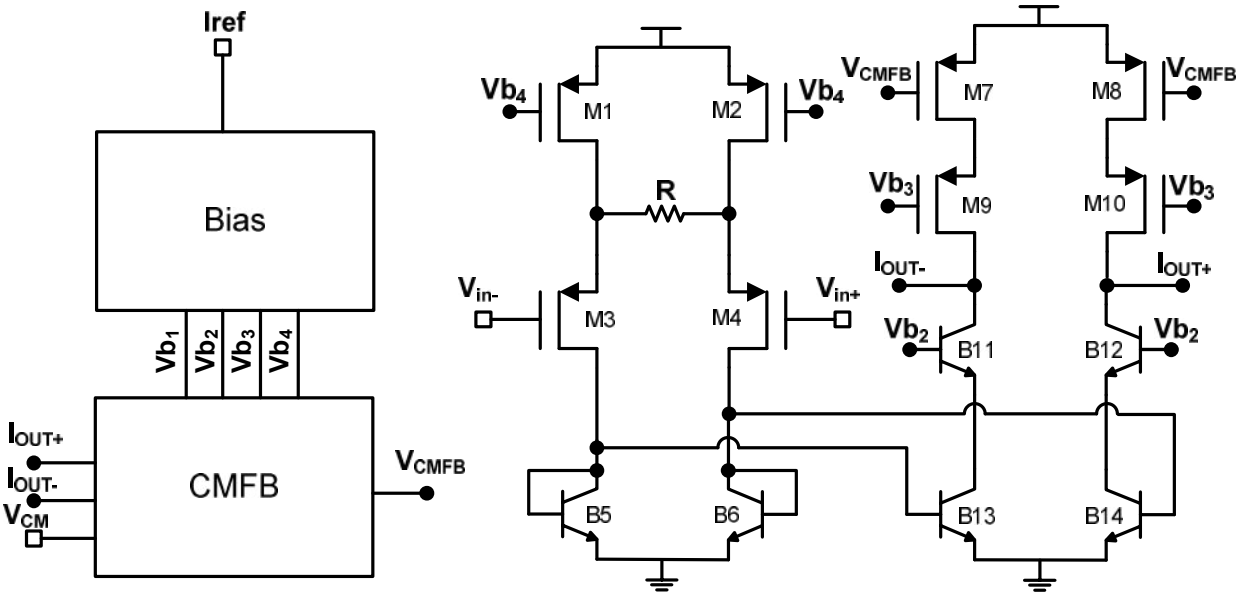

Figure 7.16. Simplified schematic of the second transconductor g_{m2} of the quadrature TL-ΣΔM.

Then, the current across transistors B5-B6 is copied in the second stage using bipolar transistors B13 and B14. In this way we can increase the bandwidth of the transconductor without expending more power than in g_{m1}. To implement the cascode stage associated to B13 and B14 we need to use bipolar transistors B11-B12. This bipolar cascode stage is faster than a pure NMOS cascode stage (as the one used in g_{m1}), but it limits the linearity of the transconductor. However, as the second transconductor in inside the loop, we prefer a faster output cascode stage rather than a more linear output cascode stage. In top of these bipolar transistors we have implemented a PMOS cascode stage (M9-M10) and a current source (M7-M8) that is controlled by the CMFB circuit.

Fig.7.16 also shows the connections with the CMFB circuit and the biasing circuit (Bias). Table 7.4 shows the sizes of the main transistors of the second transconductor.

CMOS trts.	W/L [μm]
M1,M2	150/0.35
M3,M4	150/0.35
B5,B6	Ratio=4
M7,M8	384/0.35
M9,M10	500/0.35
B11,B12	Ratio=12
B13,B14	Ratio=8

Table 7.4. Transistors of transconductor g_{m2} of the quadrature TL-ΣΔM.

CMFB circuit

For the second transconductor CMFB circuit we have implemented the same schematic as in the first transconductor (see Fig.7.15). After Spectre simulations we concluded that the CMFB circuit designed for g_{m1} was good enough to meet the requirements of the CMFB circuit of g_{m2}. Therefore no modifications were made in this circuit.

7.2.3 Single bit Quantizer

The 1-bit quantizer of the modulator is implemented as shown in Figure 7.17. It consists of a simple pre-amplifier to avoid kickback and a two stage regenerative latch similar to what was implemented in the quantizer of the bandpass modulator of this thesis (see chapter 6, section 6.3.3). The pre-amplifier was implemented using the same schematic as in the bandpass implementation of chapter 6 (see Fig.6.16) but changing its bandwidth. We increase the bandwidth of the pre-amplifier due to the specifications of the design. The Latch was also

implemented using the same schematic as in the bandpass design (see Fig.6.17). It consists in a two-stage regenerative latch similar to the one presented in [Gee99].

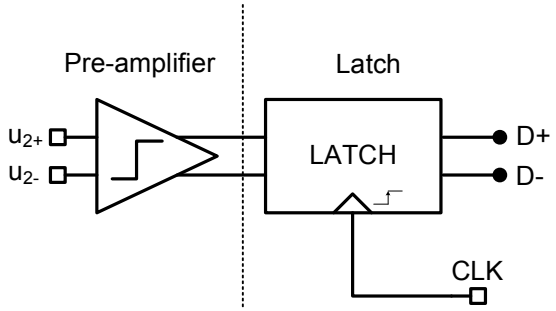

Figure 7.17. 1-bit quantizer simplified schematic of the quadrature TL-ΣΔM.

7.2.4 DACs

Next we will describe the 1-bit DAC implemented for this design. Figure 7.18 shows a simplified schematic of the 1-bit DAC scheme used. It is composed of one synchronization latch (Gigalatch) that drives the switches of a 1-bit NRZ current cell [Van01]. We used the same architecture as in chapter 6 for the bandpass design (see section 6.3.4). Also, the same considerations explained in section 6.3.4 have been taken into account in the design of the NRZ DAC of this design.

The 1-bit NRZ current cell of Fig.7.18 is similar to what was designed in [Van01], but with some changes. In this schematic, transistor M1 is the NMOS current source of the DAC, and transistors M7 and M8 are the PMOS current source of the DAC. In this design we have implemented also wide-swing current mirrors [Joh97] by placing NMOS and PMOS cascodes in each current source (transistor M2 for the NMOS cascode and transistors M5 and M6 for the PMOS cascode). Transistors M3 and M4 are the switches driven by the Gigalatch.

The full-scale current of each DAC is calculated from Table 7.1. In this design this value is composed by the difference between the NMOS and the PMOS current sources.

One restriction in the design of the DAC is its output impedance at nodes x and y of Fig.7.18. The output impedance of the DAC should be large enough to keep the Q factor of the associated resonator in the desire value through the frequency of interest (see section 4.5). This high-frequency output impedance design specification is one of the critical elements in achieving the improved high-frequency Q factor behavior in the resonators. For this reason a NMOS and PMOS wide-swing current mirrors have been designed to implement the NMOS and PMOS current sources of the DAC.

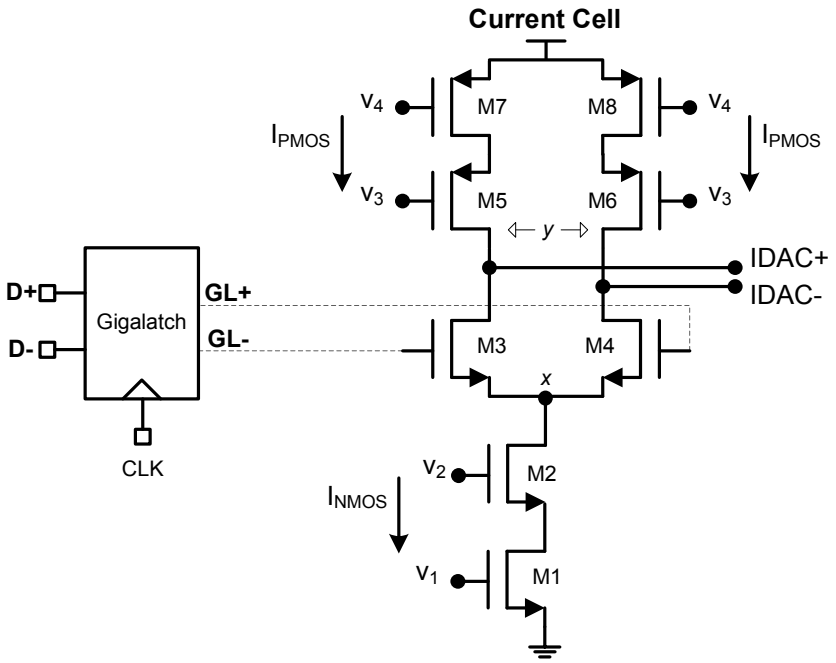

Figure 7.18. NRZ 1-bit DAC simplified schematic of the quadrature TL-ΣΔM.

Table 7.5 shows the sizes of the CMOS transistors and the current sources of the NRZ 1-bit DAC of this design.

DAC	
CMOS trts.	**W/L [μm]**
M1,M2	300/0.7
M3,M4	20/0.35
M5,M6,M7,M8	400/0.7
Current sources	**μA**
I_{NMOS}	100
I_{PMOS}	50

Table 7.5. CMOS transistors and current sources of the NRZ DAC of the quadrature TL-ΣΔM.

7.2.5 Clock generator and Digital interface

The internal clock signal is generated using an input clock buffer same as in the design of the bandpass modulator of chapter 6 (see Fig.6.19 and Fig.6.20). It is composed of a cascade of low noise amplifiers (LNA) and a differential to single-ended circuit that produce a CMOS clock signal from a low level external sinusoidal source. This CMOS signal drives the clock generator of Fig.7.13 which produces the entire necessaries clock signals to drive the two quantizers and DACs in all modes. The rest of the clock signals are also produced by this block.

7.2.6 Output interface

To measure the performance of the chip we have implemented two circuits to capture the output data of the chip.

The first one is the output register of Fig.7.13 that groups 8 consecutive output bits in a single 8-bit word to reduce the clock rate of the output digital pads. We have implemented two different dedicated output registers, each one for the I and Q path respectively. This block has been designed using the same architecture as in section 5.3.5.

The second one is a dedicated single bit DAC (AUXDAC of Fig.7.13) that is used to represent in real time the spectrum of the output data in an analog spectrum analyzer to perform online trimmings. It must be noted that this auxiliary DAC reproduces the same data as the DAC used in the feedback path and will differ from the digital capture. The architecture of this auxiliary DAC is the same as we have used for the feedback path DAC.

7.2.7 Power estimation

Once all the main blocks of the modulator are designed, we can estimate the power consumption of the chip. For this purpose we have run a transient simulation in Spectre, with a full spice transistor-level model of the modulator. For this calculation we have taken into account only the main blocks of one path of the receiver:

- g_{m1}, g_{m2}, 1-bit quantizer, 1-bit DAC.

Table 7.6 shows the rms value of an equivalent current source, connected to the power supply of each block of the modulator.

Block	Irms [mA]	Pwr [mW]
g_{m1}	3.9	12.87
g_{m2}	3.1	10.23
1-bit Quantizer	1	3.3
1-bit DAC	0.3	1
Total	8.3	**27.4**

Table 7.6. Power estimation of the quadrature TL-ΣΔM.

7.2.8 Transistor-level simulation

Finally, we have made a full SPICE transistor-level simulation of the chip in Spectre. We have used a two tone test and mode 1 in lowpass configuration to evaluate the design. For

this simulation we used two input tones around f_s, an OSR=32 and a sampling frequency of f_s=75MHz that leads to a clock input frequency of 300MHz. This value for the input clock was set by simulations of the digital interface after layout. The post-layout simulations showed that the performance of the digital interface had a limit of performance at 300MHz.

In this case, the characteristic impedance of the transmission line was set to 50Ω and the Q_0 factor of the transmission line was simulated by a parallel resistor of 1Ω at the far end of the transmission line to introduce loss in the reflection. Also, circuit simulations have shown that an estimated parasitic capacitor of the output pad is around 1.8pF. This parasitic capacity has been increased intentionally by a trimming capacitor C_p in parallel with the transmission lines to allow trimming of the transmission line mismatches. We have placed a parallel capacitor C_p=2.5pF.

Figure 7.19 shows the FFT of the modulator output computed with a transistor level simulation of 8K points. Simulation of Fig.7.19 shows that the IRR and the IMD are within the simulated performance of section 7.1, but the inband noise is higher than in the nominal simulations of section 7.1. This fact and some other simulations leaded us to the conclusion that trying to optimize the zeros of the NTF was not going to be possible in this design. For this reason we finally decided to remove transconductor g_{m12} from the design, reducing the complexity and the power consumption.

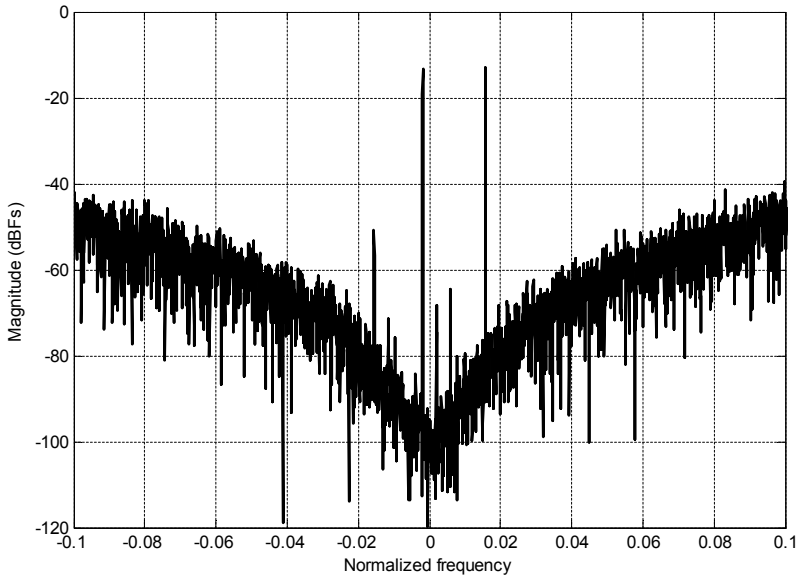

Figure 7.19. FFT (8k points) of a transistor level simulation of the quadrature TL-ΣΔM in mode 1.

7.3 Implementation and measurements

7.3.1 Layout considerations

A photograph of the prototype chip is shown in Figure 7.20. The layout of each block and the final floor planning has been completed taking into consideration the pad routing to minimize the parasitic capacity at the transmission line connections. Also we have taken into account the same precautions as in section 5.4.1. The chip measures 6 mm² due to the pad ring requirements.

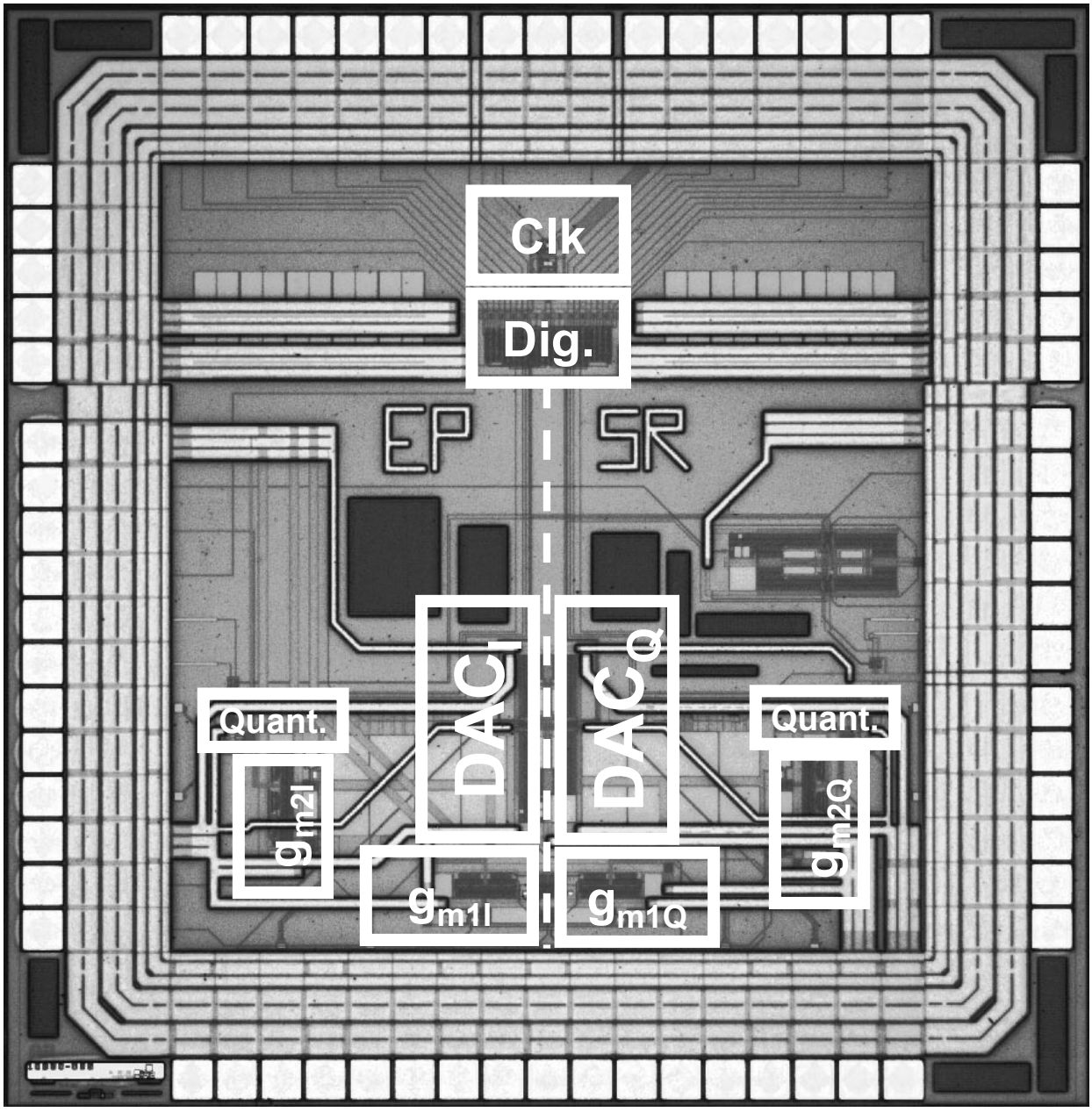

Figure 7.20. Chip microphotograph of the quadrature TL-ΣΔM.

7.3.2 Chip measurements

The test setup consisted of a PCB with current references, single ended to differential transformers to couple the input signal sources (input sine wave and input clock sine wave), an interface to a spectrum analyzer to represent the output of the auxiliary DAC and an interface to a logic analyzer connected to the digital test interface of the chip. We use the same scheme as in chapter 6, Fig.6.23, where we show a simplified schematic of the PCB used to test the chip.

Also, to test the chip, six 50Ohm off-chip coaxial resonators were used as transmission lines. Detuning of the resonators was compensated using external trimming capacitors, as explained in previous sections.

In order to capture the data and make all the measurements that we will propose in this section, we have used the same test bench as in section 5.4.2 that is represented in Fig.5.22.

Nominal measurements

First, we measured the resonance frequencies of the coaxial resonators. We founded out that the two first resonance frequencies were around DC and 50MHz for the lowpass configuration (open transmission line) and 25MHz and 75MHz for the bandpass configuration (shorted transmission line). Therefore to validate the design, we decided to use the bandpass configuration because then we could apply a higher IF signal (i.e. @75MHz) than in the lowpass configuration (i.e. @50MHz). In addition, we used the multiplexed mode to test the one path architecture to validate this new idea. In order to use the one-path bandpass configuration the sampling frequency had to be at f_s=50MHz, leading to a clock frequency of 100MHz. In this way the NTF had the first two notch at $f_s/2$ and $3f_s/2$ respectively.

As a summary of the mode used to test the chip we show the next values:

- Clock frequency: 100MHz.
- Vdd: 3.3V.
- f_s = 50MHz.
- Mode 4 = One-path Band-Pass @ $f_s/2$.
- Signal BW = 1MHz (OSR=50).

The first measurement that we realized was to trim the modulator to obtain the desire NTF. For this purpose we used an input tone of -9dBFs at 24.9MHz. Figure 7.21 shows a spectrum analyzer capture taken at the AUXDAC output, showing the expected shape for the modulator output.

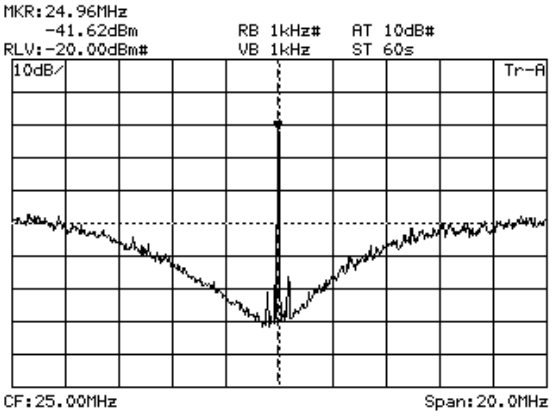

Figure 7.21. Output spectrum of the quadrature TL-ΣΔM (mode 4, bandpass configuration).

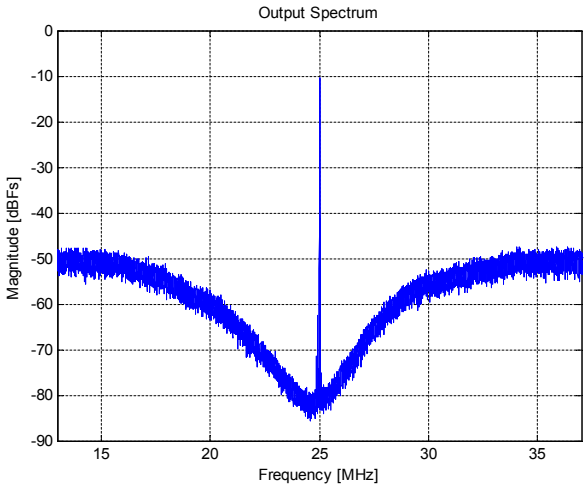

Figure 7.22. FFT (8k points) of the quadrature TL-ΣΔM (mode 4, bandpass configuration).

Figure 7.22 shows an 8K point FFT taken from the digital interface of the same data as in Fig.7.21. Figure 7.23 shows the dynamic range (SNR (solid line) and SNDR (dashed line)) of the modulator. From this plot we can estimate a dynamic range of 10 bits with a signal BW=1MHz, using an OSR=50.

Figure 7.24 shows the inband spectrum of the same data as in Fig.7.22. In this measurement we observe that the third harmonic HD3 is in the same range as the image, and that the clock feedthrough is 10 dB below. Also, we observe that the inband noise is higher that in the transistor level simulation of section 7.2.8. This effect is mainly due to two facts: this is a bandpass configuration and the Q factor of the resonators is lower than expected.

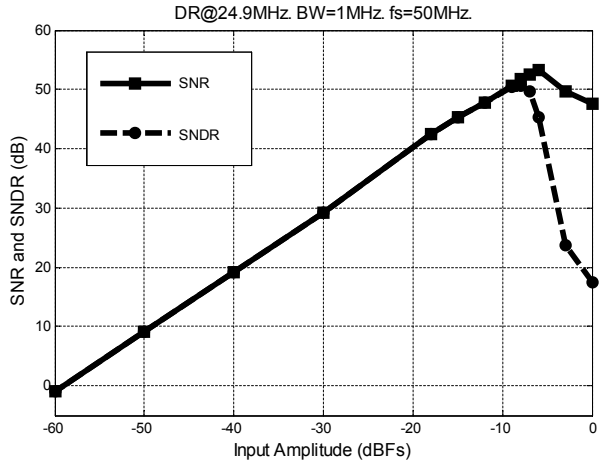

Figure 7.23. Dynamic range of the quadrature TL-ΣΔM (mode 4, bandpass configuration).

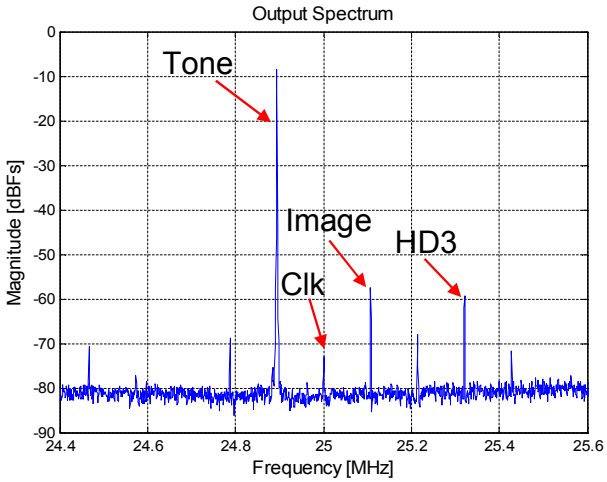

Figure 7.24. Inband spectrum of the quadrature TL-ΣΔM (mode 4, bandpass configuration).

Two tone test and IRR

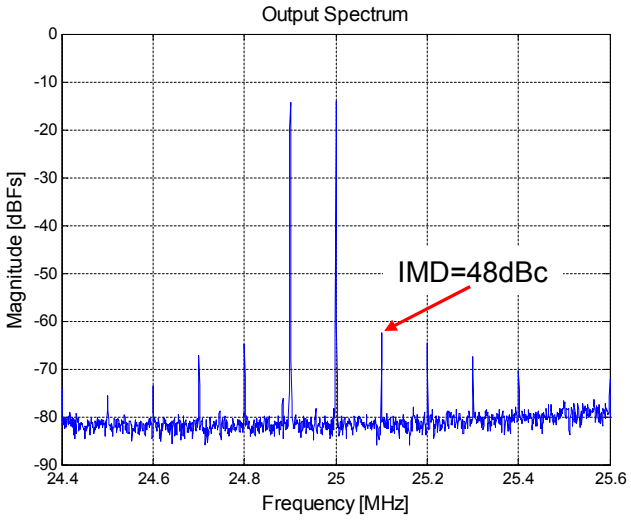

Figure 7.25. Inband spectrum of the quadrature TL-ΣΔM when a two tone test is applied.

To measure the image rejection of the modulator a two tone test has been performance. Figure 7.25 shows an inband spectrum of the modulator, where we observe that the IMD=48dBc when a two tones are applied to the modulator.

If we calculate the IRR as a function of the frequency input tone, we obtain the measurement of Figure 7.26 (solid line). In Fig.7.26 we also represented the ideal performance (dashed line) [Val01]. As we can see the IRR of our modulator is close to the ideal IRR performance.

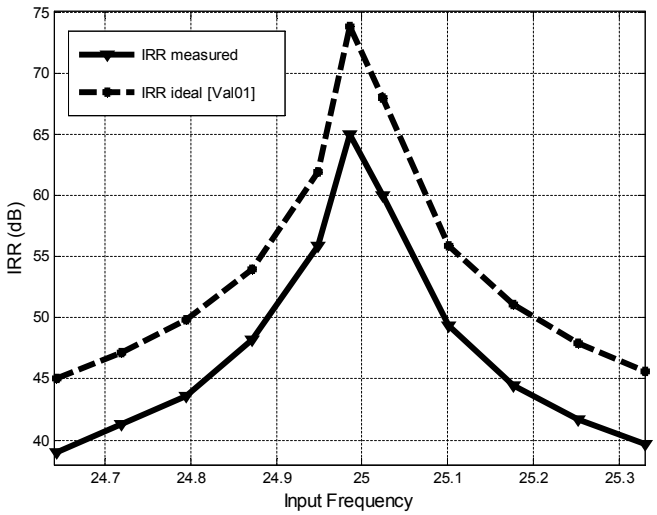

Figure 7.26. IRR of the quadrature TL-ΣΔM (___) compared with the ideal case from [Val01] (----).

Sub-sampling mode

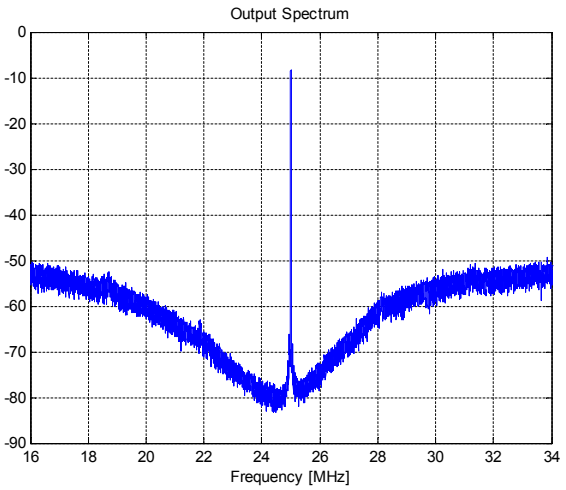

Figure 7.27. FFT of the subsampling quadrature TL-ΣΔM (mode 4, bandpass configuration).

The second measurement that we realized was to prove its capability to subsample. For this purpose we used an input tone of -9dBFs at 75.096MHz. Figure 7.27 shows an 8K point FFT taken from the digital interface.

Figure 7.28 shows the dynamic range (SNR (solid line) and SNDR (dashed line)) of the modulator in the subsampling mode. From this plot we can estimate a dynamic range of 9.5 bits with an ABW=1MHz, using an OSR=50.

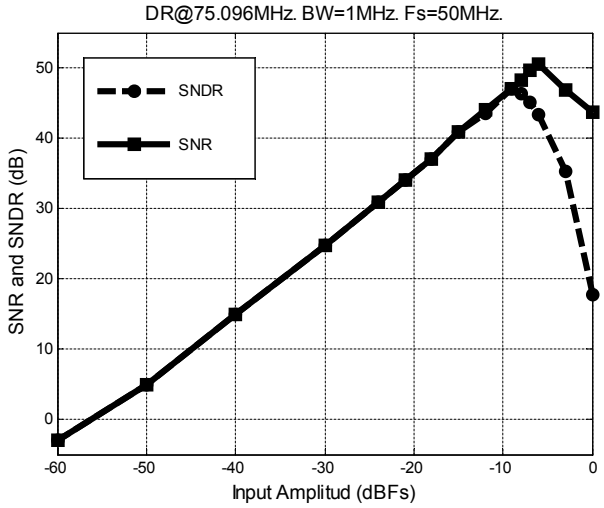

Figure 7.28. Dynamic range of the subsampling quadrature TL-ΣΔM (mode 4, bandpass configuration).

Figure 7.29 shows the inband spectrum of the same data as in Fig.7.27. In this measurement we observe that the third harmonic HD3 is in the same range as the image, and that the clock feedthrough is 10 dB below.

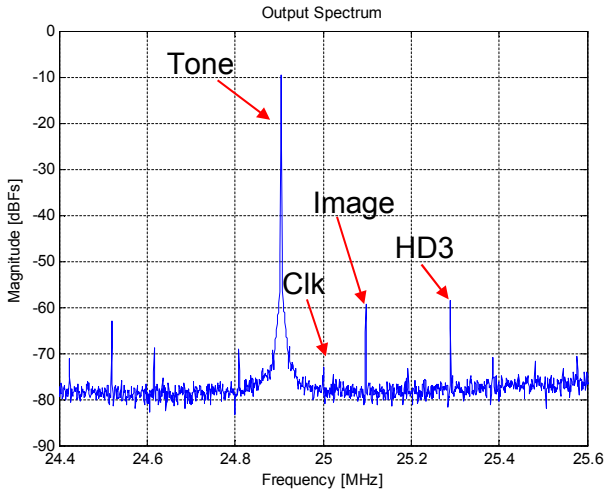

Figure 7.29. Inband spectrum of the subsampling quadrature TL-ΣΔM (mode 4, bandpass configuration).

Summarize results

At 3.3 Volt supply voltage, the power consumption of the chip was measured as 28.05 mW, including: g_{m1}, g_{m2}, DAC and the multiplexed quantizer. Table 7.7 shows a summary of the performance of the quadrature transmission line ΣΔM.

Type	TL-CT
Order	2
# Bits	1
Bandwidth (MHz)	1
f_s (MHz)	50
f_{IF} (MHz)	25/75
DR (dB)	60
IRR (dB)	>40
IMD (dBc)	48
Power (mW)	28.05
Supply (V)	3.3
Technology	0.35 μm BiCMOS

Table 7.7. Performance of the subsampling quadrature bandpass TL-ΣΔM.

If we compare these experimental results with the state-of-the-art reported in chapter 1 (see Table 1.1 and 1.2) we can conclude that, the main advantage of the subsampling bandpass transmission line ΣΔM is the possibility of digitize an IF signal at 75MHz. This value is higher than any of the IF values of the ΣΔMs reported in Table 1.1 and 1.2. Also, the one path structure that we have tested in this chapter shows an IRR performance close to the theoretical value while the modulator is free from I/Q mismatches. Another advantage of this approach is the simplicity of the circuits of the modulator compared with other solutions presented in the literature.

However, this modulator still suffers from the parasitics at the pad connections between the transmission lines and the chip. These parasitics degrade the overall performance of the modulator reducing its resolution.

7.4 Conclusions

In this chapter, a new subsampling quadrature ΣΔ modulator and its use in a radio receiver has been proposed. The presented receiver does not require quadrature mixers nor high precision sample-and-holds at the input. Furthermore, it has been shown that such a receiver has the potential to be immune against circuit imperfections like clock jitter in the DAC and loop delay. A first architecture is based on a low-pass ΣΔ modulator with separate I and Q paths that subsamples a modulated carrier located around the sampling frequency.

Also in this chapter we show simulations that include circuit non-idealities and prove the feasibility of the modulator even for the high IF values used in base station UMTS receivers.

A second architecture turns out to be insensitive to analog path mismatch due to the sharing of the loop filter for both the I and Q paths. In this case, the bandwidth requirements are more stringent than in the two paths topology but the design is free of I /Q path mismatch.

The theory is illustrated with the design and implementation of an experimental modulator in a 3.3V 0.35μm BiCMOS technology. To summarize the results, the ADC operates at a f_s=50 MHz, consumes 28mW and is able to convert I/Q narrow-band complex signals using only one path, centered both at 25 MHz and 75 MHz respectively. The dynamic range of the modulator is 10 bits with an analog bandwidth of ABW=1MHz. Also a two tone test is realized as long with an IRR test, showing an IMD close to 50 dBc, and an IRR behavior close to the theoretical one. The main advantage of this modulator compared with state-of-the-art quadrature CT-ΣΔMs is the possibility of digitize an IF signal at 75MHz using a one-path structure that is free from I/Q mismatches.

CHAPTER 8
Conclusions and future work

8.1 Conclusions

This work introduces a new sigma-delta architecture that uses a non conventional loop filter based on transmission lines. As such, the topic is innovative, promising and the mathematical modeling of the problem has led to surprising results. The experimental work carried out has proven the possibilities of these modulators, which expand what can be achieved by either CT and DT designs. As the main advantages of using a transmission line ΣΔM instead of a conventional CT-ΣΔM we may highlight the following:

- *Loop delay tolerance.*
- *NRZ DAC pulse distortion.* Using a continuous time delay based loop filter alleviates the problems caused by time-varying changes in the area of the feedback DAC pulses.
- *Clock jitter insensitivity in the DAC.*
- *Design parameters independence.* Due to the properties of transmission line modulators, the design parameters are independent of the sampling clock, only the length of the transmission lines determines the clock frequency and signal band location.
- *High Q factor of transmission lines.*
- *Subsampling of the input.*

On the other hand, a ΣΔM implemented with transmission lines has several circuit limitations that influence the design and performance of the modulator. These limitations are:

- *Effect of clock jitter in the quantizer.*
- *Mismatch among the resonators of the loop filter.*
- *Parasitic capacitance and inductance on the resonator connections.*
- *Finite Q factor of resonators and transconductor load.*

- *Non-linear distortion due to:*
    - *Dynamic range of the State Variables.*
    - *Transconductor saturation.*

The main restriction that limits the modulators designed in the thesis is the need of off-chip passive elements. The author believes that this is not a limitation of the application of this architecture and only reveals the need of more research in the technology oriented aspects, to accomplish a fully integrated solution. The achievement of such integrated solution could represent a breakthrough in communications receiver technology, as the results of the thesis predict.

The main contributions of the thesis are:

1. The mathematical modeling of delay based CT-ΣΔMs. Such modeling has never been attempted in the time domain. Only partial results presented under the focus of RF field and based on frequency domain approximations have been disclosed previously [Kap05].
2. The modeling of the practical problems inherent to a microelectronics implementation of the modulators. These problems include the modeling of parasitic and mismatch effects, a complete analysis of clock jitter, finite bandwidth effects and subsampling properties. The experimental work has been the driving force to point out the relevant issues which is missing in previously reported works [Kap05].
3. The discovery of a new quadrature subsampling modulator architecture which can be calified as minimalist circuit. This architecture multiplexes in time domain the I and Q components of a bandpass subsampled signal through the same physical circuit, thus achieving a minimal transistor count and inherent mismatch insensitivity.

A summary of the contributions as are described in the document follows:

- The theoretical analysis of the modulator has been explored in depth in chapter 2, 3 and 4.

Three experimental circuits has been designed and implemented to support the analysis. These circuits have been presented in chapters 5, 6 and 7.

- In chapter 5 we have demonstrated the feasibility of sigma-delta modulation with transmission lines as resonators in its loop filter. The prototype second-order modulator was clocked at 53.7 MHz and achieves 63dB peak SNDR at an oversampling ratio of 128. When an excessive clock jitter of 1% of the clock period is applied, the modulator SNDR is degraded by 5dB only. This is 15dB better than a conventional CT-ΣΔM with capacitive integrators.

- Chapter 6 discusses the theory behind the design of a band-pass ΣΔM using transmission lines as delay elements. The theory is illustrated with the design and implementation of an experimental modulator using a 3.3V 0.35μm BiCMOS technology. As we have seen in this chapter, modulators implemented with this architecture have the drawbacks of requiring a special circuit to limit the distortion, the lack of inherent antialiasing filtering in the STF and the mismatch of the resonators. The mismatch would require not only off-chip tuning capacitors but on-chip tuning capacitors as well. Despite of this, building a bandpass transmission line ΣΔM with this approach benefits from the high Q_0 factor of transmission lines, allows down conversion by subsampling of the input, behaves close to a discrete time modulator at high clock jitter levels and tolerates loop delay. With a careful design, this modulator potentially allows for efficient sampling of narrow-band signals at very high frequencies with simple circuitry that does not require either a mixer or high-precision sampler. To summarize the results, the ADC operates at a f_s=184 MHz, consumes 62mW and is able to convert narrow-band signals centered both at 46 MHz and 138 MHz respectively, with a maximum SNDR of 58dB assuming an analog bandwidth of ABW=360kHz.

- In chapter 7, a new subsampling quadrature ΣΔM and its use in a radio receiver has been proposed. The presented receiver does not require quadrature mixers nor high precision sample-and-holds at the input. Furthermore, it has been shown that such a receiver has the potential to be immune against circuit imperfections like clock jitter in the DAC and

loop delay. A first architecture is based on a low-pass ΣΔ modulator with separate I and Q paths that subsamples a modulated carrier located around the sampling frequency. Chapter 7 shows simulations that include circuit nonidealities and proves the feasibility of the modulator even for the high IF values used in base station UMTS receivers. A second architecture turns out to be insensitive to analog path mismatch due to the sharing of the loop filter for both the I and Q paths. In this case, the bandwidth requirements are more stringent than in the two paths topology but the design is free of I /Q path mismatch. The theory is illustrated with the design and implementation of an experimental modulator using a 3.3V 0.35μm BiCMOS technology. To summarize the results, the ADC operates at a f_s=50 MHz, consumes 28mW and is able to convert I/Q narrow-band complex signals using only one path, centered both at 25 MHz and 75 MHz respectively. The dynamic range of the modulator is 10 bits with an analog bandwidth of ABW=1MHz. Also a two tone test is realized as long with an IRR test, showing an IMD close to 50 dBc, and an IRR behavior close to the theoretical value. The main advantage of this modulator compared with state-of-the-art quadrature CT-ΣΔMs is the possibility of digitize an IF signal at 75MHz using a one-path structure that is free from I/Q mismatches.

8.2 Future work

The open issues left after the research of this thesis fall within three categories.

- **Technology**. The possibility of integrating the transmission lines on-chip would reduce the power consumption by increasing the characteristic impedance of the transmission line and would minimize the parasitic problems. This problem possesses the following trade-off: or the operating frequency is increased to the gigahertz range or the size of the transmission lines will occupy most of the space of the chip. The author envisions two solutions: use of RF-MEMS resonators based on mechanical propagation, or use of a hybrid structure that mixes lumped and distributed components to approximate the behavior of an ideal delay.

- **Circuit issues**. The main problem that limits the practical results is the distortion caused by the dynamic range of the state variables. This problem has its foundations in the system level operation of the converter. It has been shown that a hard limitation of the dynamic range is not a problem by itself, as it does not generate distortion. However recovery from saturation in the active components is the real cause of distortion. New circuit techniques need to be developed to overcome the problem of dynamic range. One possibility is to modulate the gain of the transconductors with the sampling clock, constraining the peak values of the state variables far from the sampling points. Another possible solution is to use an optimized output stage in the transconductors which does not suffer from overload recovery problems.

- **System level improvements**. There are a number of different architecture modifications that may lead to new applications. One of the most interesting is the subsampling operation, which can be improved by mixing lumped and distributed loop filters [Her08]. Another unexplored choice is the implementation of multiple resonators which do not have integer delay ratios. This would result in a NTF function with multiple zeros that accumulate in the band of interest.

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