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Published in:
Journal of Engineering

DOI:
10.1049/joe.2017.0695

Publication date:
2017

Document Version
Peer reviewed version

Nova Techset Pvt Ltd, Bangalore
Doc: H:/IET/JOE/Pagination/JOE20170695/JOE20170695.3d

The 6th International Conference on Renewable Power Generation (RPG)

19–20 October 2017

DC STATCOM in multi-terminal DC distribution power system

Q2 *Dong Chen[1], Lie Xu[2], Yan Xu[3]*

[1]*Department of Engineering, Glasgow Caledonian University, Glasgow, UK*
Q1 [2]*Institute of Energy and Environment, Royal College Building, University of Strathclyde, Glasgow, UK*
[3]*State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electricity Power University, Baoding 071000, People's Republic of China*
E-mail: dong.chen@gcu.ac.uk

Published in *The Journal of Engineering*; Received on 11th October 2017; Accepted on 3rd November 2017

Abstract: Medium-power DC network is supposed to be able to enhance the operation of active power distribution system. The concept of 'DC STATCOM' is introduced to enable better dynamic performance with reduced DC fault current in an expanded DC power system. Virtual impedance method is employed to analyse the dynamics and design the control. To cope with the oscillation problem brought by constant-power terminal, a hybrid virtual impedance-based control strategy is used for the proposed DC STATCOM. Simulation based case studies validate the proposed conditioning method with reduced DC voltage oscillations and improved system stability.

1 Introduction

The growing penetration of renewable power generation along with the growing electricity consumption from electric vehicle (EV) [1] is emerging as a new format of power distribution system. DC power technology is becoming a potentially good solution for both electricity consumers and grid operators [2–5]. As the renewable distributed generations, energy storages and EV loads are naturally interfaced by DC/AC converters it can be more efficient and economical to employ the format of DC links [6] or network to integrate the local generation, storage and loads all together in an active distribution power system.

The growing EV charging demand is it can cause overloading or load unbalancing conditions. However, if a battery charging station is used as a bidirectional energy storage system (ESS) in a DC network, it can contribute to power flow optimisation and loading ability enhancement with proper control [7].

Large terminal capacitances are conventionally placed at DC terminals contributing to undesirable DC fault behaviour for 2-level voltage-source converter (VSC) DC system. The terminal capacitances are mainly for DC voltage stability, commutation and switching ripple filtering. The larger the capacitance is, the better the performance could possibly be. However, larger capacitance can contribute to excessive current surge after a pole-to-pole fault in a few mini-seconds. It consequently gives rise to higher requirement and cost on DC protections, e.g. DC circuit breaker. Nevertheless, potentially larger foot print and extra cost concerns are other disadvantages against the use of large terminal capacitances.

The problem of reduced terminal capacitances with long distribution line is that it degrades DC voltage control. Therefore, enhanced operation has to be carried out with relatively small terminal capacitances. Some enhanced voltage control strategies are proposed in previous studies to smooth the voltage variations though; the possible impact brought about by the line impedances are overlooked as the benchmark system is relatively compact [8, 9].

To better design the control and analyse a DC power system, a comprehensive model has to be established with active voltage control considered. By modelling DC voltage droop as virtual resistance [10], static power flow can be estimated in a DC network [8]. However, it does not apply to dynamic analysis with a more sophisticated voltage regulation. State-space and non-linear stability analysis methods have also been used to analyse DC power grid dynamics and stability, but with very complicated global system analysis and/or stabilising procedure [11–19]. Modelling with virtual impedance method is, therefore, proposed as a straightforward approach for DC system dynamics modelling [14].

System stability of DC systems with closely located DC loads including constant-power load (CPL) supplied by small-scale single deterministic DC source has also been well studied in the past years [11–13, 15, 17, 19]. Specifications of impedance matching for sources and loads are investigated with uni-directional system. However, for the cases when there are multiple slack terminals and bidirectional power flow, the stability is rarely explored.

In this paper, the concept of 'DC STATCOM' is proposed to help stabilise a medium-power DC system with bidirectional power and variable loads and generations. Similar to normal STATCOM for AC power system, it does not consume real power. The proposed DC STATCOM can actively contribute to small-signal stability with limited demand on power rating and energy capacity.

This paper is organised as follows: the modelling of DC system with virtual impedance method is briefly introduced in Section 2. Then, the proposed DC STATCOM is introduced and discussed in Section 3. After that, ESS-based stabilising is introduced and discussed in Section 5 and conclusion is drawn in Section 6.

2 DC system modelling using virtual impedance

In this section, the modelling fundamentals of a DC power system including the slack DC terminals, distribution lines, power terminals and their integration are introduced using virtual impedances.

A slack terminal can actively contribute to the power balance of a DC power system [8]. AC grid-side VSC (GVSC) and ESS terminals are typically able to operate as slack terminals. DC voltage control using droop or proportional–integral (PI) controller is normally employed in slack terminals, as is illustrated by Fig. 1*a*, and the equivalent terminal model can be depicted by Fig. 1*b* [14]. In Fig. 1, Reg(*s*) refers to the DC voltage regulator, which

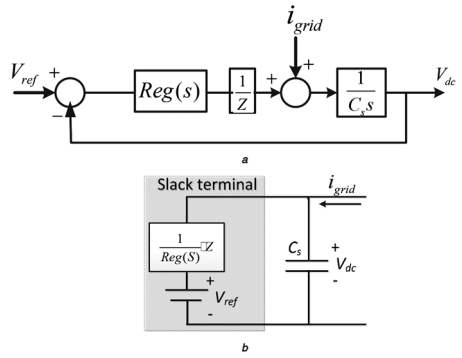

Fig. 1 *Slack terminal modelling*
a Control strategy
b Terminal model

is normally P or PI control. i_{grid} is the current coming from the DC network, C_s is the slack terminal capacitance and V_{dc} and V_{ref} are the terminal DC voltages and the DC voltage reference.

For DC distribution lines, the distributed capacitances are normally much smaller than terminal capacitance, so distributed capacitances are neglected in this paper.

A power terminal does not actively contribute to DC voltage stability [8]. It either draws or export power in the DC system independently. They can be categorised into three types: passive, constant current and constant power. The three types of terminals are demonstrated in Figs. 2*a*–*c*.

From Fig. 2*a*, it could be found that a passive (normally resistive) terminal consumes less current/power when the terminal voltage drops and there is a power deficit, whereas it absorbs more current/power when the terminal voltage rises and there is a power surplus. This characteristic can actually passively contribute to damping the voltage fluctuation.

The current consumption/injection of a constant-current terminal, as shown in Fig. 2*b*, is irrelevant to its terminal DC voltage. Therefore, the constant current can be considered as an injected perturbation noise in a linearised DC system model with infinitive impedance since for any change of voltage the change of the current is zero.

Unlike passive or constant-current terminal, a constant-power terminal consumes more current when terminal voltage drops, whereas less current when terminal voltage rises. This characteristic can deteriorate the voltage fluctuation when it is a load. Its time-domain equivalent circuit and small-signal linearisation model is shown in Fig. 2*c*. As shown, the virtual impedance of a constant load terminal is a negative incremental resistance $-R_{load}$, and its instant value can be calculated by the constant-power value P and its

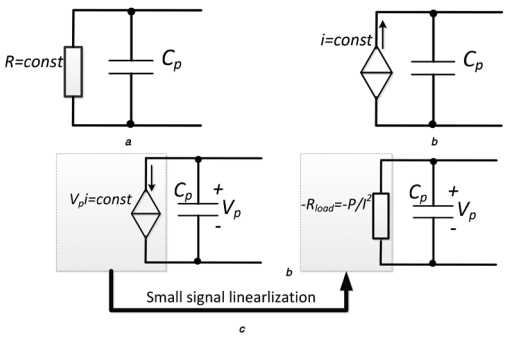

Fig. 2 *Power terminal modelling*
a Passive
b Constant current
c Constant power

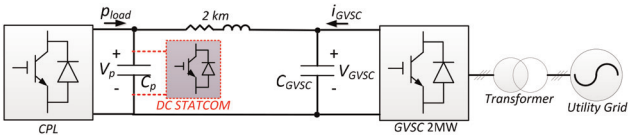

Fig. 3 *DC system with single slack terminal*

instant current I at the operational DC voltage. Larger CPL means more negative admittance value [11].

To demonstrate possible system instability brought by CPL terminals to medium-power DC networks, a sample DC system is established using MATLAB/Simulink as shown in Fig. 3. A 2 MW GVSC is employed as the sole slack terminal in this case. A CPL power terminal is located 2 km away from the GVSC. The initial parameters are: $C_{GVSC}=38$ mF; $C_p=2$ mF; line impedance is 7.2 mΩ and 0.15 mH per kilometre. The control delay of CPL is set at 1 ms, whereas the GVSC delay is 0.2 ms. The rated DC voltage is 1200 V and the natural frequency of GVSC's voltage loop is conventionally set at 10 Hz with a damping coefficient of 1. A DC STATCOM, which is physically a shunt ESS can be placed beside the CPL terminal, but is not activated in this section.

On the basis of the system depicted in Fig. 3, a power step simulation with constant voltage loop natural frequency setting is carried out to test the consequence brought by a reduced terminal capacitance (when the DC STATCOM is not connected). The relevant responses are shown in Figs. 4*a* and *b* with original capacitance 38 mF and a reduced value of 20 mF. A −0.4 MW load step is set at $t=0.1$ s. It can be seen in Fig. 4*a* that the maximum DC voltage dip at the GVSC terminal is about 50 V with larger slack terminal capacitance, whereas the voltage drop is doubled to 100 V in Fig. 4*b* as the capacitance is reduced.

A ramp load test is performed in Fig. 4*c* with P_{load} started at $T=0$ s with a ramp of 1 MW/s. It could be seen in Fig. 4*c* that the slack terminal voltage V_{GVSC} and the power terminal voltage V_p start to have significant oscillation approximately at $T=0.5$ s and $P_{load}=-0.85$ MW.

From the above case, it can be seen that reduced terminal capacitance can enlarge dynamic voltage variation and voltage oscillation can be triggered when transferring large constant power over a distance with conventional PI voltage regulation.

3 Principles of DC STATCOM

As CPL tends to cause instability and reduce system damping on the voltage loop due to its negative incremental resistance (admittance) nature. The principle 'DC STATCOM' is proposed to cancel the negative resistance by adding shunt virtual impedance with a shunt ESS to ensure the stability from the load side.

Virtual impedance method is considered here for control design. An initial idea of the proposed virtual impedance is to add a parallel positive resistance to cancel out the negative one brought by CPL, as is shown in Fig. 5*a*. This is based on the fact that a positively resistive terminal is not likely to cause instability with terminal capacitance. Moreover, to ensure a positive resistance on the CPL terminal, there shall be

$$0 < R_v < R_{load} \quad (1)$$

However, the control delay caused by a digitally controlled practical converter may give rise to a poor gain margin, as is shown in Fig. 6, and the margin tends to be poorer with smaller virtual resistance. In medium- and high-power applications, this delay can be even more significant due to lower switching frequency. To increase the gain margin, a serialised virtual inductance is proposed to be added to the virtual resistance as an RL stabiliser, which is **Q4**

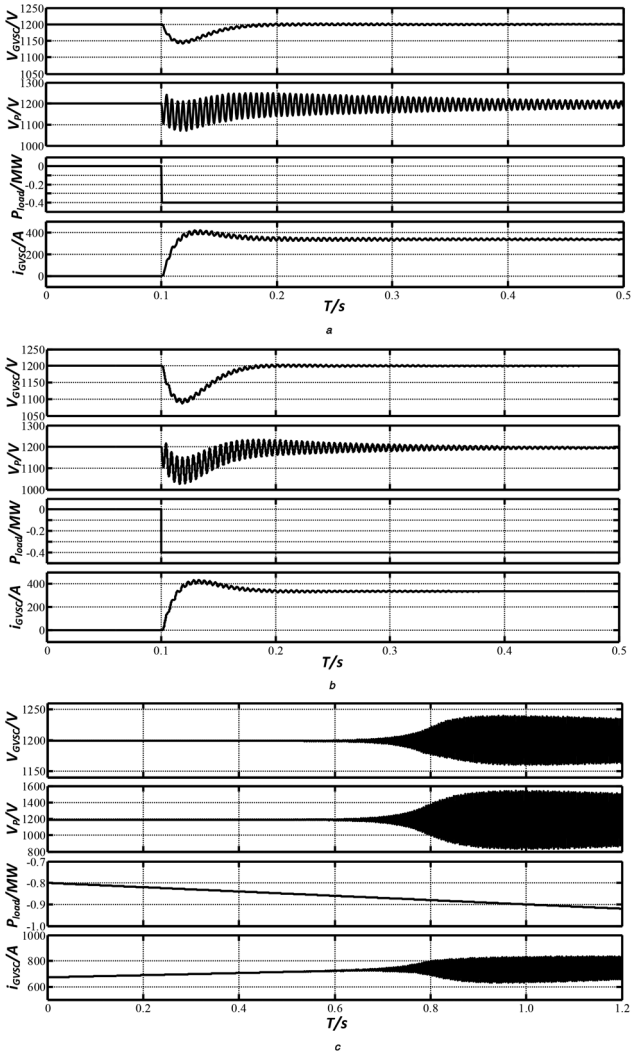

Fig. 4 *DC system performance without DC STATCOM*
a With normal physical capacitance (C_{GVSC} = 38 mF)
b With reduced physical capacitance (C_{GVSC} = 20 mF only)
c Ramp load with reduced physical capacitance (C_{GVSC} = 20 mF only)

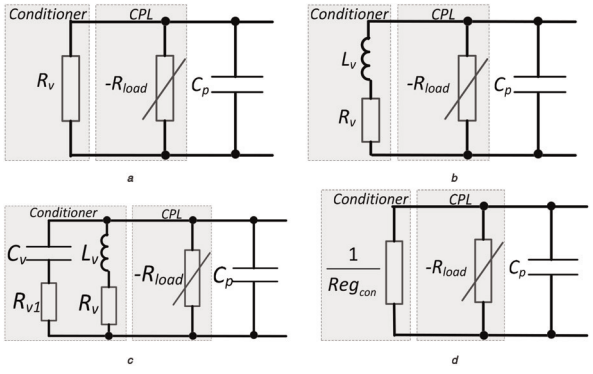

Fig. 5 *DC power conditioner on the load side*
a Virtual *R*
b Virtual *RL*
c Hybrid virtual impedance
d General equivalent

shown by Fig. 5*b*. The advantage of the virtual RL can effectively increase the gain margin by reducing the open-loop magnitude on the higher-frequency side, as is shown in Fig. 6. However, the

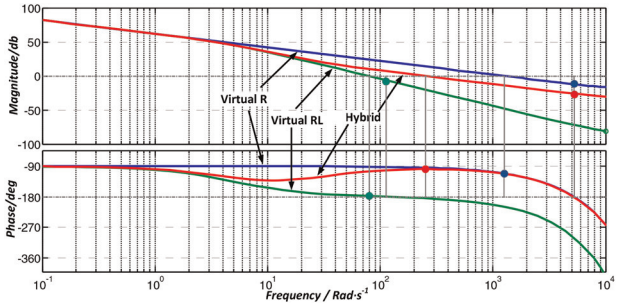

Fig. 6 *Bode plots of DC power conditioner on the load side*

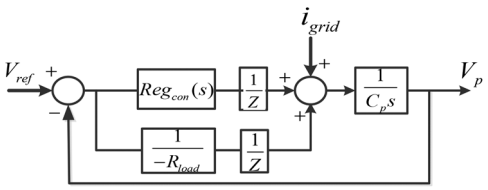

Fig. 7 *Load terminal control block*

side effect of the additional virtual inductance is a deteriorated phase margin at medium-frequency band. Adding a virtual parallel capacitor in this case does not help much, since it can be approximated as an addition to the physical capacitance and does not improve phase margin on the middle-frequency band. Instead, a virtual RC circuit is used to form a hybrid impedance to correct the phase margin as shown in Figs. 5*c* and 6. The virtual impedances can be given as

$$C_v = \frac{T_2}{R_v}; \quad L_v = R_v T_1; \quad R_{v1} = \frac{T_1}{C_v} \tag{2}$$

where R_v is the equivalent total virtual resistance and T_1 and T_2 are the correction constants. The transfer function of the conditioner $\mathrm{Reg_{con}}$ can be given by

$$\mathrm{Reg_{con}}(s) = \frac{1 + T_2 s}{(1 + T_1 s) R_v} \tag{3}$$

On the basis of (10) and Fig. 4*d*, the control block diagram can be obtained as Fig. 7. In Fig. 7, the DC network side dynamic is represented by i_{grid} and the power terminal voltage is V_p, and the digital implementation of current (power) loop control dynamics are simplified as a unit delay.

From Fig. 7 and (10), it can be found that the DC STATCOM will have a static current/power offset as long as terminal voltage V_p deviates from the predefined V_{ref}, which is practically inevitable. To eliminate the DC current offset, an extra first-order high-pass filter with a large time constant T_f, 5 s for instance, is added.

The final transfer function of the proposed virtual impedance-based regulator can be given as

$$\mathrm{Reg'_{con}}(s) = \frac{1 + T_2 s}{(1 + T_1 s) R_v} \cdot \frac{T_f s}{1 + T_f s} \tag{4}$$

4 Case study

To test the proposed hybrid conditioner, a sample DC power network is established as Fig. 8 shows. The system is configured as a 4-terminal star connection with a central point connected to a

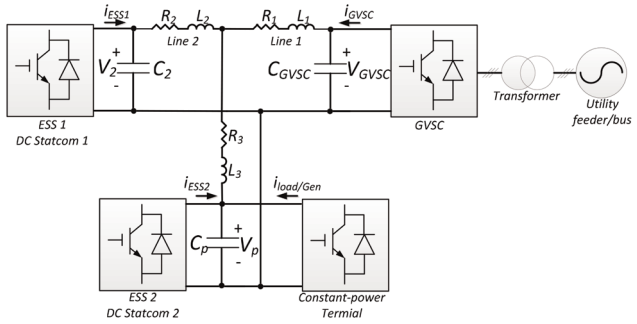

Fig. 8 *System setup*

GVSC via a short length of DC line. An extra ESS terminal ESS 2, as shown, is added in close proximity to the constant-power terminal side. The reference current directions are shown in Fig. 8. The initial parameters are as the following: $C_{\mathrm{GVSC}} = 20$ mF, $C_2 = 4$ mF, $C_{\mathrm{p}} = 2$ mF; a 0.15 mH/km, 7.2 mΩ/km DC cable is used here with Line 1 configured as 0.1 km; and Line 2 and Line 3 both as 2 km.

(1) Ramp response

The rated power is set at 2 MW and rated voltage 1200 V. The current limit of the GVSC terminal is set accordingly. A closed-loop PI voltage regulation is employed by the GVSC terminal with a natural frequency of 10 Hz and a damping coefficient of 1. It is assumed that the load and generation-side capacitances are unknown to the GVSC controller. The power loop bandwidth of the power terminal (for CPL and generation) is set as 26.5 Hz ($2500/15/2\pi$). To better demonstrate the control behaviour, assumptions are made that no system operational mode switching [3] or protection measures are triggered throughout the following tests.

To test the impact of a CPL on system stability to an expanded DC network, system test during a CPL ramp of the power terminal is performed and the results are shown in Fig. 9.

A load ramp without ESS power conditioning is tested and the simulation results are demonstrated in Fig. 9*a*. Both ESS terminals are blocked in this case. A CPL draws power P_{load} from the power terminal side at $T = 5$ s with a ramp rate of −0.05 MW/s (minus signal indicates consuming power) and i_{load} drops accordingly from $T = 5$ s. To balance the DC voltage, the GVSC immediately counters the load current as i_{GVSC} shows. The voltage is regulated closely to 1200 V at the starting part of the load ramp until at around $T = 19$ s, where the load reaches around 0.7 MW. Significant DC voltage oscillation appears as the GVSC cannot accommodate the dynamics caused by the large CPL. Both i_{GVSC} and i_{load} oscillate in the same time. This clearly shows that a CPL from far side of the GVSC can cause small-signal instability even with smoothly changing power consumption resulting severe voltage oscillations at the remote-side power terminal.

Fig. 9*b* shows the test results when a remote conditioner ESS 1 ($T_1 = 0.04$, $T_2 = 0.2$ and $R_{\mathrm{l}} = 1\ \Omega$), 4 km away from the power terminal, is activated for power conditioning. Compared to Fig. 9*a*, it can be seen that the oscillation starting point is delayed by ∼5 s, i.e. the DC voltages oscillate after the CPL reaches 0.95 MW (compared to 0.7 MW in Fig. 9*a*). Again, the power terminal voltage has the largest oscillation.

Fig. 9*c* shows the results with one operating ESS power conditioner located at the power terminal. With the same power consumption as

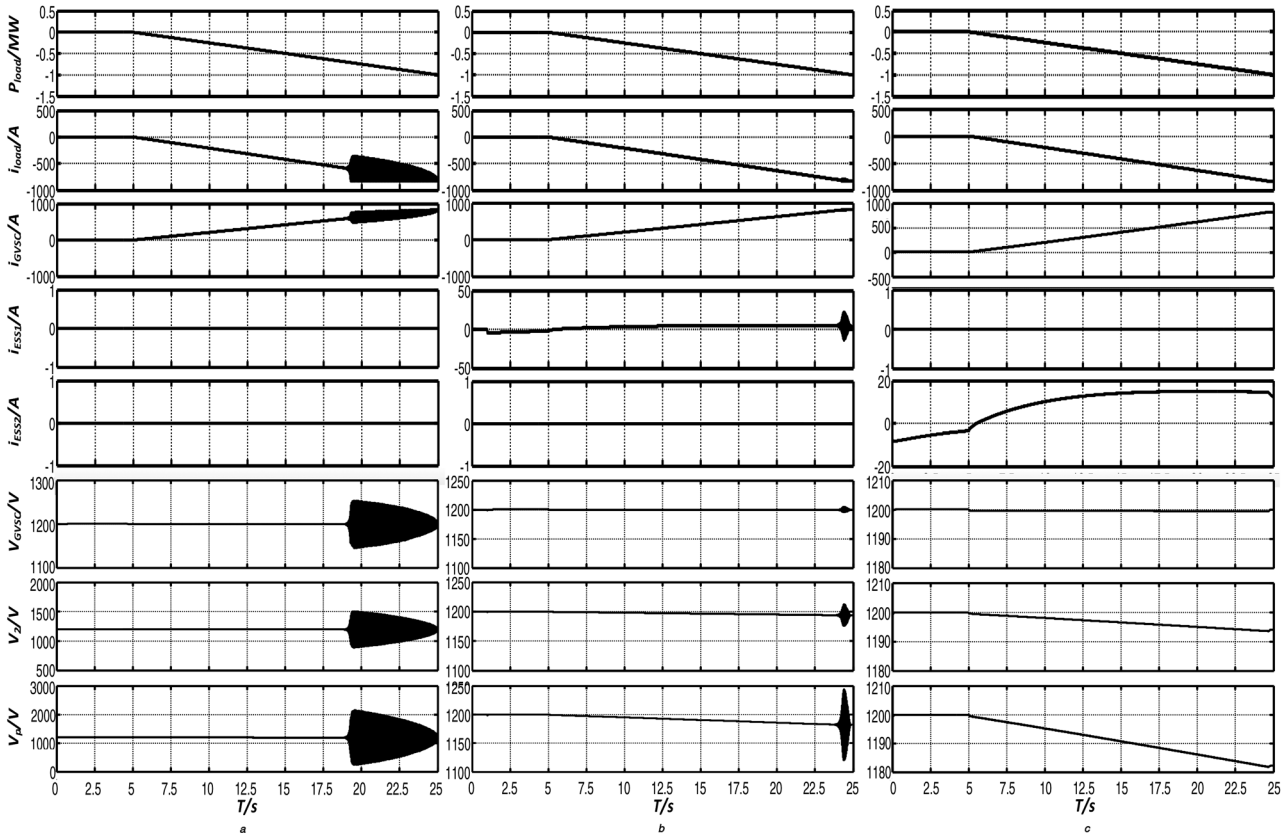

Fig. 9 *Ramp CPL test*
a Without DC power conditioning
b With remote DC power conditioning
c With local DC power conditioning

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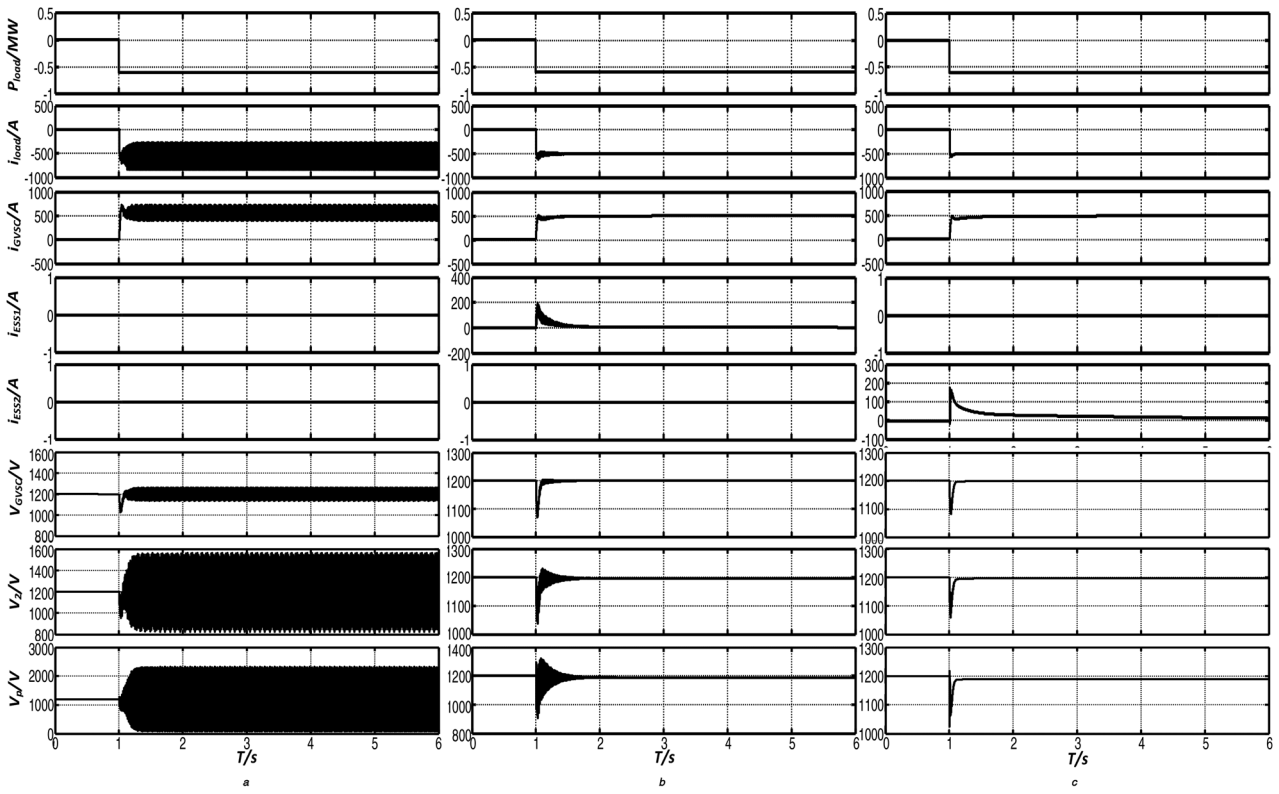

Fig. 10 *Test with constant load step*
a Without DC power conditioning
b With remote DC power conditioning
c With local DC power conditioning

Q6 in Figs. ~~12~~*a* and *b*, the ESS power conditioner with a small start current offset and decays to ∼0 at $T = 5$ s. With ESS 1 blocked, ESS 2, with the same conditioning setting as ESS 1, starts to help to accommodate the load increase. No oscillations are witnessed even though the CPL has reached 1 MW. A noticeable fact is that even though the load current has reached 833 A, the maximum conditioning current is <20 A, ∼2.5% of the CPL current rating. This means that the extra power rating demanded from the power conditioner is only a small percentage of the total rating for steady-state operation.

(2) Step response

Further tests with 0.6 MW step change of the CPL at $T = 1$ s, which is 30% of the system rated power, are performed, where the Maximum CPL current amplitude is set at 1 MW/1200 V.

Fig. 10*a* shows the results without ESS power conditioning. As seen, system instability and large voltage and current oscillations are induced immediately after the step. In comparison, Fig. 10*b* shows the results during the power step when the remote ESS 2 is activated for power conditioning. It can be seen that the oscillation is largely damped after the step and the terminal voltages converge. Considerable voltage sag is triggered by the step at each terminal, with the GVSC terminal being the lowest at 120 V and the power terminal the highest at 240 V.

With the DC STATCOM located at the closest location to the power terminal, the simulation results are shown in Fig. 10*c*. It can be noted that the oscillation caused by the load step is completely eliminated. The DC voltages are generally well maintained, the DC voltage at the GVSC terminal remains at 120 V, but the largest voltage sag at the power terminal is now reduced from 240 V in Fig. 10*b* to 190 V. The local power conditioner shares ∼25% of the step current consumption at the instant after the load step and drops to zero afterwards.

From the above studies, it can be seen that large CPL located at remote terminals in a DC system can cause instability. The proposed DC STATCOM is able to enhance the small-signal stability with limited current rating and zero energy consumption. The closer a DC STATCOM is located to the CPL, the better enhancement performance it can achieve. A DC power system with multiple DC STATCOM scan also be implemented, which shows similar improvement though the simulation results are not presented in this paper due to space limitation.

5 Conclusion

For a multi-terminal DC network of bidirectional power flow, the reduction of terminal capacitance and line impedance can lead to unstable dynamic performance. By using the proposed 'DC STATCOM' with the control designed with virtual impedance method, the system dynamics can be effectively stabilised.

6 Acknowledgments

This study was supported by the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources (grant no. LAPS17020), China, the North China Electric Power University and UK Engineering and Physical Sciences Research Council (grant no. EP/K03619X/1).

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