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Design and implementation of 30kW 200/900V LCL modular multilevel based DC/DC converter for high power applications

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Keywords: DC/DC Converter, DC fault, Modular Multilevel Converter (MMC), DC grids, Selective Harmonic Elimination.

Abstract

This paper presents the design, development and testing of a 30kW, 200V/900V modular multilevel converter (MMC) based DC/DC converter prototype. An internal LCL circuit is used to provide voltage stepping and fault tolerance property. The converter comprises two five level MMC based on insulated gate bipolar transistors (IGBTs) and metal oxide semiconductor field effect transistor (MOSFET). Due to low number of levels, selective harmonic elimination modulation (SHE) is used, which determines the switching angles in such a way that third harmonic is minimized whereas the fundamental component is a linear function of the modulation index. In addition, instead of using an expensive control board, three commercial control boards are embedded. This is required to implement the sophisticated DC/DC converter control algorithm. Simulation and experimental results are presented to demonstrate the converter performance in step up and down modes.

1 Introduction

Point to point HVDC systems have been implemented for many years, but multi-terminal DC systems and DC grids have not been developed yet mainly because of protection issues against DC faults. Additionally, DC voltage stepping is required considering a lack of standardization and need to integrate/tap in existing HVDC links [1].

Medium and high power DC/DC converters have been investigated recently for wide range of applications like offshore wind farms and high/medium voltage DC (HVDC) grids. High power DC/DC converters offer DC voltage stepping and DC power regulation with additional benefit of DC fault isolation and will play important role in future DC grids [2-3].

There are several possible technologies for high-power DC/DC converters [2-4]. A thyristor based DC/DC converter has shown excellent performance for low stepping ratios and a 30kW, 200V/900V prototype has been developed and tested [4]. Despite the advantages of eliminating transformer, both the high and low voltage side switches should be rated for high voltage level.

The transformer based DC/DC converters can achieve large stepping ratios but they suffer from transformer core losses, and core saturation in the event of faults. A five MW transformer based DC/DC converter with stepping ratio of 8 was studied in [5] and total losses of 3-4% were reported. The transformer core losses restrict these topologies to 200-300Hz frequency for high power applications [6].

An IGBT based DC/DC converter utilizing two VSC converters and a LCL circuit was proposed in [7]. This topology offers advantage of achieving high stepping ratios but without internal AC transformers, and benefit from inherent DC fault isolation. The first property implies further room for switching frequency increase with no significant loss increase, and the second advantage provides the converter with fault current limiting and interruption capability using local measurements. However, this IGBT based DC/DC converter uses two-level converter topology which uses series IGBT chains to meet high voltage requirements. This needs complex voltage sharing circuitry and controls.

To get rid of the IGBT chain issues, the LCL DC/DC converter have been designed using modular multilevel converter (MMC) rather than the conventional two-level converters in [7]. MMCs have been well known at research level for connection with 50/60Hz grids and have been commercially deployed in the Trans Bay project in California. However, their use in DC/DC converters has only been a subject of recent researches. In [9-11] MMCs are connected front-to-front via an isolating transformer to obtain voltage stepping and galvanic isolation. However, in contrast to LCL DC/DC converter, fundamental frequency is limited to a few hundred hertz to limit transformer magnetic losses.

DC fault management with MMCs has been studied recently in literature [12-14]. In [12], a MMC based fault blocking DC/DC converter has been proposed but it uses a high number of semiconductors and magnetic elements. MMCs based on half-bridge sub-modules utilize bypass thyristors to protect switches from DC fault over current [13, 14].

This paper addresses semiconductor selection, MMC inductance/ capacitance selection, and LCL circuit design applied in designing, developing, and testing of a 30kW, 200V/900V MMC based LCL DC/DC converter. In addition, this paper discusses challenges regarding the DC/DC converter assembly and its control execution. This paper proposes that three commercial control boards (sbRIO-9606) working in parallel can be used instead of an expensive control board to control the MMC based DC/DC converter.

The simulation and experimental results obtained from the converter model developed on PSCAD platform and the developed test bench is demonstrated.

2 Converter Design

Fig.1 (a) shows the topology of five level MMC based LCL DC/DC Converter. It consists of two five level MMCs powering an inner LCL AC circuit. It is assumed that the DC voltages do not change their polarity, but can deliver or sink active power. The five level MMC utilizes half-bridge sub-modules with two semiconductor switches per sub-module and comprises of two phases as depicted in Fig. 1(b). This is the minimum number of phases to interface full pole-to-pole DC voltage. With the two-phase structure considered here, there exists two inductors L_i and two capacitors C_i per port, where i denotes the ith port (i=1, 2).

2.1 Switch Selection

It is evident that the active bridge switches should be rated for associated DC voltage level and rated current. A comparison has been carried out for the available semiconductors in the market in terms of their total cost, footprint dimensions and losses while operating at rated conditions of each power port. Considering the voltage and current ratings on 200V side, MOSFET module has been selected, SK260MB10 (100V, 230A), due to cheaper and low losses in compared with IGBT module, SKM400GB066D (600 V, 400 A). For 900V side, IGBT module, SKM 145GB176D (1700, 120A) is used.

2.2 MMC Inductance and Capacitance Selection

According to [13], MMC sub-module capacitance for port i can be calculated using:

$$C_{SM} = \frac{EP.S_i}{p.N.V_{SM}^{\ 2}} \qquad (1)$$

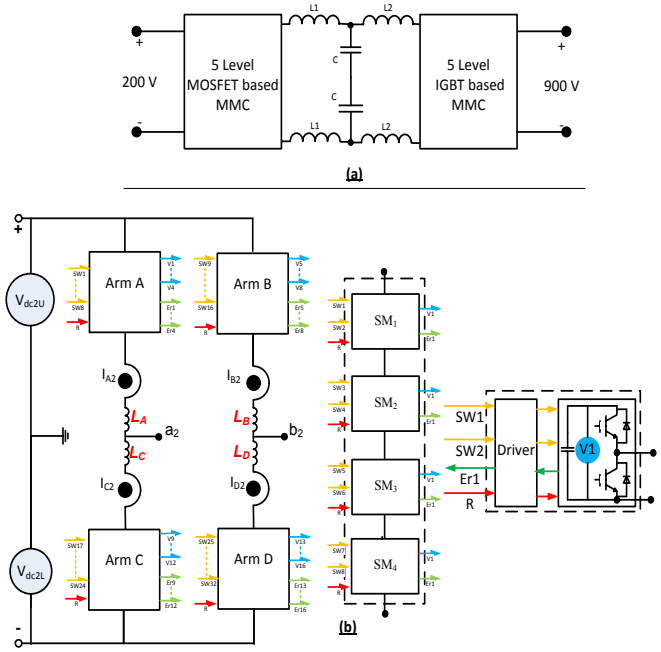

Fig.1: (a) Five Level MMC based LCL DC/DC Converter, (b) Single phase five Level MMC

where EP is the energy-power ratio typically in the range of $10J/kVA$ to $50J/kVA$, S_i is rated apparent power, p is the port converter number of phases, N is the number of sub-modules per MMC arm and V_{SM} is the nominal sub-module capacitor voltage. Simulation results confirm 2000 µF, 50 V_{DC}, DCHPI07406EW00, and 150 µF, 225 V_{DC}, DCP6I06320EB00, from WIMA can be adapted properly for low and high voltage cells.

Minimum arm inductance L_{arm} necessary to eliminate a certain even harmonic h in MMC circulating current is given by [13],

$$L_{arm} \geq \frac{N}{\omega_o^{\ 2} C_{SM}} \frac{2\left(h^2-1\right)+M_i^{\ 2}h^2}{8h^2\left(h^2-1\right)} \qquad (2)$$

where C_{SM} is sub-module capacitor, N is the number of sub-modules per MMC arm, ω_0 is angular frequency, h is a certain even harmonic, and M_i is modulation index. The selections are 5.12 µH, 160A for 200 V side and 30 µH, 35A for 900V side. The inductors have been wound in house using 270x0.45mm and 135x0.45mm Litz wire for 200 V and 900V respectively.

2.3 LCL Circuit Design

The LCL circuit design is described in [8]. The design components are based on converter nominal power level, and stepping ratio and is a compromise between converter total losses minimization and fault response from either side. It should also guarantee the local and overall resonance frequencies would be far away from switching frequency to avoid undamped oscillations. Main AC frequency of 2 kHz is selected to enable fixed value of 41.88 µF for the AC capacitor, which can be obtained from off the shelf capacitors in the market. This will demonstrate high frequency DC/DC converter benefiting from smaller overall footprint and weight as well as lower inductor loss and higher efficiency.

The AC capacitor will have high AC current magnitude. Currently, the high power high frequency capacitors are used in industry for snubber applications and for induction heating. Due to high ripple current flow through the capacitor, low ESR capacitors should be employed and film capacitors are a good candidate. However, most of these capacitors' voltage rating rapidly decreases with frequency increase and appropriate series-parallel connections should be considered to achieve the required voltage rating. The capacitors in the proposed prototype are made of an array of 30µF, 20µF and 10µF as shown in Fig.2 (a). Note that voltage rating of the selected capacitors decreases to 65 % at the converter main frequency of 2kHz.

Air core inductors have been designed and wound in house using Litz wire employed to decrease higher conduction losses at high frequencies. Each 200V side AC inductor includes 6x6 (layers by turns in each layer) Litz wire involving 2x(270x0.45mm) windings in parallel. Each 900V side inductor includes 7x10 (layers by turns in each layer) Litz wire involving 135x0.45mm copper wire. To decrease the total inductor size, weight, and loss the two pole inductors have been closely wound with a small gap in between as is in Fig. 2(b).

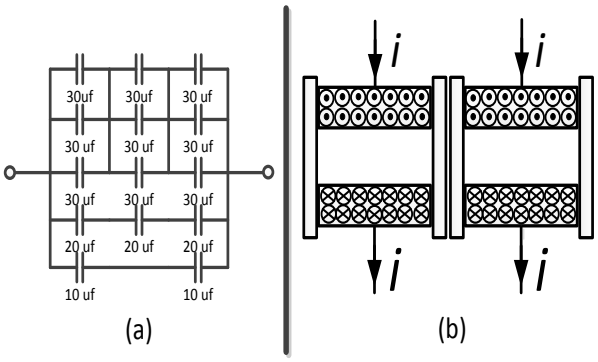

Fig.2 (a): AC capacitor, (b): AC air core inductors

This will increase the magnetic flux and results in larger total inductance of 352 µH using two 72 µH individual inductors on the LV side. The same method is applied for HV side inductors and two closely wound individual inductors of 140 µH make a total inductance of 653 µH.

3 DC/DC Converter Control

The LCL DC/DC converter control is described in [4] and it is based on one port controlling power and the other acting as a balancing port. The sinusoidal reference voltage for each MMC converter is constructed from modulation indexes (M_d and M_q) produced by controller. The reference angle for the firing logic comes from a voltage-controlled oscillator (VCO), $\theta=2\pi f_o t$, and θ is common for both converters. This is the input to the selective harmonic elimination modulator and capacitor voltage-balancing algorithm.

3.1 Selective Harmonic Elimination (S.H.E) for five level MMC

Nearest Level Control (NLC) is the most feasible and practical modulation for high voltage MMC applications with high number of levels. However, it is not applicable for a five level converter as the linearity between the modulation index and fundamental component is not achieved due to low number of levels. S.H.E is an alternative switching technique method; the semiconductor is switched ON and bypassed with considering the desired fundamental component and harmonic distortion [15].

Fig. 2 (a) shows that there are two-degree of freedom ($\propto_1$, $\propto_2$) for a five level output voltage. Switching angles are computed using the Newton-Raphson iterative technique in such a way that the fundamental component (b_1) keeps linear with modulation index whereas the third harmonic (b_3) is minimised as shown in Fig. 3 (b). Note that only for modulation index bigger than 0.56, the third harmonic is zero. This is because that for modulation index less than 0.56, $\propto_2$ is reached to 90^O (maximum value for a realistic solution) and one degree of freedom is missed as confirmed by Fig. 3(c).

3.2 Sub-Module Capacitor Voltage Balancing

To minimise switching instants (one pulse per fundamental cycle) and hence reduce losses, the capacitor voltage balancing function is activated only when the output voltage level is changed. The capacitor voltage balancing function sorts sub-module voltages based on the arm current directions. It sorts the sub-module voltages from maximum to minimum when the arm current will discharge the sub-module capacitor voltages or from minimum to maximum for when the arm current will charge the sub-module capacitor voltages.

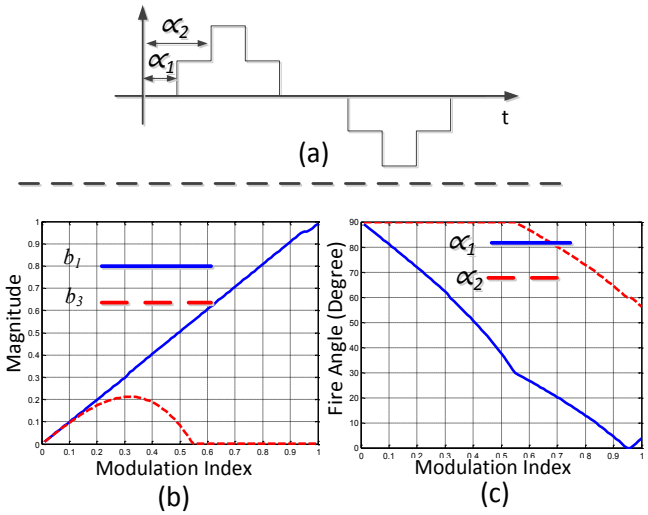

Fig. 3 (a): Output voltage (b): Fundamental and third components (c) switching angles for a five level converter switched based on Selective Harmonic Elimination.

3.3 Sub-Module Switching Function

According to number of level and sorting the sub-module capacitor voltages, the sub-module switching function determines which sub-modules to be ON/bypassed to maintain capacitor voltage balance and produce the desired output voltage.

4 Hardware Implementation

Fig. 4 shows a photograph of the developed DC/DC converter. To immunise Electro Magnetic Field (EMI) noise caused mostly by air core inductors, all control and interface boards have been installed at a separate grounded rack (left side rack). All power components including LCL components, arm inductors, 200 V sub-modules, and 900 V sub-modules are placed on top, middle, and bottom of right side rack respectively. Note that, air core inductors are installed on wood sheets as a conductive sheet can play role of an induction load which increases the system losses. In addition, 200 V and 900 V inductors are fixed perpendicular to each other to cancel their mutual induction effects.

To implement the sophisticated MMC based DC/DC converter control 32 Analogue to Digital Conversion (ADC) channels for 200 V and 900 V sub-module voltages, 8 ADC channels for 200 V and 900 V arm currents, 6 ADC channels for AC and DC bus voltages, 64 Digital Output to control the sub-module semiconductors, and 32 Digital Input for the sub-

Fig.4: 30kW, 200V/900V MMC based DC/DC Converter

module semiconductors, and 32 Digital Input for the sub-module short circuit protection are required. However, a control board with these features is a quit expensive. To employ an effective cost management, three sbRIO-9606 National Instrument commercial control boards are proposed to execute the DC/DC converter control, as one Master and two Slaves as shown in Fig. 5.

The sbRIO-9606 is an embedded control and acquisition device including a real-time processor, a user-reconfigurable FPGA, and I/O on a single PCB. It is employed to control the DC/DC converter in a real time manner. Each control board features are a 400 MHz industrial processor, a Xilinx Spartan-6 LX45 FPGA, 16-Channel12-Bit Analog-to-Digital Converter up to 100k samples per second, and a RIO Mezzanine Card connector, which is a high-speed, high-bandwidth connector that provides direct access to the processor and 96 3.3 V digital I/O FPGA lines. In addition, this device features an Ethernet port that can be used to conduct communication between host (PC) and the controller.

The master control board measures the 200 V DC bus voltages, 900 V DC bus voltages, AC capacitor voltages, 200 V arm currents, and 900 V arm currents. The DC and AC side currents are calculated from arm currents. These values are compared with the respected thresholds to protect the DC/DC converter control against AC and DC side faults. The protection logic outcome, which is zero in presence of fault, is one bit which transmitted to the slave boards. In addition, the master control computes the d and q axis modulation indexes based on the DC/DC converter control strategy for the 200 V and 900 V converters. The S.H.E block selects the number of levels based on the modulation indexes and the switching angles saved at the lookup tables. To transmit the number of levels to the Slave boards, 3-bits can cover all possible states that are 0, 1, 2,..., 4for a five level converter. To send the arm current direction to the slave boards, another 4-bits, each bit represents each arm, are required. The Master control board merges 8 separate bits as shown in Fig. 5 and sent to slave boards through the Serial Peripheral Interface (SPI).

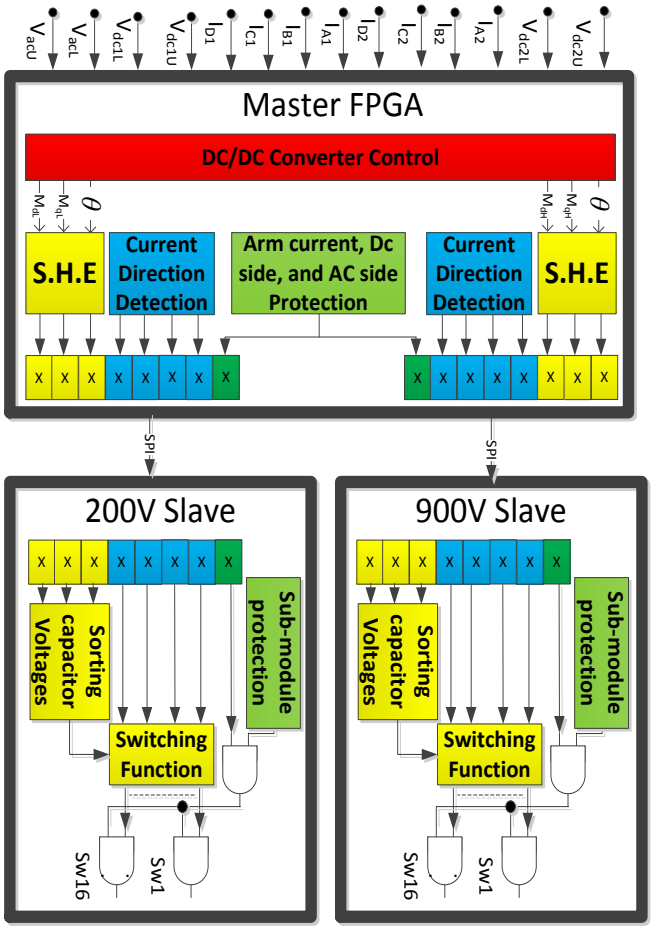

Fig. 5 : Executing the DC/DC converter control using three identical control boards.

With a common serial protocol, there is no control over when data is sent or any guarantee that both transmitter and receiver are running precisely at the same rate. In contrast, SPI works in a synchronous manner, which means that it uses separate lines for data and a "clock" that keeps both side in perfect synchronisation. The clock is an oscillating signal that tells the receiver exactly when to sample the bits on the data line. This could be the rising (low to high) or falling (high to low) edge of the clock signal. When the receiver detects that edge, it will immediately look at the data line to read the next bit. We set 3.2 MHz as the clock frequency clock and so the data in slave boards can be updated with 400 kHz.

The dedicated slave boards individually control the 200 V and 900 V sub-module switches. Each slave board measure 16 sub-module voltages as input of the sorting capacitor voltage function. Capacitor voltages are monitored as well to protect sub-module capacitors against the over voltages in case that the balancing algorithms is failed. Short circuit sub-module protections are implemented by monitoring V_{CE} on each sub-module switches at the 200 V and 900 V converters. As shown in Fig. 5, the sub-module output protection associated with top-level protection scheme executed by the Master control board to turn off all switches in presence of the undesirable occurrences and faults.

The capacitor voltage sorting function and the switching function use the transmitted number of levels and arm current directions to determine the sub-module switching states. To mitigate noise issues due to high power level, optical fibre cables from the slave controllers to the driver inputs have been used. SKHI22AR driver boards have been adopted to provide gate signals for the high and low voltage switches.

5 Simulation and Experimental Results

The DC/DC converter is tested in step up and step down modes linking pre-developed 30kW 200V and 900V voltage source converters (VSCs) acting as power source and sink. Both VSCs have been built in house with detailed design description presented in [3].

The converter performance is validated through simulation results obtained from test system modelling on PSCAD platform. The simulation results obtained in step up mode at 30 kW output power. Fig. 6 (a) and (b) show AC current and voltage at 900 V and 200V sides respectively. The results are obtained in open loop mode with modulation indexes M_d=0.11 and M_q= 0.95 on 200 V side and M_d=0.44 and M_q=-0.77 on 900 V side. Note that modulation index have been selected so that the voltages and currents at either sides are in-phase. It confirms that the reactive power circulation on both side are zero.

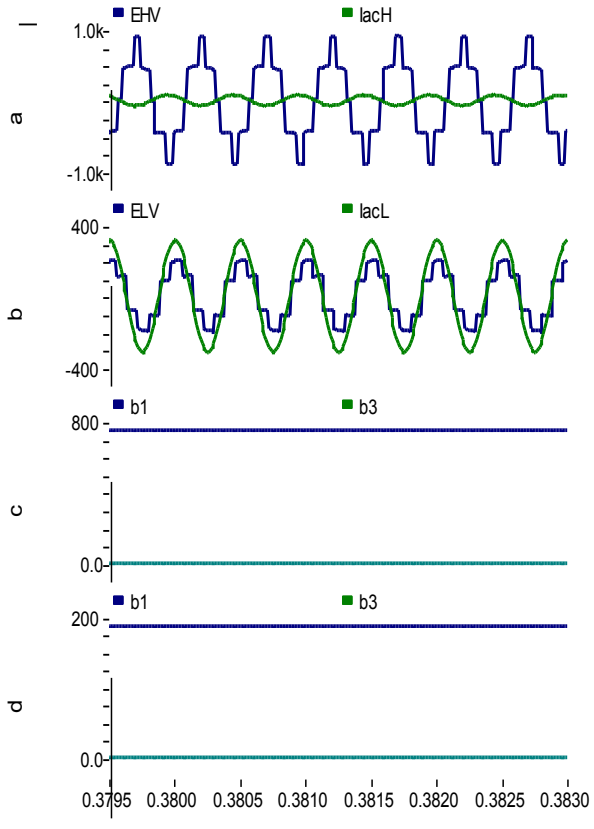

Fig. 6: (a): AC voltage and current at 900 side, (b): AC voltage and current at 200 side, (c): Fundamental and third components at 900 side, (d): Fundamental and third components at 200 side.

With closed loop operation, reactive power can be kept on zero for all operating ranges that will guarantee implementation of maximum efficiency strategies. Fig. 6 (c) and (d) show the first and third harmonic magnitudes of output voltage at 900 V and 200V side, which confirms that third harmonic, are kept at zero at both AC terminals. Fig. 7 (a) and (b) show the sub-module capacitor voltages for one arm at 900V and 200 V sides respectively, which confirm the performance of the capacitor balancing and switching functions.

At the first step of experimental tests, 900V and 200V MMC converter individually has been tested through an R-L load that confirms the switching function and the sorting capacitor performance. Fig. 8 (a) shows 200 V output voltage and current respectively whereas Fig. 8 (b) shows cell capacitor voltages at one of the arms at the 200 V side. As it can be expected the output voltage has five different levels and cell capacitor voltages are balanced around 50V.

At the present, we are pursuing to complete the full experimental tests to include the closed loop control.

6 Conclusion

A 30 kW, 200V/900V transformer-less LCL MMC based DC/DC converter was designed, built and tested in open loop mode. The DC/DC converter was tested by installing the converter between two 200V and 900V VSCs. To improve the DC/DC converter efficiency and control performances two refinements have been addressed. First, the cell semiconductor states ON and bypass when the output voltage level is changed. Second, the switching angles have been determined based on S.H.E in such away the main output voltage component is proportional with modulation index whereas the third harmonic keeps minimum. In addition, to employ an effective cost management, the paper presented how the sophisticated DC/DC converter control can be split and executed on three commercial control boards instead of using one control board which is expensive .

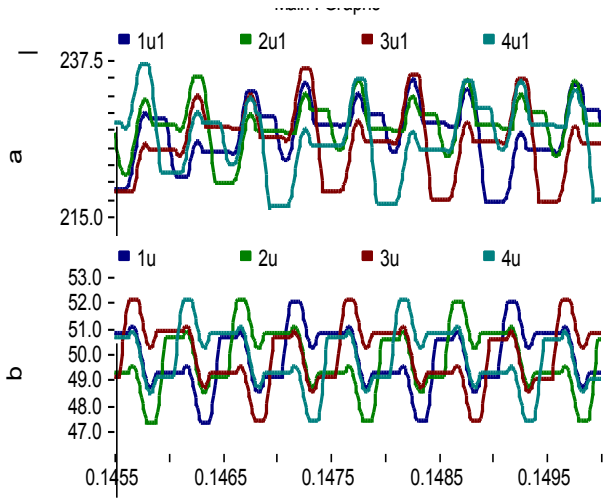

Fig. 7 (a): Cell capacitor voltages at 900 V side, (b): Cell capacitor voltages at 200 V side.

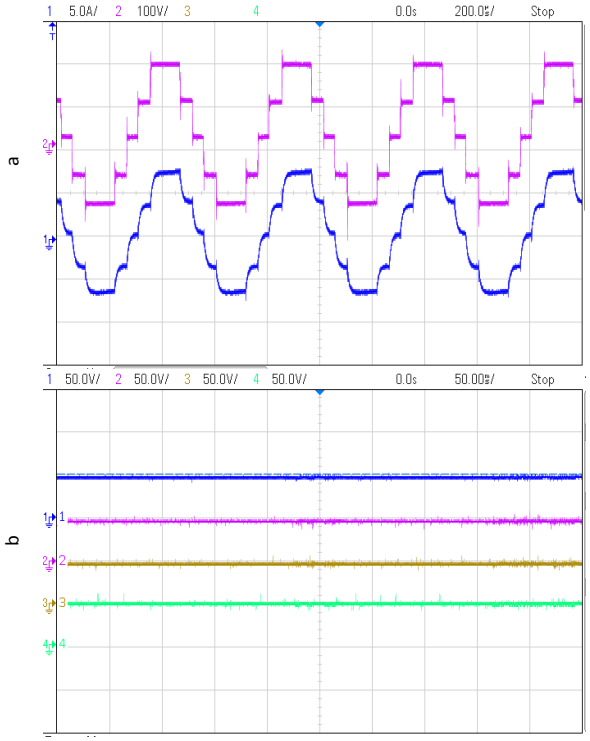

Fig. 8 (a): AC voltage and current at 200 side, (b) Cell capacitor voltages at 200 V side.

This research is on-going to implement and test the DC/DC converter associated with a new closed loop system to achieve zero reactive power circulation at both AC side from partial to full load ranges.

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