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Knezevic, Sasa; Stojanovic, Radovan; Karadaglic, Dejan; Asanin, Bogdan

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# A Single Chip System for ECG Feature Extraction

Saša Knežević, Radovan Stojanović
Faculty of Electrical Engineering
University of Montenegro
Podgorica, Montenegro
sasaknezevic@live.com, stox@ac.me

Dejan Karadaglić
School of Engineering and Built Environment
Glasgow Caledonian University
UK
Dejan.Karadaglic@gcu.ac.uk

Bogdan Ašanin
Faculty of Medicine
University of Montenegro
Podgorica, Montenegro
basanin@ac.me

*Abstract* — **This paper proposes an on-line system for feature extraction from ECG signal. The QRS detector, RR interval calculator, heart rate calculator and additional modules are developed in VHDL code and embedded in a single FPGA chip. The overall design has a low hardware occupation, 1838 LEs, and minimal number of setting parameters, only two, sampling and clock rates. The achieved accuracy is 97.5%. As such, it is very suitable for embedding in wearable health care systems, portable instruments and telemedicine devices. The methodology for QRS detection, system architecture and preliminary testing results are presented.**

***Keywords-FPGA; Discrete Wavelet Transform; QRS complex; RR interval; heart rate***

## I. INTRODUCTION

Features from ECG signal are of fundamental importance for monitoring health status and diagnosis of many diseases. Detection of QRS complexes is the first step in determining heart rate (HR), heart rate variability (HRV) and detecting cardiac arrhythmias (CA). Many algorithms for QRS detection exist and several of them employ Wavelet Transform (WT), which demonstrated good performances in analyzing non-stationary signals, like ECG [1]. Very often, the algorithms for feature extraction from ECG, including QRS detection, are implemented off-line using dedicated software running on personal computer.

On the other hand, the field of telemedicine and wearable health care systems are among the fastest growing areas, where autonomous, miniature, low-cost, ultra-low-power devices, usually, based on a single chip, play main role. In addition to digitalization, data storage and communication, these chips need to perform complex signal processing, all in real-time. It is not a trivial task considering the limitations in arithmetic power, memory resources, consumption budget, etc.

Thus, there is an essential need to optimize different signal processing algorithms, including those for ECG processing, for their on-chip implementation. Some trials are presented in [2], [3] and [4], which use Digital Signal Processors (DSPs), Microcontrollers (MCs) or Field Programmable Gate Arrays (FPGAs). Among them, FPGAs have many advantages including low price, inherent parallelism, design and testing, flexibility and feasibility to transform to Application Specific Integrated Circuit (ASIC) design. Comparing to the implementations in DSPs or MCs, the FPGA design can work with much higher throughput, can be integrated with other modules on the same chip and has more processing power for further development of the system.

This paper presents a trial to compromise good characteristics of FPGA and wavelets through the development and implementation of on-line single-chip system for QRS detection and calculation of RR intervals (RRI) and HR. First, ECG signal is decomposed by Discrete Wavelet Transform (DWT) optimized in [3]. Then, QRS complexes are detected by technique based on modulus maxima and adaptive thresholding. Last, RRI and HR are calculated by counter circuits and sent out in a user defined format.

In the following text, the theoretical background, the system architecture and preliminary testing results are presented.

## II. DWT TRANSFORM AND QRS DETECTION

In practice, DWT is computed by passing the signal through a Low-Pass ($L_d$) and a High-Pass ($H_d$) filters successively according to the Mallat's decomposition scheme shown in Fig. 1 [5]. For each decomposition level $i$, $1 \le i \le N$, the $L_d$ and $H_d$ filters are followed by downsampling operator $\downarrow 2$ expressed as $(X \downarrow 2)[n]=X[2n]$, what is in fact the reduction of sampling rate by 2. $A_i(n)$ and $D_i(n)$ are approximation and detail coefficients for $i^{th}$ decomposition level. The coefficients for $L_d$, $H_d$, can vary from the simplest ones like Haar, over Daubechies up to those like Quadratic Spline, having different vector lengths and, usually, floating point interpretation. The

Haar wavelet is considered to be the simplest one where filters are of two elements wide.

Haar transform (HT) has a number of advantages; it is (i) conceptually simple, (ii) fast, (iii) memory efficient, since it can be calculated in a place without a temporary array. Also, it is reversible without the edge effect that can be a problem with some other WTs. But, this transform has several limitations, mainly in signal compression and noise removal from faster signals, which is not an issue in case of ECG. Like any other WT, the HT can be generalized to an integer to integer version. One technique is proposed in [3], where:

$$A_1[n] = \left\lfloor \frac{1}{2}X[2n] + \frac{1}{2}X[2n+1] \right\rfloor \quad (1)$$

$$D_1[n] = X[2n] - X[2n+1] \quad (2)$$

and $\lfloor\ \rfloor$ denotes rounding operator. As seen, the approximation and detail coefficients can be computed by simple arithmetic units like adder/subtractor and shifter, without multiplier, because $\lfloor x/2 \rfloor = x \gg 1$, where "$\gg$" is the right shift operator.

DWT is capable of distinguishing the QRS-complexes within ECG signal. The $D_i(n)$ coefficients across the scales show that the peak of the QRS complex, position of R wave, corresponds to the zero crossing (zc) between two modulus maxima within $D_i(n)$. Fig. 2 illustrates the decomposition of real discrete ECG signal $X(n)$ up to the 4th level, $D_1(n)$, $D_2(n)$, $D_3(n)$ and $D_4(n)$. For each decomposition level, the QRS complex produces two modulus maxima (min and max) with opposite signs, with a zc between. Thus, the problem of QRS detection translates to the problem of finding the occurrence of local min, zc and local max points. Energy of QRS complex mainly belongs to $D_3(n)$ and $D_4(n)$, while higher levels contain components produced by motion artifacts and baseline wandering. It means that three levels of decomposition, $D_1$, $D_2$ and $D_3$, are enough for QRS detection that is used in this project.

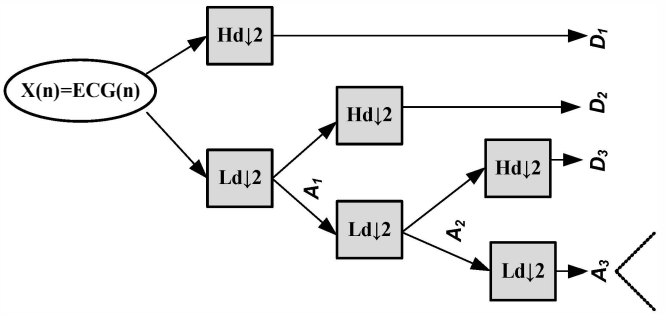


Figure 1. Mallat's decomposition scheme used for wavelet decomposition of ECG signal.

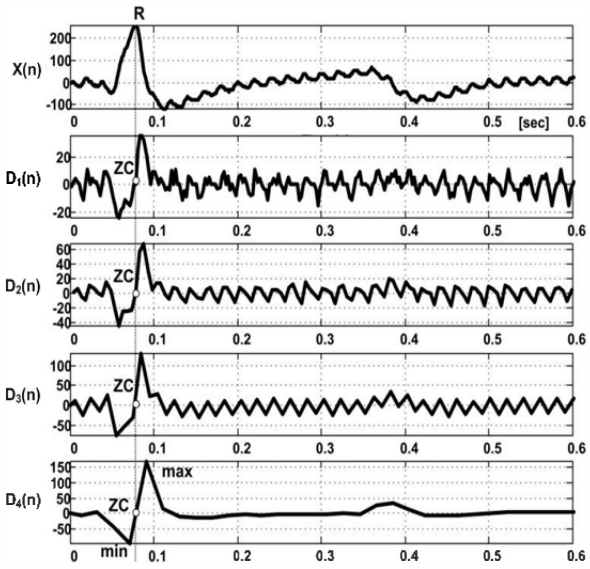


Figure 2. ECG signal and four levels of its Haar wavelet decomposition.

## III. FPGA IMPLEMENTATION

### A. System architecture

Block diagram of the overall system is given in Fig. 3. It consists of several modules and uses 50 MHz clock rate.

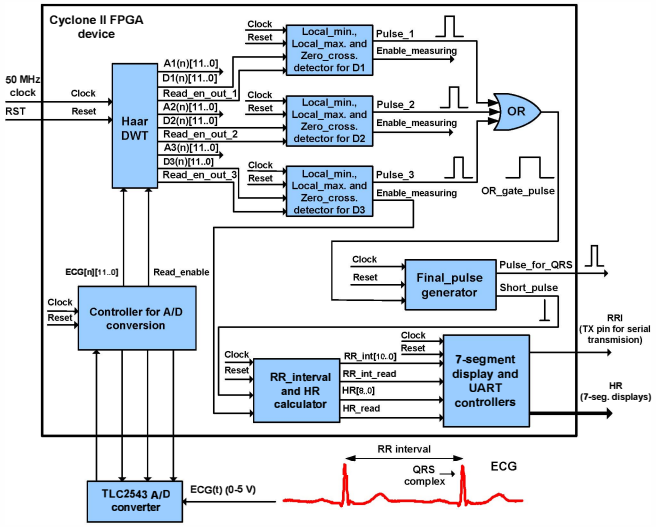


Figure 3. Block diagram of the system for feature extraction of ECG signal.

Analog signal $ECG(t)$ is digitalized by 12bit A/D convertor TLC2543 (TI) under sampling frequency of $f_s=800Hz$. The digital samples $ECG[n][11..0]$ are fed to the *Haar DWT* block whose outputs are details $D_i(n)[11..0]$ and approximations $A_i(n)[11..0]$, i=1..3. The detail coefficients, collected during 1s, from all levels, make arrays $D_1[NC_1...1][11...0]$, $D_2[NC_2...1][11...0]$ and $D_3[NC_3...1][11...0]$, $NC_i=1s*f_s/2^i$, $NC_1=400$, $NC_2=200$ and $NC_3=100$. Each of these arrays is then searched by module *Local_min., Local_max. and Zero_cross. detector* in order to find characteristic points, *local min, zc and local max.* In case

of their occurrence in true sequence, the *Pulse_i* is generated. Condition for successful detection of QRS complex is appearance of at least one *Pulse_i* at the inputs of OR gate. Afterwards, the *Final_pulse generator* produces a *Pulse_for_QRS* which is sent out of chip. Simultaneously, the *Short_pulse,* which represents the rising edge of *Pulse_for_QRS*, is forwarded to the module *RR_interval and HR calculator,* the outputs of which are 7-segment display bits (for HR) and serial communication signal (RRI).

### B. Local min, max and zero crossing

Each module *Local min, Local max and Zero-cross.* consists of 5 sub-modules: *Local_min. detector; Local_max. detector; Zero_cross. detector*; *State machine for QRS recognition* and *Pulse generator,* Fig. 4.

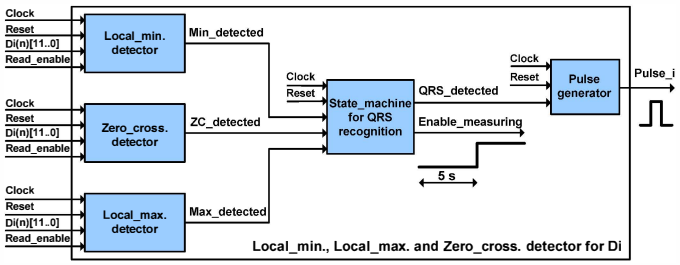


Figure 4. Block diagram of sub-system for detection of QRS complexes.

The architecture of *Local_min. detector* and *Local_max. detector* is almost the same, Fig. 5, following the logic from Fig.6. The difference is in operators "<" or ">", calculation procedures for adaptive thresholds "$T_{ni}$", "$T_{pi}$" and decision rules for detecting local min and local max, signals *Min_detected*, *Max_detected.*

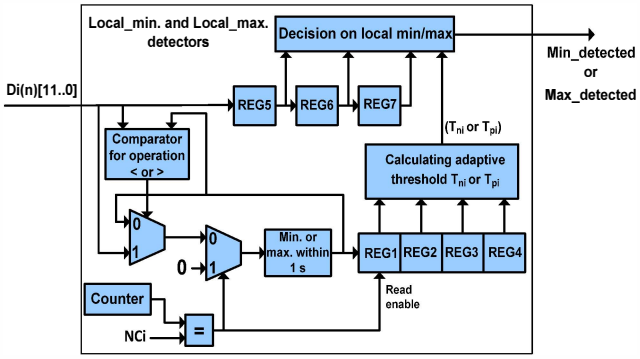


Figure 5. Architecture of hardware for finding modulus maxima in DWT.

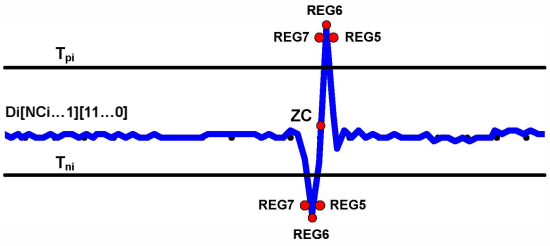


Figure 6. DWT of ECG with $T_{pi}$ and $T_{ni}$ thresholds for finding modulus maxima.

The positive and negative thresholds are adapted by:

$$T_{pi} = \frac{5}{8} AV_{i+},\ T_{ni} = \frac{5}{8} AV_{i-} \quad (3)$$

where $AV_{i+}$ and $AV_{i-}$ present the mean values of the four successive max/min values, collected during 4 seconds, previously stored in registers *REG1*, *REG2*, *REG3* and *REG4*,

$$AV_{i+} = \frac{1}{4}\sum_{k=1}^{n} \max(D_i[k][NC_i..1][11..0]) \quad (4)$$

$$AV_{i-} = \frac{1}{4}\sum_{k=1}^{n} \min(D_i[k][NC_i..1][11..0]) \quad (5)$$

where $D_i[k][NC_i..1][11..0]$ are details in k[th] second, k=1..4. Decision on local min/max is based on the contents of three registers *REG5*, *REG6* and *REG7* and adaptive thresholds $T_{pi}$ or $T_{ni.}$ In distinction to *REG1..REG4, REG5,* registers *REG6* and *REG7* contains three successive points $D_i(n)[11..0]$, $D_i(n-1)[11..0]$ and $D_i(n-2)[11..0]$. The decision rules are as following:

$$If\ (REG7 < REG6)\ and\ (REG6 > T_{pi})\ and\ (REG5 < REG6)\ then\ Local\_max = REG6 \quad (6)$$

$$If\ (REG7 > REG6)\ and\ (REG6 < T_{ni})\ and\ (REG5 > REG6)\ then\ Local\_min = REG6 \quad (7)$$

Fig. 7 shows a block diagram of zero-crossing circuit that works under principle $D_i(n)[11..0]>0$ and $D_i(n-1)[11..0]<0$. It is the same for all decomposition levels and only sign bits are compared.

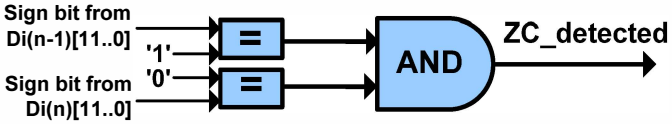


Figure 7. Block diagram of circuit for detection of zero-crossings in DWT.

### C. QRS recognition

QRS recognition is carried out using a state machine whose combinational inputs are *Min_detected*, *ZC_detected* and *Max_detected*. State machine has four states, Fig. 8, and the initial state is state of initial adaptation of the QRS detector, after powering-up. The initial state lasts for 5 seconds and it serves for initial suiting of the adaptive thresholds, because of loading of registers *REG1*, *REG2*, *REG3* and *REG4*. In the process of adaptation the quest for the QRS complex is not done, and the output signals *QRS_detected* and *Enable_measuring* are at low. After initial adaptation, the signal *Enable_measuring* becomes high and process of QRS detection begin. From the initial adaptation state, a state machine goes to the state in which the local minimum of $D_i$ is expected, state-*Local minimum search*. When high level appears to the input of the state machine that is connected to the circuit for local minimum detection, the machine switches to state for searching zero-crossing, state-*Zero crossing search*, and after crossing zero, the state machine switches to the search for a local maximum of $D_i$, state-*Local maximum search*. Detection of QRS complex is

successful if local max is detected after local min and zc. Then *QRS_detected* synchronized output is generated.

*QRS_detected* from the state machine is fed to the *Pulse_generator*, which generates *Pulse_i* of 30 ms duration. *Pulse_1*, *Pulse_2* and *Pulse_3* are passing through the OR gate creating *OR_gate_pulse* which is in fact the overlapped summation. *OR_gate_pulse* is fed to the *Final_pulse generator* which produces *Pulse_for_QRS* of 20 ms duration. *Pulse_for_QRS* happens only if between two sequent *OR_gate_pulses* passed 200 ms that is considered as down physiological limit for *RR* interval. Simultaneously with *Pulse_for_QRS* this circuit generates *Short_pulse* of one clock duration, which is forwarded to RRI and HR calculators.

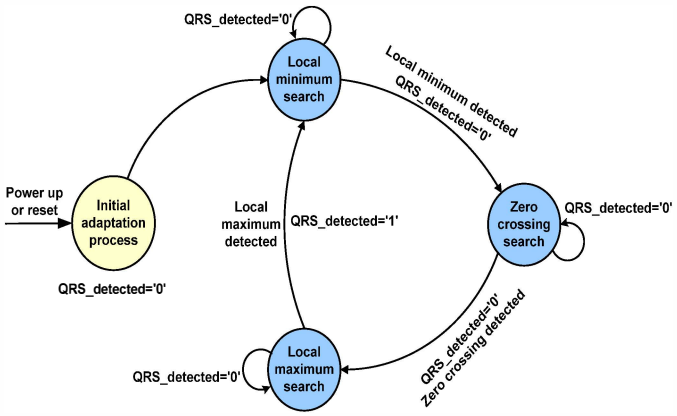


Figure 8. State machine for detection of QRS complexes.

## D. Calculating RRI and HR

The circuit for RRI and HR calculation consists of four counters (*C1*, *C2*, *C3* and *C4*), two latch registers and one shifer, Fig. 9. It starts after initial adaptation, when signal *Enable_measuring* is high. Output *RR_int[10..0]* gives binary equivalent of RR intervals in ms, while *HR[8..0]* gives beats per min. *C2* is clocked each 1 ms using overflow *(of.)* of *C1,* and latched by *Short_pulse.* C4 is clocked by *Short_pulse* and latched each 15 s using *C3's* overflow. The final *HR* in beats per minute is obtained by left shifting "<<2", that is in fact "x4", 60s=15x4s.

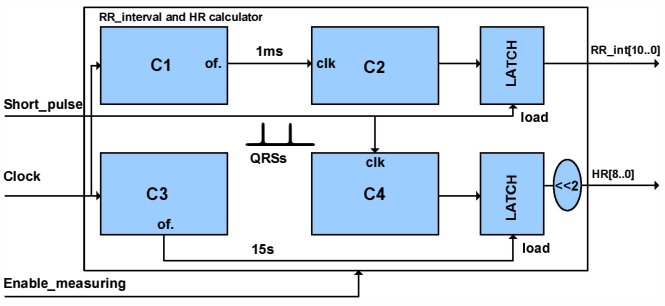


Figure 9. Architecture of RR_interval and HR calculator.

## IV. Testing and Results

Designed system was implemented on Cyclone II FPGA chip EP2C70F896C6N [6]. All modules, functions and routines are implemented in VHDL. Prototyping and testing was performed on-line using Altera's DE2-70 development board. TLC2543 A/D converter from TI is employed for digitizing ECG signals. RR intervals were transferred out via serial port, while HR values are observed by 7-segment displays.

The records from the MIT-BIH Arrhythmia Database [7] were used to test the system. These records represent different heart rhythms, and contain variety of waveforms and artifacts that ECG feature extractor might encounter in everyday clinical practice. The signals are applied directly to the designed system, without prior filtering for noise removal or stabilization in term of base line.

Only feature extractor occupies 1459 LEs of FPGA chip. Together with A/D controller, RS232 serial communication module and 7-segment display module, it is 1838 LEs, that is 2.68% of EP2C70F896C6N chip capacity.

Fig. 10 shows the oscilographs of ECG signals and digital pulses at output of the QRS detector, at the pin of the FPGA chip, *Pulse_for_QRS*. Fig. 10 (b) shows the result of the detection for signal affected by noise and baseline wandering. As seen, the designed system has good characteristics in noise environment.

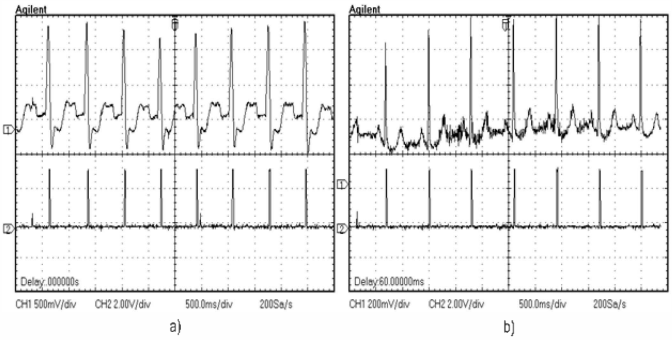


Figure 10. ECG signals and pulses that indicate detections of QRS complexes.

There is some delay in the detection of QRS complexes, because of the algorithm, Fig. 11. After the detection of local minimum and zero-crossing, the system should detect the local maximum and then to decide. The result of QRS detection at three levels of decomposition is shown in Fig. 11 (a), *Pulse_1, Pulse_2 and Pulse_3*, while Fig. 11 (b) shows *Pulse_for_QRS*. The delay in the detection of QRS complex for ECG signal in Fig. 11 (b) is about 16 ms.

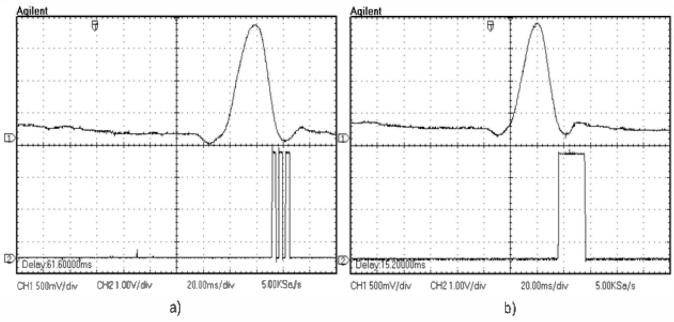


Figure 11. QRS complex, individual pulses (a) and cumulative pulse (b) for its indication.

The results of the detection of QRS complexes in 10 half-hour recordings from the MIT-BIH Arrhythmia database are summarized in Table I. Test of QRS detector lasted for five hours. Testing was conducted on a total of TB=22031 beats, where there were FP=105 false detections and FN=424 missed detections. Using the formula ACC[%]=100(1-(FP+FN)/TB), for every of the records, the average accuracy of the QRS detector is $ACC_{av}$=97.53%. It may be noted that the detection results vary for different signals.

RR intervals, calculated by FPGA chip, for all 10 signals reproduced from the MIT-BIH Arrhythmia Database were recorded in *. Txt files using computer. The same signals were previously analyzed using the National Instrument's (NI) Biomedical Workbench PC software [8]. Comparison of results obtained using NI's software and the results achieved by the designed FPGA system for record no. 103 is given in Fig. 12. It is obvious that the results match quite well. Missed detections of the QRS complexes can be identified as three prolonged intervals on the graph of RR intervals measured by the FPGA chip in Fig. 12 (b), compared with the corresponding intervals in graph for NI's software in Fig. 12 (a). Achieved false detections of QRS complexes, which did not occur for record no. 103., would be recognized by the appearance of RR intervals whose values are less than the intervals computed in computer software.

TABLE I. RESULTS OF REAL-TIME TESTING OF QRS DETECTOR

| Record no. | TB | FP | FN | ACC (%) |
|---|---|---|---|---|
| 100 | 2273 | 0 | 1 | 99.95 |
| 101 | 1865 | 4 | 9 | 99.30 |
| 102 | 2187 | 3 | 39 | 98.07 |
| 103 | 2084 | 0 | 3 | 99.85 |
| 104 | 2230 | 48 | 121 | 92.42 |
| 105 | 2572 | 19 | 15 | 98.67 |
| 106 | 2027 | 0 | 211 | 89.59 |
| 107 | 2137 | 8 | 14 | 98.97 |
| 109 | 2532 | 7 | 5 | 99.52 |
| 111 | 2124 | 16 | 6 | 98.96 |

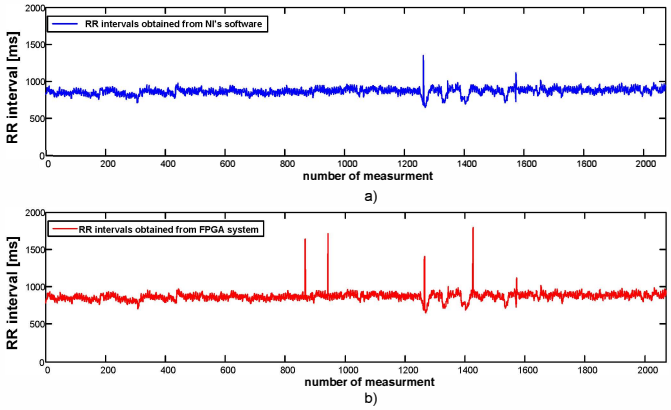


Figure 12. Values of RR intervals, calculated with NI's Biomedical Workbench software (a), in comparison with values obtained from FPGA feature extractor in real-time (b).

## V. CONCLUSION

A system and methodology for on-line QRS detection and RR interval and heart rate calculation are presented. All tasks are implemented in single FPGA chip. The system is imune on various noise, achieving accuracy of more than 97% behind low occupation of silicium resources. As such, system is ideal for embeded systems or wearable health care devices.

## ACKNOWLEDGMENT

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