A Dual-Sensing Thermo-Chemical ISFET Array for DNA-Based Diagnostics

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***Abstract*—This paper presents a 32x32 ISFET array with in-pixel dual-sensing and programmability targeted for on-chip DNA amplification detection. The pixel architecture provides thermal and chemical sensing by encoding temperature and ion activity in a single output PWM, modulating its frequency and its duty cycle respectively. Each pixel is composed of an ISFET-based differential linear OTA and a 2-stage sawtooth oscillator. The operating point and characteristic response of the pixel can be programmed, enabling trapped charge compensation and enhancing the versatility and adaptability of the architecture. Fabricated in 0.18μm standard CMOS process, the system demonstrates a quadratic thermal response and a highly linear pH sensitivity, with a trapped charge compensation scheme able to calibrate 99.5% of the pixels in the target range, achieving a homogeneous response across the array. Furthermore, the sensing scheme is robust against process variations and can operate under various supply conditions. Finally, the architecture suitability for on-chip DNA amplification detection is proven by performing Loop-mediated Isothermal Amplification (LAMP) of phage lambda DNA, obtaining a time-to-positive of 7.71 minutes with results comparable to commercial qPCR instruments. This architecture represents the first in-pixel dual thermo-chemical sensing in ISFET arrays for Lab-on-a-Chip diagnostics.**

***Index Terms*—ISFET, Dual Sensing, Lab-on-a-Chip, Point-Of-Care Diagnostics, Duty Cycle Modulation, Frequency Modulation, DNA Amplification**

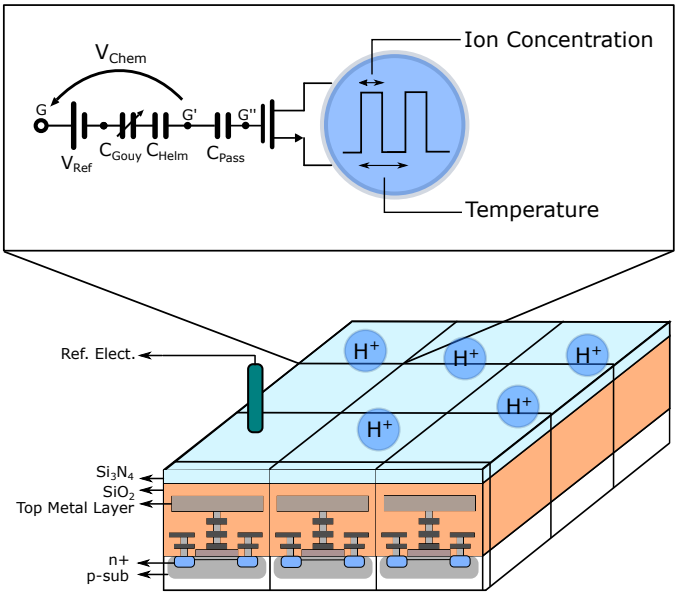

Fig. 1: 3D model and cross section of ISFET array. Detail presents CMOS-Based ISFET macromodel connected Dual-Sensing Front-End

I. Introduction

THE superior performance of CMOS-based biosensors in terms of cost, size and miniaturization has enabled the development of a wide range of Lab-on-a-Chip (LoC) devices for biomedical applications, integrating sensor, instrumentation and post-processing on a single die [1]. These LoC platforms are shifting the current health-care paradigm, moving the patient diagnosis from centralised laboratories to the Point-of-Care (PoC).

The Ion-Sensitive Field Effect Transistor (ISFET), a biosensor capable of detecting changes in pH, is one of the most successful biosensors for the realisation of PoC diagnosis devices. Leveraging on its standard CMOS implementation [2], ISFETs achieve low cost, compact form factor and monolithic nature, catalysing the development of a wide range of ISFET-based LoC platforms. These applications range from multi-ion detection [3]–[5], where different electrolytes on a solutions are analysed; to DNA based amplification detection, with implications on rapid diagnosis of infectious diseases [6]–[8]; as well as pH-based DNA methylation detection for epigenetic monitoring [9], [10].

Despite the rapid development of ISFET applications, these sensors face several challenges to enable its integration as part of Point-of-Care platforms. Firstly, the fabrication of ISFET arrays on standard CMOS processes introduces a set of non-idealities that limit the performance of the sensor, requiring either compensation or mitigation of these effects. During this fabrication process, charges get trapped between the different passivation layers, creating pixel-to-pixel mismatch in array-based ISFET platforms. This phenomena, known as ”trapped charge”, requires pixel-wise calibration to achieve an homogeneous chemical image. Furthermore, the poor quality of the pH sensitive Si_3N_4 passivation layer creates a monotonic drift at the output, and the capacitive division formed by the Si_3N_4 and SiO_2 layers leads to the attenuation of the input chemical signal. Overall, these phenomena reduces ISFET pH resolution and set challenging requirements on subsequent

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instrumentation [11].

Secondly, DNA-based diagnostic applications of ISFET platforms are based on thermally sensitive protocols, such as Loop-mediated Isothermal Amplification (LAMP) [12]. These protocols require precise thermal control to enable robust and reliable amplification results. This thermal control have been previously realised using benchtop equipment [7], on-chip heaters [13] and Peltier modules [6]. These heating elements require accurate temperature information in real-time to enable precise close-loop temperature control. The solution temperature is measured using external thermal sensors or dedicated on-chip temperature pixels at the chip surface [6], [7]. This last approach is suitable for portable applications and provides local thermal information at the expense of chemical spatial resolution and transmission bandwidth.

Finally, the need for portability has catalysed the use of power harvesting techniques and battery solutions to achieve autonomous operation [5]. However, these supply schemes require reduced power consumption as well as robust sensing under various supply conditions. ISFET sensing topologies have so far been based on single-ended front-ends, whose performance is highly dependent on an specific supply level [14].

The architecture proposed in this paper overcomes these key limitations through a robust and fully-differential dual-sensing ISFET front-end capable of encoding temperature and ion activity in the same output PWM signal. The thermal information at the chip surface is modulated into the frequency of the output signal, enabling temperature sensing without sacrificing spatial resolution. The chemical information, encoded into the duty cycle on a PWM signal, leverage on the pixel's differential approach to achieve low sensitivity to process variations and operation at different supplies, while exploiting the proven benefits of oscillator-based architectures in terms of programmability and scalability [15], [16] to compensate for ISFET non-idealites and enhance the flexibility and versatility of the pixel.

The proposed architecture merges for the first time both temperature and chemical sensing in the same pixel, while providing a robust sensing scheme where non-idealities and external factors are either mitigated or compensated through programmable terminals. The paper is structured as follows: Section II covers the ISFET's principle of operation and its main challenges faced on its implementation in unmodified CMOS. In Section III the proposed pixel architecture is explained, describing its principle of operation and detailing the design considerations. The pixel architecture is integrated into the wider system described in Section IV. The fabricated system and testbench is described in Section V, and the measured results obtained are reported in Sections VI and VII. This architecture is applied to DNA amplification detection, as described in Section VIII. Finally, a summary of the achievements and a comparison with the state-of-the-art is provided in Section IX.

II. ISFET Overview

The Ion-Sensitive Field-Effect Transistor (ISFET) [17] can be thought as an standard MOS transistor that detects variations on the charge density at its gate due to changes on the ion concentration of a solution. This is achieved by removing the standard gate connection and replacing it by a Ag/AgCl reference electrode immersed in the target solution. The potential of this electrode is coupled through the solution and an ion-sensitive insulating layer to the floating gate, setting the operation point of the device.

Figure 1 exemplifies an array-based ISFET fabricated in unmodified CMOS processes [2]. Leveraging on the intrinsic pH sensitivity of the standard Si_3N_4 passivation layer, the $[H^+]$ concentration modulates the potential sensed by the floating gate. This modulation is modelled as a shift in the threshold voltage of the MOS device, which is mathematically expressed as follows:

$$V_{th_{ISFET}} = V_{th_{MOSFET}} + V_{chem} \tag{1}$$

$$V_{chem} = \gamma + \alpha S_N pH \tag{2}$$

where V_{chem} groups the potentials generated by chemical contributions. In Eq. 2, γ is a constant solution-dependent term and S_N is the ideal Nernstian sensitivity, approximately 59 mV/pH at ambient temperature, attenuated by α, a parameter ranging from 0 to 1.

Several non-idealities are introduced during the ISFET fabrication in standard CMOS technology, limiting the sensor performance and imposing strict requirements to ISFET instrumentation and post-processing steps. These phenomena, such as capacitive attenuation, trapped charge or monotonic drift, have been the main focus of the recent literature, exploring both sensor adaptation and system compensation schemes [11].

III. Pixel Architecture

The benefits of the Oscillator-based approach have been widely examined and demonstrated across the literature [15], [16], [18], [19], providing scalability, linearity, robust measurement against process variations and programmable sensor response. In this paper, the benefits are expanded by proposing a compact 2-stage Sawtooth Oscillator capable of sensing and encoding both ion concentration and solution temperature into a single PWM output signal, achieving dual-sensing thermo-chemical measurement. This PWM signal has two modulated variables: the ion concentration sensed by the ISFET is encoded into the duty cycle, leveraging on a differential sensing approach to achieve robustness, linearity and programmability; and the solution temperature is modulated onto the frequency of the PWM signal, benefiting from large dynamics and quadratic sensitivity. The modulation mechanisms of each sensing schemes as part of the Sawtooth Oscillator are now analyzed in detail.

A. Chemical Sensing

The presented architecture, illustrated in Figure 2, encodes the ion information sensed by the ISFET into the duty cycle of a PWM signal. This sensing scheme is composed by two sub-blocks:

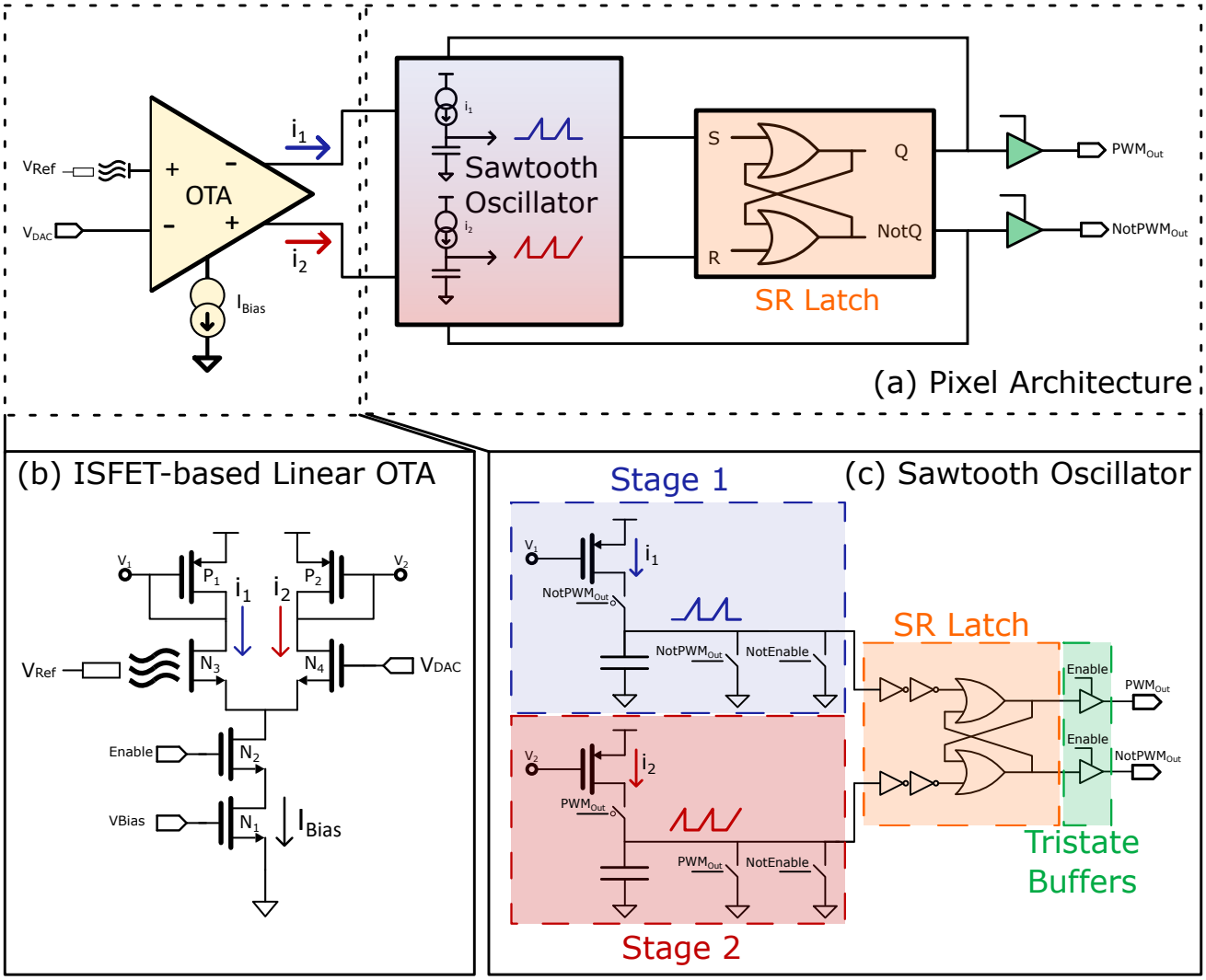


Fig. 2: Sawtooth Oscillator High Level Schematic showing (a) Overall pixel structure, composed by (b) ISFET-based Linear OTA transforming input differential voltages V_{ISFET} and V_{DAC} into differential currents i_1 & i_2 which will be mirrored to (c) 2-Stage Sawtooth Oscillator, creating a PWM signal from the mirrored currents i_1 & i_2 by charging capacitors alternatively

1) ISFET-based Linear OTA: The ISFET-Based Linear OTA creates a differential output current from a differential input voltage. An ISFET replaces one of the MOSFET at the differential pair, providing pH sensitivity, while the second branch is biased through an off-pixel voltage, V_{DAC}. When this differential pair is operating at the linear region, any variation at the ISFET gate would trigger a change in the differential currents i_1 and i_2. Assuming the differential pair is matched ($g_{m3} = g_{m4} = g_m$), these current differences can be described as Eq. 3 and 4:

$$I_{Bias} = i_1 + i_2 \tag{3}$$

$$i_1 - i_2 = \frac{g_m}{2}(V_{ISFET}(pH) - V_{DAC}) \tag{4}$$

where $V_{ISFET}(pH) = V_{g''}$ and $g_m \propto I_{Bias}$ for a constant V_{ov}. From Eq. 3 and 4, it is derived two externally programmable parameters that can tune the sensor's behaviour:

- I_{Bias} controls the linear range and the sensitivity. This current can be set using an external current source or a biasing voltage.
- V_{DAC} sets the equilibrium point of the linear OTA

This programmability is simulated to confirm the equations. Figure 3 presents simulated data of the evolution of i_1 with any difference between V_{ISFET} and V_{DAC}. The differential currents generated in this stage are mirrored to the sawtooth oscillator, modulating its PWM response.

2) 2-stage Sawtooth Oscillator: Sawtooth Oscillators are a type of relaxation oscillator which creates a PWM waveform by charging alternatively two capacitor [20], [21]. These oscillators, previously used for sensing purposes in [15], [16], [21], [22], are known for exhibiting high linearity control and low jitter.

To chemically modulate the oscillator's duty cycle, the capacitor at each stage is charged linearly by the differential currents generated on the ISFET-Based OTA, being only one capacitor charging at a time. When the charging capacitor

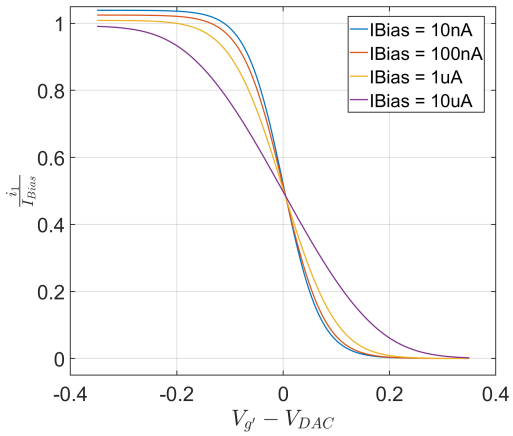


Fig. 3: Simulation of linear OTA current under different biasing conditions

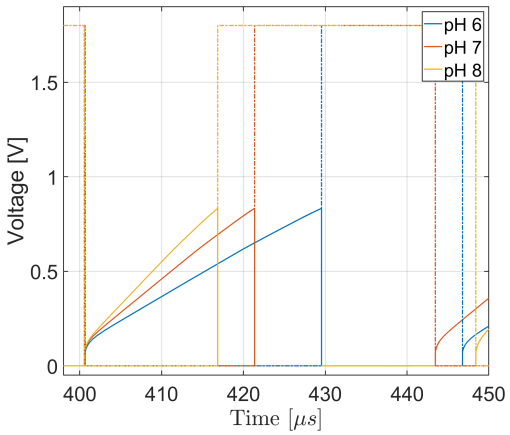


Fig. 4: Simulation of Sawtooth Oscillator under different pH conditions, assuming a sensing layer sensitivity of 30 mV/pH and $I_{Bias} = 10nA$

reaches the inverter threshold voltage, the SR latch toggles the oscillator polarity, inverting the charging process: the previous capacitor is discharged and the second capacitor starts accepting current. This charging process creates a delay on each stage defined by:

$$T_{charge} \propto \frac{V_{th_{Inv}} \cdot C}{I(pH, V_{DAC})} \tag{5}$$

being $V_{th_{Inv}}$ the inverter threshold voltage, C the value of the stage's capacitor and I the current fed into the stage, either i_1 or i_2. From T_{charge}, the duty cycle is defined as follows:

$$PWM_{DutyCycle} = \frac{T_{charge_{S2}}}{T_{charge_{S1}} + T_{charge_{S2}}} \tag{6}$$

$$PWM_{DutyCycle} \propto \frac{i_1}{i_1 + i_2} \tag{7}$$

Eq. 7 shows that any difference between these differential currents i_1 and i_2 creates a difference in the delay time of each stage, hence modulating the duty cycle of the output PWM signal. Figure 4 presents a simulation of this phenomena, showing both the charging waveforms and the generated PWM signal.

B. Thermal Sensing

Each pixel encodes its local temperature into the frequency of the output PWM signal, obtaining spatial information of the distribution of temperatures across the array. This frequency modulation scheme leverages on the thermal sensitivity of N1 when operated on weak inversion region, creating a variation on the biasing current that increases the oscillator frequency. This biasing current thermal sensitivity can be modelled as follows [23]:

$$I_{d_{sub}}(T) = I_0(T) \exp \frac{V_{gs} - V_{th}(T)}{nkT/q} \left(1 - \exp \frac{-V_{ds}}{kT/q}\right) \tag{8}$$

where $I_0(T)$ is a technology specific parameter with a thermal dependency expressed in Eq.9, and V_{th} is the thermally controlled threshold voltage as shown in Eq.10.

$$I_0(T) = \mu_0 C_{ox} \frac{W}{L} e^{1.8} (kT/q)^2 \tag{9}$$

where μ_0 is the zero bias carrier mobility, C_{ox} the gate oxide capacitance and W and L the transistor sizes.

$$V_{th}(T) = V_{th0} + \left(K_1 + \frac{K_2}{L} + K_3 V_{bs}\right)\left(\frac{T}{T_0} - 1\right) \tag{10}$$

where V_{th0} refers to the threshold at T_0, K_1 is the temperature coefficient of the threshold voltage, K_2 is the channel-length coefficient of the threshold voltage, K_3 is the bulk-bias coefficient of the threshold voltage and V_{bs} is the bulk-source potential.

Assuming that $V_{ds} > 4U_t$, the thermal dependency of the biasing current can be simplified to:

$$I_{d_{sub}}(T) = K_\alpha T^2 \exp \frac{-K_\beta}{T} \tag{11}$$

with K_α and K_β defined as:

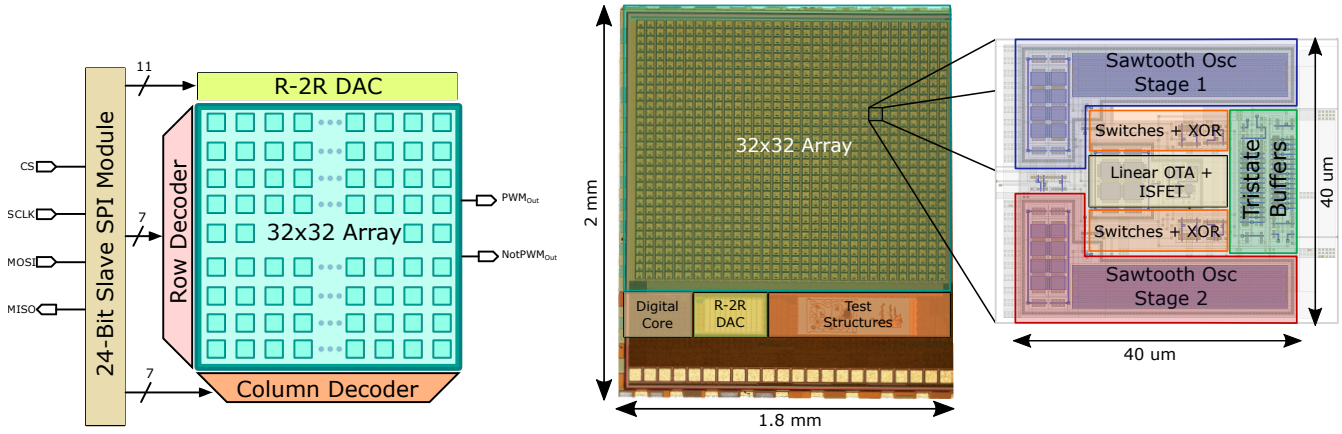
$$K_\alpha = \frac{\mu_0 C_{ox} \frac{W}{L} e^{1.8} \left(\frac{k}{q}\right)^2}{\exp \frac{K_1 + \frac{K_2}{L} + K_3 V_{bs}}{T_0 nk/q}} \tag{12}$$

$$K_\beta = \frac{-V_{gs} + V_{th0} - K_1 - \frac{K_2}{L} - K_3 V_{bs}}{nk/q} \tag{13}$$

This relationship is complex and includes several quadratic and exponential terms. However, as discussed on Section VII, the transfer function can be later approximated as a quadratic relationship for the input range of our application.

IV. System-Level Architecture

The pixel architecture is integrated into a system is composed by 3 blocks, described hereafter.



(a) System Diagram

(b) Chip Microphotograph & Pixel Layout

Fig. 5: System Architecture illustrating (a) the high level system architecture, presenting the different blocks and their interconnections with the 32x32 array, and (b) silicon prototype of this system, with the detail portraying the pixel layout and its internal structure.

A. ISFET Array

A 32x32 ISFET array is created using the pixels presented in Section III. Each pixel contains under its active area a linear OTA, two current mirrors, a two 31x4μm^2 capacitors yielding 65fF each, control switches, a SR latch and tristate buffers. The pixels are uniquely addressed using Row and Column signals, activating only one pixel at a time. All pixels share a global V_{DAC} input and the PWM_{Out} & $NotPWM_{Out}$ datapath, as illustrated in Figure 5a. In-pixel tristate buffers performs the output datapath control, allowing only one pixel to transmit.

B. On-Chip DAC

A global on-chip R-2R 11-bit DAC enables pixel-wise programmability of operation point by generating a V_{DAC} signal. The DAC input code is generated externally and transmitted though SPI. This value can be tailored for each pixel to compensate for trapped charge and other non-idealities. Global DAC approach was selected over column-, block- or pixel-wise DAC to maximise ISFET sensing area, as multiple DAC blocks would require large silicon area, additional digital circuitry and multiple IO pads for parallel readout.

C. SPI Interface and Row/Column Decoders

A 24-bit slave SPI unit is included as an standard interface with external devices. The SPI message provides the digital code for the aforementioned DAC (V_{DAC}) and selects a target pixel through Row and Column decoders.

V. Fabricated System

This section describes the test elements used to obtain the results presented in Sections VI & VII, as well as the resources and algorithms employed.

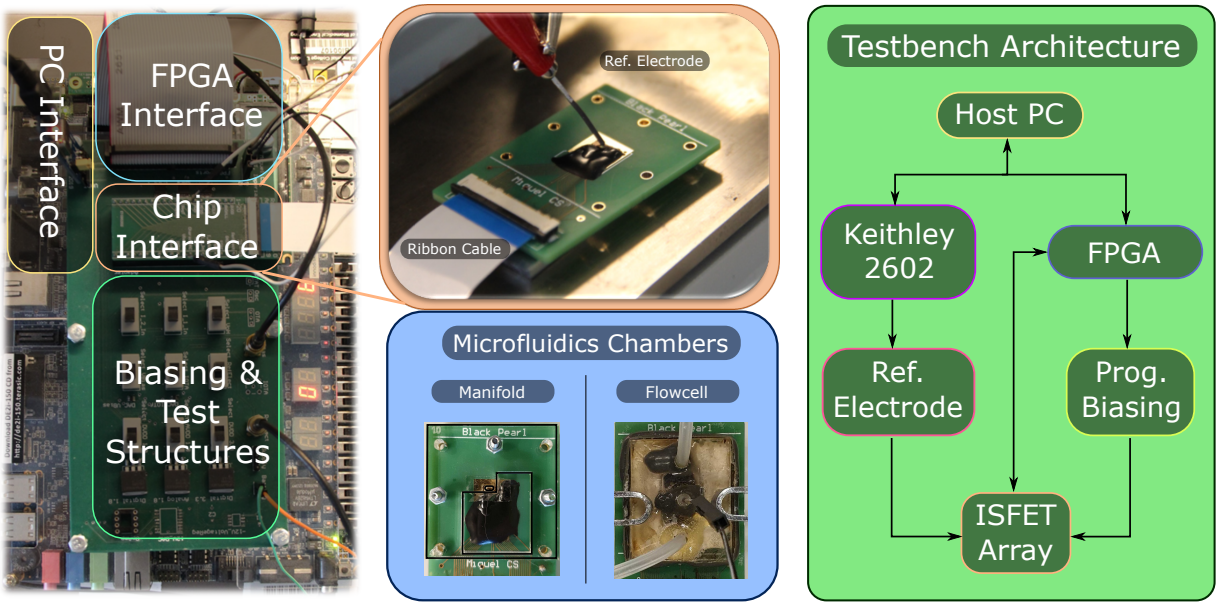
A. Silicon Prototype & Testing Platform

The chip was fabricated in TSMC 0.18μm M6 CMOS technology, using its standard passivation (Si_3N_4) for pH sensing layer. The entire system occupies 1.8x2mm^2, where each pixel occupies 40x40 μm^2 with matching active area. In order to shield this active area from the oscillatory behaviour, a M4 layer connected to ground is introduced. A microphotograph of the silicon prototype is shown in Figure 5b, where all relevant blocks are highlighted.

The testing platform built to characterize the silicon prototype performance is composed by 5 elements.

- **Cartridge** ⇒ A compact cartridge is designed to interconnect the silicon prototype to the testing platform, as presented in Figure 6a. The chip is attached to the ground plane using conductive epoxy (EPO-TEK H20E), and all bond-pads are covered using electrically insulating epoxy (EPO-TEK T7139). The cartridge is connected to a testing platform through a ribbon cable.
- **Testbench PCB** ⇒ The testing PCB handles the powering, biasing and communication between the control devices and the silicon prototype.
- **FPGA Platform** ⇒ The FPGA Development Platform terasIC DE2i-150 handles the SPI communication with the cartridge platform and the sampling and digitization of the output PWM signal. Furthermore, the FPGA platform stores in memory the DAC values required for the pixel-wise calibration, allowing trapped charge compensation and drift cancellation. The FPGA system is connected to the host PC through a serial interface, executing pre-programmed actions upon PC request.
- **Keithley 2602** ⇒ The Keithley, controlled by the Host PC, provides the Ag/AgCl reference electrode potential.
- **Host PC** ⇒ The Host PC provides a MatLab-based user interface that coordinates the different tests, display the status of the experiments and stores its results.

Figure 6b illustrates the architecture and the communications interfaces required for this platform to operate.



(a) Test-bench platform for system characterization

(b) Test-bench architecture

Fig. 6: Measurement setup for characterisation of silicon prototype. (a) Motherboard architecture, with details on chip interface and microfluidic chambers utilised. (b) Communication structure between different testbench blocks

B. Microfluidic Components

Three strategies have been followed to enable solution compartment during experimentation.

- The first and simplest, presented in the top right of Figure 6a, consist on placing a small sample of the solution on the surface of the chip. However, this strategy was only valid for initial functionality verification as the sample quickly evaporates.
- A acrylic manifold is utilized as reaction chamber, preventing sample leakage and evaporation, as well as ensuring consistent testing conditions across experiments. The manifold is screwed to the cartridge, exposing only a reduced chip area and holding a reaction volume of $4.41\mu L$.
- A flowcell is designed to perform sequential flow of different pH buffers, enabling the verification of the architecture pH sensitivity. This flowcell is attached to the cartridge using fixing clamps, and the reference electrode is inserted through middle opening.

These two microfluidic devices are presented in Figure 6a.

C. Buffer preparation

In order to assess the pH sensitivity of the architecture, a set of pH buffers (6, 7 & 8) are prepared. Firstly, a background solution is initially prepared with 1M Tricine (Sigma Aldrich T0377), 3M KCl (Sigma Aldrich 60137) and de-ionised water. The pH of this background solution is adjusted by adding either 1M HCl (Sigma Aldrich 318949) or 1M NaOH (Sigma Aldrich 71463), monitoring the exact pH value using Sentron SI400 pH meter.

D. Temperature Characterization & Control

The temperature of the platform is regulated using a Veriti 96-Well Thermal Cycler (Applied Biosystems). This enables precise temperature control required to evaluate the sensor performance under different thermal conditions, as well as to perform LAMP DNA amplification experiments described in Section VIII.

VI. Experimental Results: Chemical Sensor

This section presents the results obtained from the electrical and chemical characterization of the ISFET. Unless stated, these experiments were performed under $I_{Bias} = 10nA$.

A. Characteristic Response Analysis

The ISFET array characterization analysis are obtained by immersing the Ag/AgCl reference electrode into a pH 7 solution and sweeping its potential throughout the sensing range, while maintaining V_{DAC} at a constant voltage. By observing the output change to this reference electrode sweep for each pixel, the Input Range, Electrical Sensitivity, Linearity and Trapped charge across the array can be evaluated. An example of the duty cycle response obtained on each pixel is presented in Figure 7, defining the linear range between 15% and 85%. From this curve, the pixel parameters can be obtained following equations 14, 15 & 16.

$$InputRange = max(Ref.Elect.) - min(Ref.Elect.) \quad (14)$$

$$S_{Elect} = \frac{max(PWM) - min(PWM)}{max(Ref.Elect.) - min(Ref.Elect.)} \quad (15)$$

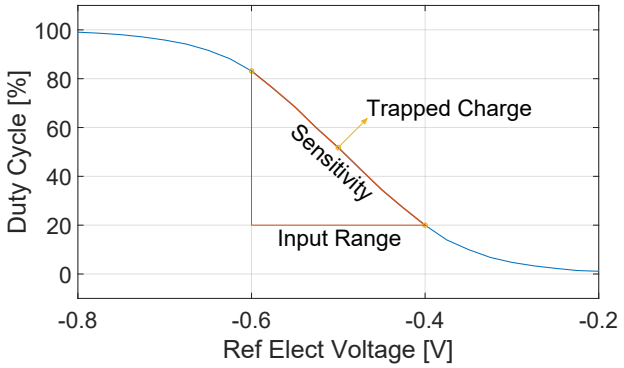
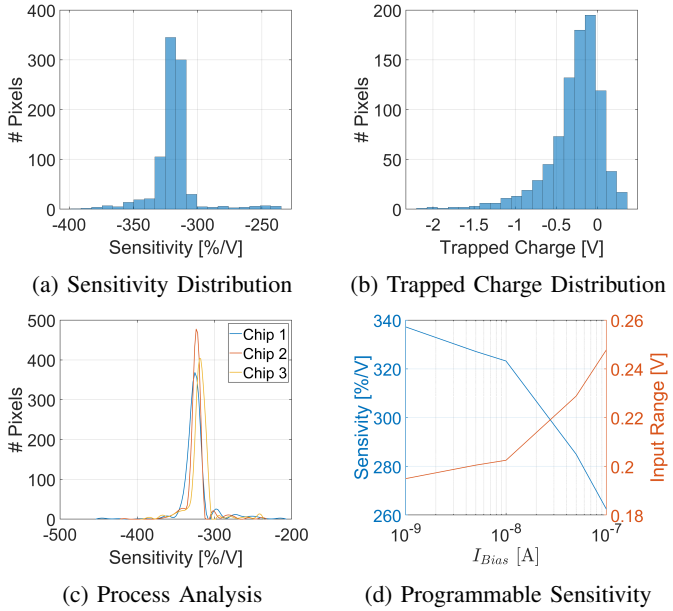


Fig. 7: Pixel Characterisation Curve

$$TrappedCharge = Ref.Elect.(PWM = 50\%) \quad (16)$$

The distribution of sensitivities and trapped charge across the array are provided in Figure 8a & 8b, and Table I summarizes the mean value of the parameters along with the standard deviation between pixels. The small values of standard deviation on sensitivity and linearity prove the robustness of this architecture, achieving an homogeneous and highly linear characteristic response across the array. The distribution of trapped charge is in line with previously reported values in the literature [6], [24]



(a) Sensitivity Distribution (b) Trapped Charge Distribution

(c) Process Analysis (d) Programmable Sensitivity

Fig. 8: Characterization Analysis obtained from pixel characterisation curves, extracting (a) Sensitivity distribution across the array, (b) Trapped Charge distribution and (c) Sensitivity distribution for 3 different chips. Figure (d) shows the programmability of this architecture and the associated trade-off between input range and sensitivity

1) Effect of Process Variations: The characterization experiment is replicated for different chips to evaluate the effect of process variations on the architecture. Figure 8c presents these results, demonstrating the robustness against fabrication mismatches.

TABLE I: Characterization Results

Parameter	Mean	Std. Dev.
S_{Elect} [%/V]	321.65	0.1754
Range [V]	0.2025	0.019
Linearity [R^2]	0.9986	0.0037
Trapped Charge [V]	-1.299	1.01

2) Programmable Sensitivity: As described in Section III-A, I_{Bias} tunes the linear range and the sensitivity of the architecture. This was tested by observing the characterization curves for different I_{Bias} values, obtaining the results presented in Figure 8d. A trade-off between range and sensitivity is observed: higher I_{Bias} achieve larger input range by decreasing the sensitivity and viceversa. Furthermore, an increase on I_{Bias} will also have an effect on the oscillation frequency, which in turn has a negative impact on the Over-Sampling Ratio.

B. Attenuation Analysis

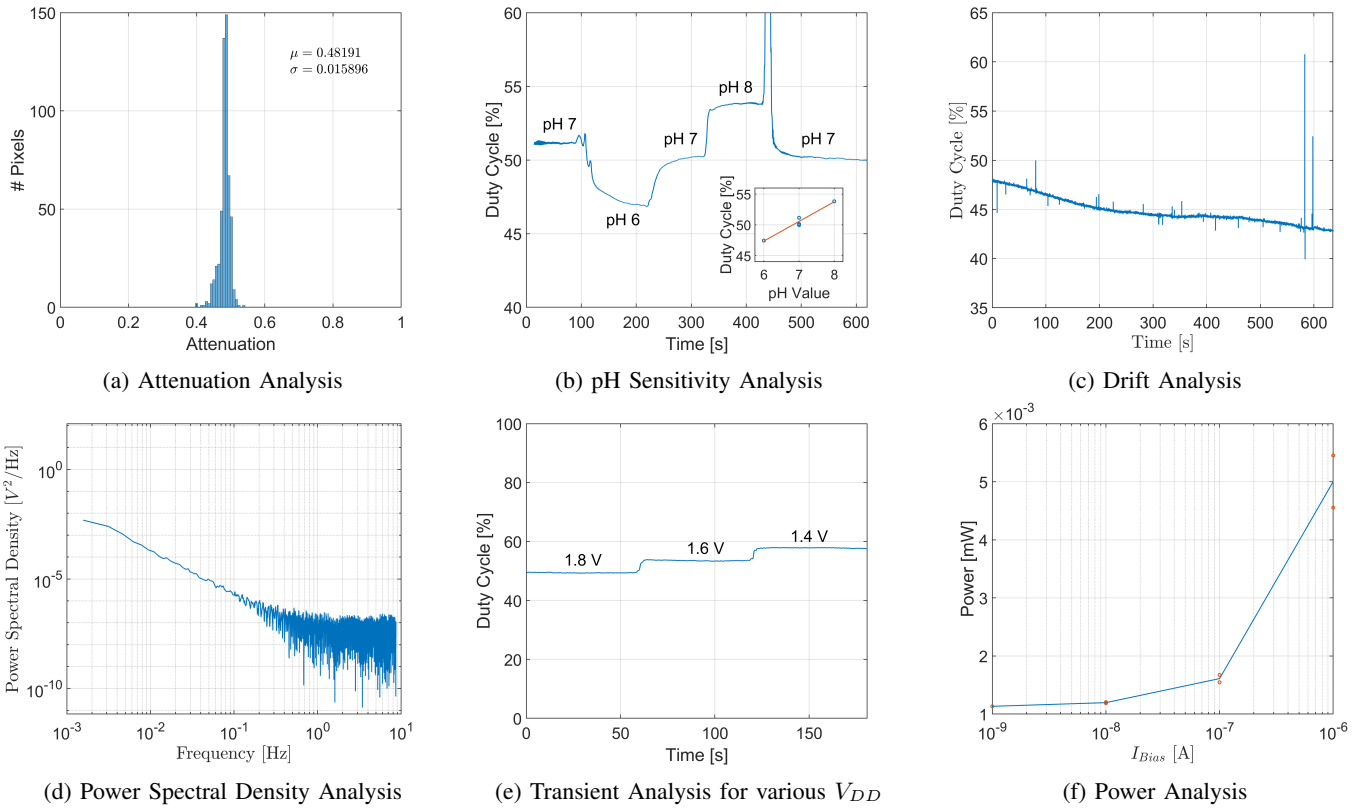
Due to the additional capacitance introduced at the floating gate on standard CMOS fabrication, the chemical signal is attenuated through a capacitive division [11]. To assess this attenuation, the characterization curves obtained in Section VI-A are compared with a sweep in V_{DAC} voltage with constant reference electrode potential. As V_{DAC} directly modifies the potential at the gate, this response can be regarded as the characterization curve in the absent of capacitive attenuation. Hence, the capacitive attenuation can be obtained by calculating the ratio between these sensitivities.

For this experiments, a sweep across V_{DAC} range is performed while maintaining the reference electrode potential constant, and each pixel response is recorded. These results are compared with the characterization curves of each pixel, obtained following the same experimental setup and analysis presented in Section VI-A. The ratio between the two slopes is calculated for each pixel, obtaining the attenuation distribution presented in Figure 9a with a mean of 0.4819 and a standard deviation of 0.0159.

C. pH Sensitivity

The pH sensitivity of the native CMOS passivation layer, Si_3N_4, is verified by sequentially flowing different pH buffers over the surface of the chip. After each step, a pH 7 solution is inserted to provide a reference to measure differences between buffers. The influence of the monotonic drift, described in detail in Section VI-D, can be regarded as linear for the experiment duration, allowing its removal through linear interpolation.

Figure 9b presents the response to the pH changes. Any pH variation triggers a modification of the floating gate potential of the ISFET, leading to a duty cycle change at the output following the electrical sensitivity described in Section VI-A. Using this result, the pH sensitivity can be calculated using Eq. 17.



(a) Attenuation Analysis

(b) pH Sensitivity Analysis

(c) Drift Analysis

(d) Power Spectral Density Analysis

(e) Transient Analysis for various V_{DD}

(f) Power Analysis

Fig. 9: Chemical Sensor Characterization

$$S_{pH} = \frac{\Delta\%}{\Delta pH} \cdot \frac{1}{S_{Elect}} \tag{17}$$

The obtained data yields a pH sensitivity $S_{pH} = 11.8mV/pH$, a value aligned with previously reported CMOS-based ISFET architectures [6], [7]. Considering this pH sensitivity and an expected pH step between 0.5 and 2.2 pH units [6], [7] on LAMP DNA amplifications, the dynamic range reported in Section VI-A is suitable for monitoring on-chip DNA reactions.

D. Chemical Drift & Noise Analysis

The native CMOS passivation, Si_3N_4, undergoes a hydration process when immersed in a solution, creating a hydrated SiO_2 layer which modifies the insulator capacitance value [25]. This variation at the superficial layer is reflected at the output as an slow and monotonic drift following a negative exponential trend [26].

The drift present in our system is characterized by exposing the array to a pH 7 buffer and monitoring the evolution of the output. One single chemical pixel is calibrated to maximize sampling rate and sampled for 10 minutes, obtaining the monotonic drift presented in Figure 9c. From this curve and the sensitivity results from Section VI-A, a drift rate of 3.8 mV/min is calculated.

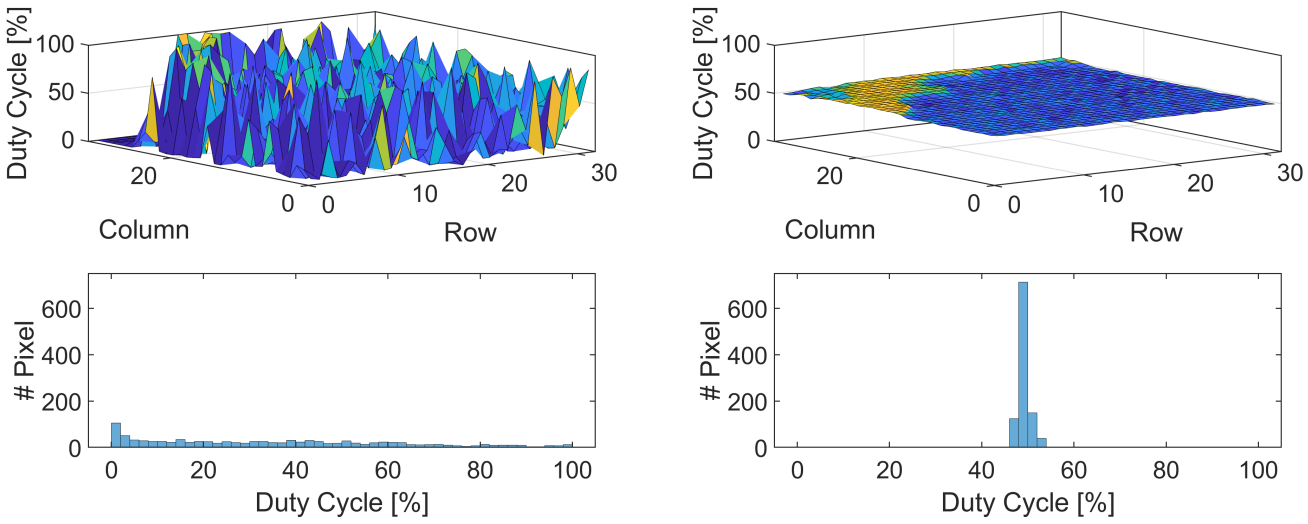
Using this drift measurement, the pH resolution of the architecture can be estimated by calculating its Power Spectral Density (PSD), presented in Figure 9d, and integrating it over the frequency range of interest, which for DNA amplifications is established between 10 mHz and 8 Hz [6], [16]. Following this criteria, a pH resolution of 0.1105 pH is obtained. This pH resolution value indicates the suitability of this architecture for LAMP DNA amplification detection, considering previous reported pH changes on LAMP reactions range between 0.5 and 2.2 pH steps [6], [7]

This pH resolution is bounded by two phenomena: Firstly, due to the slow time constant of pH changes and DNA amplification reactions, the chemical information spectral bandwidth overlaps with flicker noise, preventing post-processing filtering. Secondly, this chemical flicker noise has been demonstrated to be at least one order of magnitude higher than the MOSFET counterpart [27], limiting pH resolution.

E. Variable Supply Operation

Over the last few years, ISFET arrays have been integrated into portable [28] and wearable [5] platforms. These platforms are powered by batteries or power harvesting techniques, requiring architectures that can operate at scenarios where power budget and supply levels are key factors.

To assess the architecture suitability to different supply levels, the operation of the architecture under 3 supply voltages - 1.4V, 1.6V & 1.8V - is evaluated. During the experiment, the pixel is calibrated and the output duty cycle is monitored for 3 minutes, while maintaining V_{DAC} and I_{Bias} at a constant



(a) Array at Ideal Reference Electrode Potential

(b) Calibrated Array

Fig. 10: Calibration Results, presenting the raw array output (above) and the subsequent pixel output distribution (below) at different stages of the calibration. Figure (a) presents the array output after the completion of Step 1 of the calibration, while Figure (b) presents the calibrated response of the array

value. Every minute, the value of the voltage is decreased by 0.2V, achieving the result presented in Figure 9e. The offset generated between the different supply levels can be calculated using these results, yielding -21.28 %/V.

F. Power Consumption

The impact of I_{Bias} on the power consumption is analyzed by measuring power measurements under different biasing conditions. The results of this experiment are provided in Figure 9f, where the power consumption follows I_{Bias} trend due to the exponential correlation between the biasing current and the oscillation frequency. For the standard $I_{Bias} = 10nA$ at room temperature, a power consumption of 1.19 mW is obtained.

G. Trapped Charge Compensation

Significant mismatch between pixels across the array are created during the standard CMOS fabrication due to trapped charge accumulated at the floating gate [29]. To maximize the dynamic range of all pixel, this pixel-to-pixel mismatch needs to be compensated.

As introduced in Section III-A, the terminal V_{DAC} from the linear OTA can be used for this purpose, compensating for trapped charge in a pixel-by-pixel basis by balancing the input voltages V_{ISFET} and V_{DAC}. To achieve this, a 2-step calibration scheme is developed:

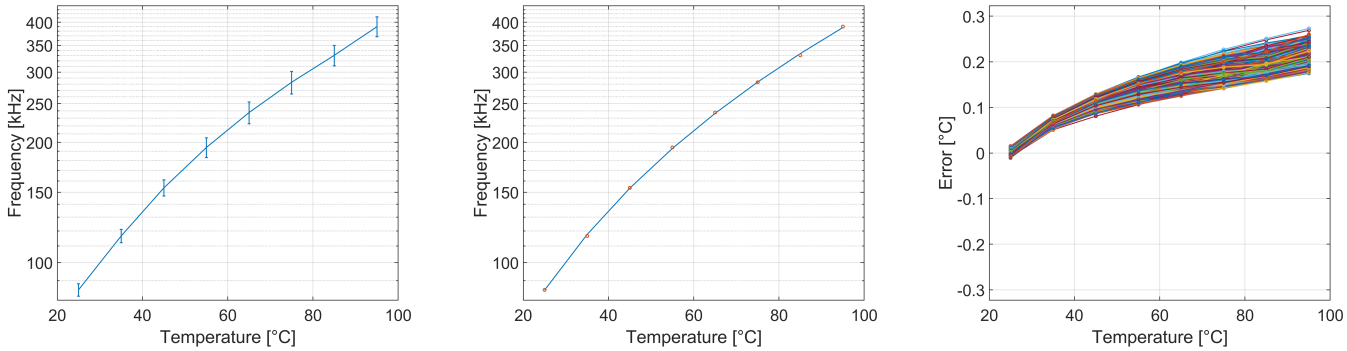
1) **Step 1 - Reference Electrode Potential Sweep:** The Ag/AgCl Ref Elect potential is swept through the sensing range, recording at each step the number of active pixels - this is, with an output duty cycle between 15% and 85%. The value with most active pixels will be selected as the ideal potential.
2) **Step 2 - Trapped Charge Compensation:** A Proportional controller is used to control the ideal V_{DAC} value for each pixel by taking the difference between the target duty cycle range - 48% to 52% - and the measured value. This controller generates a new value for V_{DAC} each array scan for each individual pixel, which is stored and applied in the next iteration. The compensation process for each pixel is repeated until all pixels are within the target duty cycle, V_{DAC} is out of range or after a specific number of iterations.

Results after steps 1 & 2 are provided in Figures 10a & 10b. It can be seen that the first calibration step distributes uniformly the pixels throughout the active range, and the compensation stage set all pixel at the dynamic range midpoint, with a mean value of 49.97% and a standard deviation of 1.76%. This process yield a 99.5% of active pixels calibrated at the target duty cycle range, homogenizing pixel response across the array.

VII. Experimental Results: Thermal Sensitivity

In Section III-B the equations governing the thermal sensitivity of the architecture were presented. This section presents the results obtained during the pixel characterization as a frequency-modulated temperature sensor. To assess the sensor performance, the pixel is calibrated to 50%, V_{DAC} is maintained constant and V_{Bias} is biased through a external voltage source.

In this experiment, the array is exposed to different temperatures, from 25°C to 95°C in 10°C steps, and the PWM signal frequency is measured, generating Figure 11. The characterisation of the sensor is presented in Figure 11a, plotting the evolution of the pixel frequency with every increase in temperature as well as the standard deviation presented across



(a) Thermal Calibration Curve (b) Quadratic fitting (c) Accuracy Analysis

Fig. 11: Thermal Sensor Characterisation (a) Evolution of pixel frequency with temperature. Curve represents mean frequency value, and error bars represent standard deviation. (b) Quadratic fitting based on mean value of frequency characterisation curves. (c) Pixel-by-pixel accuracy analysis, showing the thermal error between the pixel fitting curve and the sensed frequency

the array. Secondly, the quadratic relationship between temperature and frequency described in Section III-B is confirmed through the results presented in Figure 11b. Performing this quadratic fitting to the data-set, a transfer function can be obtained.

$$f(T) = 18.21 \cdot T^2 + 2140.05 \cdot T + 2041.7 \qquad (18)$$

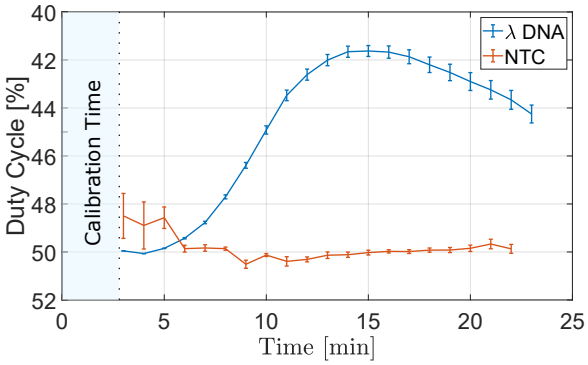
This fitting is also included in Figure 11b, validating the approximation described in Section III-B. To evaluate the sensor's accuracy, a quadratic fitting for each pixel is obtained and its measurement error is evaluated at each thermal point, as presented in Figure 11c. This analysis yields a maximum accuracy of 0.23°C.

Finally, the resolution of the system and its suitability for LAMP applications is evaluated by sampling the thermal sensor's output for 10 minutes at 63°C, which is LAMP's reaction temperature. Using this data and the procedure described in Section VI-D, a resolution of 0.9282°C is obtained. These results confirm the dual-sensing nature of this pixel architecture, achieving both chemical and thermal sensing, and validates the viability of this sensor for monitoring LAMP amplifications, where reaction occurs between 60 and 65°C [12]

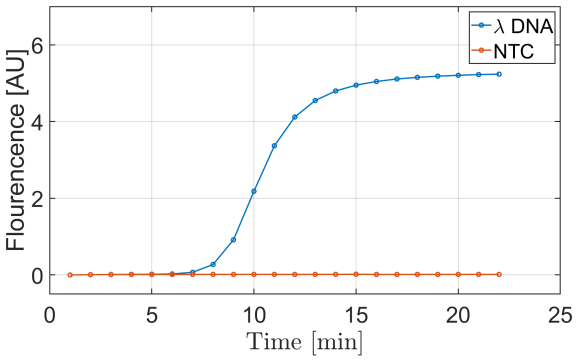
VIII. LAMP DNA Amplification and Detection

In this section, we demonstrate the feasibility of the Lab-on-Chip platform comprising the dual-sensing ISFET array for real-time DNA amplification and detection using LAMP. For this experiment, an acrylic manifold was placed on top of the ISFET array creating a chamber where the LAMP reaction was loaded. This reaction is biased via a reference electrode which is in contact with the solution. LAMP DNA amplification occurs at constant temperature (typically 63 ^{o}C) and requires 4 to 6 primers for amplification to occur, achieving high amplification speed ($<$ 20 min) and high amplification efficiency producing around $> 10^9$ copies of the targeted DNA fragment at the end of the reaction [38].

Here, DNA isolated from bacteriophage lambda ($\#N3011S$, New England BioLabs) was diluted to a final concentration of $1 \cdot 10^6$ copies per reaction and used as the target for DNA amplification. LAMP primers for specific detection of phage lambda DNA were used as described



(a) Amplification curve of of synthetic lambda DNA at 10^6 copies per reaction carried-out in the Lab-on-Chip platform. A non-template control (NTC) was also included. Curve represents mean pixel value, and error bars represent standard error.



(b) Amplification curve of of synthetic lambda DNA at 10^6 copies per reaction carried-out in a commercial qPCR instrument. A non-template control (NTC) was included

Fig. 12: Lambda DNA amplification and detection on a commercial qPCR instrument and on the Lab-on-Chip platform

TABLE II: State-of-the-art Performance Comparison - ISFET Arrays

Parameters	**This Work**	**[30]**	**[6]**	**[31] [24]**	**[7] [32]**	**[33]**	**[34]**
Sensing Domain	Duty Cycle	Time	Time	Voltage	Current	Voltage	Voltage
Process	180nm	180nm	350nm	350nm	350nm	180nm	350nm
Supply Voltage	1.8 V	1.8 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
Pixel Size	40 x $40\mu m^2$	26 x $26\mu m^2$	37 x $31\mu m^2$	60 x $70\mu m^2$	6.5 x $7.8\mu m^2$	10 x $10\mu m^2$	50 x $50\mu m^2$
Array Size	32x32	32x32	78x56	32x32	64x200	64x64	8x8
pH Sensitivity	11.8 mV/pH	30mV/pH	11.74 mV/pH	39.6mV/pH	24.1 mV/pH	26.2 mV/pH	57mV/pH ‡
pH Resolution	0.1105 pH	0.013 pH	0.017 pH	0.066 pH	0.101 pH	-	-
% Calibrated pixels	99.5%	100%	95%	100%	-	-	100%
Power Consumption	1.19 mW	11.286 mW	7.5 mW	10.12 mW	$150\mu W$	105.6 mW	-
Multi-Sensing	✓ Ion & Temperature	✗	✓ †	✗	✗	✓ Ion & Light	✓ Ion & Light
Operated at Variable Supply	✓	✗	✗	✗	✗	✗	✗
Programmable	✓	✗	✓	✗	✓	✗	✓

† Ion & Temperature are separate pixels
‡ Gain of 10

TABLE III: State-of-the-art Performance Comparison - Multisensing Systems

Parameters	**This Work**	**[35]**	**[36]**	**[6]**	**[37]**
Sensing Modality & Domain	Ion ⇒ Duty Cycle Temperature ⇒ Frequency	Humidity ⇒ Frequency Temperature ⇒ Frequency	Gas ⇒ Voltage Humidity ⇒ Voltage Temperature ⇒ Voltage	Ion ⇒ Time Temperature ⇒ Time	Potential ⇒ Voltage Impedance ⇒ Current Light ⇒ Voltage Temperature ⇒ Current
Process	CMOS 180nm	CMOS 180nm	MEMS $1.5\mu m$	CMOS 350nm	CMOS 130nm
Sensor Size	$40x40\mu m^2$	0.2 mm^2	-	$37x31\mu m^2$	$80x100\mu m^2$
Array Size	32x32	Single Sensor	Single Sensor	78x56	21x21x9
Spatial Information	✓	✗	✗	✓	✓
In-Pixel Multisensing	✓	✗	✗	✗	✗
Application	DNA Amplification	NA	Env. Monitoring	DNA Amplification	Cell Imaging

TABLE IV: System Performance Summary

Parameters ($I_{Bias} = 10nA$)	**Spec**
Technology	TSMC $0.18\mu m$ M6
System Size	$2mm$ x $1.8mm$
Pixel Size	$40\mu m$ x $40\mu m$
Fill Factor	98.4%
Array Size	32x32
Sensing Domain	Ion Concentration ⇒ Duty Cycle Temperature ⇒ Frequency
Supply Voltage	1.8V
Pixel Performance	
Chemical Sensor	
E. Sensitivity	321.65 $\%/V$
Linear Range	0.2025 V
Linearity [R^2]	0.9986
Attenuation	0.4819
pH Sensitivity	11.8 mV/pH
pH Resolution	0.1105 pH
% Calibrated pixels	99.5%
System Power Consumption	1.19 mW
Thermal Sensor	
Center Frequency	85.45 kHz
Thermal Sensitivity (@ 35 °C)	3.41 kHz/°C
Resolution	0.9282°C
Accuracy	0.273°C

in [39]. Real-time DNA amplification experiments were performed in parallel in a commercial qPCR instrument (LightCycler 96, Roche Instruments) and on the Lab-on-Chip platform (LoC).

The results with both, the Lab-on-a-Chip platform and the benchmark instrument, are presented in Fig. 12 where a non-template control (NTC) and a positive reaction were included as the sample set. The results obtained with the LoC platform are shown in Fig. 12a. The pH of the solution at the end of the experiment decreased by 2.16 pH units due to the release of protons during DNA amplification. The time-to-positive (TTP) of the reaction was calculated using a threshold of 1.5% duty cycle change after monotonic drift removal. Using this method, the estimated time-to-positive (TTP) was 7.71 ± 1.47 min. The same reactions were carried out in a conventional qPCR instrument and the results are presented in Fig. 12b where the y-axis corresponds to fluorescence (AU) and the x-axis to time. The obtained average TTP was 7.76 ± 0.40 min. The TTP of the reaction on the qPCR instrument was calculated using the cycle-threshold method, C_t [40], setting a threshold at 0.2 of normalized output data.

The DNA amplification curves and TTP values obtained demonstrate the capability of the proposed LoC platform to carry-out DNA amplification reactions detection with accuracy comparable to a conventional qPCR instrument. This technology opens the doors for performing the identification on-chip of additional pathogens relevant for clinical diagnosis.

IX. Conclusion

A dual-sensing 32x32 ISFET array capable of detecting on-chip DNA amplification reactions is presented. The pixel senses both ion activity and temperature, encoding them into the duty cycle and the frequency of the output PWM signal respectively. This dual-sensing architecture eliminates the need for extra on-chip temperature pixels, enhancing spacial resolution. Furthermore, the pixel architecture, composed by a linear OTA connected to a 2-stage sawtooth oscillator, leverage on a differential approach to achieve resilience to process variations and is capable of operating at different voltage supplies, becoming a suitable candidate for battery-powered or power-harvested portable platforms. The system presents several degrees of programmability, enabling the modification

of the sensor characteristic response and operation point to compensate for ISFET non-idealities. To demonstrate this programmability, pixel-to-pixel mismatches due to trapped charge were corrected using the programmable terminals, achieving an homogeneous response across the array.

A summary of the system performance is provided in Table IV, and its comparison with the state-of-the-art is provided in Table II. This pixel architecture is the first example of dual thermo-chemical sensing in a single pixel, presenting good robustness and programmability while maintaining a compact form factor and pH resolution. We anticipate that the presented pixel programmability and versatility can be key to mitigate further ISFET non-idealities such as drift, eliminating in real-time the monotonic output change and facilitating the early detection of both pH changes and DNA on-chip amplification reactions.

We envision that the presented architecture will set the basis for the next generation of portable ISFET platforms, where sensor adaptability to different applications is enhanced through multi-sensing, robustness to external conditions and pixel-level programmability. By sensing multiple features at the same spatial point, these systems can become self-aware of both internal and external conditions and react accordingly through multi-level sensor programmability, opening new horizons for the field of smart sensors.

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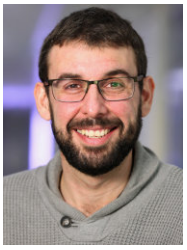

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Pantelis Georgiou (AM'05–M'08–SM'13) received the M.Eng. degree in electrical and electronic engineering and the Ph.D. degree from Imperial College London (ICL), London, U.K., in 2004 and 2008, respectively. He is currently a Reader with the Department of Electrical and Electronic Engineering, ICL, where he is also the Head of the Bio-Inspired Metabolic Technology Laboratory, Centre for Bio-Inspired Technology. His research includes bio-inspired circuits and systems, CMOS based Lab-on-Chip technologies, and application of microelectronic technology to create novel medical devices. He has made significant contributions to integrated chemical-sensing systems in CMOS, conducting pioneering work on the development of ISFET sensors, which has enabled applications, such as point-of-care diagnostics and semiconductor genetic sequencing and has also developed the first bio-inspired artificial pancreas for treatment of Type I diabetes using the silicon-beta cell. He received the IET Mike Sergeant Medal of Outstanding Contribution to Engineering in 2013. In 2017, he was also awarded the IEEE Sensors Council Technical Achievement award. He is a member of the IET and serves on the BioCAS and Sensory Systems technical committees of the IEEE CAS Society. He is also the CAS representative on the IEEE Sensors council and the IEEE Distinguished Lecturer in Circuits and Systems.