Tbulk-BICS: A Built-In Current Sensor Robust to Process and Temperature Variations for Soft Error Detection

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***Abstract*—This paper presents a parameterized current sensor able to detect transient ionization in the silicon substrate. Each sensor is controlled by a set of trimming bits that can be used to attune the sensitivity of the sensor compensating process and temperature variations. By choosing different configurations in the trimming bits, it is possible to adjust the performance of the sensor, which can increase the number of transistors monitored by a single sensor reducing the area overhead. Monte Carlo simulations are used to evaluate the sensor behavior. Results from a case-study circuit with embedded Tbulk-BICS confirm the efficiency of the technique.**

***Index Terms*—Built-in current sensor, fault tolerance, process variations, soft errors.**

I. Introduction

THE International Technology Roadmap for Semiconductors (ITRS) has identified that beyond 90 nm CMOS technology soft errors severely impact field-level product reliability, not only for embedded memory, but for combinational logic as well [1]. Soft errors are upsets with transient effects that can occur in combinational and sequential circuits due to the interaction of energetic particles with the integrated circuit [2], [3]. Particles are present at space environment, generated by solar activity, and at sea level, as for instance atmospheric neutrons and protons, which may create secondary ions such as alpha particles when interacting with atoms in the target device.

When an energetic particle strikes a sensitive circuit node, it ionizes a semiconductor region, inducing a current that injects or extracts electrical charge from the struck circuit node. The injected or extracted charge may change the logical state at the struck node. With technology scaling, the amount of charge used to store information at the nodes of sequential or combinational logic is continuously decreasing, and less charge from an energetic particle is needed to change the logical state at a node. Consequently, soft errors have become more frequent [1], [2].

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Detecting soft errors in the combinational and sequential logic is extremely important to avoid errors in the circuit application. However, it is a complex task as the internal circuit signals are becoming of the same order of magnitude of the transient currents generated by the energetic particle strike. Hence, a mechanism able to distinguish transient currents provoked by ionization of the substrate to internal circuit signals is mandatory to detect and mitigate transient faults.

Built-in Current Sensors (BICS) connected directly to the circuit substrate (bulk-BICS) have been proposed to detect soft errors in sequential and combinational logic [4]. Each bulk-BICS is connected directly to the bulk of a set of transistors, which allows the bulk-BICS to detect any current discrepancy that may occur during a particle strike in that silicon substrate region. Bulk-BICS present a low area overhead and a negligible performance penalty.

However, process variations may affect the functionality of the bulk-BICS, reducing its ability to detect soft error. It is well-known that variations in the process fabrication of the circuit can affect the transistors parameters, such as the width (W) and length (L) of the transistor channel, the transconductance parameter (K'), the threshold voltage (V_T) and others, which may change the transistor behavior [5]. It is also important to highlight that the continuous exposure of integrated circuits to radiation on space may lead to electrical parameter variations. An example is threshold voltage shifts due to fixed charge generation in the silicon dioxide, as a consequence of the total radiation dose to which the device is exposed [6].

This work presents a parameterized bulk-BICS controlled by trimming bits that are able to compensate process variations, referred here by Tbulk-BICS. By configuring the trimming bits, it is possible to adjust the performance of the Tbulk-BICS to ionization detection. In this way, it is possible to guarantee soft error detection even in the presence of temperature and process variations, as analyzed by Monte Carlo simulations. In addition, the trimming bits can be configured to increase the detection efficiency of the Tbulk-BICS. Electrical simulations results show that Tbulk-BICS can be more sensitive to low deposited charges and can monitor a higher number of transistors at the same time compared to the standard bulk-BICS by simply changing the configurations of the trimming bits.

II. Detecting Soft Errors by Using Bulk-BICS

When an energetic particle strikes a sensitive region in a semiconductor device, it creates a track of electron-hole pairs that can cause a transient current to flow through the pn junction altering the voltage of the circuit stroke node [7]. The sensitive

sites are the surroundings of the reverse-biased drain junctions of a transistor biased in the off state. This voltage change lasts until the charge is conducted away via open current paths to V_{DD} or ground, returning the struck node to its original state. If the transient pulse amplitude is high enough and its duration is long enough, compared to the gate delays, the pulse may propagate through circuit stages and change the results of a computation. Hence, not only the amount of deposited charge but also the transient pulse amplitude and duration are key parameters for evaluation of circuit sensitivity to soft errors.

The width of the induced transient voltage pulse is dependent on the energy of the incident particle, the charge stored at the affected node, the charge collection efficiency of the affected junction, bias level of the junction and other process level parameters. Usually, device simulation is used to analyze the collected charge behavior in a certain technology and layout circuit. The maximum charge collection current depends on the energetic particle linear energy transfer (LET) value and process parameters. At the electrical Spice level, the charge deposition mechanism can be modeled by a double exponential current pulse at the particle strike site, as shown by [8]:

$$I_P = I_0(e^{-t/\tau\alpha} - e^{-t/\tau\beta}) \tag{1}$$

where I_0 is approximately the maximum charge collection current, $\tau\alpha$ is the collection time constant of the junction and $\tau\beta$ is the time constant for initially establishing the ion track. In the circuit simulations and modeling, $\tau\beta$ is assumed to be much smaller than $\tau\alpha$, while $\tau\alpha$, is used as a variable parameter, which is in line with experimental findings, as explained by [8]. Electrical transient analysis can be performed injecting a double exponential current pulse as given by (1), with the values of I_0 and $\tau\alpha$, being used as the variable parameters to determine the minimum charge Q_C corresponding to a given $\tau\alpha$.

The maximum charge collection current I_0 depends on the energetic particle linear energy transfer (LET) value and process parameters. Once the values of $I_0, \tau\beta$, and $\tau\alpha$ are determined for a given technology and particles of interest, any circuit designed in that technology may be evaluated at the circuit level modeling the charge deposition mechanism by (1).

Built in current sensors (BICS) connected to the power lines have been used in the past years to detect permanent faults and bit-flips in integrated circuits [9]. However, these sensors have limitations in detecting transient faults in the combinational logic since the transients generated by ionization are at the same order of magnitude of the normal signals propagated to the circuit. A BICS scheme (bulk-BICS) connected directly to the transistors substrate was proposed in [4].

Bulk-BICS analyzes the current that appears at the transistors bulk terminals. During normal operation, the current at the bulk terminal is negligible. Only the leakage current flows through the biased junction, which is still very low compared to the current generated by energetic particles. So, when an energetic particle generates a current in the bulk, it is very clear to the bulk-BICS that ionization has happened.

There are two bulk-BICS, the N-BICS that is connected to the bulk of a set of NMOS transistors and the P-BICS that is connected to the bulk of a set of PMOS transistors, as shown in Fig. 1. Each N-BICS and P-BICS can monitor a certain silicon area that contains a number of NMOS and PMOS transistors, respectively. These transistors implement combinational or sequential logic in the circuit. Fig. 1 shows 6 different regions in a standard cell layout approach with the bulk-BICS. Once a bulk-BICS detects ionization, it is known that a transient current pulse has occurred in one of the sensitive nodes of the monitored region and that can be nodes from combinational or sequential circuit. Then, the bulk-BICS output can be used by a mitigation technique to perform some correction action such as re-computation.

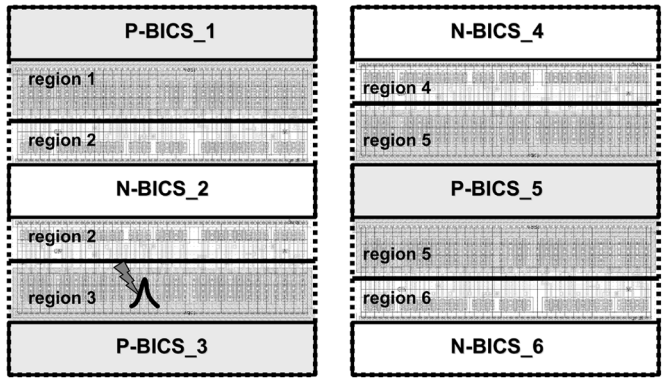

Fig. 1. Example of a standard-cell layout with embedded bulk-BICS sensors. For instance, sensor P-BICS_3 detects ionization at the substrate of region 3.

In order to achieve high speed soft error detection by the bulk-BICS, structures similar to sense amplifiers are used. This structure can be observed through the transistors 5, 6, 7 and 8, in Fig. 2. And the bulk-BICS indicates detection when the structure formed by the transistors 5, 6, 7 and 8 flips.

In the N-BICS case, the output is at logic '0' for "not-detection" state and at logic '1' for "detection" state. Thus, the virtual ground (Gnd' in Fig. 2) is provided to bulk (p-well) of the CMOS circuit, through the transistors 5 and 9. For a high sensitivity and high detection speed, the transistors 5 and 7 must have a small W/L ratio and the transistors 6 and 8 must have a large W/L ratio.

Complementarily, in the P-BICS case, the output is logical '1' for "not-detection" state and is logical '0' for "detection" state. Thus, the virtual $V_{DD}(V'_{DD}$ in Fig. 2) is provided to bulk (n-well) of the CMOS circuit, through the transistors 6 and 9. For a high sensitivity and high detection speed, the transistors 6 and 8 must have a small W/L ratio and the transistors 5 and 7 must have a large W/L ratio.

Table I shows the aspect ratio for each transistor in Fig. 2, for a bulk-BICS designed in the 32 nm technology Predicative Technology Model (PTM) [10].

III. Analysis Of The Bulk-BICS Under Process and Temperature Variations

The drain current of a MOS transistors in saturation and linear regions, may be expressed as in (2) and (3), respectively [8]:

$$I_D = \frac{K'}{2}\frac{W}{L}(V_{GS} - V_T)^2 \tag{2}$$

$$I_D = \frac{K'}{2}\frac{W}{L}\left[(V_{GS} - V_T) - \frac{V_{DS}}{2}\right]V_{DS} \tag{3}$$

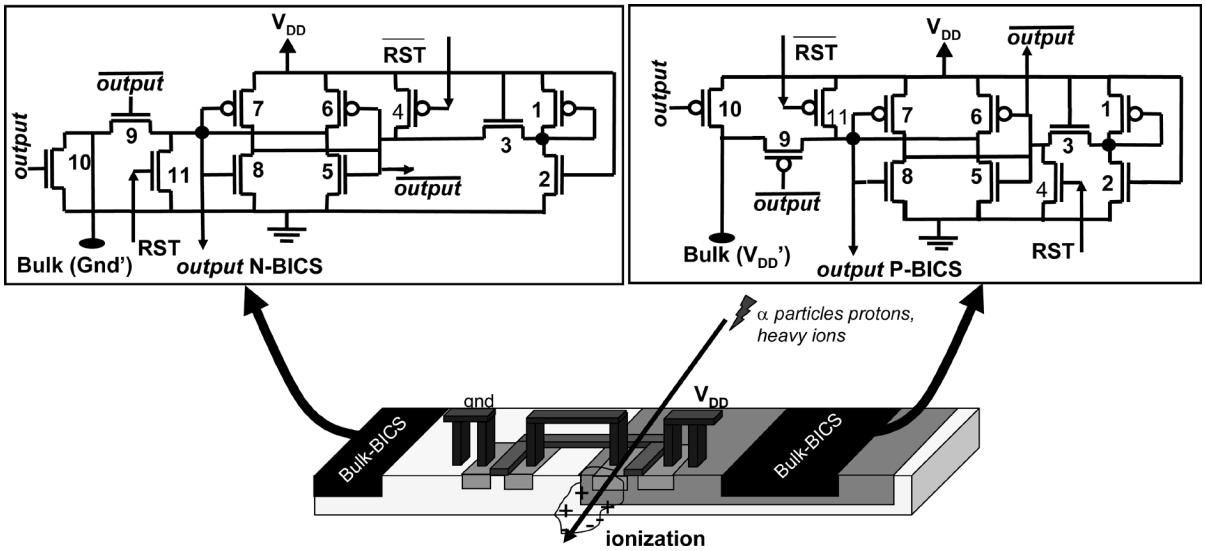

Fig. 2. High-speed SET Detection Bulk-BICS.

TABLE I
BULK-BICS TRANSISTORS DIMENSIONS FOR 32 nm CMOS TECHNOLOGY

transistor	N-BICS		P-BICS	
	W (nm)	L (nm)	W (nm)	L (nm)
1	160	32	160	32
2	64	1500	64	1500
3	320	32	320	32
4	320	32	320	32
5	64	320	320	32
6	320	32	64	320
7	64	320	320	32
8	320	32	64	320
9	320	32	320	32
10	64	32	64	32
11	320	32	320	32

TABLE II
PROCESS PARAMETERS EXERCISED ATA MONTE CARLO SIMULATIONS

	PMOS				
	Typical	SS corner and δ(%)		FF corner and δ(%)	
L_{int} (m)	2.70E-09	2.07E-09	-23.33	3.33E-09	23.33
V_{th0} (V)	-4.52E-01	-0.54	19.69	-0.36	-20.13
$k_1(V^{0.5})$	5.14E-01	0.59	14.98	0.43	-15.37
$\mu_0(cm^2/V.s)$	3.50E-03	2.51E-03	-28.28	4.92E-03	40.57
N_{dep} (cm^{-3})	3.10E+18	4.11E+18	32.58	3.10E+18	0.00
x_j (m)	1.01E-08	1.11E-08	10.00	9.07E-09	-10.00

	NMOS				
	Typical	SS corner and δ(%)		FF corner and δ(%)	
L_{int} (m)	2.70E-09	2.07E-09	-23.33	3.33E-09	23.33
V_{th0} (V)	0.50	0.59	17.76	0.41	-18.16
k_1 ($V^{0.5}$)	0.55	0.63	14.13	0.47	-14.31
$\mu_0(cm^2/V.s)$	0.04	3.39E-02	-13.95	4.59E-02	16.56
N_{dep} (cm^{-3})	4.03E+18	5.24E+18	30.02	4.03E+18	0.00
x_j (m)	1.01E-08	1.11E-08	10.00	9.07E-09	-10.00

where K' is the transconductance parameter and $\mathrm{V_T}$ is the threshold voltage. The channel length modulation effect is ignored in (2), [8].

Due to process variations, K', $\mathrm{V_T}$ and other parameters may vary, and affect the drain current and junction capacitances. As discussed in [1], in a typical situation of process variation, an increase in K' is accompanied by a decrease in $\mathrm{V_T}$, or vice versa. This correlation between K' and $\mathrm{V_T}$ can be interpreted as an "inverse" relationship between them. In [1], an understanding about the most commonly modeled process corners in typical CMOS processes is discussed.

In Table II, a set of parameters for typical CMOS process and across process variations corners are presented. The "FF" and "SS" corners correspond to "fast" (increased $\mathrm{I_D}$) and "slow" (decreased $\mathrm{I_D}$) MOS devices respectively. But, it is possible also to see the "SF" and "FS" corners that correspond to "slow NMOS and fast PMOS" and "fast NMOS and slow PMOS" devices respectively. The typical values and deviations (δ) were used in Monte Carlo simulations to evaluate the behavior of the bulk-sensors under process and temperature variations. The modified parameters are the length offset fitting from I-V without bias $(\mathrm{L_{int}})$, threshold voltage of long channel device at $\mathrm{V_{bs}} = 0$ and small $\mathrm{V_{ds}}(\mathrm{V_{th0}})$, first-order body effect coefficient $(\mathrm{K_1})$, the carrier mobility (μ_0), channel doping concentration at depletion edge for zero body bias $(\mathrm{n_{dep}})$; and the doping junction depth $(\mathrm{x_j})$.

The temperature dependence of MOS devices is an important performance characteristic of CMOS circuits [8]. It can be found from the (1) and (2), once the primary temperature-dependent parameters are K' and $\mathrm{V_T}$. The temperature dependence of K' and $\mathrm{V_T}$ is given in (4) and (5), respectively [1]:

$$\mathrm{K'} = \frac{K_0'}{T^{1.5}} \tag{4}$$

$$V_T = V_{T0} - (m_{\mathrm{VT}})T \tag{5}$$

$\mathrm{K_0'}$ and $\mathrm{V_{T0}}$ are the value for K' and $\mathrm{V_T}$ respectively at absolute zero. With increase in temperature, both K' and $\mathrm{V_T}$ decrease. Analyzing (1) and (2), it can be seen that the drain current of a MOS device decreases as K' decreases, and increases as $\mathrm{V_T}$ decreases. However, with increase in temperature the drain current

TABLE III
MONTE CARLO SIMULATION RESULTS: PERCENTAGE OF BULK-BICS UNABLE TO DETECT IONIZATION AT THE SUBSTRATE DUE TO PROCESS VARIATIONS, AT THREE DIFFERENT TEMPERATURES

Temperature (°C)	Bulk-BICs that presented the effect described as Case 1	Bulk-BICS that present the effect described as Case 2 for a deposited minimum current of I_0=200uA and τ_α=30ps
-20	71.3 %	4.2 %
27	24.1 %	27.8 %
80	1.7 %	76.9 %

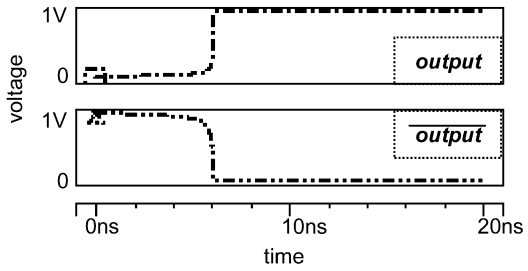

Fig. 3. Bulk-BICS under FF corner conditions.

decreases, once the temperature dependence is more intense in K' than V_T.

In order to analyze the impact of process and temperature variations on the bulk-BICS presented in Fig. 2, the variability estimated according to [9] for the 32 nm technology Predicative Technology Models (PTM) was used. Monte Carlo simulation was performed to identify the behavior of a case-study circuit under process and temperature variations. A 4-bit adder designed in 32 nm technology (PTM model) was used as a case study circuit.

Basically, two effects were observed in the bulk-BICS under process and temperature variations:

- **Case 1:** the BICS can flip by itself, i.e., the BICS can stabilize itself in "detection" state permanently, thus becoming a faulty circuit. This occurs when both NMOS and PMOS are "fast" (process corner FF).
- **Case 2:** the BICS can not detect soft errors generated by low or medium current pulses. This occurs when both NMOS and PMOS are "slow" (process corner SS).

Monte Carlo simulations are presented in Table III. In this table, it is shown the number of bulk-BICS that fail on soft error detection due to process variations from 1000 bulk-BICS samples. The experiments were performed for three different temperatures $-20°C$, $27°C$ and $80°C$. Up to 71.3% of the bulk-BICS presented the effect described as case 1 (flipped by itself) at low temperature. This number can reduce to 17% at higher temperatures. When the sensitivity of the sensor is analyzed, 42% of the sensors could not detect the minimum induced current because of the process variations at low temperature. This number increases to up to 76.9% for higher temperatures. These results show that the bulk-BICS may not work properly in the presence of process variations and a solution must be provided.

Two examples, one of case 1 and one of case 2 effects, are illustrated as follows. The first effect shown in Fig. 3 was analyzed at temperature $-20°C$ and in the FF process corner. When the bulk-BICS is reset at time $t = 0$, the N-BICS comes back to "detection" state due to this process corner combination. The same behavior is observed for the P-BICS case.

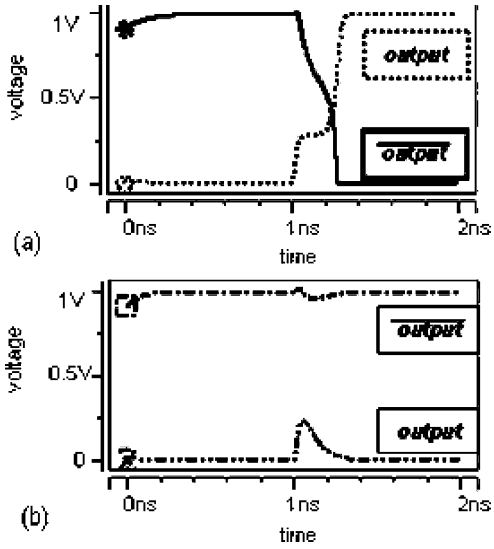

Fig. 4. (a) Bulk-BICS under typical conditions and (b) BICS under SS corner conditions.

The second case was analyzed at temperature $80°C$ and in the SS process corner. Simulation results are presented in Fig. 4. A current pulse with amplitude of 200 μA and $\tau\alpha$ of 30 ps was injected at $t = 1$ ns in a CMOS circuit connected to a sensor with "typical" NMOS and PMOS parameters at $T = 30°C$. This current models a deposited charge of 6 fC. In Fig. 4(b), the same pulse is injected for the N-BICS with "slow" NMOS and PMOS parameters at $T = 80°C$. It can be observed that N-BICS in typical conditions can easily detect the current pulse, while the N-BICS with "slow" NMOS and PMOS parameters at $T = 80°C$ does not detect the same current pulse. The same behavior is observed for the P-BICS case.

It is important to mention that due to process variations, the bulk-BICS can change its inherent sensitivity to soft error as well. In [13], it is shown that variations in the process can make the BICS more or less susceptible to transients. Usually, the variation makes the latch more prone to flip in one direction than the other, as discussed in [13].

IV. THE PROPOSED TBULK-BICS

Based on the discussed results, the sensor must be capable of compensate process and temperatures variations. Once a process corner occurs in a sensor due to process or temperature variations, it is necessary to adjust the transconductance of the sensor's transistors to ensure soft error detection. One option is to replace one single transistor by a set of transistors in parallel and one in series. Each gate of the parallel transistors is controlled by a value stored in a memory cell. This set is called trimming transistors and the storage cells are known as trimming bits [10], [11]. In this way, it is possible to calibrate the trimming bits to a certain transconductance value that allows the correct operation of the sensor in presence of process variations.

The adjustment can be done digitally. The proposed Tbulk-BICS suggests that transistors 5 and 7, for the N-BICS case, and of the transistors 6 and 8, for the P-BICS case, must be replaced by a set of transistors, as described in Fig. 5. In this figure, 'x' is the complement of the output of N-BICS for the transistor 5 or is the output of P-BICS for the transistor 8; and

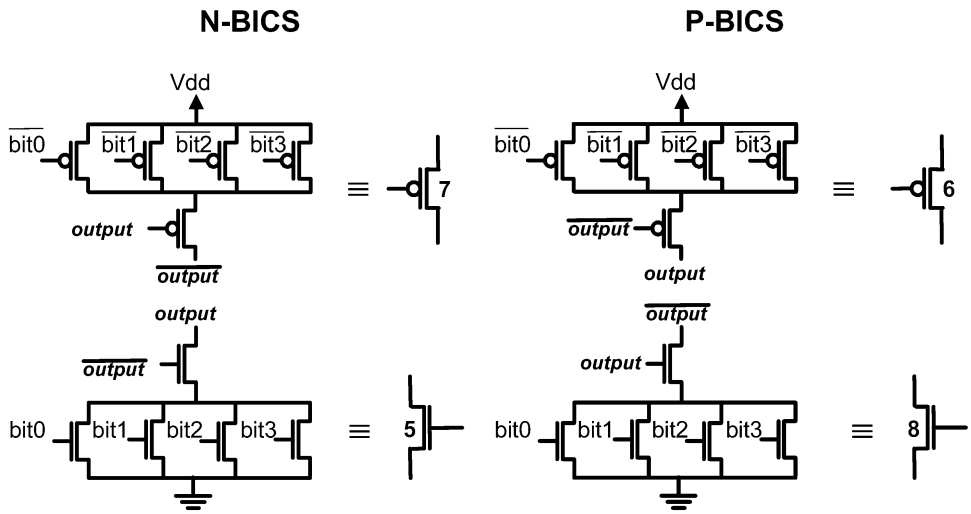

Fig. 5. Transistors with transconductance digitally adjustable by trimming bits. The dimensions are: transistors 0, 1, 2 and 3 have $L = 8^{*}L0$, $L = 4^{*}L0$, $L = 2^{*}L0$ and $L = L0$, respectively, while W is always $2^{*}LMIN$. $LMIN = 32$ nm and $L0 = 2.5^{*}LMIN$. Transistors 'x' and 'y' have $W = 2^{*}LMIN$ and $L = LMIN$.

TABLE IV
VALUES OF $\beta = K'W/L$ FOR EACH BIT COMBINATION C

C	β	C	β	C	β
0001	$0.066\beta_0$	0110	$0.400\beta_0$	1011	$0.733\beta_0$
0010	$0.133\beta_0$	0111	$0.466\beta_0$	1100	$0.800\beta_0$
0011	$0.200\beta_0$	1000	$0.533\beta_0$	1101	$0.866\beta_0$
0100	$0.266\beta_0$	1001	$0.600\beta_0$	1110	$0.933\beta_0$
0101	$0.333\beta_0$	1010	$0.666\beta_0$	1111	$1.000\beta_0$

'y' is output of N-BICS for the transistor 7 or is the complement of the output of P-BICS for the transistor 6 (see Fig. 2). For high precision calibration, the transconductance values can be adjusted by using four bits.

Table IV shows the transconductance value for each combination of trimming bits, where $\beta = K'.W/L$, C stands for the bit combination, and β_0 stands for the original transconductance (where the trimming bits are not used). The combination "0000" is not used, since it leads to a transconductance equal to zero.

The Tbulk-BICS behavior has three important parameters that must be tested. First, the sensor must be able to reset and keep the reset state as long as no charge is deposited in the substrate (bulk). This step tests the effect described in case 1, which can be due to process and temperature variations. Second, the sensor must be able to detect a range of deposited charges, modeled by current injection performed directly in the substrate. This step tests the effect described as case 2 in Section III. In this case, it is necessary to have a circuit able to inject current directly into the circuit substrate and it is important to have a good controllability of the amount of current and consequently the deposited charge. And finally, it is interesting to test the response delay of the Tbulk-BICS during soft error detection, and consequently which is the minimum time allowed between soft errors.

The trimming bits must be adjusted by a test circuit able to analyze the behavior of the sensor and choose the best configuration to guarantee efficiency in the soft error detection. Once a design is fabricated with a set of Tbulk-BICS, it is necessary to perform two test campaigns:

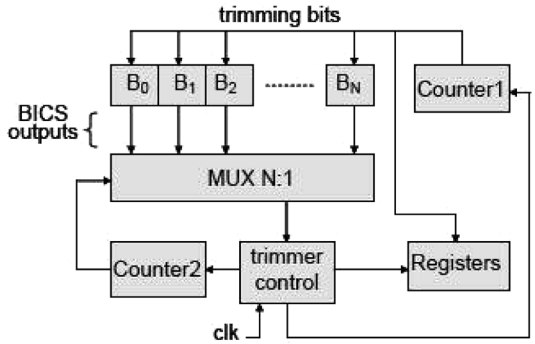

Fig. 6. Trimmer control circuit with the Tbulk-BICSs.

- Manufacture testing: where the sensors are tested for permanent and intermittent faults produced by the fabrication process.
- Calibration testing: where the sensor sensitivity is adjusted by configuring the trimming bits in order to ensure the correct behavior in presence of process and temperature variations.

These two testing steps are important to determine the sensors that have been fabricated and configured properly and the ones that have defects. A sensor that fails in the manufacture testing is not classified as a defective sensor before the calibration testing is performed.

V. RESULTS

The same case-study evaluated in Section III was now analyzed with the Tbulk-BICS. The experiments were divided into three parts. The first part proposes a trimmer control circuit solution and verifies the behavior of the entire circuit (including case study circuit and Tbulk-BICS). The second part aims to validate the capability of the Tbulk-BICS to detect soft errors in the presence of process and temperature variability. The final part analyzes the effect of the configuration of the trimming bits on the sensor sensitivity and on the number of transistors that can be monitored at the same time by a single sensor.

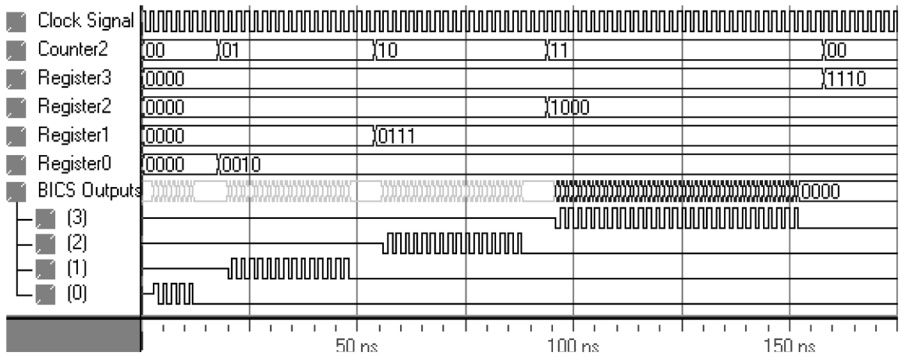

Fig. 7. Trimmer circuit simulation.

A. Trimming Bits Customization Circuit

The control part of the test circuit must test each Tbulk-BICS individually and set the best bit combination for each sensor. The schematic is shown in Fig. 6. In this schematic B represents a BICS and N is the number of BICS. The trimmer circuit is composed by one MUX N:1, two counters, N registers and one control unit. Counter1 has I bits, where I is the number of trimming bits, while Counter2 has J bits, where $\mathrm{J} = \log_2$ (N), and each register has I bits.

The trimmer circuit works as follow: Counter2 informs which BICS is being tested. The first is B0. For each BICS, Counter1 sweeps the bit combinations, starting at the lowest transconductance value, i.e., starting at "$00\cdots01$" (see Table III). The bit combinations are swept to find the best possible combination.

The sweep works as follow: the BICS is reset and in the next clock cycle it is evaluated by the control unit. If its output is in the "detection" state (this means that the bits combination generated a low transconductance value), the BICS is reset and evaluated again, for the next combination of bits (Counter 1++). This occurs until the trimmer circuit finds the first (the best) combination of bits. When the trimmer finds a bits combination for B0, this combination is stored in Register0. Counter2 is then incremented and the procedure is repeated until the bit combinations for all N BICS are found. If there is no combination of trimming bits able to satisfy the correct functionally, the Tbulk-BICS is then set as a defective sensor.

In order to validate the proposed test circuit, the test circuit and the trimming based sensors were described in a hardware description language (HDL) and simulated at logical level. Considering the behavior of the proposed BICS under process variations, at the HDL level the BICS outputs are modeled as "detection" state (logic '1') or "not-detection" state (logic '0'), according to the trimming bits. For the SS corner example, the BICS is stable in "not-detection" state from "0010" to "1111" bit combinations and is stable in "detection" state for the "0001" bit combination. In this case, at the HDL level for the SS corner example, the BICS output is logic '0' if the trimming bits value is equal or greater than "0010" or logic '1' if the trimming bits value is less than the best combination "0010."

Fig. 7 shows the self-test circuit simulation. In this example, there are four BICS (B0, B1, B2 and B3), where each BICS has its transconductance adjusted by 4 trimming bits, and consequently, there are four 4-bit registers, Counter1 has 4 bits and Counter2 has 2 bits. In this simulation B0 and B3 are modeled as the BICS under SS and FF corner conditions, respectively, and B1 and B2 as the BICS under intermediate process variations. Thus, the best bit combinations for B0, B1, B2 and B3 are, respectively, "0010," "0111," "1000" and "1110."

At time $\mathrm{t} = 0$ the test starts. Initially, B0 is tested, and Counter2 is "00." As Counter1 starts from "0000," two clock cycles are spent to achieve the best bit combination ("0010") for B0. Note that at this time, the combination found is stored in the Register0. After, Counter2 is incremented and B1 is adjusted. This procedure is performed until the last BICS (B3) is adjusted. At about $\mathrm{t} = 160$ ns, the four BICS are adjusted, i.e., the best trimming bit combinations for all BICSs are stored in the registers.

Please note that although the use of trimming techniques to adjust analog circuits under process variations (such as voltage/current references, oscillators, A/D and D/A converters), requires external test, the trimming circuit here proposed can be built in the chip, because the data tested (BICS outputs) is in the digital domain. The BICS outputs are logic '1' for the "detection" state, and logic '0' for "not-detection" state. This results in a negligible cost in terms of test time.

B. Monte Carlo Simulation for Tbulk-BICS Validation

The first objective is to verify that the proposed Tbulk-BICS can detect different current shapes in the presence of process and temperature variations. A large set of electrical simulations with the case-study circuit and the Tbulk-BICS were performed with different process variability conditions and at different temperatures. The Tbulk-BICS were able to successfully detect the injected current pulses when the trimming bits were correctly configured.

The Tbulk-BICS transistors were dimensioned as described in Table I to detect a large range of induced current shapes and deposited charges in the case study circuit. The final scheme respects the original design presented in Fig. 2 with the modifications proposed at Fig. 5. In order to simulate different deposited charges and transients with different durations, $\tau\alpha$ and I_0 were modified according to (1).

The trimming bits were adjusted to be able to detect small current pulses in presence of corner process variations and temperatures. Fig. 8 shows the Monte Carlo simulation results for 3 different temperatures when 100 Tbulk-BICS were evaluated under process variations.

The trimmer control circuit starts configuring the Tbulk-BICS by the configuration "0001," but not all

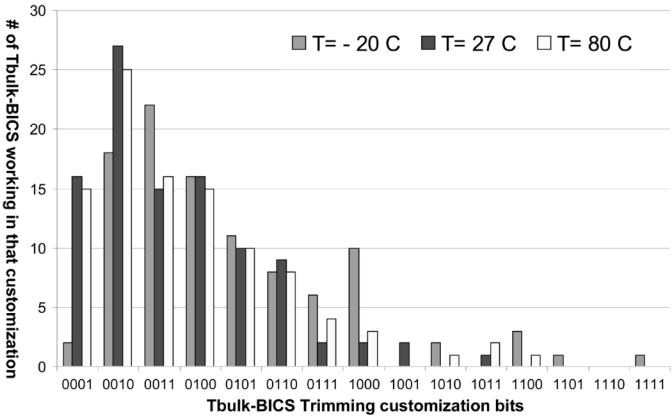

Fig. 8. Monte Carlo simulation results for 100 Tbulk-BICS: for each trimming configuration bits at three different temperatures, there is a certain amount of Tbulk-BICS customized by those trimming bits that work well in that process and temperature conditions.

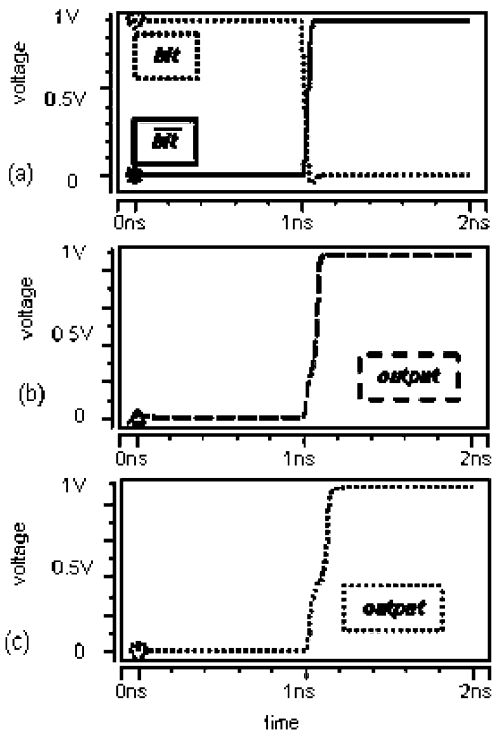

Fig. 9. (a) Soft Error in a memory cell and Bulk-BICS detection: (b) FF conditions and (c) SS conditions.

Tbulk-BICS can work properly under this configuration. The ones that fail at "0001" are then configured to "0010." The ones that fail in at "0010" are then configured to "0011" and so on. Note that there are just few Tbulk-BICS that were configured at the last configurations, such as "1101" and "1111."

Fig. 9 show the electrical simulation results of one example at $\mathrm{T} = -20°\mathrm{C}$. Fig. 9(a) shows results for a 1 to 0 flip of a memory cell at $\mathrm{t} = 1$ ns. This figure shows that the memory cell flips if a current pulse is injected with amplitude of 200 μA and $\tau\alpha = 30$ ps (injected charge equal to 6 fC). In this case, the injected charge flips the memory cell and the flip is detected by N-BICS, as shown in Fig. 9(b), for N-BICS with the bits combination "0010" and under SS corner conditions. Fig. 9(c) shows

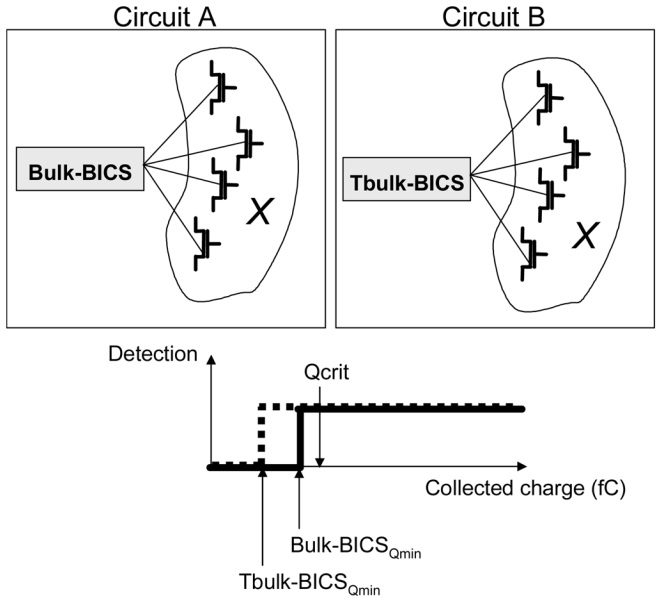

Fig. 10. Bulk-BICs vs. TBulk-BICSs for SET detection sensitivity and area overhead.

TABLE V
ANALYZING THE MINIMUM SENSITIVITY OF STANDARD BULK-BICS AND THE PROPOSED TBULK-BICS FOR SET DETECTION WHEN X TRANSISTORS ARE CONNECTED TO EACH SENSOR

Case	Parameter X	$\tau\alpha$ (ps)	I_0 (μA)	
			Bulk-BICS	TBulk-BICS
1	10	20	330	165
2	20	20	490	220
3	40	20	845	315
4	80	20	1525	655

N-BICS detection under FF corner conditions and with the bits combination "1110," for the same current pulse. Simulations at different temperatures were also performed and the BICS was found to work perfectly for all values.

C. Analyzing the Tbulk-BICS Sensitivity

Once the SET detection capability of the Tbulk-BICS was verified in the presence of variability in temperature and process, the second goal is to analyze how the sensitivity of the Tbulk-BICS can shift when using the trimming bits compared to the standard bulk-BICS. For this comparison, the bulk-BICS was designed in order to do not flip by itself in the presence of a FF corner case. But this designed sensor can loose its sensitivity in the presence of the SS corner case.

The example shown in Fig. 10 presents two circuits A and B, where in circuit A there are X transistors connected to each bulk-BICS and in circuit B there are also X transistors but now connected to each Tbulk-BICS. If both BICS are dimensioned with the same transistor sizes, which BICS can present a higher sensitivity for the collected charge?

Results presented in Table V shows that for 4 different cases, where the number of transistors connected to each sensor (parameter X) varies, for the same parameter $\tau\alpha$, the Tbulk-BICS could always be able to detect collected charges with a lower current peak (I_0) compared to the standard bulk-BICS. This means that the Tbulk-BICS could always be parameterized to be

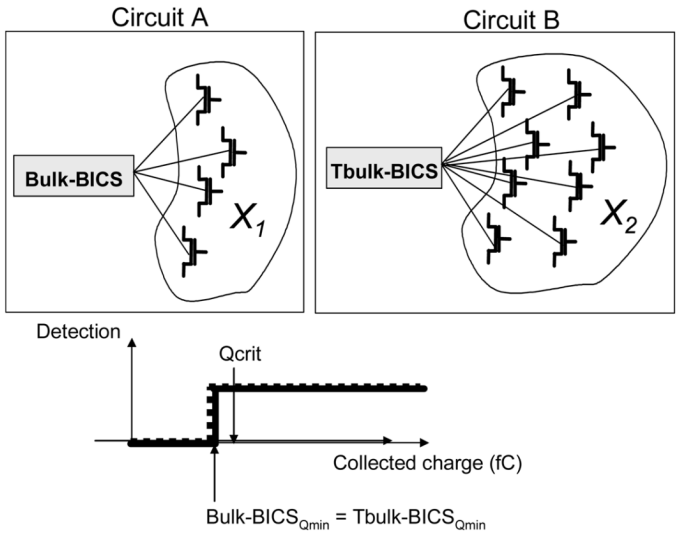

Fig. 11. Bulk-BICs vs. TBulk-BICSs for SET detection sensitivity and area overhead.

TABLE VI
COMPARISON OF THE NUMBER OF TRANSISTORS MONITORED BY A SINGLE BICS FOR A FIXIED MINIMUM REQUIRED SENSITIVITY WHEN USING BULK-BICS AND TBULK-BICS

Case	τ_α (ps)	I_0 (μA)	X_1	X_2
1	30	250	9	47
2	40	350	31	77
3	55	450	70	114

more sensitive to collected charges than the standard bulk-BICS, if both are monitoring the same number of transistors.

Now let one analyze the example shown in Fig. 11. In this case, there are two circuits A and B, where in circuit A there are X_1 transistors connected to each bulk-BICS, while in circuit B there are X_2 transistors connected to each Tbulk-BICS. If both BICS are dimensioned with the same transistor sizes and both BICS are able to detect the same minimum collected charge, which sensor can monitor a large number of transistors at the same time?

The answer is shown in Table VI. X_2 can be considerably larger than X_1, as expected. Results show that for 3 different cases, where the parameters $\tau\alpha$ and I_0 vary, in other words, the minimum detectable collected charge varies, the Tbulk-BICS could always be able to detect this minimum collected charges when monitoring a larger number of transistors. This means that because the Tbulk-BICS can be parameterized, it is possible to find an efficient configuration of the trimming bits that makes the Tbulk- BICS more sensitive to minimum collected charges than the standard bulk-BICS, or more efficient in terms of the number of transistors that can be monitored at the same time by a single BICS.

VI. CONCLUSION

The authors have presented the Tbulk-BICS to detect transient faults in combinational and sequential circuits in the presence of process and temperature variations. The proposed trimmer circuit, which can be built in the chip, was validated through Monte Carlo simulations. Results show the efficiency of the Tbulk-BICS to detect transient faults in the presence of process and temperature variation corners. Future work will focus on the design, fabrication and test of a chip with an integrated Tbulk-BICS under radiation and laser ground testing at different temperatures.

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