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Design of a D-Band CMOS Amplifier Utilizing Coupled Slow-Wave Coplanar Waveguides

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***Abstract*—This paper validates a design and modeling methodology of coupled slow-wave waveguides (CS-CPW) by presenting a D-band CMOS low-noise amplifier (LNA) which utilizes the CS-CPW for impedance matching. The robustness and feasibility of using the CS-CPW as a matching element in wideband millimeter-wave (mm-wave) silicon circuit designs are studied. Furthermore, the key design details of a mm-wave LNA are discussed. The designed monolithic microwave integrated circuit (MMIC) amplifier has a gain greater than 10 dB from 135 GHz to 170 GHz with a peak gain of 15.7 dB at 160 GHz. The amplifier has a measured noise figure of 8.5 dB from 135 to 170 GHz, and an output-referred 1-dB compression point of -16.5 dBm at 160 GHz. The total power consumption of the amplifier is 32 mW.**

***Index Terms*—Amplifier, coupled transmission lines, coupled slow-wave coplanar waveguide, CMOS, D-band, LNA, millimeter wave integrated circuit, MMIC, S-CPW, Slow-wave coupled line, Silicon, 140 GHz, 170 GHz.**

I. Introduction

ADVANCES in CMOS technology enable the design of front-end circuits at millimeter-wave (mm-wave) frequencies. Radio applications beyond 100 GHz, such as mm-wave imaging systems [1], short-distance high data-rate communication links [2], radar systems [3], and even atmospheric remote sensors [4], [5] will benefit from the high-yield, cost-effective (in terms of mass production), and the high-level of integration offered by CMOS technology. The design of mm-wave CMOS circuits above 100 GHz is challenging because of the low-gain in active devices and a high-loss in passive components. Despite the fact that the latest CMOS technology nodes can provide a moderate gain at mm-wave frequencies, the challenge remains in the design of low-loss passives due to the close proximity of a low-resistive silicon substrate.

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In mm-wave designs, transmission lines are preferred for the matching networks rather than lumped elements because the reactance of transmission lines is more predictable and less influenced by the surroundings compared to that of lumped spiral inductors. Furthermore, transmission lines are scalable in length which makes them ideal components for mm-wave matching network designs.

A transmission line type which is widely used in mm-wave designs is the coplanar waveguide (CPW) because it provides a high inductive quality factor by using well-defined ground-current return paths [6]. However, traditional CPWs in a CMOS process suffer from a loss arising from the low-resistivity silicon substrate [7]. Microstrip lines (MS-lines) in CMOS, on the other hand, are shielded from the lossy silicon substrate by a ground-plane which is usually realized with the lower metal layers from the technology. However, the lower metal layers are typically thinner in a deep sub-micron CMOS technology. Therefore, the MS-lines suffer from high conductive losses. Moreover, the distance between the signal line and the ground plane is limited in standard CMOS technologies. Hence, the MS-lines have a low-inductive quality factor compared to that of the CPWs. Use of a slow-wave coplanar waveguide (S-CPW) [8] can solve the problems mentioned above associated with the design of the transmission lines. The S-CPW utilizes slow-wave shielding under the conventional CPWs to reduce the electric field coupling to the substrate, whereas the ground-current return paths remain the same as in regular CPWs [7].

Another line type, a coupled transmission line, is widely used in microwave filter and coupler designs [9]. However, it has been shown that the coupled transmission line can also be used as an impedance transformer through proper choice of even- and odd-mode characteristics impedances [10]. The use of coupled transmission lines as the matching elements in mm-wave multistage amplifier designs have a few advantages over the conventional matching structures. Most importantly, the potential modeling errors and loss of the DC-decoupling capacitors [5], [11]-[13] can be avoided by using coupled line structures. Furthermore, the structure is robust to process variations [14].

The coupled line structures are usually realized with an MS-line. However, with the microstrip coupled (MS-CP) lines on silicon, it is often challenging to obtain the required odd- and even-mode impedances needed for an impedance transformation. This is because the odd- and even-mode impedances are dependent on each other and there is no possibility to control those independently [15]. In addition to this, MS-

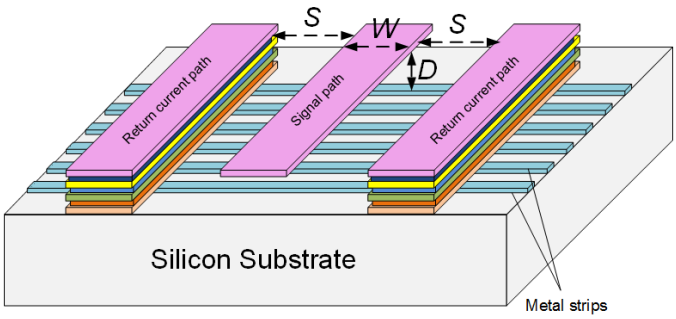

Fig. 1. Simplified view of a slow-wave coplanar waveguide (S-CPW) structure in CMOS technology. Metal strips are placed in between the conventional coplanar waveguide and the silicon substrate. The densely-spaced metal strips are positioned perpendicular to the direction of signal propagation.

CP lines have a low-inductive quality factor like in the same way as regular MS-lines. To implement the coupled lines on silicon technologies in an efficient manner and to control the odd- and even-mode impedances separately, an engineering method is approached in [16]. In [16], a design and modeling methodology of a coupled slow-wave coplanar waveguide (CS-CPW) is proposed which includes well-defined ground-current return paths for the even-mode signal propagation and slow-wave shielding. The well-defined ground-current return paths for the even-mode give an opportunity to control the odd- and even-mode impedances independently and, consequently, the CS-CPW structure offers significant flexibility in achieving a broad range of impedance transformation ratio.

Besides the CS-CPW presented in [16], another way of implementing the CS-CPW is proposed in [17]. However, there the CS-CPW is used for designing the coupled-lines couplers and used cut shielding strips. In this work, the design and modeling technique of the CS-CPW proposed in [16] is verified by realizing a D-band CMOS low-noise amplifier (LNA) which utilizes the CS-CPWs as matching elements. A theoretical analysis is also conducted to study the feasibility and robustness of the CS-CPW as a matching element in mm-wave CMOS amplifier designs. Moreover, an extensive study is carried out on the design of an optimum transistor layout for mm-wave LNA circuit designs.

This paper is organized as follows. In Section II, the S-CPW structure and its modeling are briefly reviewed to support the concept of designing the CS-CPW. Section III introduces the design and modeling technique of the CS-CPW in detail. Analysis of the CS-CPW as an impedance transformer and its robustness is covered in Section IV. Section V describes the key design details of the D-band amplifier. Finally, the measured performance of the LNA is presented and compared with the state-of-the-art published results in Section VI.

II. S-CPW Transmission Line

In silicon technology, an S-CPW structure is formed by placing densely-spaced metal strips under the conventional CPW structure to prevent the penetration of electromagnetic (EM) fields into the low-resistive silicon substrate. A simplified view of an S-CPW in CMOS technology is shown in Fig. 1. The metal strips are placed perpendicular to the direction of RF signal propagation. The widths of the metal strips and the gap between two adjacent strips must be much smaller than the vertical distance of the signal line to the bottom metal strips to ensure that the metal strips under the signal lines behave like a good Faraday cage [18]. A Faraday cage is a conductive enclosure with a fine metal mesh which can attenuate the EM fields. The amount of attenuation depends on the frequency of operation because the thickness of holes or gaps present in the enclosure must be significantly smaller than the wavelength of the EM waves.

When the substrate is shielded, the capacitive quality factor of the regular CPW is improved. Nonetheless, since the signal path and the ground-current return paths do not change, the inductive quality factor remains the same. Furthermore, the effective dielectric constant and thus the wavelength of an S-CPW is adjustable by varying the gap between the signal line and the metal shields plane *(D)*. This artificial wavelength reduction allows more compact implementation of the transmission lines for the impedance transformations and interconnections [8].

However, modeling of the S-CPWs by EM simulations is complicated due to the presence of densely-gridded metal shields, and can only be accurately modeled by a 3-D simulator [19]. Usually, modeling by a 3-D simulator is tedious and time-consuming. In [18], a simple and computationally efficient modeling technique is proposed to characterize the S-CPW structures that can also be modeled by a 2.5-D simulator, which is simpler compared to a 3-D simulator. In the proposed technique, the EM analysis is decoupled into two, independent electric- and magnetic-analysis. The magnetic-problem properties are defined by the resistance and inductance (R and L) of the metal conductors whereas the electric-problem properties are defined by the capacitance and shunt conductance (C and G) of the dielectric materials. The R, L, C, and G values are the per-unit length frequency-dependent distributed-transmission line parameters from the telegrapher's equation [20] which support the transverse electromagnetic (TEM) propagation. It is assumed that the slotted bottom metal shields of the S-CPW structure do not carry any longitudinal currents. Therefore, the shields have a negligible influence on the R and L parameters. A small amount of eddy currents, however, may be induced but they are negligible [18]. Nonetheless, for sufficiently dense metal shields, the C and G parameters per unit length are identical to those where a solid metal replaces the gridded metal strips. This condition is valid when the above-explained Faraday cage phenomenon is satisfied [18]. Thus, the R and L parameters can be simulated from the conventional CPW structure where there are no metal shields underneath the structure, and the C and G parameters are simulated from the structure where a solid metal shield replaces the gridded metal shields of the S-CPW.

III. CS-CPW Transmission Line

A CS-CPW transmission line is formed in silicon technology by placing a similar kind of densely-spaced slotted metal strips as in the S-CPW under two closely-spaced signal lines

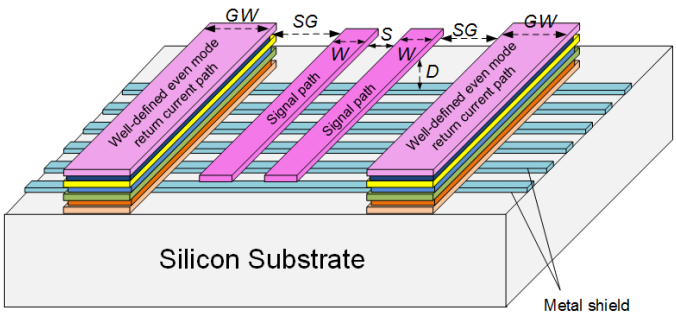

Fig. 2. Simplified view of a coupled slow-wave coplanar waveguide in CMOS technology. Densely-spaced metal strips are placed in between the coupled transmission lines and the silicon substrate. Side grounds are utilized on both sides of the signal lines to explicitly model the even-mode ground-current return paths.

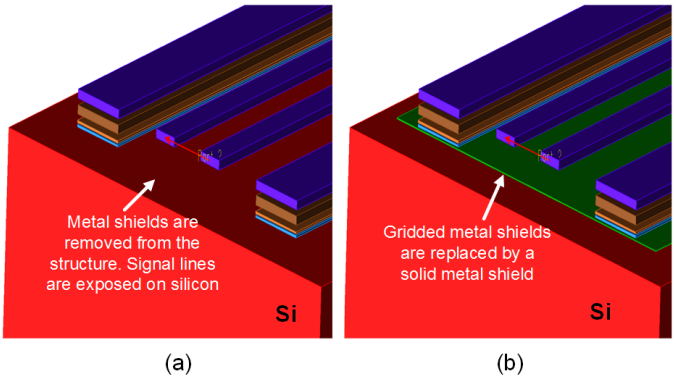

Fig. 3. Illustration of odd-mode electromagnetic analysis of a CS-CPW. (a) Analysis of odd-mode R and L parameters. (b) Analysis of odd-mode C and G parameters.

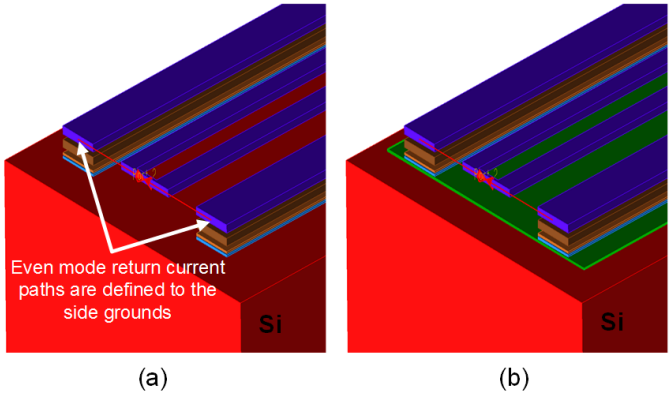

Fig. 4. Illustration of even-mode electromagnetic analysis of a CS-CPW. (a) Analysis of even-mode R and L parameters. (b) Analysis of even-mode C and G parameters.

and side ground lines. The slow-wave grids (slotted metal strips) can be placed either as floating [8] or grounded [18]. The idea of putting the metal strips as floating is to ensure the voltage on the shield to be 0 V with respect to the CPW. Furthermore, the grounded shield may yield circuit parasitics. Nevertheless, we have preferred grounded shielding for two main reasons. First, if grounded, the EM simulations are more well-defined. Second, as stated in [18], a floating shield might not provide adequate substrate isolation, and results in significant substrate loss especially at high frequencies. A simplified view of a CS-CPW in CMOS technology is shown in Fig. 2.

When a coupled line is used in a differential design, the knowledge of odd-mode line parameters is the matter of interest, exact knowledge of the even-mode parameters is less critical as shown in [21]. However, when a coupled line is used as an impedance transformer, both the odd- and even-mode line parameters are equally important [10]. Therefore, the ground lines are placed on both sides of the signal lines to provide well-defined even-mode ground-current return paths in order to explicitly model the even-mode line parameters as explained in [16].

A similar methodology for modeling the S-CPW structure discussed in the previous section can be used to model the CS-CPW structure as explained in [16]. For modeling a CS-CPW structure, the EM problem is first divided into odd- and even-mode analysis, and then each mode is further separated into the R & L, and the C & G analyses.

A. Odd-mode Analysis

In the odd-mode analysis, the two signal lines of the CS-CPW structure are excited by the signals that are equal in amplitude but opposite in polarity. The odd-mode line parameters can be defined by changing the geometric parameters of the CS-CPW: the widths of the signal lines *(W)*, the gap between the signal lines *(S)*, and the distance from the signal lines to the metal shield planes *(D)* [see Fig. 2].

The odd-mode line parameters, R_{odd} and L_{odd} can be obtained from the EM structure shown in Fig. 3(a), where there are no bottom metal strips. The other two line parameters, C_{odd} and G_{odd} can be obtained from the EM structure shown in Fig. 3(b) where the slotted bottom metal strips are replaced by a solid metal plane.

B. Even-mode Analysis

In the even-mode analysis, the two signal lines from the CS-CPW structure are excited by the signals which have the same amplitude and polarity. The even-mode ground-current return paths are defined by the side ground lines as shown in Fig. 4. The even-mode line parameters can also be controlled by modifying the geometric parameters of the CS-CPW: the widths of the signal lines *(W)*, the gap between the signal lines *(S)*, and the distance from the signal lines to the metal shield planes *(D)*. Since the side ground lines define the even-mode ground-current return paths, the even-mode line parameters can further be modified by adjusting the gaps between the signal line and the CPW ground line *(SG)* and by changing the width of the ground lines *(GW)*.

The even-mode R and L parameters denoted as R_{even} and L_{even} can be obtained from the EM structure shown in Fig. 4(a), where the bottom metal strips, shown in Fig. 2 are removed from the CS-CPW structure. The even-mode C and G parameters denoted as C_{even} and G_{even} can be obtained from the EM structure shown in Fig. 4(b) where the slotted bottom metal strips are replaced by a solid metal plane.

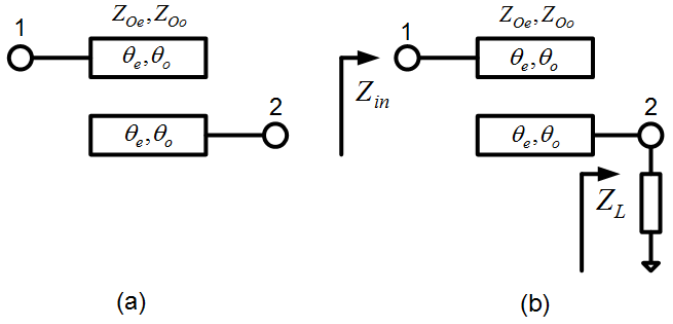

Fig. 5. Coupled line in inhomogeneous medium.

C. Scalable CS-CPW model

S-parameter data sets obtained from the above-explained four EM simulations are used to calculate the line parameters, R_{odd}, L_{odd}, C_{odd}, G_{odd}, R_{even}, L_{even}, C_{even}, and G_{even} by using the equation sets stated in [22]. Afterward, these line parameters are used to characterize a scalable CS-CPW model by odd- and even-mode characteristic impedances (Z_{0o}, Z_{0e}), relative effective dielectric permittivity (ϵ_{ro}, ϵ_{re}), and attenuation per meter (α_o, α_e) [20]. Finally, the essential model parameters are inserted into a scalable lossy coupled transmission line model called $CLINP$ from the simulator Keysight's ADS [23] to realize the scalable CS-CPW model.

IV. Analysis of Coupled Slow-wave Coplanar Waveguide

A. CS-CPW as an Impedance Transformer

Coupled lines realized in a microstrip environment usually assume that the odd- and even-mode phase velocities are equal [14]. However, since in a CS-CPW, the even-mode ground-current return paths are defined to the side ground lines, the effective dielectric permittivity, therefore, the phase velocities can be different in odd- and even-mode propagation. This scenario can be better described by the two identical coupled transmission lines embedded in an inhomogeneous dielectric medium. The impedance matrix of an inhomogeneous coupled line section as in Fig. 5(a) can be written as [24]

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \tag{1}$$

where

$$Z_{11} = Z_{22} = -j\frac{Z_{0e}cot\theta_e + Z_{0o}cot\theta_o}{2}$$

$$Z_{12} = Z_{21} = -j\frac{Z_{0e}csc\theta_e - Z_{0o}csc\theta_o}{2} \tag{2}$$

Here, θ_e and θ_o are the electrical lengths and Z_{0e} and Z_{0o} are the characteristic impedances of the coupled line section of Fig. 5(a) for even- and odd-mode, respectively. If port 2 is terminated with an impedance Z_L as in Fig. 5(b), the input impedance seen from port 1 can be written as

$$\begin{aligned} Z_{in} &= Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22}+Z_L} \\ &= -j\frac{Z_{0e}cot\theta_e + Z_{0o}cot\theta_o}{2} + \frac{\frac{1}{4}\left(Z_{0e}csc\theta_e - Z_{0o}csc\theta_o\right)^2}{Z_L - j\frac{Z_{0e}cot\theta_e + Z_{0o}cot\theta_o}{2}} \end{aligned} \tag{3}$$

After some simplification the real and the imaginary part of the input impedance can be written as

$$Z_{in}(Re) = \frac{Z_L(Z_{0e}csc\theta_e - Z_{0o}csc\theta_o)^2}{4{Z_L}^2 + (Z_{0e}cot\theta_e + Z_{0o}cot\theta_o)^2} \tag{4}$$

$$\begin{aligned} Z_{in}(Im) = &\left(\frac{(Z_{0e}csc\theta_e - Z_{0o}csc\theta_o)^2}{4{Z_L}^2 + (Z_{0e}cot\theta_e + Z_{0o}cot\theta_o)^2} - 1\right) \\ &\times \left(\frac{Z_{0e}cot\theta_e + Z_{0o}cot\theta_o}{2}\right) \end{aligned} \tag{5}$$

For the MS-CP lines, at resonance, where θ_o=θ_e=$\pi/2$, the impedance transformation is dependent on the square of the difference between the even- and odd-mode characteristic impedances and not on their absolute values according to (4) and (5). The length of the line is adjusted to match the imaginary part. This imaginary part can be further controlled by adding reactive components at the open ends of the coupled line [10].

On the other hand, for the CS-CPWs, since the even- and odd-mode electrical lengths may not be equal, the impedance transformation is not only dependent on their difference in characteristic impedance but also on their even- and odd-mode electrical lengths (4). Nevertheless, the effect of this inhomogeneity on impedance transformation is not significant and is examined in the following sub-section.

B. Robustness of Coupled line Structures

First, to see the robustness of the CS-CPW structures to the fabrication and process variations, a CS-CPW structure is simulated with three different process corners from the chosen CMOS technology. The corners are defined as RC_{min}, RC_{max}, and $RC_{nominal}$, and these basically differ by different dielectric thicknesses. The even- and odd-mode characteristic impedances and effective dielectric permittivity of a CS-CPW for the different process corners are simulated and shown in Fig. 6. It can be observed from this figure that about $\pm$12% change in characteristic impedances and $\pm$15% change in effective dielectric permittivity may occur from the process variations. Nevertheless, the difference between the even- and odd-mode characteristic impedances and effective dielectric permittivity remain relatively constant over the different process corners.

The effect of these changes on the even- and odd-mode characteristic impedances on impedance transformation is deduced by using (4) and (5), and plotted in Fig. 7. Both a CS-CPW and an MS-CP line are simulated for this analysis. Different odd- and even-mode electrical lengths are set for the CS-CPW, whereas for the MS-CP line equal electrical lengths are used. The values are taken from the nominal process corner of the technology. A physical length of 162 μm for the CS-CPW and

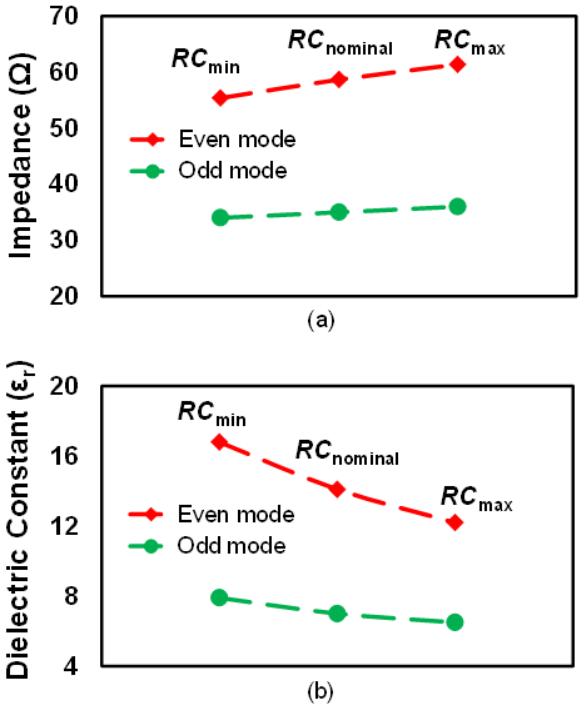

Fig. 6. Variations of odd- (green) and even-mode (red) (a) impedances and (b) effective dielectric permittivity of a CS-CPW for different process corners from the technology.

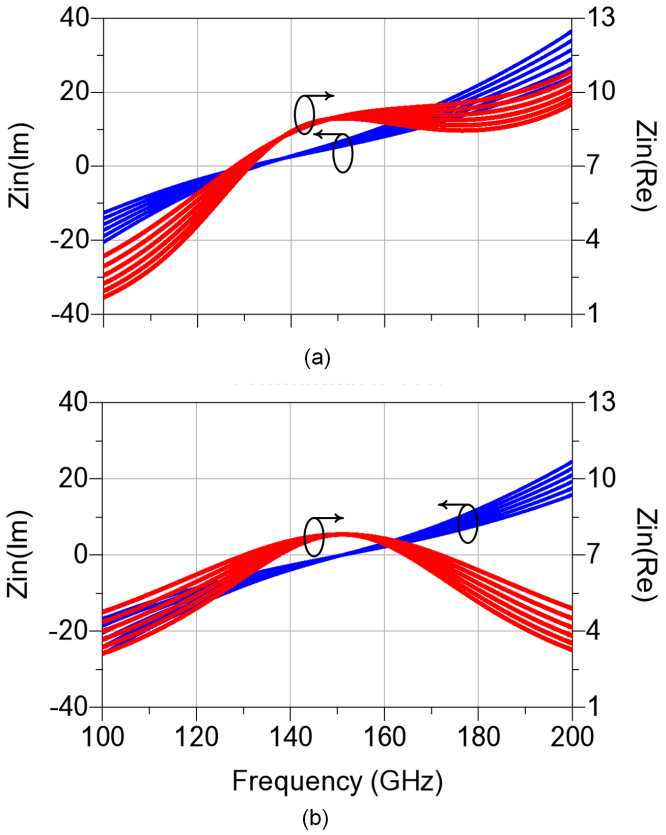

Fig. 7. Effect on input impedance for changing odd- and even-mode impedances by ±12% with 4% stepping while keeping their difference constant (a) CS-CPW line and (b) MS-CP line.

245 μm for the MS-CP line are used to simulate the quarter wavelength line at 150 GHz.

the real and imaginary parts of the input impedances seen from port 1 of Fig. 5(b) are plotted in Fig. 7. The even- and odd-mode impedances are varied by ±12% with 4% stepping from the nominal value while their differences are kept constant. For this study, the value of Z_L in Fig. 5(b) has been set to 20 Ω. It is obvious from Fig. 7 that both CS-CPW and MS-CP line structures show a negligible effect on the impedance transformation in changes to the absolute values of odd- and even-mode characteristic impedances. This property indicates the tolerance of such structures to the technology variations and modeling errors at mm-wave frequencies. Even though the CS-CPWs have different electrical lengths in odd- and even-mode propagation, it shows a minimal effect on the impedance transformation within a wide bandwidth. Like the MS-CP line structures, the impedance transformation is mainly dependent on the difference between the even- and odd-mode characteristic impedances also for the CS-CPWs. Furthermore, the analysis results in Fig. 7 show that the impedance transformation does not change rapidly over frequency. This phenomenon further indicates the potentiality of using the coupled line structures (for both types: CS-CPW and MS-CP line) as the matching elements for the broadband mm-wave amplifier designs.

C. Advantages of CS-CPW over MS-CP line

The previous sub-section show that both the CS-CPWs and the MS-CP lines are useful matching elements in reliable and wideband mm-wave amplifier designs. Nonetheless, the CS-CPWs have a few key advantages over the MS-CP line. Most importantly, the CS-CPW structures can offer independent controllability over the odd- and even-mode characteristic impedances. This fundamental property of the CS-CPW offers great flexibility for impedance transformation. We have learned from Section III that the odd-mode line parameters are dependent on three geometric parameters, *W, S,* and *D*, whereas, the even-mode line parameters are dependent on five geometric parameters, *W, S, D, SG,* and *GW*. Since the even-mode ground-current return paths are explicitly defined to the side-ground lines, therefore, these two additional geometric parameters have an influence on the even-mode line parameters. From the other side, in the odd-mode propagation, a virtual ground is created in between the signal lines, and all the field currents are confined to the signal lines area. Therefore, the side-ground lines have an insignificant influence on the odd-mode line parameters. To support this statement, we have varied the geometric parameters *SG* and *GW* and we have observed the changes in odd- and even-mode impedances. It can be seen from Fig. 8 that the presence of side ground lines has a negligible influence on the odd-mode impedances, and the even-mode impedance can be adjusted without altering the odd-mode impedance.

Important figures of merit for a transmission line on silicon are the inductive quality factor (Q_L) and the capacitive quality

TABLE I
PROS AND CONS OF DIFFERENT TRANSMISSION LINES ON SILICON

Transmission line type	Shielded from Silicon	Inductive Quality factor	Capacitive Quality factor	$\lambda/4$ Resonator length	CAD modeling	Routing in layout	Separate controllability of odd- and even-mode impedances
CPW	no	good	poor	longer	unreliable*	complex	N/A
MS line	yes	poor	good	longer	reliable	easy	N/A
S-CPW	yes	good	good	shorter	reliable	complex	N/A
MS-CP line	yes	poor	good	longer	reliable	easy	no
CS-CPW	yes	good	good	shorter	reliable	complex	yes

*simulation results may be erogenous because the EM fields travel to the lossy silicon substrate and that is often hard to capture in simulation.

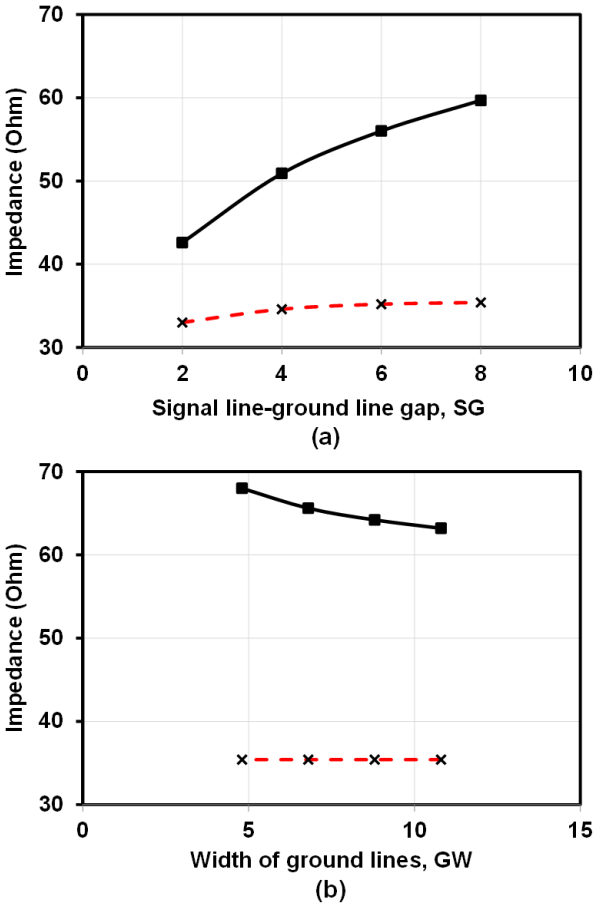

Fig. 8. Changes in odd- (dashed) and even-mode (solid) impedances when (a) the gap between the signal line and side-ground line is varied and (b) the width of the side-ground line is varied.

factor (Q_C) [6]. Therefore, we have simulated a CS-CPW and an MS-CP line and compared the quality factors in Fig. 9. As expected, the CS-CPW has a better inductive quality factor and similar capacitive quality factor compared to the MS-CP line in the odd-mode propagation. Nevertheless, a better capacitive quality factor in the even-mode propagation is achieved because of the defined even-mode ground-current return paths to the side-ground lines.

Finally, based on our studies, we have drawn a table (Table I) and compared the pros and cons of the transmission lines those are commonly used on a silicon substrate.

D. Limitation of the presented CS-CPW structure

Theoretically, with the CS-CPW structure, it is possible to match to any impedance. However, due to technology specific design rules, we cannot modify the geometric parameters of the CS-CPW arbitrarily. Hence, it is not feasible to achieve all kinds of impedance transformations. Based on the simulations, a maximum difference between Z_{0o} and Z_{0e} of 40 Ω is achievable with the technology in use. Nonetheless, the ratio of Z_{0o} and Z_{0e} can be increased further by improving the capacitive coupling by utilizing specialized structures, for example, the one used in [25].

The limitation in the bandwidth of matching of the presented CS-CPW structure is being studied, and the insertion loss from two impedance matching ratios are plotted in Fig. 10. Going back to Fig. 5(b), Z_{in} is matched to Z_L for the matching ratio of 1:6.25 ($Z_{in} = 50\Omega$ to $Z_L = 8\Omega$) and the matching ratio of 1:2 ($Z_{in} = 30\Omega$ to $Z_L = 15\Omega$) at 150 GHz. In both cases, the CS-CPW section has $Z_{0o} = 30\Omega$ and $Z_{0e} = 70\Omega$. A bandwidth of 15% (w.r.t. -1.5 dB insertion loss) is obtained with the higher matching ratio; whereas for the lower matching ratio, 25% bandwidth is achieved. One important point that is not captured in this analysis, open-stabs at the open ends of the CS-CPW, and the length of the matching section, also has an influence on impedance matching.

V. AMPLIFIER DESIGN

A. Technology

The D-band MMIC amplifier is fabricated using a commercially available 28-nm CMOS FDSOI process. A simplified cross section of the process back-end of line (BEOL) is shown in Fig. 11. The BEOL consists of a thick aluminum layer ($ALUCAP$) and ten copper layers ($M1$-$M10$). The relative thicknesses of the metal layers are indicated as 1x, 2x and 8x.

B. Transistor design

At mm-wave frequencies, it is critical to get the most of what a transistor has to offer in terms of gain and noise performances. To this end, the transistor layouts should be optimized to minimize the device parasitic resistances and capacitances. The layout techniques to enhance the RF performance of transistors have been investigated extensively in [26]-[28]. A common approach used by circuit designers is to select an optimum unit gate width for a single finger and then place these fingers in parallel to form a transistor [26],

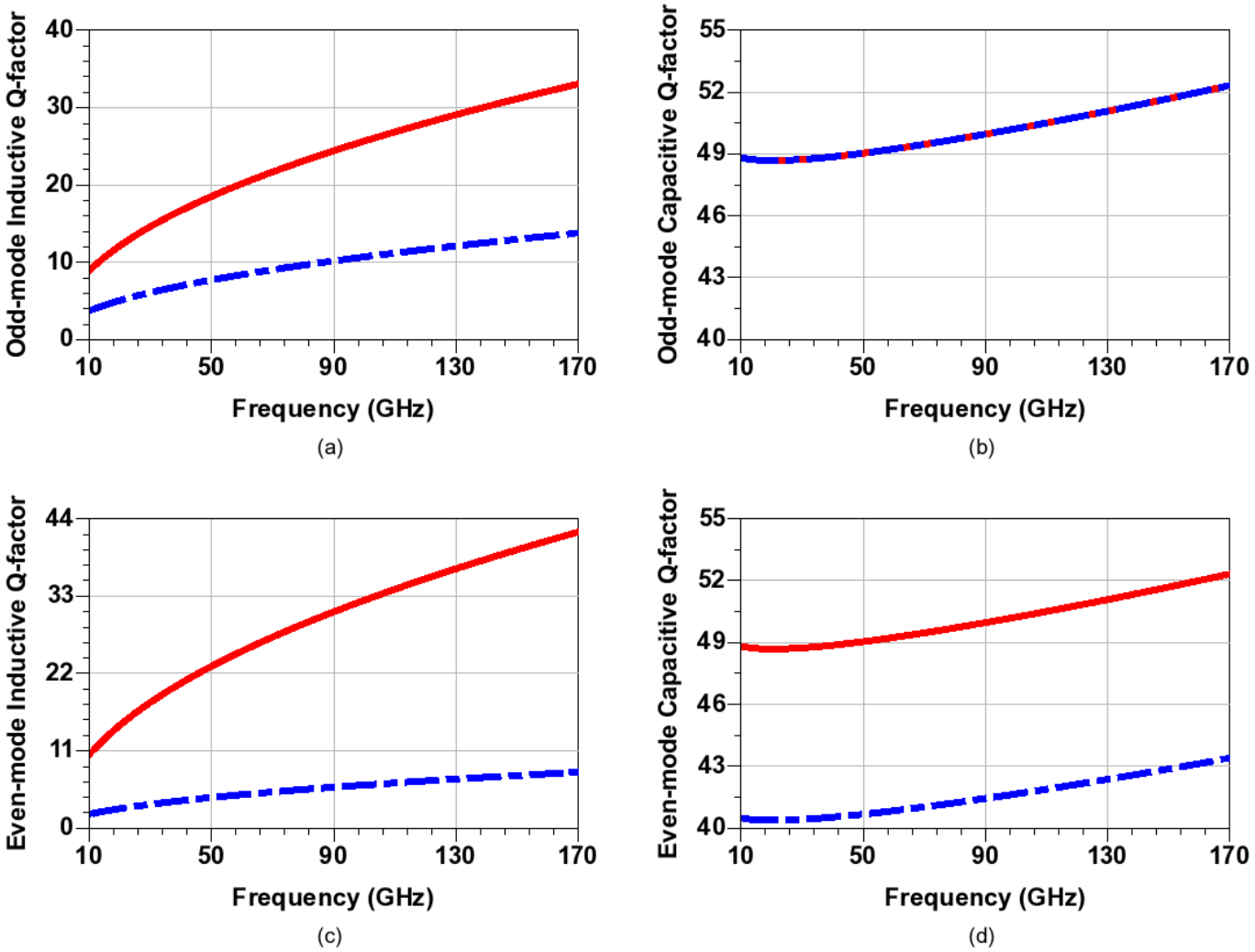

Fig. 9. Simulated Q_L and Q_C for a CS-CPW (solid) and an MS-CP line (dashed) in odd- and even-mode propagation. (a) Odd-mode Q_L. (b) Odd-mode Q_c. (c) Even-mode Q_L. (d) Even-mode Q_c. The same odd impedances are chosen for both line types for fair comparison.

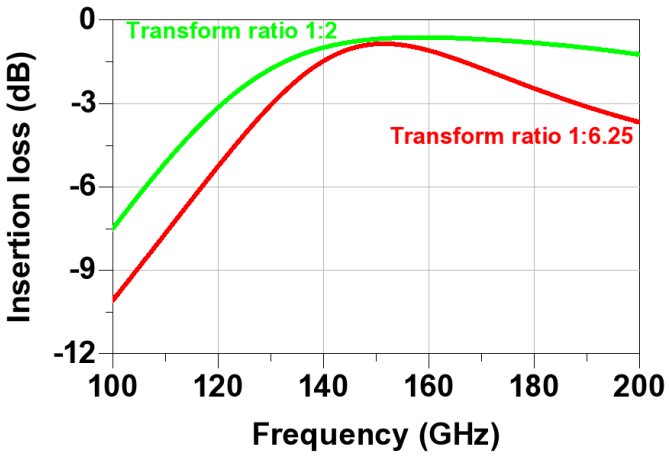

Fig. 10. Insertion loss of a CS-CPW section while matching ratio is 1:2 (green) and 1:6.25 (red) over frequency.

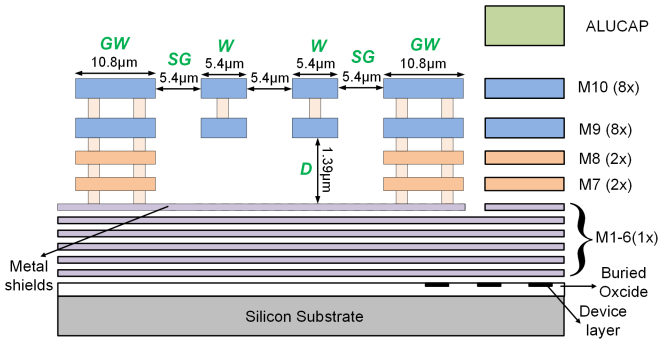

Fig. 11. Cross-section of the simplified 28-nm CMOS FDSOI process back-end of line with slow-wave coupled transmission line used in this work.

[29], [30]. Ideally, altering the number of fingers should affect neither the gain [31] nor the minimum noise [12] of the transistor. However, in practice, the parasitics arising from the metal sections connecting the fingers to the device port will degrade both the gain and the noise performances. Moreover,

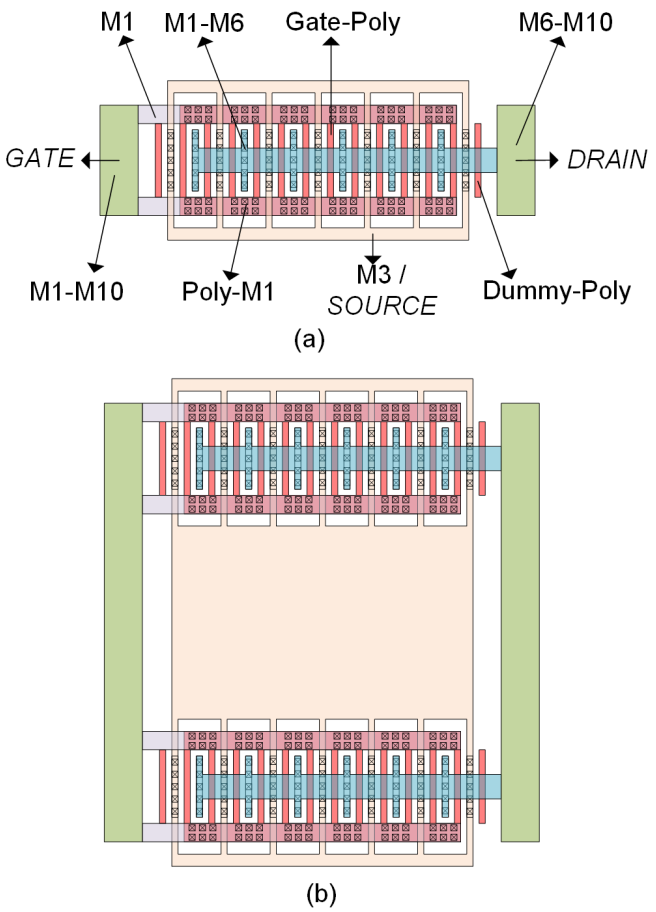

Fig. 12. (a) Layout of a unit cell transistor (b) Connection of the device.

the layout of the transistor will stretch only in one dimension making the distributed effects more prominent. As a result, the modeling of the device becomes more challenging. This is critical particularly in CMOS, where many extremely narrow fingers in parallel are required, in contrast to GaAS FETs with metal gates, where relatively few fingers of wide devices are typically used [6].

To overcome this problem, we have optimized the layout of the unit cell transistors which we can connect in parallel to other unit cells without deteriorating the gain and noise performances of the transistor. First, the general structure of the unit cell is arranged in order to minimize the parasitics associated with the transistor layout. Second, the finger width and the number of fingers in a unit cell are optimized in order to achieve low noise performance at mm-wave frequencies. Finally, several unit cells are connected in parallel, and the resultant noise performance is compared with that of a single cell.

Fig. 12(a) illustrates the layout of a unit cell transistor and how several of them can be connected to increase the transistor size. The layout details of the unit cell can be summarized as follows. Poly-silicon gates are connected to the $M1$ layer on both sides of each finger with two rows of poly-to-$M1$ via arrays in order to reduce the gate resistance *(R_g)*. The double-sided source connection through $M3$ layer reduces the source resistance *(R_s)* while keeping the gate-to-source capacitance *(C_{gs})* low. While a lower C_{gs} leads to a lower minimum noise figure [32], reducing R_g and R_s improves both the maximum frequency of oscillation *(f_{max})* [33] and the noise performance [32]. The drain connection at the $M6$ layer lays above the fingers so that both gate-to-drain and drain-to-source capacitances (C_{gd} and C_{ds}) remain low. A lower C_{gd} will lead to a higher f_{max} and gain [34], while a lower C_{ds} will simplify the matching. The technology in use offers both regular- and relaxed-pitch transistors. The relaxed-pitch transistors are chosen because they have a higher cut-off frequency *(f_t)* and higher transconductance *(g_m)* [35]. Finally, dummy poly strips are placed on both sides of the device to minimize the effects of undercutting the poly on the outer edges after patterning. Without the dummy poly strips, the poly would have been etched out more under the outermost gates, resulting in a mismatch between the parallel fingers [36].

Once the general structure of a unit cell is fixed, the analysis moves on to optimize the finger width and number of fingers in the unit cell which can significantly affect the high-frequency noise performance of the transistor. However, first, we need to decide how to measure the noise performance of a device at mm-wave frequencies. The well-known Frii's equation indicates that the overall noise performance of a cascade depends both on the noise factor *(F)* and the available power gain of each stage [37]. Using Frii's equation, Haus and Adler have shown that the noise measure *(M)* is the merit to evaluate the noise performance of the individual stages in a multi-stage LNA [38]. Unlike the noise factor, the noise measure takes into account both the noise and the gain of an amplifier stage. Basically, the lower the *M*, the better the noise performance of an individual stage. Furthermore, the minimum noise measure *(M_{min})* of a transistor remains the same when a lossless feedback element is connected to the transistor, meaning that the M_{min} is a valid figure of merit regardless of the feedback configuration utilized [39]. Therefore, the M_{min} is chosen as the figure of merit when comparing the mm-wave noise performances of different transistors.

To start with, we have simulated the noise and the S-parameters of a set of unit cell transistors having different numbers of fingers. In CMOS transistors, it is preferred to use narrow fingers close to 1 μm [6], [26], hence, for this study, we have considered the finger width to be 0.9 μm. In order to make a fair comparison, the layout parasitics generated through RC extraction up to the top metal layer are included in the device simulations, and all transistors are biased with an equal current density. The M_{min} values have been calculated with the equation set given in [40] which makes use of the noise and the S-parameters of the device. Fig. 13 illustrates the change in the M_{min} value with an increasing number of fingers in a unit cell transistor at 160 GHz. As can be seen, the M_{min} increases monotonically with the number of fingers in a unit cell. This is mainly because the $M1$ layer connecting the fingers to the gate port of the transistor gets longer, and consequently the gate resistance increases.

Finally, multiple unit cell transistors are connected in parallel, and the change in the M_{min} value is observed with an increasing number of unit cells. Again, the layout parasitics

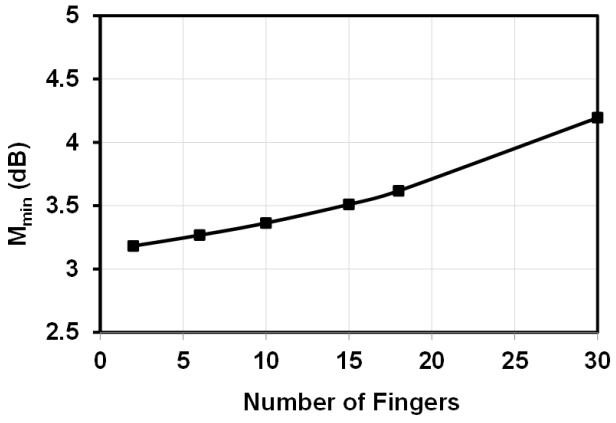

Fig. 13. M_{min} vs. number of fingers in a unit cell transistor at 160 GHz.

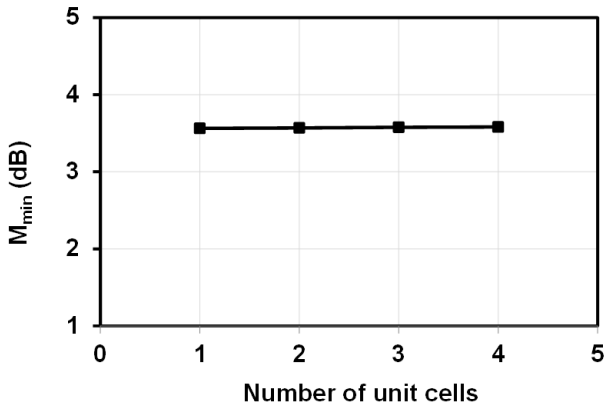

Fig. 14. M_{min} vs. number of unit cells at 160 GHz where each cell contain 12 fingers.

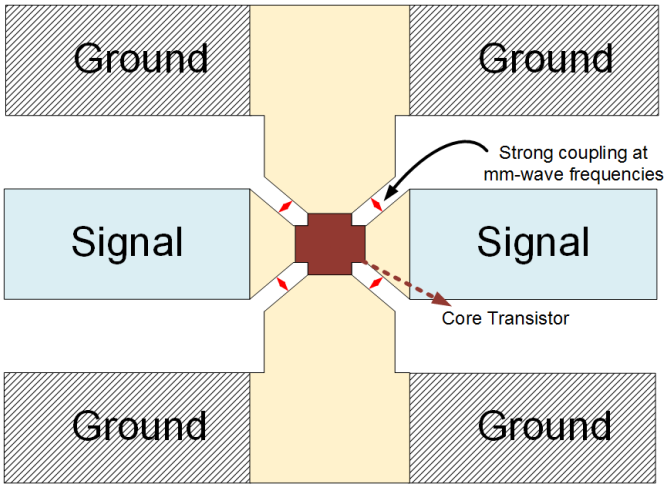

Fig. 15. Core device and the access for the CPW design environment showing coupling among different sections of access metalization.

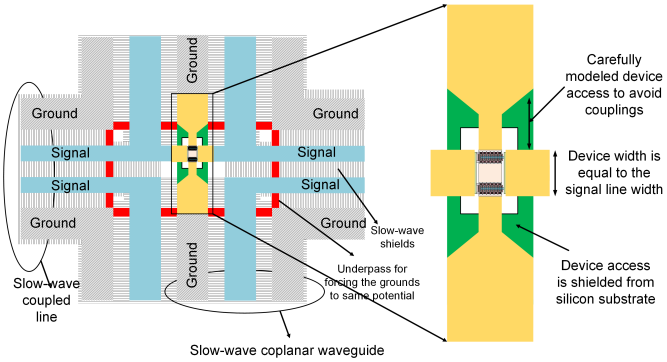

Fig. 16. Carefully designed device access and detail connection of device to slow-wave coupled lines.

generated through RC extraction up to the top metal layer are included in the device simulations to account for the connecting wiring between the cells. Fig. 14 clearly depicts that the M_{min} value remains the same as the number of unit cells connected in parallel increases, meaning that the proposed strategy of transistor size scaling works effectively without deteriorating the noise performance of the device at mm-wave frequencies.

In fact, a few more points, which are not captured in the above analysis, need consideration when selecting the number of fingers in a unit cell. For example, if the unit cells consist of only a few fingers to obtain a M_{min}, the device layout may become dramatically large in the Y- direction for a wide transistor (Fig. 12). Especially, when the layout size in the Y- direction exceeds the transmission line width remarkably, the distributed effects of the connecting wiring may reduce the gain and noise performances of the device. Moreover, the RC extraction tool can fail to predict the distributed effects correctly if the device is excessively long. In our design, for transistors in the circuit, we have chosen the number of fingers in a unit cell so that the M_{min} of the device remains low and the device layout is the same width as the transmission line connected to the device.

In the CPW design environment, apart from the careful device layout drawing, designing the device access is very critical. The device access facilitates the signal connections between the core device and the CPW, and consists of tapered metal sections connecting the source ports of the device to the CPW grounds, and metal connections for the input and output ports of the device. At mm-wave frequencies, device access can have a remarkable effect on the characteristics of the device [41], as it creates additional parasitics due to via stacks and the coupling among different sections of access metallization as shown in Fig. 15. Furthermore, device access may cause the device to suffer from substrate losses if not shielded properly. In this work, we have carefully designed the device access to avoid those couplings and shielded them from substrate loss as shown in Fig. 16. The connection of the transistor to the CS-CPWs, which is the critical part of the amplifier design in a CPW environment, is also shown in Fig. 16.

C. Circuit design

Based on the studies carried out in the previous section, a unit cell consisting of 12 fingers with 0.9 μm width is chosen, and two of these unit cells are connected in parallel for the implemented transistors. A possible layout of such a transistor

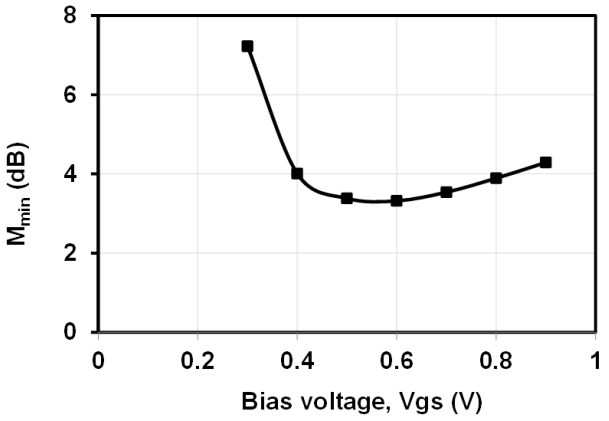

Fig. 17. M_{min} of a 12-finger unit cell for different bias points at 160 GHz.

is shown in Fig. 12(b). Bias points of the transistors must be selected carefully to obtain better gain, noise and linearity performance at mm-wave frequencies. To find the optimum, we have simulated the M_{min} of the selected unit cell transistor under different bias conditions with the nominal supply voltage of 1 V, and the results are shown in Fig. 17. The post-layout simulations of the device considering V_{GS} = 0.63 V and V_{DS} = 1 V show the f_t and f_{max} of around 290 and 430 GHz, respectively, as well as the maximum stable gain (MSG) of 7.8 dB and minimum noise figure (NF_{min}) of 2.95 dB at 160 GHz.

Two of the most common topologies in mm-wave CMOS amplifiers are cascode and common-source *(CS)* topologies, both with advantages and disadvantages. The cascode topology provides high gain (frequencies $<<$ f_{max}), good stability and low power consumption. Furthermore, being nearly unilateral, cascode topology gives good reverse isolation, and therefore, simplifies the matching [42]. Regular cascode stages, however, have a large parasitic capacitance at the shared junction node of the two transistors which presents low impedance at high frequencies. As a result, the gain of the cascode structure drops significantly as the frequency of operation approaches to f_{max}. Moreover, the noise figure (*NF*) of the cascode increases since the noise contribution of the common-gate device becomes significant. It is possible to resonate out the capacitance at the inter-stage node by placing a series inductor between the two transistors. However, this inductor introduces additional losses and can complicate the modeling of the gain stage. Nevertheless, the *CS* topology provides a higher output voltage swing at the output. Furthermore, it does not suffer from an inter-stage parasitic capacitance. Therefore, when operating close to the cut-off frequency, the *NF* of a common-source is lower compared to that of a cascode. In this work, the common-source topology is chosen for the design of the D-band LNA, mainly due to its superior noise performance.

The amplifier is matched to a compromise of the noise and the gain performance. For wideband performance, the staggered matching technique is implemented. The CS-CPW structures are adopted as the matching elements to validate the proposed modeling technique. Furthermore, any potential modeling error from the DC-decoupling capacitors is avoided by using the CS-CPWs. By proper choice of odd- and even-mode characteristics impedances of the CS-CPWs, the real part of the impedances seen by the transistors are controlled. The lengths of the CS-CPW are set to a quarter of the wavelength at the center frequency and tuned for the best performance. The open stubs added at the open end of the CS-CPWs are used to match the imaginary part of the required impedance. The imaginary part of the impedance is partially controlled also by tuning the lengths of the CS-CPWs. The open stubs are designed with the S-CPWs. A simplified schematic of the designed D-band MMIC amplifier is depicted in Fig. 18.

The modeling parameters of the CS-CPWs, (*W*, *S*, *D*, *SG*, and *GW*) are adjusted for the required odd- and even-mode impedances. The signal lines of the CS-CPWs are formed by strapping two top copper layers ($M10$ and $M9$) on top of each other and connecting them together with vias [see Fig. 11] to reduce the resistive losses. The metal shield strips are situated in the $M6$ metal layer, and they are designed using the minimum design rules, i.e. minimum metal strip width and spacing, in order to suppress the induced current flow in the direction of the propagating mm-wave signals. The means of the exclusion layers prevent the dummy metal generation in proximity to the signal lines in order to maintain the simulated characteristics of the designed lines. The modeling parameters and the corresponding line characteristics of the CS-CPW and the S-CPW used in this design are stated in Table II.

The gates of the transistors were biased through large resistors to avoid any unwanted low-frequency oscillation. On both the gate and drain bias lines, custom-designed RF-short circuiting capacitors along with quarter wavelength transmission lines are used. The quarter wavelength transmission lines used in the bias lines are also realized with the S-CPWs. For the short-circuiting RF shunt capacitors, custom-designed plate capacitors are used. The capacitors are designed and modeled in a microstrip environment. The maximum widths of the bottom metal layers are typically narrow in CMOS technologies; therefore, a gridded ground plane must be used. The metal layers $M5$ and $M6$ are used to form the ground-plane. The 100 μm pitched Ground-Signal-Ground (GSG) RF pads are used at the input and the output of the circuit for RF probing. The pads are realized on the aluminum layer ($ALUCAP$), and a similar gridded ground plane, as with the RF short-circuiting capacitors, is used. In order to reduce the pad parasitic losses, the signal pad size is reduced to 45 μm $\times$ 40 μm, the minimum area required for the on-wafer probing. However, the ground pads are comparatively larger and galvanically connected to the ground metal layers $M5$ and $M6$. The 3-D models of the designed capacitor and the RF pad are illustrated in Fig. 19.

VI. Measurements

The micrograph of the MMIC is shown in Fig. 20. The total chip area including the probing pads is 0.5 mm^2. The total power consumption of the circuit is 32 mW from a 1-V supply. On-wafer measurements were carried out to characterize the manufactured amplifier.

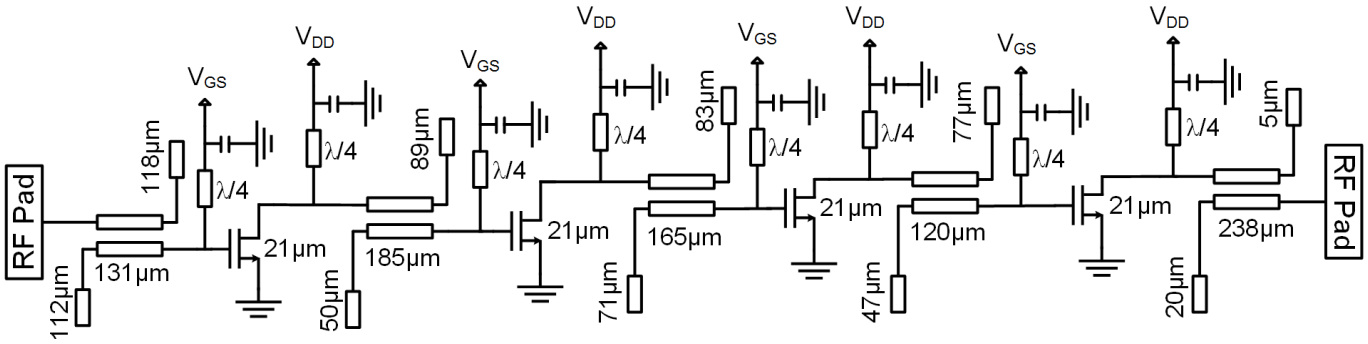

Fig. 18. Simplified schematic diagram of the designed amplifier that utilizes slow-wave coupled lines (for simplicity, bias networks are not shown).

TABLE II
DIMENSIONS OF THE TRANSMISSION LINES

Transmission line type	Signal width	Gap between two lines	Gap between Signal-line-to side-ground line	Ground conductor width	Signal-line-to-metal shield distance	Shield strip width	Shield strip spacing
CS-CPW	5.4 μm	5.4 μm	8.1 μm	10.8 μm	1.39 μm	0.114 μm	0.114 μm
S-CPW	10.8 μm	-	10.8 μm	10.8 μm	2.87 μm	0.114 μm	0.114 μm
Corresponding Transmission Line Parameters							
Transmission line type	**Characteristic impedance**		**Relative dielectric constant**		**Attenuation/m**		
CS-CPW	Z_{0o}=35 Ω, Z_{0e}=58 Ω		ϵ_{ro}=7, ϵ_{re}=14		α_o=750, α_e=790 @60GHz		
S-CPW	Z_0=39 Ω		ϵ_r=8		α=1700 @130GHz		

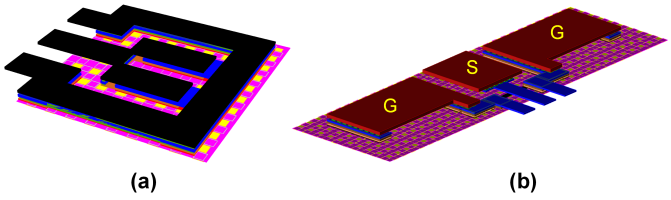

Fig. 19. 3-D simulation models for the custom made (a) RF short-circuit capacitor and (b) RF pad.

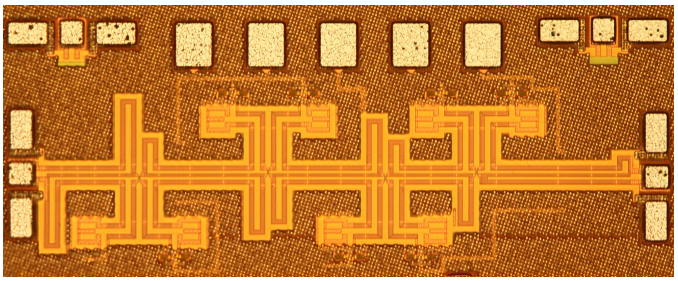

Fig. 20. Micrograph of the D-band CMOS amplifier that utilizes slow-wave coupled lines. The core die area is 1 mm × 0.34 mm.

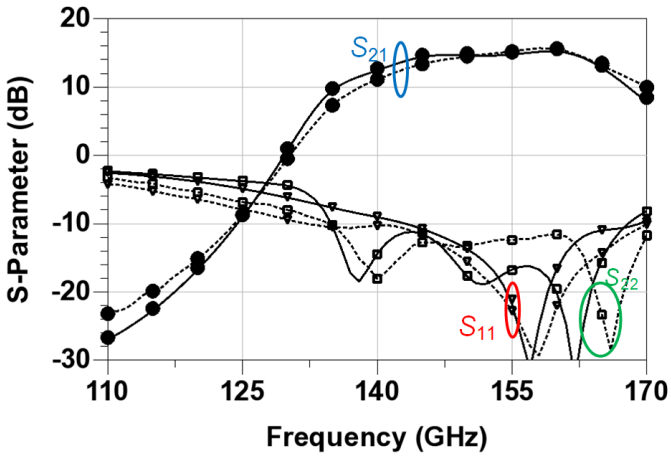

Fig. 21. Simulated (solid) and measured (dashed) small signal performance of the amplifier.

A. S-Parameter Measurements

The small-signal S-parameters were measured in the D-band (110-170 GHz) with a measurement setup which consists of a vector network analyzer system, WR-6 frequency extenders, and probes. The setup is calibrated up to the probe tips with line-reflect-reflect-match (LRRM) calibration on an alumina substrate (Cascade Microtech: 138-357).

Fig. 21 shows the D-band measured and simulated S-parameters of the amplifier. Excellent agreement between the simulated and measured results suggests that the CS-CPW modeling approach is valid. Furthermore, it also indicates that the CS-CPW structures can be used as the impedance matching elements and that they are suitable for mm-wave CMOS amplifier designs.

The designed amplifier has a peak gain of 15.7 dB at 160 GHz with a 3-dB bandwidth of 23 GHz (143-166 GHz), and more than 10 dB gain from 138 GHz to 170 GHz. Input and output mm-wave losses of the amplifier are greater than 10 dB from 135 GHz to 170 GHz. The reverse isolation ($|S12|$) is higher than 40 dB, and the circuit is unconditionally

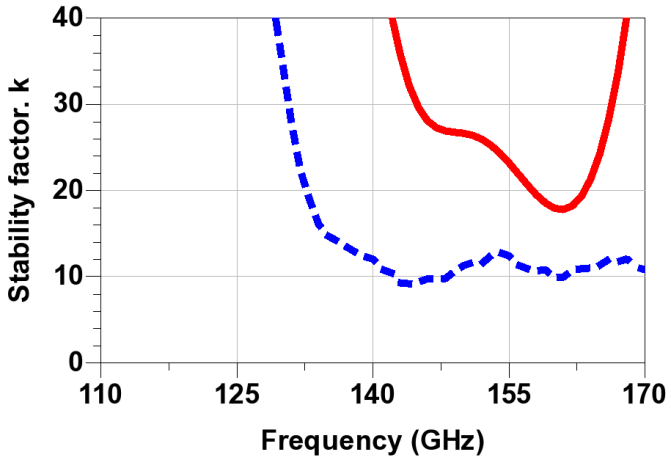

Fig. 22. Simulated (solid) and measured (dashed) stability factor of the amplifier.

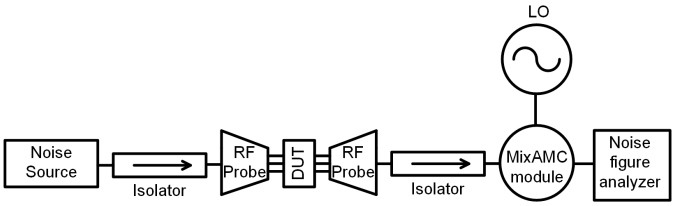

Fig. 23. D-band Noise figure measurement setup.

stable over the whole frequency range. The measured and the simulated stability factors are illustrated in Fig. 22.

B. Noise Measurement

The noise measurement was carried out on-wafer using the Y-factor method. A simplified block diagram of the D-band noise measurement setup is shown in Fig. 23. A MixAMC module, which consists of a sub-harmonic mixer and an amplifier-multiplier chain, was used to down convert the D-band signal with a minimum backend noise contribution to the baseband signal. After which the down-converted signals were measured using a noise figure analyzer. The required LO source consists of a multiplier chain fed from a synthesizer. Isolators were used to reduce the impedance mismatches in both the noise receiver and noise source. The measurement was carried out in three steps as described in [43]. First: characterization of the passives presents in the measurement chain, i.e. isolators, RF probes, etc., Second: noise receiver calibration, and Third: noise measurement of the DUT.

The measured and simulated noise figures are shown in Fig. 24. The amplifier has a noise figure of around 8.5 dB from 135 GHz to 170 GHz.

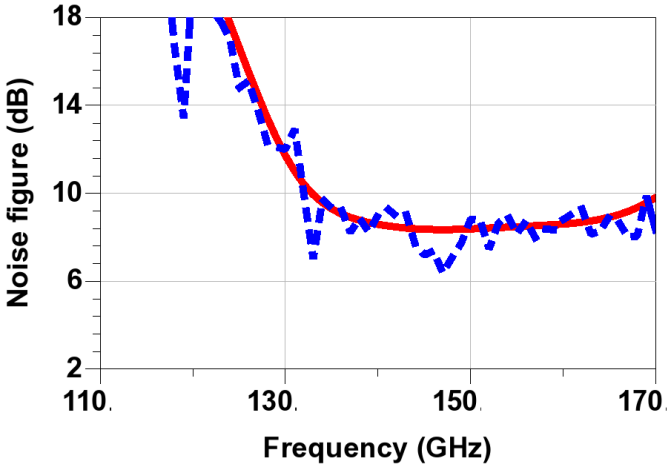

Fig. 24. Simulated (solid) and measured (dashed) noise figure of the designed amplifier.

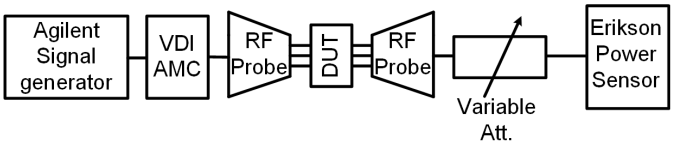

Fig. 25. D-band large-signal measurement setup.

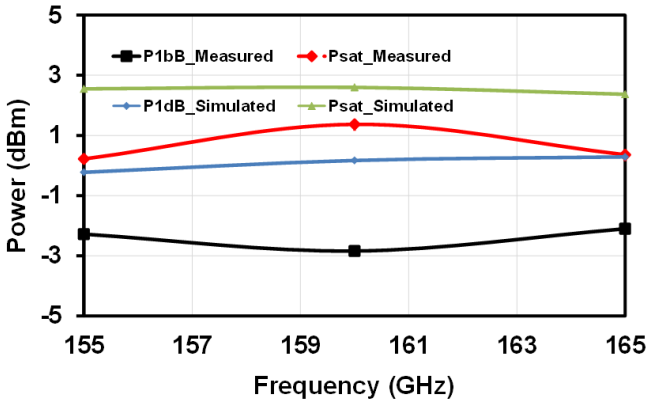

Fig. 26. Simulated and measured P_{1dB} and P_{sat}.

C. Power Measurement

Fig. 25 shows the power measurement setup. The D-band signal was generated using VDI-AMC multiplier chains, and the output power was monitored using an Erikson power sensor. The insertion loss of the WR-6 GSG coplanar waveguide probes was obtained by measuring the loss of the series combination of the input and output probes when placed on a thru line (on an alumina substrate) and the net series insertion loss was divided by half as in [44]. The large-signal measurement and simulated results are presented in Fig. 26. It is seen that the measured output 1-dB compression point (P_{1dB}) is greater than -3 dBm, and the saturated output power (P_{sat}) is larger than 0 dBm from 155 GHz to 165 GHz. The measured and simulated results are in fairly good agreement.

VII. Conclusion

The use of a CS-CPW as a matching element is introduced and its potential is demonstrated in mm-wave CMOS amplifier designs. The key properties of a CS-CPW are analyzed, and the structures are proven to be robust under process variations.

TABLE III
COMPARISON WITH STATE-OF-THE-ART D-BAND CMOS AMPLIFIERS

Reference	Tech.	Topology	Gain (dB)	3-dB Bandwidth (GHz)	Pdc (mW)	Noise Figure (dB)	Area (mm2)
[45]	65-nm bulk	Single Ended 5-stage cascode	19 @ 170 GHz	15 (160-175 GHz)	66	-	0.37 (core)
[46]	65-nm bulk	Single Ended 4-stage CS	16 @ 150 GHz	30 (120-150 GHz)	115.2	-	0.38 (total)
[47]	65-nm bulk	Single Ended 3-stage CS	8.2 @ 150 GHz	27 (143-170 GHz)	25.5	-	0.4 (total)
[48]	40-nm bulk	Single Ended 6-stage CS	16.8 @ 133 GHz	13 (125-138 GHz)	89	-	0.3 (total)
[49]	65-nm bulk	Differential 3-stage cascode	20.6 @ 144 GHz	4 (142-146 GHz)	102	-	0.21 (total)
[50]	65-nm bulk	Differential 4-stage cascode	7.1 @ 147 GHz	10 (142-152GHz)	104	-	0.35 (total)
[51]	28-nm CMOS	Differential 3-stage CS	16 @ 135 GHz	10 (128-138 GHz)	33	-	0.22 (total)
[52]	65-nm CMOS	Single Ended 4-stage CS	14.4 @ 126 GHz	17 (121-138 GHz)	22.6	12	1.9 (total)
This work	**28-nm FDSOI CMOS**	**Single Ended 4-stage CS**	**15.7 @ 160 GHz**	**23 (143-166 GHz)**	**32**	**8.5**	**0.34 (core)**

Optimization of the active device is discussed, and the critical stage of connecting the transistors in a CPW environment is presented for mm-wave amplifier designs. Table III summarizes the measured results and compares this work with recently published CMOS amplifiers operating in the D-band. The first cycle developed an mm-wave amplifier utilizing CS-CPWs as matching elements shows a wideband frequency response with a low noise figure of 8.5 dB. To the best knowledge of the authors, the presented amplifier achieves the lowest noise figure with the widest bandwidth among previously shown wideband CMOS amplifiers operating in the D-band.

Most importantly, an excellent agreement between the measured and the simulated results indicate the validity of the CS-CPW modeling methodology which is straightforward and applicable to any silicon technology.

ACKNOWLEDGMENT

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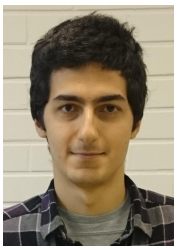

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