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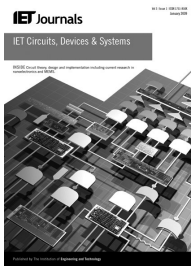

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Analysis of circuit conditions for optimum intermodulation and gain in bipolar cascomp amplifiers with non-ideal error correction

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Abstract: The cascoded-compensation or 'Cascomp' amplifier offers excellent distortion reduction and thermal distortion rejection, but has not seen widespread use because of a limited gain and increased complexity compared with other topologies. The original theory showed that with the addition of an ideal error amplifier the circuit will completely compensate distortion for suitably chosen degeneration and bias values. This research presents a new, rigorous mathematical proof for conditions of compensation. The authors further develop the proof to include the non-idealities of the error amplifier. It is shown that there exists a second bias point, not exposed by the original analysis that offers improved gain while maintaining distortion cancellation. By reducing the error amplifier degeneration resistance, one can increase a Cascomp circuit's overall gain by several dB while maintaining theoretically perfect distortion compensation. A robust bias point is proposed, which takes the advantage of this new theory by optimising circuit values resulting in a comparatively broader and deeper third-order distortion null. The proposed theory is confirmed with simulation and measurement that show agreement within the bounds of process and component error limits.

1 Introduction

Many techniques have been proposed and investigated for the reduction of non-linearity in amplifiers. In radio frequency (RF) amplifiers, in particular, the third-order non-linearity is of greater importance because it leads to in-band distortion components within a radio channel.

One notable example is the Cascomp amplifier configuration, which first appeared in a patent filing [1]. In 1981, the first report appeared in the engineering literature [2]. The Cascomp theoretically allowed full compensation (cancellation) of all distortion, including third-order distortion and distortion arising from thermal effects, as a consequence of Quinn's novel topology. Many improvements to the topology were patented and used by Tektronix in the 1980s [3–7]. More recently, Cascomp style amplifiers, referred to as 'cross-coupled pairs', have been used in CMOS applications to eliminate third-order intermodulation (IM3), for example, see [8–10]. Other common distortion reduction methods, for example [11, 12], do not trade-off as much gain as Cascomp topologies, suggesting that improvement of the fundamental gain is important in making a Cascomp topology more useful as an amplifier.

The circuit used to explain the operation of the Cascomp is reproduced in Fig. 1. It is composed of a main amplifier, which is the outside cascoded differential pair, and an error amplifier, represented in this figure as an ideal transconductance amplifier. Ideally, the transistors of each side share the same emitter/collector currents, therefore any voltage induced across the base–emitter junction of Q_1 and Q_2 will be replicated across the base–emitter junctions of Q_3 and Q_4. The input voltage to the main amplifier, $V_{\mathrm{IN(m)}} = (V_{\mathrm{IN(m)+}} - V_{\mathrm{IN(m)-}})$, is split between the base–emitter junctions of Q_1 and Q_2 and the emitter degeneration resistors, R_{M}. The input voltage loop can be described by

$$V_{\mathrm{IN(m)}} = \Delta V_{\mathrm{BE12}} + 2V_{R_{\mathrm{M}}} \tag{1}$$

where $V_{R_{\mathrm{M}}}$ is the voltage drop across each of the main amplifier degeneration resistors, R_{M}. The $\Delta V_{\mathrm{BE12}} = V_{\mathrm{BE1}} - V_{\mathrm{BE2}}$ term gives rise to a non-linear output current component, whereas the $V_{R_{\mathrm{M}}}$ term gives rise to a linear component. The error amplifier, G_{ME}, amplifies the main amplifier output to produce third-order distortion compensation. Compensation occurs because the third-order component contributed by the main amplifier is out of phase with the error amplifier contribution because of the cross-coupling of the collectors. Now the differential output current, Δi_{01} must be described by

$$\Delta i_{01} = \frac{V_{\mathrm{IN}}}{2R_{\mathrm{M}}} - \frac{\Delta V_{\mathrm{BE12}}}{2R_{\mathrm{M}}} + \Delta V_{\mathrm{BE34}} G_{\mathrm{ME}} \tag{2}$$

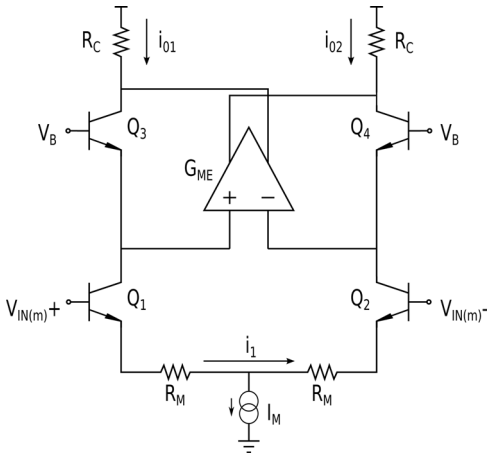

Fig. 1 *Cascomp circuit with an ideal error amplifier*

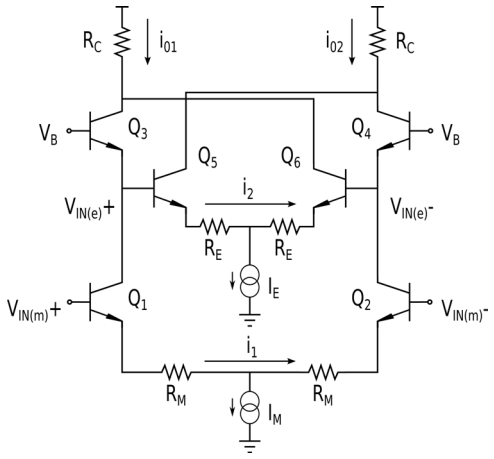

Fig. 2 *Cascomp circuit with cross-coupled DP used as the non-ideal error amplifier*

R_E and I_E now affect the error compensation

where G_{ME} is the transconductance of the error amplifier and ΔV_{BE34} is the replicated input base voltage across Q_3 and Q_4. Of course any conditions that cause ΔV_{BE12} not to equal ΔV_{BE34} will reduce the equation's accuracy. This equation shows that compensation [Note that the factor of 2 arises because the Cascomp configuration used in this paper uses one current source and two degeneration resistors whereas Quinn uses two current sources and one degeneration resistor. The two circuits are essentially the same and the factor of 2 only reflects the definition of the topology.] will occur when

$$G_{ME} = \frac{1}{2R_M} \tag{3}$$

However, (3) assumes an 'ideal' error amplifier, when in practice the error amplifier contributes its own non-linearity into the output current and increases the main amplifier's non-linearity. Because of the assumption of an ideal error amplifier, this equation gives no insight into the full range of suitable bias points or the best overall gain that can be obtained. Current literature on the Cascomp topology has not progressed past this ideal assumption.

This paper provides a mathematical basis for an improved understanding of the Cascomp topology in BJTs, which can potentially be extended for use with technologies such as HBTs. Other authors have investigated related techniques to improve linearity in FET amplifiers [8–10]; however, a rigorous investigation and comparison in a FET technology is beyond the scope of this paper. In the following analyses, it is shown that when a simple BJT error amplifier is modelled as a non-ideal differential amplifier with its own emitter degeneration, a more effective bias point for maximising gain and minimising distortion can be found compared with that suggested by the original Cascomp theory. We confirm the analysis with simulations and measurements.

2 Circuit compensation analysis

The proof of compensation when using an ideal amplifier, presented in the last section, is derived simply by considering the base–emitter voltages. If we consider a Cascomp circuit with a non-ideal error amplifier, as seen in Fig. 2, we observe that ΔV_{BE34} contains linear terms because of the error amplifier's own degeneration as well as non-linear terms from the error amplifier's base–emitter characteristic. In this case (2) no longer describes the output differential current and (3) no longer is a condition for cancellation. Hence we propose a more rigorous method based on the proof by Garuts [13] for emitter coupled pairs, which is a similar topology to the Cascomp circuit. We derive the output current contribution for the main amplifier (outside cascoded differential pair) and then the non-ideal error amplifier (inside compensating differential pair) contribution separately. For now we assume base current losses, and anything that causes $\Delta V_{BE12} \neq \Delta V_{BE34}$ are negligible. These are addressed later in the text.

2.1 Main amplifier

Firstly, we define the output currents as in Fig. 2, ignoring the error amplifier for now.

$$i_{o1} = \frac{I_M}{2} + i_1 \tag{4}$$

$$i_{o2} = \frac{I_M}{2} - i_1 \tag{5}$$

Summing the input voltage around the main amplifier's inputs, we obtain

$$V_{IN(m)} = 2R_M i_1 + V_{BE1} - V_{BE2} \tag{6}$$

Substituting the Ebers–Moll model into (6) gives

$$V_{IN(m)} = 2R_M i_1 + V_T \ln\left(\frac{i_{o1}}{I_s}\right) - V_T \ln\left(\frac{i_{o2}}{I_s}\right) \tag{7}$$

and then by substituting (4) and (5) into (7) and simplifying we obtain a transfer function in terms of $V_{IN(m)}$ and i_1. Terms are collected and the equation is simplified in (8)

$$V_{IN(m)} = 2R_M i_1 + V_T \ln\left(\frac{1 + 2\frac{i_1}{I_M}}{1 - 2\frac{i_1}{I_M}}\right) \tag{8}$$

This is the transfer function of the main amplifier.

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2.2 Non-ideal error amplifier

We apply the same process to the non-ideal error amplifier. Again referring to Fig. 2, we can form an input voltage loop to describe $V_{IN(e)} = V_{IN(e)+} - V_{IN(e)-}$ in terms of i_2.

$$-V_{BE3} + V_{BE4} = 2R_E i_2 + V_{BE5} - V_{BE6} \tag{9}$$

We know that $V_{BE1} - V_{BE2}$ is replicated across the base–emitter junctions of Q_3 and Q_4, although this is only true if the V_{CE} values of each transistor are assumed to be equal. For now, any error associated with this assumption is assumed negligible and is addressed later in the text. Therefore by combining (9) with $V_{BE1} - V_{BE2}$, we obtain i_1 in terms of i_2. Substituting the Ebers–Moll equation for the base–emitter voltages gives an explicit representation of i_2. This is useful as it can be solved for i_1 in terms of i_2, so

$$i_1 = \frac{-I_M}{2}\frac{(2i_2 - I_E) + (2i_2 + I_E)e^{(2i_2R_E/V_T)}}{(-2i_2 + I_E) + (2i_2 + I_E)e^{(2i_2R_E/V_T)}} \tag{10}$$

This can then be substituted into the main amplifier transfer function given by (8) leaving $V_{IN(m)}$ in terms of i_2

$$V_{IN(m)} = 2R_M X_2 + V_T \ln\left(\frac{1 + 2\frac{X_2}{I_M}}{1 - 2\frac{X_2}{I_M}}\right) \tag{11}$$

where X_2 is the full expression for i_1 given by (10). This leaves a transfer function for the input voltage $V_{IN(m)}$ in terms of only the error amplifier current contribution i_2.

2.3 Output current analysis

These derivations show two transfer functions describing the main amplifier's and error amplifier's current contributions to the output current, so it is now possible to find their third-order distortion components and any resulting minima when they are summed at the Cascomp's output. Mathematically, if we look at the output current for both the main and error amplifiers, we see the same gain components add together at the output of the complete Cascomp circuit [13]. Simple series expansions of the currents i_1 or i_2 are not possible as (8) and (11) are insoluble for these variables in terms of $V_{IN(m)}$. Therefore we use an alternate method where the derivative of i_1 or i_2 with respect to $V_{IN(m)}$ is found by inverting the first derivatives of (8) and (11) with respect to the differential currents i_1 and i_2. The following series expansions of the transfer functions (8) and (11), give (12) and (13) which describe the main and non-ideal error amplifier gain components, A_m and A_e, respectively.

$$i_1 = i_{0(m)} + A_{m1}V_{IN(m)} + A_{m3}V_{IN(m)}^3 \tag{12}$$

$$i_2 = i_{0(e)} + A_{e1}V_{IN(m)} + A_{e3}V_{IN(m)}^3 \tag{13}$$

Note that differential configurations generally reject even-order gain components and the assumption has been made that fifth-order and higher components can be neglected. The dc bias currents $i_{0(m)}$ and $i_{0(m)}$ can be ignored as they do not affect the gain components. The error amplifier collectors are cross-coupled; therefore the differences in main and error amplifier gain components are

$$i_1 - i_2 = (A_{m1} - A_{e1})V_{IN(m)} + (A_{m3} - A_{e3})V_{IN(m)}^3 \tag{14}$$

Considerable algebraic manipulation is required to obtain the fundamental gain coefficients A_{m1} and A_{e1}, and the third-order gain coefficients A_{m3} and A_{e3}. These are shown in (18)–(21). It is now obvious there is a minimum occurring in the third-order components and hence a cancellation in the output distortion because of the error amplifier's third-order gain term being positive (i.e., the third-order error current is out of phase with the third-order main current).

As a verification, it is possible to arrive at Quinn's cancellation condition by replacing (10) with the ideal transconductance equation

$$i_2 = G_{ME}V_{IN(e)} \tag{15}$$

If the same steps are then followed and the third-order gain coefficients are found for the ideal error amplifier case we then obtain the following

$$A_{e1\_ideal} = \frac{2G_{ME}V_T}{I_M R_M + 2V_T} \tag{16}$$

$$A_{e3\_ideal} = \frac{2G_{ME}I_M R_M V_T}{(I_M R_M + 2V_T)^4} \tag{17}$$

Using the main amplifier gain coefficients, these can be reduced down to the cancellation condition given in (3).

$$A_{m1} = \frac{I_M}{(2I_M R_M + 4V_T)} \tag{18}$$

$$A_{e1} = \frac{-I_E V_T}{(I_E R_E + 2V_T)(I_M R_M + 2V_T)} \tag{19}$$

$$A_{m3} = \frac{-2I_M V_T}{(I_M R_M + 2V_T)^4} \tag{20}$$

$$A_{e3} = \frac{4I_E V_T R_M\left(I_E^3 I_M R_E^3 + 6I_E^2 I_M R_E^2 V_T + 12I_E I_M R_E V_T^2 - \frac{16V_T^4}{R_M}\right)}{(I_E R_E + 2V_T)^4 (I_M R_M + 2V_T)^4} \tag{21}$$

3 Bias analysis and optimisation

To gain insight into what this derivation suggests as an optimal bias point, we evaluate the gain coefficients graphically. Firstly, we evaluate the third-order minima given by the ideal error amplifier's gain coefficients. We then compare this to the non-ideal error amplifier's gain coefficients and its non-ideal third-order minima.

3.1 Ideal Cascomp

Fig. 3 shows the theoretically determined fundamental gain coefficients, when R_E and I_E are swept and R_M and I_M are fixed at 10 Ω and 20 mA, respectively. The plot data were calculated using terms (18) and (19). This shows the expected result in that increasing the error amplifier gain, through lowering R_E and increasing I_E, increases the Cascomp's overall gain.

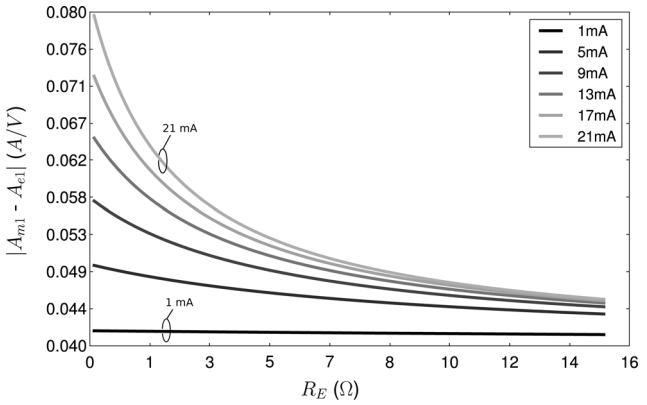

Fig. 3 *Theoretical fundamental coefficient cancellation of a Cascomp amplifier for fixed R_M and I_M*

R_E is swept for values of I_E
The *y*-axis reflects the magnitude of the fundamental gain

Fig. 4 shows the theoretically determined third-order gain coefficients for an ideal error amplifier, calculated using the terms (17) and (21). G_{ME} is substituted by the transconductance model for a degenerated differential pair. This was already calculated for the main amplifier as the term (18). Although these data are not fully representative of Quinn's ideal proof, which uses a linear function for G_{ME}, it does illustrate why information on bias points is lost in the former compared with the non-ideal case. This figure shows one cancellation point for each value of I_E.

In terms of circuit currents, we can explain this effect by considering the third-order currents through both of the main and error amplifiers. The error amplifier's total third-order distortion is required to be the same magnitude as the main amplifier to produce cancellation. To increase the size of the error amplifier's cancellation current, we can either increase I_E for a given R_E or reduce R_E. According to the ideal theory, for low R_E values, we do not produce the required cancellation current in the error amplifier unless low values of I_E are chosen, which greatly reduces the fundamental current as well. Essentially, this means there is no meaningful optimisation of circuit parameters to maximise gain and minimise distortion.

3.2 Non-ideal Cascomp

The theoretically determined third-order gain coefficients for a non-ideal error amplifier are expressed in Fig. 5, obtained using the terms (20) and (21). Comparing this with Fig. 4, two nulls now occur for higher values of I_E, whereas lower values of I_E lead to finite minima but not a complete null. If this non-ideal case is compared with its fundamental gain coefficients in Fig. 3, then we observe that bias points having two null conditions yield more fundamental gain in the second null (the null occurring at the lowest R_E value). This implies that a Cascomp amplifier is more effective when biased in this second null and that the second null position can be chosen through appropriate circuit values. This bifurcation of the IM3 minima occurs because the proposed non-ideal theory now considers the error amplifier transfer function to be a function of the main amplifier transfer function. The main amplifier third-order distortion is now considered to be amplified through the error amplifier as well.

It is also important to note the effects of R_M and I_M. These scale the fundamental gain of the Cascomp's output, but they also scale the third-order gain component as well. For example, an increase in R_M will shift the two nulls in Fig. 5 further apart for each I_E value. This changes the position of the second null such that it occurs at even lower values of R_E and even higher relative values of fundamental gain (relative because increasing R_M decreases the overall fundamental gain). This observation means that it should be possible to tailor the cancellation point of the Cascomp circuit to suit the transistors used, which may be limited by their internal emitter resistances. Conversely, a smaller R_M means larger gain in the main amplifier.

3.3 Simulated Cascomp

The proposed non-ideal theory is confirmed by simulating a Cascomp circuit in SPICE and focusing on the lower values of R_E. Bipolar models are used from [14], a commercial 0.5 μm BiCMOS process, to compare the proposed theory with a practical circuit. Circuit values were kept the same as the theory calculations with R_E and I_E swept, and with $R_M = 10\ \Omega$ and $I_M = 20$ mA. The third-order distortion level can be seen in Fig. 6. The fundamental output is not shown as it is equivalent to that predicted by theory.

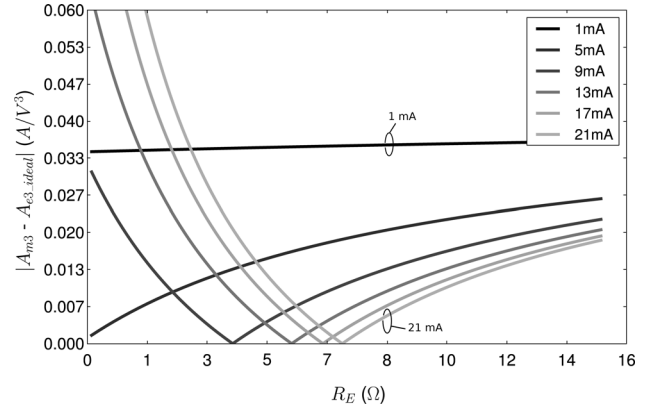

Fig. 4 *Theoretical third-order coefficient cancellation of an ideal Cascomp amplifier for fixed R_M and I_M*

R_E is swept for values of I_E
The *y*-axis reflects the magnitude of the total IM3 product and the nulls indicate IM3 cancellation

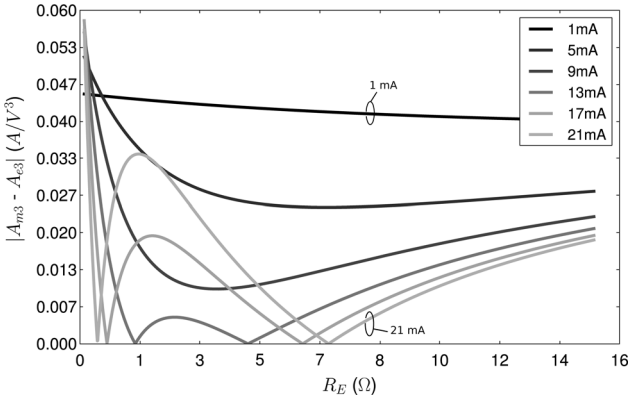

Fig. 5 *Theoretical third-order coefficient cancellation of non-ideal Cascomp amplifier for fixed R_M and I_M*

R_E is swept for values of I_E
The *y*-axis reflects the magnitude of the total IM3 product and the nulls indicate IM3 cancellation

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Fig. 6 yields a result that confirms the proposed non-ideal theory. For the same circuit values, we obtain a cancellation locus equivalent to the non-ideal theoretical third-order gain plot predicted by (18)–(21) and implied by Fig. 5. As an example, theory predicts at $I_E = 20$ mA we obtain nulls at both R_E equal to 7 and 0.5 Ω. Simulation results show nulls occurring at approximately 6 and 1 Ω for $I_E = 20$ mA. This variation is expected because of the parasitic resistance of the bipolar models which effectively shifts the R_M and R_E values.

3.4 Optimisation

Considering only the circuit parameters R_E and I_E, with other parameters fixed, it becomes obvious that an optimal bias point for distortion reduction in a Cascomp is one that maximises I_E and minimises R_E. This will give the best fundamental gain and third-order intercept point (OIP3) possible. If R_M is considered as a variable parameter, the best bias point is not obvious. To optimise for R_M, simulations were performed varying this parameter while observing IM3. All models and simulation variables are held the same as previous simulations. I_M and I_E are now chosen to be fixed at 20 mA each, with R_E swept.

Fig. 7 shows a proposed optimum bias point. Three different R_M values are chosen around this point. At $R_M = 8.4\,\Omega$, the region between the two nulls produces a minimum output-referred OIP3 of 30 dBV for the simulated circuit. This bias point maximises IP3 in terms of the degeneration resistors and may be of use if process variation is a problem.

Fig. 8 compares the proposed optimum bias point (where R_M has been increased to move the two nulls very close together) with a bias point where R_M is smaller (and therefore its nulls are further separated). This clearly shows the benefit of the optimised case as the region between the two nulls has relatively low IM3 compared with each null of the nominal case. This results in a wide range in which IM3 is consistently very small. To provide some form of benchmark, this figure also includes the simulated IM3 of a differential pair (DP). These simulations were performed

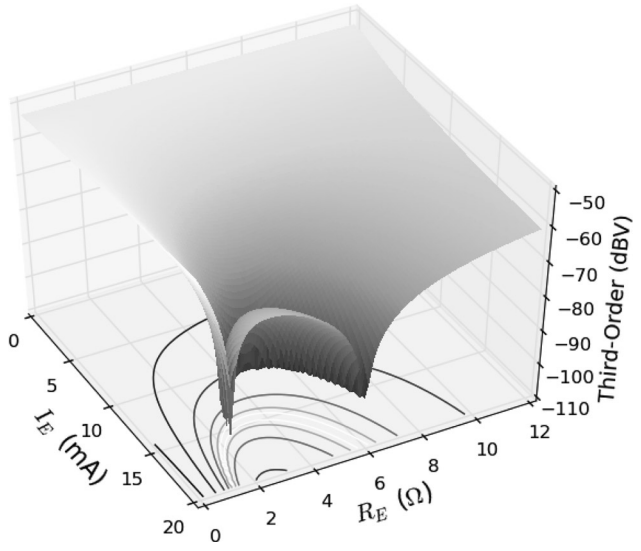

Fig. 6 *Simulated third-order output (dBV) of a non-ideal Cascomp amplifier for fixed R_M and I_M over a 56 Ω load*

Note that the z-axis values have been clipped (at −105 dBV) in the null positions to allow for readability

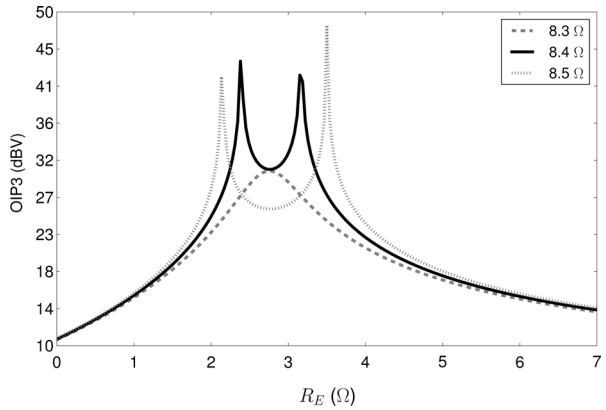

Fig. 7 *Simulated OIP3 (dBV) of a non-ideal Cascomp amplifier across a 56 Ω load*

R_E is swept for fixed I_M and I_E at 20 mA
This shows the approximate optimum bias point in terms of distortion for different values of R_M

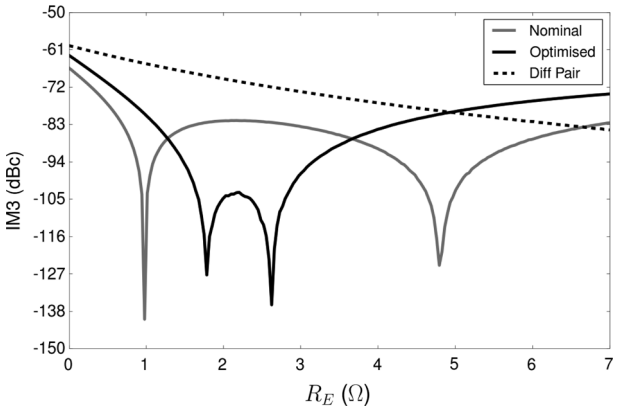

Fig. 8 *Simulated IM3 of a non-ideal Cascomp amplifier relative to the carrier*

R_E is swept for fixed I_M and I_E at 20 mA
This shows the relative levels of third-order distortion between two Cascomp bias points, and a DP for reference

such that the fundamental output levels are as close as possible as well as the emitter current densities being equal in each circuit. Although this is still not a completely fair comparison because of the differences in topology and emitter degeneration between the Cascomp and DP, it does highlight the improvement in IP3 when using a Cascomp and the benefit of optimising R_M in a Cascomp circuit.

4 Process errors

A large issue with biasing in a Cascomp's IM3 null is the variation in circuit parameters, which leads to shifts in the null positions. The most notable is the apparent emitter resistance for both main and error amplifiers, which can shift because of parasitic resistance and process variation.

In this section, we present simulations that highlight the major sources of error. All simulation results in this section were obtained using the same models and methods presented in the previous section.

4.1 Transistor parameters

The transistor parameter with the largest effect on the null position is the current gain, β. If we assume absolute

process variation to be ±20%, the bias point can be shifted out of the IM3 null. Simulations are performed to show the effects of ±20% absolute variation in current gain on the nominal circuit presented in Fig. 2. R_E is swept with I_E held at 20 mA. This simulation showed that current gain has a relatively minor impact compared with other process errors. Simulations show that variations in early voltage, V_{AF}, have no significant effect on the null positions. [A folded cascode at the circuit's output can be used to minimise the impact of differences in transistor V_{CE} values. It can also be used to reduce the accumulation of V_{CE} and reduce the required power supply voltage. It is important to note that this circuit technique does not affect the presented theory.] Other transistor parameters including saturation current, I_S, were found to have a relatively minor impact with absolute variations.

Mismatch process errors in the transistor parameters β, V_{AF} and I_S are assumed to be ±2% at worst. Monte Carlo simulations (done over 1000 iterations) showed that these transistor parameter variations did not have a significant impact compared with absolute variations.

In general, these simulations showed transistor parameter variations were not a significant problem with the exception of absolute current gain variation. Furthermore, if β is large then its effects are significantly reduced. These observations also indicate that the assumption of $\Delta V_{BE12} = \Delta V_{BE34}$ in the derivation of the non-ideal theory is indeed reasonable provided β is large.

4.2 Resistance error

The greatest variations in the null positions are because of process errors affecting the total degeneration resistance at the emitters of the main and error amplifiers. Fig. 9 shows the impact on distortion nulls with absolute variations of ±5% in the emitter resistors R_M. When R_M varies both nulls move to occur at different R_E values. In comparison with variations in β, there is a much larger shift in the null positions.

In high-precision applications manufacturing tolerances are a common problem. There are many well-established techniques for post-fabrication circuit trimming to address these problems (usually after packaging to minimise stress effects) involving some form of programming to select incremental component elements or injecting small currents [15, 16]. Externally trimming the bias current I_E would allow for full correction back into the distortion null. The need for trimming would clearly be dependent on the application, but we consider it a reasonable solution to address resistance variations in a Cascomp.

5 Experimental results

Measurements were made to confirm this theory using the circuit shown in Fig. 2. The circuit was constructed using discrete components and CA3083 transistor arrays. The values I_E and R_E in the error amplifier were swept and the output current of the circuit was captured using an Agilent 3561A Dynamic Signal Analyser. Current sources were controlled and swept using an Agilent E5270 Precision Measurement Mainframe. The main amplifier's current I_M was held at 20 mA (10 mA per side) and measurements were taken at three values of R_M at 5.6, 10.4 and 15.2 Ω, respectively. The amplifier was driven with a two-tone signal at 11 and 13 kHz at input levels of −22.25 dBV/tone. The load resistors were chosen to be 56 Ω, meaning the amplifier was operated well below compression.

The results can be seen in Figs. 10 and 11 that show the cancellation loci created for the last two R_M–I_M points. Measurements show that as R_M is increased, the loci changes, following what would be expected from theory. As R_M increases, smaller distortion components are required from the error amplifier for cancellation, so the distortion nulling starts to occur at lower values of I_E. When R_M is at low values there are no cancellation points for the shown I_E range. A locus of cancellation is produced when R_M is increased (Fig. 10). When R_M is further increased, this locus moves further to lower I_E values at higher R_E values (Fig. 11).

In these measurements, cancellation occurs at slightly smaller than expected values of R_M. For example, Fig. 11 shows a cancellation locus that occurs in simulation at $R_M = 15.9\ \Omega$, rather than the measurement value of 15.2 Ω. This error can be reconciled with simulation by considering the component tolerances in the measurement circuit. The CA3083 data-sheet states the parasitic resistances as $R_b = 0$, $R_e = 0$, $R_c = 10\ \Omega$. This is confirmed by performing flyback measurements [17] on a CA3083 transistor and therefore we assume that they are negligible in this case. The

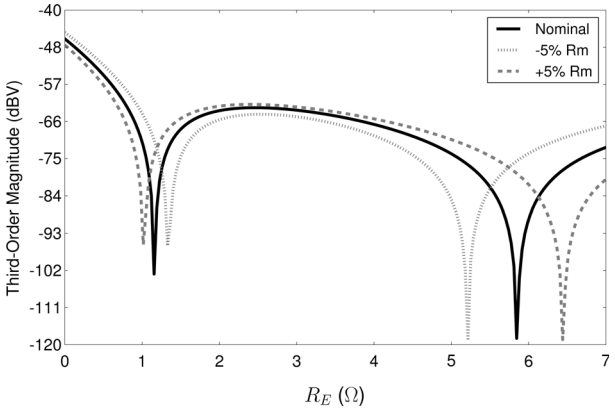

Fig. 9 *Simulated third-order output (dBV) of a non-ideal Cascomp amplifier*

'Nominal' is the normal circuit presented in Fig. 2
' ±5% R_M' indicates respective 5% absolute variation of the main amplifier emitter resistance
R_E is swept for fixed R_M, I_M and I_E

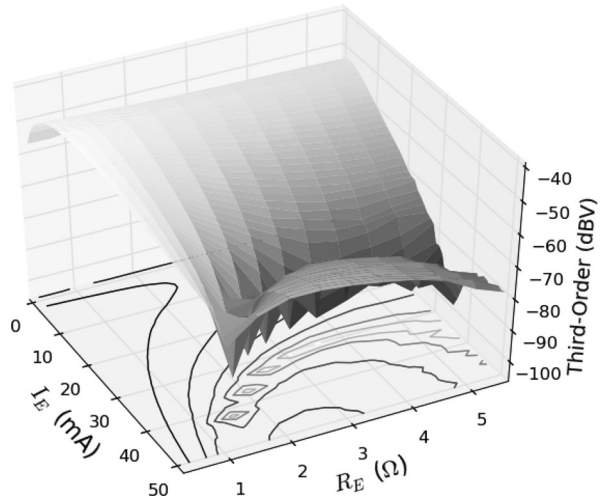

Fig. 10 *Measured third-order output of a Cascomp amplifier for a fixed $R_M = 10.4\ \Omega$ and $I_M = 20$ mA*

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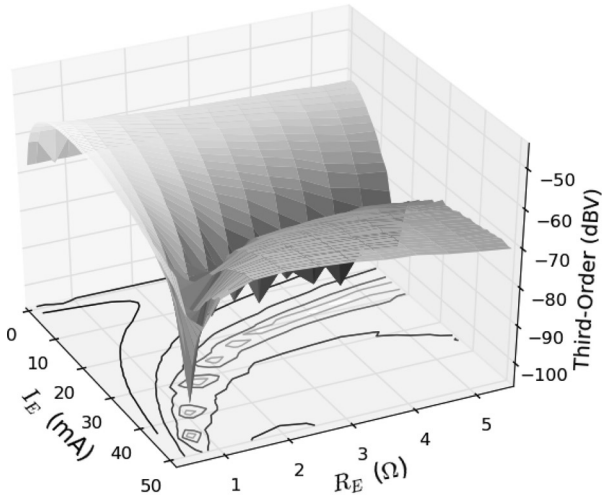

Fig. 11 *Measured third-order output of a Cascomp amplifier for a fixed $R_M = 15.2\ \Omega$ and $I_M = 20$ mA*

discrepancy arises from the error in R_M, R_E, I_M and I_E used in the measurements, which is assumed to be 5% for resistances and 1% for current sources (set by the parameters of the E5270). Simulations are repeated with the conditions used in Fig. 11, and with $R_M = 15.2\ \Omega + 5\%$. For comparison, this simulation is shown in Fig. 12. The cancellation locus matches the locus seen in Fig. 11 with minimal error. Therefore the measurements show excellent agreement with simulation and theory when component tolerances are taken into account.

Measurements done on the fundamental frequency components show improved overall fundamental gain at lower values of R_M, which is to be expected. All of these measurements follow theory showing further increased fundamental gain when R_E is low and I_E is high.

6 Verification of optimisation benefits

Estimates can be made as to how effective this optimisation of a Cascomp circuit will be. The exact increase in gain and IP3 is dependent on the technology used and the accuracy of

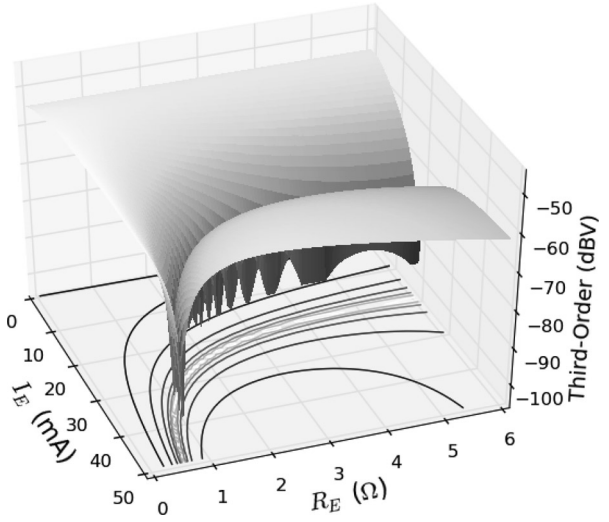

Fig. 12 *Simulated third-order output (dBV) of a non-ideal Cascomp amplifier for comparison with the measurement in Fig. 11*

These data use the same component values and circuit setup as the measurements

Table 1 Comparison of bias points for the Cascomp at $I_M = 20$ mA

Bias	R_M, Ω	R_E, Ω	I_E, mA	Gain, dB	OIP3, dBV
conventional	15.2	8.0	20	1.50	26.46
new	15.2	2.0	35	2.02	30.18
optimised	8.0	4.1	40	5.78	38.95

fabricated emitter resistors and/or the parasitic base and emitter resistances of the specific transistor cell layout, as well as the circuit's bias variation with temperature and supply voltage. These are the major factors that can shift third-order cancellation to different bias points. As we see from the simulation and measurement plots, cancellation at smaller values of R_E is better defined and variations that change the effective emitter resistance will move the bias point from the null.

Using the measurement data obtained, if a conventional Cascomp bias point is taken (the literature assumes I_M is about double I_E [1]) and is compared against a bias point chosen with a reasonably small R_E and large I_E, we obtain a measure of the achievable increase in gain and IP3. Referring to the cases enumerated in Table 1, the 'Conventional' bias point is similar to that cited in the original literature, which has a large R_M and R_E. The 'New' bias point has taken the same R_M value as the 'Conventional' but with optimised R_E and I_E to obtain the maximum gain and IM3 null. The 'Optimised' bias point also varies R_M to an estimation of the best possible bias point for the Cascomp circuit derived from the foregoing theory. This is the proposed optimised bias point shown in Fig. 7. The example measurements suggest that this bias point will yield an improvement of 4 dB in gain and an increase of over 10 dBV in OIP3 in a practical situation.

7 Conclusions

The previous literature on the Cascomp circuit has suggested that the most effective bias point, in terms of gain and IP3, can be found by assuming its error amplifier is ideal. We show that when an ideal error amplifier is considered, the equations do not accurately represent the cancellation of distortion components contributed by the error amplifier. This paper presents an improved non-linear analysis of the Cascomp circuit, including the non-linearity of the error amplifier. This analysis has identified a point of bifurcation in the conditions that allow an IM3 null. By analysing the theoretical IM3 coefficients of the non-ideal main and error amplifiers, theory suggested a more effective bias point at lower values of R_E where gain and IP3 are increased.

Simulation and measurements are presented confirming the theoretical analyses. By considering the plots of the measured variation in the optimum R_E and I_E values for a given I_M–R_M point, the predicted gain and IP3 effects were observed. Since gain is increased in an amplifier with low degeneration and high bias current, we are able to find the IM3 null, which is at optimum for these conditions. Using the predicted optimum bias values we can obtain an increase in gain of 4.3 dB and increase in OIP3 of 12.5 dBV compared with a traditional Cascomp circuit using the conventional bias point.

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