Application of Nonlinear Transistor Characteristics

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Abstract

This research presents three works all related by the subject of third-order distortion reduction in nonlinear circuits. Each one is a novel extension to previous work in that branch of electronics literature. All three follow the procedure of presenting a novel algebraic proof and following up with simulations and/or measurements to confirm the theoretical result. The works are generally themed around nonlinear low-frequency bipolar transistor circuits.

Firstly, an investigation is conducted into a well documented effect in bipolar-junction transistors (BJTs) called inherent third-order distortion nulling. This effect is shown to be a fundamental result of the transistor's transfer function acting upon an input signal. The proof of a single BJT emitter-follower amplifier's inherent null is examined which is well documented in the literature. This forms the basis for a novel extension in Darlington transistors where theory suggests the third-order null occurs at double the collector current of a single BJT. Discrete measurements of a CA3083 transistor array are undertaken and compared with theory and simulation data. These measurements confirm theory with reasonable accuracy.

A temperature and process variation independent bias circuit is developed to solve one issue with using third-order distortion nulling. This work is interesting in that it branches into series resistance compensation for translinear circuits and stands as a useful circuit in its own right. Using stacks of matched forward-biased semiconductor junctions which conform to translinear conditions, a bias current can be generated which theoretically removes temperature and series resistance dependence on the particular BJT used. This proves useful for the previous work in distortion nulling, but also allows direct and accurate measurement of series resistance. Again, simulation and measurement data is

obtained from discrete measurements of the proposed circuit, and the results conform with theory to a reasonable degree.

Lastly, this work presents the analysis of a cascoded-compensation (Cascomp) amplifier. It presents the first fully non-linear derivation of the Cascomp's transfer function and its associated harmonic and intermodulation distortion components. The derivation reveals an interesting characteristic in which the third-order intermodulation distortion has multiple local minima. This characteristic has not yet been presented in the literature, and allows better optimisation of Cascomp amplifiers in any application. Again, this characteristic and its potential benefits are confirmed with simulation and discrete measurements.

Observations of the presented works are discussed and built upon in the last chapter. This leads to suggestions on future research topics branching on from these works.

Acknowledgements

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1 Outline

All electronic circuits are inherently nonlinear. Both passive and active components are often assumed linear because their nonlinearity is extremely subtle and goes unnoticed. However, due to rising demands on technologies where bandwidth is at a premium, circuit component's subtle nonlinearity can start to become significant. As more sophisticated telecommunications systems are developed, increased performance is required from their amplifying stages. Unfortunately, nonlinearity degrades the performance of these systems. Engineers therefore follow strict guidelines defining the levels of linearity and efficiency that an amplifying stage needs to achieve. Power amplifier design has a heavy focus on these two parameters.

Some relevant applications where the reduction of nonlinearity is paramount include Doherty power amplifiers for use in wireless communication networks [1] and heterojunction bipolar transistor (HBT) power amplifiers for use in wireless communications networks [2]. Both examples aim to increase linearity and efficiency through optimising the topology and the semiconductor device's transfer characteristics. Of course, nonlinearity is an important parameter in

many other fields of amplifier design. An example is analog-to-digital converters where voltage level shifts due to distortion [3]. The work in this thesis mainly focuses on nonlinearity in amplifiers and techniques to reduce distortion.

Common methods of distortion reduction in amplifiers generally fall into three categories; feedback, feedforward, and predistortion. Each offers its own advantages and disadvantages. A designer will generally consider all specifications imposed on the amplifier design, and choose the most suitable method. In modern radio-frequency applications, predistortion techniques dominate amplifier design in wireless communication systems due to its relative simplicity and low-cost. This is also partly due to power amplifiers operating close to compression. Predistortion excels at canceling distortion due to the compression effects of a semiconductor device and power amplifiers typically press this boundary [4]. However, predistortion still has its disadvantages so modern designs tend to combine and synergise different methods of distortion reduction.

This thesis presents a number of ideas and experiments related to the reduction of nonlinearity in different topologies of bipolar transistor amplifiers. The distortion of interest is weakly nonlinear which is a major focus in engineering literature surrounding modern radio-frequency and microwave amplifier design. Strong distortion components such as clipping are neglected in this work. Each of these ideas is expected to be a useful and novel contribution to their respective literature. Distortion reduction techniques for bipolar technologies are not as popular due to the heavy use of field-effect devices in industry. However, heterojunction transistors find use in many applications where distortion is required to be minimised. Because bipolar device models translate accurately into heterojunction devices models, these ideas translate well into the literature.

1.1 Thesis Motivation

The three major works in this thesis are tied together under the general theme of distortion in amplifiers and circuit techniques which reduce it. However, the motivation for each is rather distinct and not necessarily related to the other works. This section describes the motivation for the three works in chapters 3, 4, and 5 respectively and then defines the specific aims and goals of each.

1.1.1 Third-Order Distortion Null

A long-known characteristic that occurs in single bipolar transistor amplifiers is a minima or null appearing in its third-order distortion component. This has been addressed in the literature for a long time, but due to the characteristic occurring at low bias currents, the effect isn't useful in many cases. Amplifier designers often want to push bias current as high as possible, for example to increase the frequency performance of the device. Unfortunately, this is in conflict with utilising the distortion null for increased linearity, hence the characteristic is generally not useful.

One could make the characteristic useful if it could be made to occur at higher bias currents. This work focuses on analysing the characteristic in a different configuration of bipolar transistors, such that the third-order distortion null occurs at a higher bias current.

1.1.2 Translinear Extraction

Following on from the previous work in utilising the distortion null in bipolar devices, it is observed that a limitation of using this null is its dependence on temperature and series resistance variation. A method is required for removing these dependencies from a bias current that is driving a bipolar device. The literature shows few practical entries on methods related to this.

Temperature dependence can be dealt with by invoking the translinear principle, for example the bandgap voltage reference circuit that produces a temperature independent voltage [5]. Based on this principle, one can develop a bias circuit to fit the criteria required for the distortion null. This work focuses on developing a bias circuit that rejects temperature dependence and series resistance variation by utilising the translinear principle.

1.1.3 Cascoded Compensation

Agilent Technologies has expressed interest in understanding a cascoded compensation (Cascomp) amplifier and exploring techniques to increase its performance. The company produces many commercial HBT amplifier products for use in wide-band applications, and they are considering an HBT Cascomp ampli-

fier as an alternative topology. Unfortunately, the conventional Cascomp setup does not meet the gain and linearity requirements to justify further research, but an analysis and implementation which shows better gain and linearity performance would be valuable to them.

In this work, a more rigorous method of analysing the nonlinearity of the Cascomp amplifier is explored. This leverages the fact that the current literature on the Cascomp amplifier does not consider all sources of nonlinearity.

1.1.4 Aims and Goals

Here, the initial goals of the three novel pieces of work are summarised. These are:

1. Extend an analysis of bipolar transistor nonlinearity to the Darlington configuration.
2. Develop a biasing technique that compensates for temperature and series resistance variation.
3. Develop a full nonlinear analysis of a cascoded compensation amplifier.

Leading on from these goals, each chapter may explore some topics such as parameter optimisation, impact of second-order effects and practical application.

1.2 Thesis Outline

This work is divided into six chapters:

Chapter 2 describes the associated background knowledge the work has used. It focuses on general concepts related to all works in this thesis. This includes the basis of distortion and the different types that manifest in amplifiers. The different measures of these distortion types are also defined. Bipolar transistor models are necessary to theoretically predict distortion. Hence, the two most common device models are described and are used for the majority of this work. The parameters of the bipolar models which describe the nonideality of a transistor are defined and discussed. Common distortion reduction techniques are also identified and explained.

Chapter 3 introduces the concept of an inherent third-order intermodulation null in a single bipolar transistor amplifier. This concept is reasonably well established in the literature, however we re-define this concept using a proposed derivation method. It is shown that this method agrees with existing derivations. This method is then used to theoretically show the inherent null occurs in Darlington transistors. The effect is confirmed with simulations and measurements.

Chapter 4 presents the concept of the translinear principle. Following on from the last chapter, third-order distortion nulling requires a bias circuit which is independent of temperature and of process variation in the transistor's intrinsic and extrinsic resistances. The translinear principle is utilised to develop a circuit which can accurately bias a common-emitter amplifier in its inherent third-order null. The theory of this bias circuit is presented and it is shown how different emitter-ratios can be used to cancel series resistance effects. A circuit design is developed and investigated based on a BiCMOS technology. Measurements and simulations are presented regarding its operation.

A Cascomp circuit is investigated in **Chapter 5**. A leading RF amplifier design company has expressed interest in understanding this circuit to a higher degree. Up until this point, the literature has assumed a linear relationship between the main and error amplifiers of the Cascomp. This chapter describes a new method for deriving the transfer function of a Cascomp amplifier. A new nonlinear transfer function is presented and it is shown that new characteristics of the Cascomp arise in the third-order distortion components. This was previously masked by the linear assumption used in the literature. These new characteristics are analysed with simulations and measurements. Conclusions are drawn regarding the newly found characteristic and the amplifier transfer function's accuracy.

The research is concluded in **Chapter 6.** Observations are made on potential future work regarding all three of the presented circuit techniques.

1.3 Original Work

The work presented in this thesis resulted in a number of publications. Two conference papers where presented and published; one national, one international. A contribution was made to a further conference paper as well. A journal paper

regarding the Cascomp work has also been accepted for publication.

List of Publications:

- Balsom, T., Scott, J. & Redman-White, W.. (2011). "Third–order nulling effect in Darlington transistors". In Proceedings of the 18th Electronics New Zealand Conference, ENZCon 2011, Massey University, Palmerston North, 21-22 November 2011, pp. 82-86.
- Balsom, T., Redman-White, W., & Scott, J. (2012). "Bipolar amplifier bias technique for robust IM3 null tracking independent of internal emitter resistance". 2012 IEEE 55th International Midwest Symposium on Circuits and Systems, vol 55, pp. 606-609.
- Jull, H., Balsom, T. & Scott, J. (2012). Cascomp BJT Amplifier vs. traditional configurations. Paper 97, Proceedings of The 19th Electronics New Zealand Conference (ENZCon), Dunedin, New Zealand, 10-12 December, 2012.
- *[Accepted for Publication]* Balsom, T., Redman-White, W., & Scott, J. (2012). "Analysis of Circuit Conditions for Optimum Intermodulation and Gain in Bipolar Cascomp Amplifiers with Non-Ideal Error Correction" (2014) IET Circuits, Devices & Systems.

2

Introduction

Three novel works are described in this thesis, tied together under the common theme of distortion reduction. Hence, each three works in the following three chapters contain their own literature reviews and background information that is directly relevant to its work. This introductory chapter is structured such that it acts as a linking chapter, giving context and background for the following novel works. It defines the fundamental concepts around distortion reduction for those unfamiliar with the topic. It also presents a general literature review on modern distortion techniques that are not directly relevant in each of the following chapters.

To begin, this chapter introduces a base definition for distortion and describes why it is an important research topic in modern electronics. This is followed by definitions of common measures of distortion which are used in the following chapters. The chapter then outlines the fundamental transistor models and their application. Also discussed are the non-idealities of BJTs and their impact on distortion through the device models. The chapter then presents a review of modern literature associated with distortion in amplifiers.

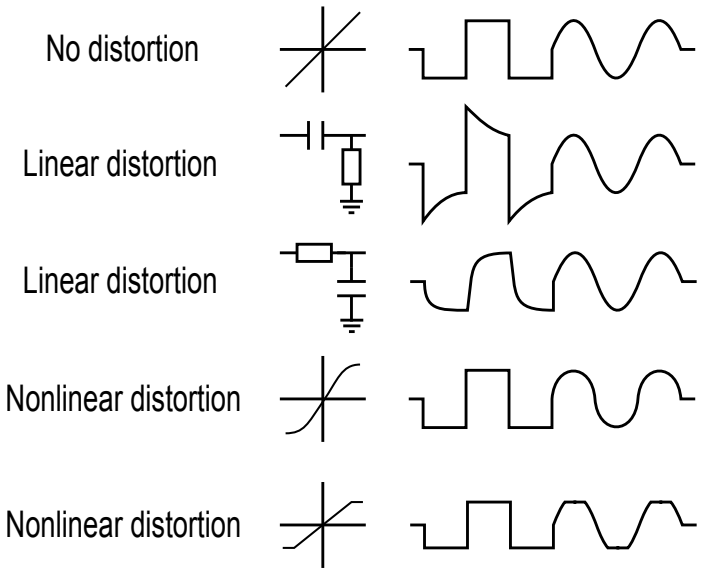


Figure 2.1: Linear and Nonlinear distortion waveforms. The right-hand column is the result of passing a pure square/sine wave through the common electronic transfer functions represented in the middle column. Waveform 1 shows no distortion. Waveform 2 and 3 show linear distortion through a high-pass and low-pass filter respectively. Waveform 4 and 5 show nonlinear distortion through nonlinear transfer functions.

2.1 Definition of Distortion

As a signal passes through any electronic component it has some transfer function imposed on it, modifying the output signal from its original state. This is the definition of distortion in its simplest form. In order to give this definition any practical meaning we separate distortion into two categories, linear and nonlinear. Nonlinear distortion of a signal is identified by an event which adds new frequency components into the output signal. Linear distortion does not add new frequency components, but rather changes the size or ratio of the original frequency components. Graphical representations of both types are shown in Fig. 2.1.

Nonlinear distortion can further be separated into two sub-categories, strong and weak nonlinear distortion. Strong nonlinear distortion arises from gross changes to the output frequency spectrum, namely clipping or device saturation. This area has been well covered in the literature [6]. Weak nonlinear distortion arises from slight changes to the output frequency spectrum, generally produced

by the transfer function of active devices. The generated distortion tones are orders of magnitude smaller than the input signal's fundamental frequency, but not so small as to have an insignificant impact on the system. The following works have a major focus on this category of distortion. So for simplicity the general term of distortion will refer to weak nonlinear types of distortion.

Distortion is a major focus when it comes to amplifiers in modern electronics. Power amplifiers (PA) are regularly used in modern telecommunication systems with the purpose of amplifying a signal to be transmitted through an antenna. Examples of major driving technologies for this type of system are wireless local area networks (WLAN), cellular devices, and global positioning systems (GPS). When designing PA's the biggest design consideration can be the trade-off between power efficiency and linearity of the output signal. High power efficiency is required as a PA generally has to drive an antenna at high power levels, resulting in large amounts of power being drawn from the supply. Increasing efficiency reduces operating costs and extends performance capabilities of the wireless device. Nonlinearity effectively causes transmission error in the system. Typically a system operates in a limited transmission band and a decrease in linearity causes the distortion components of a signal to spread into neighboring transmission channels. Most systems will attempt to filter signal nonlinearity out before transmission but filters are not perfect and fail to filter frequency components close to the source frequency. Hence, to achieve optimal linearity in the system while not trading off other desired characteristics of transmission system, other techniques must be used to minimise distortion. This gives rise to much of the amplifier designs today, which aim to reduce an amplifier's weak nonlinear distortion inherently in the circuit design.

2.2 Measures of Distortion

To accurately evaluate an amplifying stage we employ different measures of distortion. Each distortion measure is useful for specific applications but may not be useful in others. All measures are grounded by Taylor's Theorem, which states that any function can be represented as an infinite sum of the function's derivatives. In electronics, we often use the Maclaurin Series (a Taylor series centered around zero) to describe nonlinear devices as we are interested in

alternating current (AC) centered around a direct current (DC) bias. In weakly nonlinear distorting systems we can assume that the DC bias is the center of the input and output signals, therefore making our series expansion derivatives centered around zero. This makes the use of a Maclaurin series valid. We also assume that the system is operating in steady-state to avoid complex analysis of the start-up characteristics. This allows the less complex analysis of system transfer characteristics.

Let us consider a general transfer function, y, to be some function of x,

$$y = f(x). \tag{2.1}$$

Taylor's theorem allows us to replace the function applied to x with the following form,

$$y(a) = f(a) + f^1(a)(x-a) + \frac{f^2(a)}{2!}(x-a)^2 + \frac{f^3(a)}{3!}(x-a)^3 + ... \tag{2.2}$$

where $f(x)$ is expanded around the point $x = a$. Note that the series is truncated to the third-order for simplicity. Using a Maclaurin series allows us to simplify this to be

$$y(0) = f(0) + f^1(0)x + \frac{f^2(0)}{2!}x^2 + \frac{f^3(0)}{3!}x^3 + ... \tag{2.3}$$

Since the derivatives are now constants with x going to zero, they can be treated as such. One more step of simplification allows the description of a transfer function to be written as

$$y = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + ... \tag{2.4}$$

where a_n is the nth-order constant describing the magnitude of each term. These are often called the coefficients of the expansion. This form allows the coefficients to describe the magnitude of each term in a simple manner with a_n containing the factorial along with the derivative term. Note that if the coefficients a_2 and higher are zero, then the system is linear.

Each coefficient can be obtained using

$$a_n = \frac{1}{n!}\frac{d^n y}{dx^n}\bigg|_{x=0} \tag{2.5}$$

where again $y = f(x)$ is the transfer function.

Due to the fundamental nature of signal transmission, sinusoidal waves are almost always used as an input to amplifying systems. Using Fourier theory, we know that any sinusoidal signal can be represented by a power series of pure sine or cosine signals. This law, combined with Taylor's theorem allows an accurate description of distortion in all systems.

2.2.1 Harmonic Distortion

A fundamental result of distortion in nonlinear circuits is the generation of frequency components in the output signal which occur at integer multiples (harmonics) of the input frequency. This is called harmonic distortion, occurring due to a single sinusoidal input frequency.

Let a time-variant input function for an amplifier, $x(t)$, be defined as a pure sinusoidal wave

$$x(t) = A_1 \cos(\omega_1 t). \tag{2.6}$$

Substituting this function into Eq. 2.3 for a generalised transfer function will yield a series of coefficients describing the magnitude of the harmonic distortion terms in the output signal. In the interest of simplicity, this is commonly truncated after the third-order term and higher order terms are assumed negligible. This derivation yields the following,

$$\begin{aligned} y &= a_0 + \frac{a_2 A_1^2}{2} \\ &+ \left(a_1 A_1 + \frac{3 a_3 A_1^3}{4} \right) \cos(\omega_1 t) \\ &+ \left(\frac{a_2 A_1^2}{2} \right) \cos(2\omega_1 t) \\ &+ \left(\frac{a_3 A_1^3}{4} \right) \cos(3\omega_1 t). \end{aligned} \tag{2.7}$$

Eq. 2.7 shows the fundamental output tone (occurring at ω_1), and the second and third-order harmonic components (occurring at $2\omega_1$ and $3\omega_1$ respectively). The bracketed term associated with each harmonic component is the term which describes the magnitude of that frequency component. This is dictated by the

transfer function the input signal is driven through, which set the coefficients, a_n. These bracketed terms can be observed individually to obtain the magnitude of any harmonic component that is of interest[1]. The two remaining terms describe the DC component in the output signal.

A simple way to characterise the components of harmonic distortion in a system is total harmonic distortion (THD). It is the ratio of the sum of harmonic component powers compared with the fundamental component's power. THD is expressed as a percentage of distortion relative to the fundamental tone or in decibels (dB). Mathematically, it is expressed as

$$THD = \frac{\sum P_{HDn}}{P_{Fund}}, \tag{2.8}$$

where P_{HDn} is the power of the nth-order harmonic, and P_{Fund} is the power of the fundamental tone.

THD is a common measurement in high resolution data acquisition systems and high-fidelity audio equipment. For such systems it is important that all frequency components have minimal distortion, as it is not practical to filter the output [7]. Hence, THD is used to give an average of the distortion contribution of all harmonic components.

2.2.2 Intermodulation Distortion

Intermodulation distortion (IMD) is the distortion that occurs due to two or more sinusoidal input frequencies. This measure is employed where the fundamental tones of the input signal are required to be linear and the remaining spectrum can be filtered upon receiving the signal. Unfortunately, the third-order intermodulation distortion components appear adjacent to the fundamental tones. In telecommunication systems, transmission bands can be closely neighboring each other in the frequency spectrum. Thus, third-order distortion components can leak over into neighboring transmission bands causing unwanted interference. As previously mentioned, this is difficult to filter because the components occur close to the fundamental tones.

[1] Of interest to this work is the magnitudes of distortion components in transistor amplifiers. The full derivation of the single tone distortion components using the Ebers-Moll transfer function can be found in Appendix A.

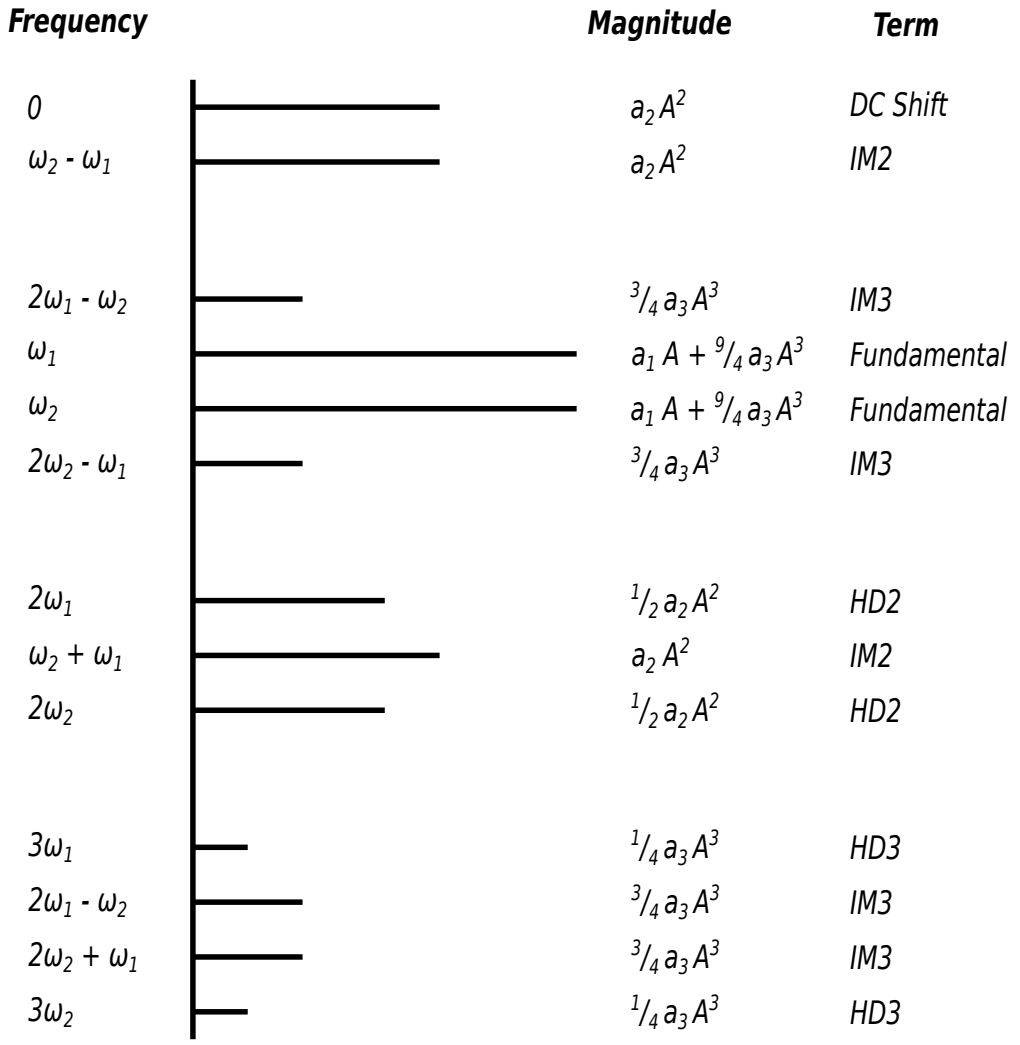


Figure 2.2: Frequency spectrum of harmonic and intermodulation tones generated by a two input signal through a generic transfer function.

Consider an input created by two sinusoidal tones,

$$x(t) = A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t). \tag{2.9}$$

Again, substituting this into Eq. 2.3 yields second and third-order coefficients[2]. Fig. 2.2 summarises the output signals frequency components (again truncated to the third-order) for a generalised transfer function. The harmonic terms are

[2]The full derivation of the two tone distortion components in a transistor amplifier using the Ebers-Moll transfer function can be found in Appendix A. This will make the coefficients specific to the Ebers-Moll function compared with the generalised form in Fig. 2.2

labeled as HD_n and the intermodulation terms IM_n for the nth-order power. Again, the series expansion coefficients are a_n for the nth-order power. Each coefficient shows the magnitude for each respective frequency component.

The intermodulation tones appear at different combinations of sums and differences of the fundamental frequencies. Of particular interest are the third-order components $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ which occur adjacent to the fundamental tones. As mentioned previously, these components are particularly difficult to filter due to their position. For this reason, circuit techniques which reduce third-order intermodulation distortion component are sought-after in amplifier design.

2.2.3 Third-Order Intercept Point

Analysis of distortion performance in RF amplifiers is commonly measured by the "intercept point" of the important frequency component relative to the fundamental component. When addressing the third-order distortion, this measure is called the third-order intercept point (IP3). It is a purely theoretical position in the amplifier's operating state, where the third and fundamental components become equal in terms of output power. Typically, the third-order frequency component is used however the second and fifth order components are used in some applications. This is due to the third-order component's intermodulation property where it manifests close to the fundamental tones, making it the most significant distortion component in many cases. The benefit of this measure is it gives a value which is independent of compression that begins to occur due to device saturation. Therefore, system distortion characteristics can be compared without the need to model compression characteristics. Figure 2.3 shows a graphical example of an IP3 point, where the dashed lines indicate the gradients of the linear regions of each component. The intercept point of these gradient lines indicate the IP3 point.

IP3 can be calculated by assuming that the linear region of the third order component has a gradient of 3, and the linear region of the fundamental component has a gradient of 1. These gradients are the result of plotting functions of the form $y = kx^n$ on a log-log scale. When a log function is applied, using basic logarithmic identities one can form the straight line equation as $\log(y) = k\log(x) + \log(a)$. Considering the form of a Taylor series expansion

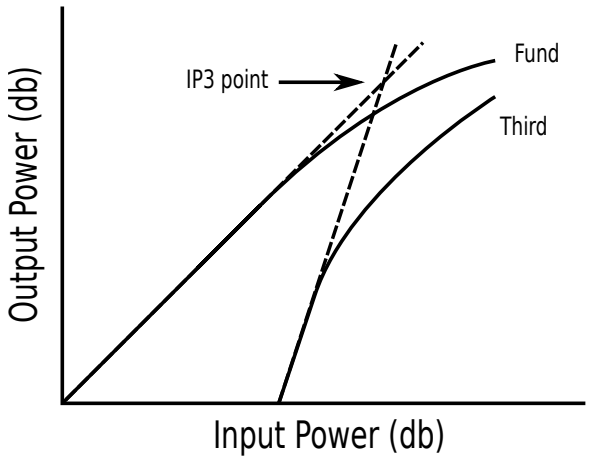


Figure 2.3: Graphical representation of third-order intercept point (IP3) on a input power vs. output power plot for a generic amplifier.

describing the third-order component, one can see it matches the form $y = kx^n$, hence n will be the gradient.

This means that an estimate can be made directly from a spectral analysis of the output. Often, the IP3 is referred to the input or output power level. Input-referred third-order intercept point (IIP3) uses the input power of the fundamental tone. Output-referred third-order intercept point (OIP3) uses the output power of the fundamental tone. OIP3 and IIP3 can be calculated using the equations below,

$$OIP3 = P_{Fund} + \frac{\Delta P_3}{2}, \tag{2.10}$$

$$IIP3 = (P_{Fund} - G) + \frac{\Delta P_3}{2}, \tag{2.11}$$

where P_{Fund} is the magnitude of the output fundamental tone, G is the gain of the amplifier, and ΔP_3 is the difference in magnitude between the fundamental and the third-order components at the output.

Care must be used when using this measure. Eq. 2.10 assumes the power measurements are taken at a position where the gradients are close to 1 and 3 respectively. This only occurs at lower input powers. At higher input powers, 5th and higher order terms begin to affect the third-order component resulting in a skewed gradients [8].

2.3 Distortion in BJT Circuits

The models commonly used to describe a BJTs transfer function are described in this section. In particular, the focus is on how distortion is generated through these models. This work is based around low-frequency input signals, however we will also explore how these models change with higher frequencies. This section aims to justify why low frequency will extend rather well into higher frequency works. This is based on the heterojunction bipolar transistor (HBT) and its close relationship to BJT operation.

2.3.1 BJT Models

In order to predict how a transistor circuit will operate, theoretical models are used to describe the transfer of voltage or current from the input node to the output node. Ebers and Moll invented the first practical large-signal model for a BJT [9]. This was followed up by Gummel and Poon who extended the model to include more subtle characteristics of a BJTs transfer function [10]. In modern electronics, a further improved version of the Gummel-Poon model is used for circuit simulation software, generally labeled as SPICE Gummel-Poon (SGP).

The classic mathematical model used for BJTs is the Ebers-Moll model. In its simplest form, it is written as

$$I_C = \alpha_f I_S e^{\frac{V_{BE}}{V_T}} \tag{2.12}$$

where I_C is the collector current, V_{BE} is the input signal, I_S is the base-emitter reversed biased saturation current, α_f is the unity gain factor, and V_T is the thermal voltage (written as $V_T = \frac{nkT}{q}$).

The commonly used equivalent circuit for the Ebers-Moll model is shown in Fig. 2.4. The equations which further describe this equivalent circuit can be found readily in electronics literature.

The Gummel-Poon model extends the Ebers-Moll model to account for other important phenomena in the transistor. For example, the transistor's current-gain being dependent on collector current, base-width modulation and high level-injection [11]. It is more comprehensive than the Ebers-Moll model and hence is used as the basis for most electronic simulation software like SPICE

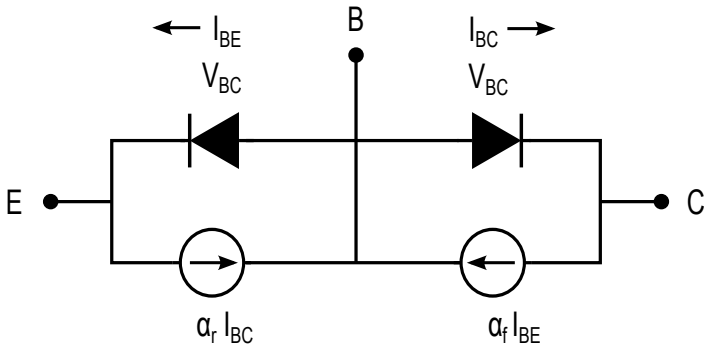


Figure 2.4: Large signal equivalent circuit for the Ebers-Moll model.

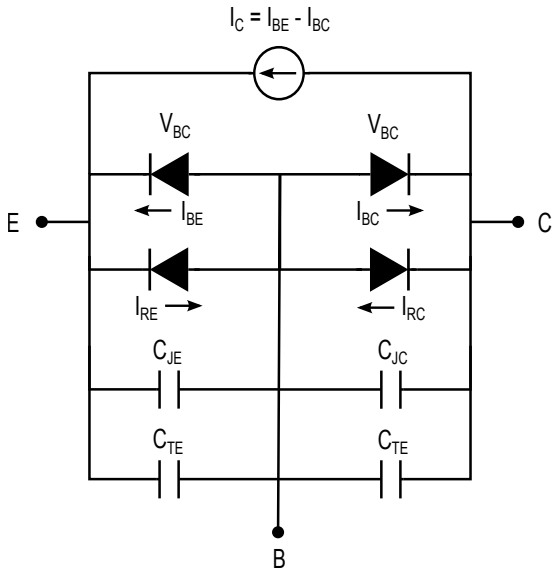


Figure 2.5: Large signal equivalent circuit for the Gummel-Poon model.

(Simulation Program with Integrated Circuit Emphasis) [12].

The large-signal equivalent circuit used in the Gummel-Poon model is shown in Fig. 2.5. Two extra diodes, with the currents I_{RE} and I_{RC}, show the reverse currents when the transistor is under reverse-bias conditions. This model also includes junction capacitances which will be covered later in the chapter.

The Gummel-Poon collector current for a forward-biased transistor is defined as

$$I_C = \frac{I_S}{q_b} e^{\frac{V_{BE}}{V_T}} - \frac{I_S}{q_b} e^{\frac{V_{BC}}{V_T}} \tag{2.13}$$

where q_b is the base charge to zero-bias base charge ratio. This ratio is described by more complex equations (containing modeling for temperature and current

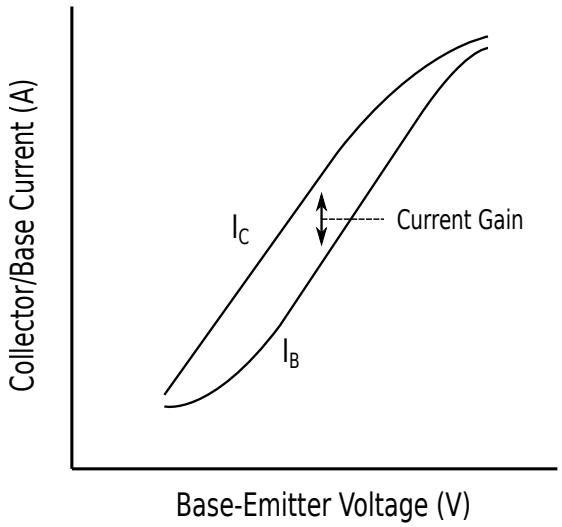


Figure 2.6: Gummel plot showing the nonlinear variation of collector current, I_C, relative to base current, I_B. This leads to the nonlinearity of current gain and higher and lower collector currents.

gain non-linearity) which can be found in the original paper [10].

With the definition of the Gummel-Poon model stated, we now explore one important phenomenon that the model considers over the Ebers-Moll model. The current gain dependence on collector current is elegantly displayed by a Gummel plot, which shows base-emitter voltage versus current for a BJT device. This is seen in Fig. 2.6, which shows as collector current increases we observe a nonlinear difference in the ratio of collector to base current.

Note that the region at mid-range currents is rather linear, and this is a fair assumption for most BJT devices as the current gain will have minimal variation in this region. This allows the use of simplified models when deriving distortion theoretical products. In the Ebers-Moll model this is considered to be a linear relationship. In some cases this nonlinearity in current gain must be considered to achieve accurate operation in a BJT amplifier.

Of course, the two presented models only describe the saturation region of operation while other equations are used to describe both the active and cutoff regions. For this thesis, we are only interested in the saturation region of amplification. There are also other more complex models that are used heavily in industry. Such examples are the vertical bipolar inter-company model (VBIC) and the MEXTRAM model. These models further account for the very subtle

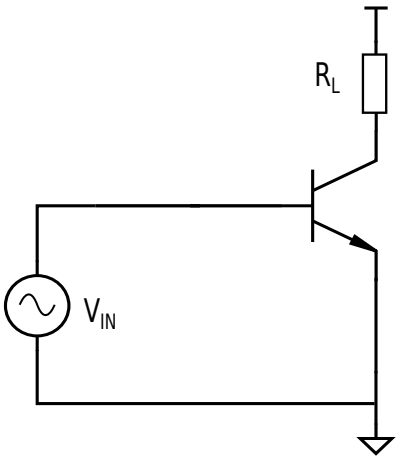


Figure 2.7: A typical single BJT transistor common-emitter amplifier used for transfer analysis.

characteristics of a bipolar transistor.

2.3.2 BJT Distortion Characteristics

Combining the presented Ebers-Moll model with the previously presented distortion theory allows the prediction of BJT circuit distortion characteristics. Let us consider the most simple BJT amplifier in the form of a common-emitter amplifier, seen in Fig. 2.7.

The input signal contains both AC and DC components as in Eq. 2.14. This is substituted into the Ebers-Moll model in Eq. 2.15.

$$V_{IN} = A_1 cos(\omega t) + V_{DC}, \tag{2.14}$$

$$i_C = I_S e^{\frac{A_1 cos(\omega t) + V_{DC}}{V_T}}. \tag{2.15}$$

The DC component of the input signal is separated out by simplifying Eq. 2.15 to be

$$i_C = I_{CQ} e^{\frac{A_1 cos(\omega t)}{V_T}}, \tag{2.16}$$

where I_{CQ} equals the DC portion of the input signal (given by $I_{CQ} = I_S e^{\frac{V_{DC}}{V_T}}$). Using Eq. 2.4, a Taylor expansion is applied to Eq. 2.16 which yields the series

expansion[3] of the transfer function as

$$\begin{aligned} i_C &= I_{CQ} + I_{CQ}\frac{A_1^2}{4V_T^2} \\ &+ I_{CQ}\left(\frac{A_1}{V_T} + \frac{A_1^3}{8V_T^3}\right)cos(\omega t) \\ &+ \frac{1}{4}I_{CQ}\left(\frac{A_1}{V_T}\right)^2 cos(2\omega t) \\ &+ \frac{1}{24}I_{CQ}\left(\frac{A_1}{V_T}\right)^3 cos(3\omega t). \end{aligned} \tag{2.17}$$

This equation describes the output distortion as a function of the input signal, for a fundamental input tone occurring at ω. The second and third harmonic occur at 2ω and 3ω respectively and higher order terms have been truncated.

It is important to note that the distortion component's position in frequency is only dependent on the input signal frequency, while the magnitude of the component is dependent on temperature, DC bias, and input signal magnitude. It also depends on subtle BJT characteristics such as base-width modulation which will be discussed later in the chapter. This derivation gives a good representation of how distortion components are derived and how one can analyse an amplifier's transfer characteristics.

2.3.3 Effects of Frequency

A BJT's physical structure contains parasitic capacitances which are created between the different structural layers of the device. From basic theory, it is known that a capacitor's impedance decreases with increased frequency. Therefore, as input signal frequency increases, so does the effect of these capacitances upon the device's transfer characteristics. To understand this effect, consider the updated Ebers-Moll equivalent circuit in Fig. 2.8, including the important parasitic junction capacitances. C_{JE} is the capacitance from the base node to the emitter node, and C_{JC} is the capacitance from the base node to the collector node.

Consider the impedance looking into the base connection. If the impedance

[3] The full derivation of the single tone coefficients for a BJT can be found in Appendix A.

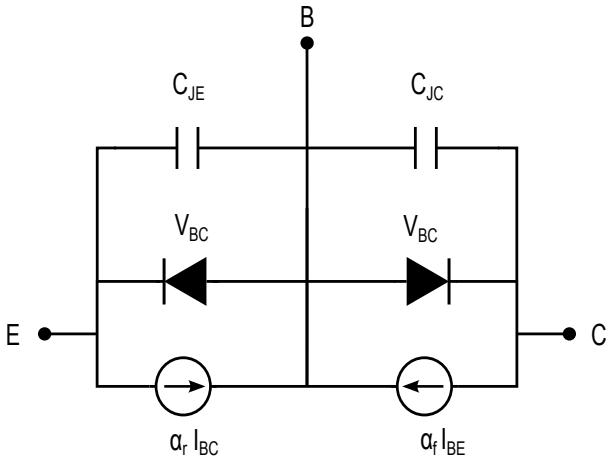


Figure 2.8: Ebers-Moll large signal equivalent model of a BJT, now including the two parasitic junction capacitances.

of these capacitances is low, then the input signal leaks through to the emitter/-collector node, decreasing the effective input signal level. From fundamental electronics theory we know that as frequency increases the gain of the amplifier will decrease. At some point the gain of an amplifier will reach unity; a current gain of 1 is reached. This is called the cutoff frequency, f_T, and can be calculated through Eq. 2.18. General purpose transistors have a f_T of roughly 50 MHz to 1 GHz.

$$f_T = \frac{1}{2\pi C_{ie} r_e} \tag{2.18}$$

where C_{ie} is the capacitance seen looking into the input node, and r_e is the resistance seen looking into the emitter [13].

Junction capacitances are also inherently non-linear. They can be described by the functions below and a general plot is shown in Fig. 2.9.

$$C_{JE} = \frac{C_{JE0}}{(1 - V_{BE}/\phi_E)^{m_E}}, \tag{2.19}$$

$$C_{JC} = \frac{C_{JC0}}{(1 - V_{BC}/\phi_C)^{m_C}}, \tag{2.20}$$

where C_{JE0} and C_{JC0} are the capacitance values at zero-bias across the respective junction, ϕ_E and ϕ_C are the base-emitter and base-collector barrier potentials, and m_E and m_C are the base-emitter and base-collector gradient factors related to the doping of the junction [11]. The non-linearity of the capacitances make

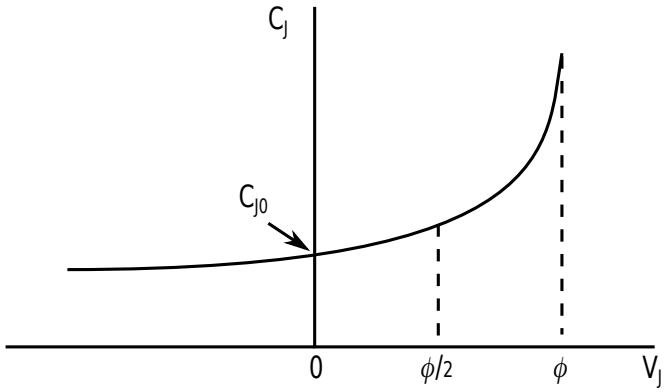


Figure 2.9: Plot of junction capacitance versus junction voltage, showing the nonlinearity of the capacitance at higher voltages.

the algebraic derivations of distortion far more complex at high frequencies and hence it is ignored in a lot of cases. This includes most SPICE simulators which instead approximate the capacitor's nonlinear function to a simpler form.

In this work we focus on low-frequency application, so input signals used are well below the cutoff frequency of a standard transistor. Applications requiring distortion reduction still exist at low frequencies such as audio applications, low-noise amplifiers (LNAs) and mixers. There also exists different transistor structures which have far higher cutoff frequencies than a standard BJT, allowing low-frequency distortion analysis to be sufficiently accurate and insightful.

2.3.4 Heterojunction Bipolar Transistors

The performance of BJT devices can be increased through modifications to the base junction of the device. The base substrate can be built using differing materials from the emitter and collector, such as silicon-germanium, indium-phosphide or indium-gallium-arsenide. During manufacture, the base substrate is graded with these materials such that the device's bandgap is narrower at the collector than the emitter. This has the effect of increasing the switching speed, increasing current gain and increasing cut-off frequency of the device. The resulting device is called a heterojunction bipolar transistor (HBT).

HBTs are an attractive technology for use in radio-frequency (RF) applications. Among other reasons, this is due to their extremely high frequency cutoff, with literature confirming values well into the hundreds of GHz range [14, 15].

Practically, a BJT and a HBT operate under extremely similar theoretical laws. The Ebers-Moll equation will accurately describe the transfer function up until the junction capacitances become non-negligible. Because of the high cutoff frequency, distortion analysis is accurate up to very high frequencies [16]. Base-width modulation and high level injection effects also have a decreased impact in HBTs [17].

One drawback of using HBTs is the increased manufacture complexity and cost. This is due to the multiple layers of diffusion required to fabricate the devices base junction. HBTs are only used in IC technologies and are rarely found as a discrete device.

2.4 BJT Non-idealities

Non-idealities of a BJT are characteristics of the device which skew the transfer function away from the idealised Eq. 2.12. Sometimes, a circuit design can force some system-wide condition in which a nonideality has a negligible impact, for example a bandgap voltage reference rejects changes in temperature. However, this is not always possible. It then becomes important to account for the impact of nonidealities in a system.

Here we will summarize five specific non-idealities that can skew the transfer function and affect distortion in a BJT device. Each one needs to be considered in order to make accurate predictions of distortion levels in amplifiers.

2.4.1 Temperature

Temperature is a fundamental factor in the operation of a semiconductor device. This stems from the semiconductor physics of a PN junction, in which the junction's built-in barrier voltage is a function of temperature [6]. It has a direct impact on the Ebers-Moll model in Eq. 2.1 through the thermal voltage, V_T, which increases proportionally with temperature. Second-order effects also occur due to device parameters having a dependence on the barrier junction voltages. This impacts model parameters such as the saturation current I_S, junction capacitors, and the current gain [11].

There is little one can do to minimise temperature variations in a single

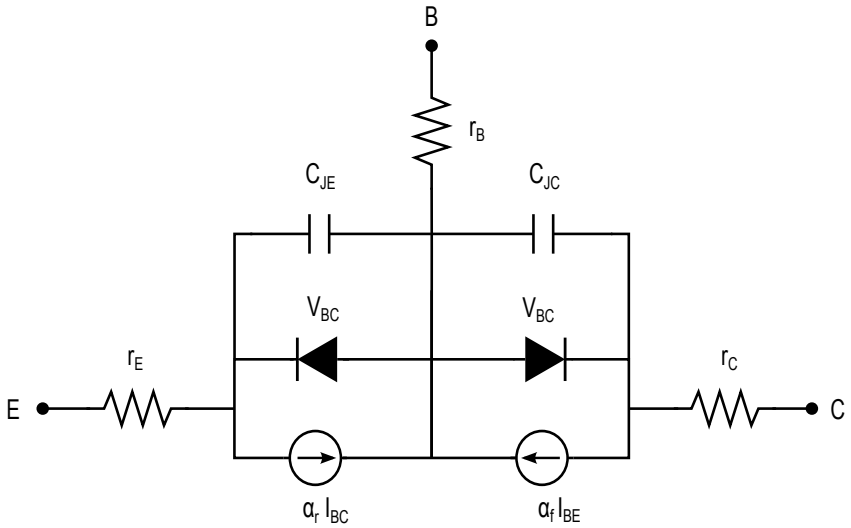


Figure 2.10: Ebers-Moll large signal equivalent model of a BJT, now including parasitic resistances.

semiconductor component. However, some circuit design techniques lessen the impact of temperature, and in some cases make it negligible for a certain parameter. For example, using integrated transistors on an IC as opposed to discrete transistors, minimises the temperature difference between each transistor. This occurs because the displacement between each semiconductor junction is minimised in an IC therefore the junctions will experience a smaller temperature difference relative to each other. Consequently, the transistors are very close in terms of their temperature dependent parameters (current gain, saturation current etc) and a temperature resistant circuit can be designed around this relationship. One example is the centroid circuit layout [18].

2.4.2 Parasitic Resistance

The imperfect structure of a BJT device means that there are some unwanted resistive components between the terminals of the device. This can be caused by the resistivity of the semiconductor material or the bonding and connections of the device package. These are often termed the parasitic or extrinsic resistances of the transistor and can be modeled by the inclusion of extra base, collector, and emitter resistances. Fig. 2.10 shows the Ebers-Moll equivalent circuit model adjusted to include parasitic resistances.

If parasitic resistances are large enough, they can change the operation of an

amplifier. Consider an applied DC base-emitter voltage for the device in Fig. 2.10. This voltage must now be divided between the base-emitter junction and the emitter and base resistors. This changes the DC operating point of the amplifier. The emitter resistor has the effect of degenerating the amplifier (commonly called emitter degeneration in the literature) which linearises the amplifier and reduces its gain. As shown later in the chapter, this is the implementation of feedback inside the packaged device.

Other BJT parameters depend on these parasitics. For example, at high frequencies, r_B, sets the input noise current which is important for low-noise applications [16]. Other parasitic resistances also exist in a BJT device. However for the purposes of this work they will have a negligible impact and therefore can be excluded.

2.4.3 Base-width Modulation

Base-width modulation is the name given to the dependence of collector current on collector-emitter voltage. It is also commonly called the Early effect. The impact of this dependence is perhaps best represented as an I_C vs. V_{CE} plot, shown in Fig. 2.11. Ideally, a transistor should maintain a constant collector current I_C for any value of collector-emitter voltage V_{CE} while it is operating in the active region. However, as V_{CE} increases, the reverse-bias voltage across the collector-base junction also increases. In turn, this increases the junction's depletion region and decreases the effective base width of the device. We know from semiconductor physics that saturation current (and therefore collector current) will increase proportionally with base width [6]. Hence, the collector current will vary proportionally with collector-emitter voltage in the active region.

The effect can be modeled by including a term in Eq. 2.12. This is seen below in Eq. 2.21

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \left(1 - \frac{V_{CE}}{V_A}\right), \tag{2.21}$$

where V_A is the Early voltage (shown on Fig. 2.11). Generally, discrete transistors have an Early voltage of roughly -50 V to -100 V. The effect can become negligible as the Early voltage increases and V_{CE} decreases.

Following from the series expansion of a common-emitter amplifier in Eqs. 2.15-2.17, we can include base-width modulation resulting a new term bound to

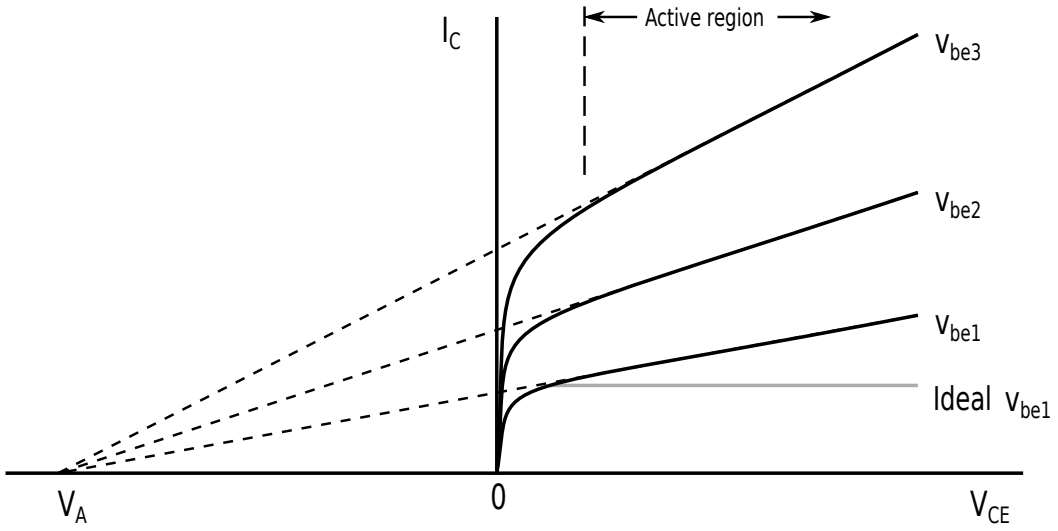


Figure 2.11: Graphical representation of base-width modulation, showing the dependence of collector current on collector-emitter voltage for a number of different V_{BE} values.

the distortion components. The DC quiescent current now contains the base-width modulation effect.

$$\begin{aligned} i_C &= I_{CQ} + I_{CQ}\frac{A_1^2}{2} \\ &+ I_{CQ}\left(\frac{A_1}{V_T} + \frac{3A_1^3}{4V_T^3}\right) sin(\omega t) \\ &+ \frac{1}{2} I_{CQ}\left(\frac{A_1}{V_T}\right)^2 sin(2\omega t) \\ &+ \frac{1}{6} I_{CQ}\left(\frac{A_1}{V_T}\right)^3 sin(3\omega t), \end{aligned} \tag{2.22}$$

where I_{CQ} is now defined as

$$I_{CQ} = I_S e^{\frac{V_{DC}}{V_T}}\left(1 + \frac{V_{CE}}{V_A}\right). \tag{2.23}$$

From this derivation, we see the base-width modulation effect can be considered as a scale factor to the DC current, therefore having the effect of scaling the generated distortion components. It is commonly modeled as a resistor in parallel with the device output ports.

Consequently, due to the scaling of I_{CQ} from base-width modulation, the

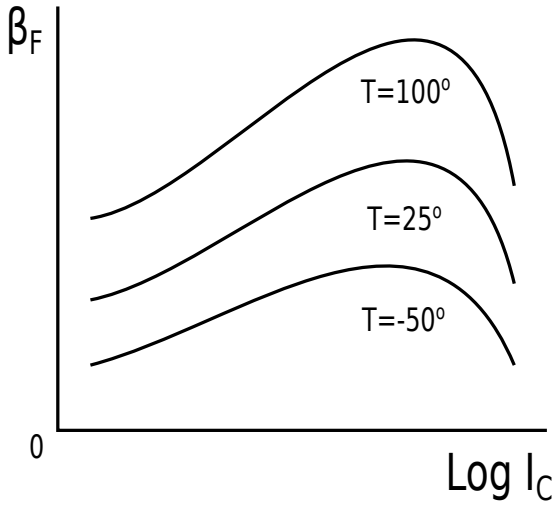


Figure 2.12: Graphical representation of the nonlinear variation in current gain.

current gain of a transistor is also scaled. This is modeled by Eq. 2.24 below.

$$\beta = \beta_0 \left(1 + \frac{V_{CE}}{V_A}\right). \tag{2.24}$$

In some cases the entire effect is simply ignored and its impact assumed negligible due to a sufficiently high Early voltage. Good examples of this are many of the upcoming references [19, 20, 21, 22].

2.4.4 Nonlinear Beta

Previously, Fig. 2.6 introduced a Gummel plot which shows a generalised relationship between base and collector current in a BJT. The ratio of the two currents represents the current gain, β. Observing this plot shows a clear nonlinear relationship between the two currents. If current gain is plotted, the result is a nonlinear curve as shown in Fig. 2.12. This nonlinearity stems partly from low and high current effects in the semiconductor junctions.

At low base currents, we observe a deviation from the expected log-linear base current. This is observed in Fig. 2.6 at the bottom end of the base current trace. This is caused partly by a recombination process occurring in the base region. As electrons travel into the base junction, some combine with the majority carriers of the region (holes for a NPN device). Usually, the base is thin and lightly doped

so the impact of base recombination is small. However, at low base currents the effect becomes non-negligible. This results in a nonlinear current gain at low base/collector currents [6] [11].

At high current levels, both the base and collector come under the effect called current crowding. Bipolar devices generally have a very thin base layer and a current will experience an intrinsic non-negligible base resistance as it travels through this region. This causes a non-uniform distribution of current-density in the emitter region, resulting in current crowding at the edges of the emitter junction. As current increases to high levels, the effect manifests as a decrease in the log-linear trend of collector current, and hence a nonlinear beta at higher currents.

Finally, both currents are modified by high-level injection and by base-width modulation [11]. High level injection effects can be assumed negligible if the devices are not operated at high currents.

This current gain nonlinearity is important to consider when devices in the same circuit are operating at different bias currents. This introduces error into output of the circuit due to the discrepancy in current gain between the two devices.

2.4.5 Process Variation

Unfortunately, transistor fabrication processes are imperfect and result in semiconductor devices having slightly different structural parameters. In particular, the current gain and saturation current parameters can vary due to mismatches in the emitter-area ratios [23]. Generally, smart fabrication techniques are employed to minimise the mismatch between devices in each fabrication run. This is a fundamental reason why integrated BJT circuits are more accurate compared to discrete circuits. In an IC, each transistor is fabricated on the same wafer under the same conditions, resulting in minimal variation of emitter-area ratios. This intra-wafer variation is called mismatch variation, and generally results in no more than 1-2% variation in modern processes[4].

The parameters of all devices on an entire wafer can also vary from that ex-

[4]These values are the authors estimates based on various references [24, 25, 26] and personal communication with the project supervisors [27, 28]. Exact process variations are dependent on factors such as the total area of the circuit layout.

pected from the fabrication process. Commercial devices state fixed parameter values on their respective datasheets and SPICE models. Therefore, measurements can have some variation from what theory and simulation predict, due to entire fabrication runs varying slightly from their stated norms. This inter-wafer variation is called absolute variation, and generally results in no more then 20% variation in modern processes. Note that the percentages for both variation types are dependent on the specific fabrication process, and the size of the device being fabricated.

Both types of process variations can have varying degrees of impact depending on the application. For example, in translinear bias circuits both can result in non-negligible errors in the circuit [29]. A bias current is required to be a certain value, and both types of variations can shift the current. Conversely, in an differential amplifier circuit fabricated on a single wafer, absolute variation is not impactful in terms of input offset voltages. This offset is only determined by the mismatch between specific devices, and hence only the mismatch variation [23].

Consideration of both process variations is important for making a circuit design commercially viable. Indeed, any circuit can be trimmed or adjusted post-production to compensate for process variation. However, this results in a less cost-effective product, or more complex implementations for the consumers. Considering process variation during the design of a circuit is good engineering practice.

2.4.6 Summary of Non-idealities

This section summarises what are considered the main non-idealities involved with the following works. Indeed, there is a large amount of literature based around the subtleties of transistor transfer characteristics which is not covered here. The presented theoretical models only account for the most basic non-idealities. Furthermore, the SGP model does not account for all BJT effects such as self-heating [17]. So it is possible works based on these models have small inaccuracies.

We justify the use of these models by using a process of theoretical prediction, simulation, and physical measurement. By comparison of measurement and simulation back with theory, the total inaccuracy of theory in inherently

Technique	Linearisation	Bandwidth	Efficiency	Complexity
Feedback	Good	Narrow	Medium	Medium
Feedforward	Good	Wide	Low	High
Predistortion	Medium	Medium	High	Low

Table 2.1: Comparison of linearisation techniques in amplifiers.

quantified as a whole. This process follows three steps:

- Theoretical prediction using the Ebers-Moll model. This gives a general idea of what to expect from a circuit.
- Simulation using an advanced model like SGP. This gives an accurate evaluation of the circuit characteristics.
- Measurement of the circuit. This confirms the accuracy of the theoretical and simulated predictions.

If each step matches the other steps to a reasonable degree, we can be sure the unaccounted non-idealities have a negligible impact on the system.

2.5 Linearisation Techniques

By understanding the models of the semiconductor devices, one can develop techniques which manipulate the characteristics of the models in order to linearise the amplifier's transfer function. This section briefly describes three common methods used in modern BJT amplifiers. Each technique has certain advantages and disadvantages [30]. These are summarised in Table. 2.1.

2.5.1 Feedback

Feedback can broadly be defined as the act of taking a portion of the output signal and adding it back into the input signal. This can have a positive effect of correcting the input signal such that the output signal has smaller distortion components. In terms of amplifiers there are four common types of feedback

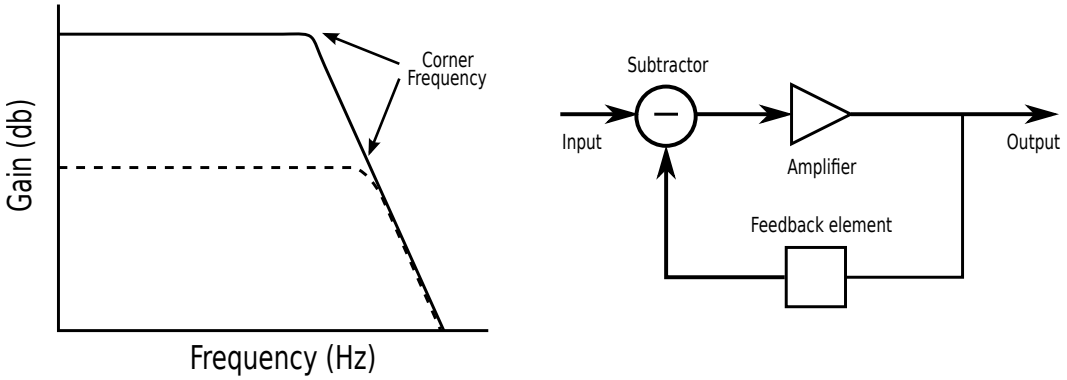


Figure 2.13: *Left:* Bode plot for a generic amplifier. Solid line shows open-loop gain of a generic amplifier (no feedback). Dashed line shows feedback added to the generic amplifier, decreasing gain and increasing bandwidth. *Right:* General configuration of a feedback topology using a feedback element to adjust the input dependent on the output.

amplifiers; current, voltage, transconductance and transresistance. These are defined as such based on what they sample at their output and sum at their input (more detailed explanations of these types is readily found in the literature [6]).

When considering BJT amplifiers, feedback is commonly separated into two categories; series and shunt feedback. One common technique is to use series feedback in the input loop of a common-emitter amplifier. This is also called resistive emitter degeneration in the literature. By adding a resistor in series with the active junction of a transistor, the input signal voltage is divided between the nonlinear junction and the linear resistor. This can be thought of as a current sample of the output current which is then fed back into the input signal as a voltage. This has the effect of reducing the magnitude of all frequency components in the output spectrum up until the corner frequency of the amplifier. Effectively it is a trade-off in gain for decreased output distortion components. One other beneficial effect is the small increase in bandwidth of the amplifier, due to the global compression of all frequency components. Fig. 2.13 shows the effects of feedback.

At high frequencies, the amplifier's loop gain must remain low enough to maintain stability in the amplifier. For this reason, feedback is only used in small amounts in some broadband and RF amplifiers. Often a filter is used at the amplifier input to maintain stability which further reduces the amplifier operational bandwidth.

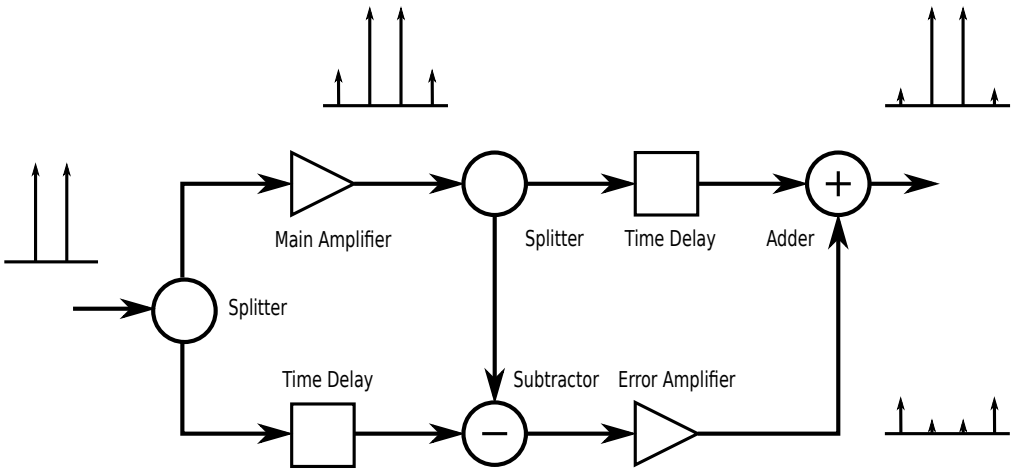


Figure 2.14: General configuration of a feedforward topology using both a main and error amplifier stage.

Feedback amplifiers suit applications where gain is not important or in excess. A circuit design can then trade it off for increased linearity or bandwidth. However, sometimes gain is important so designers look for other methods of distortion reduction. Compared to other techniques, feedback still results in a rather narrow band of stable operation which is another drawback of feedback [4].

2.5.2 Feedforward

Feedforward can broadly be defined as the act of comparing the input and output signals of an amplifier, modifying a portion of it to have a complementary distortion characteristic, and recombining it with the main amplifier's output signal. The error correction occurs after amplification of an input signal. A generic circuit setup will include two stages, a main amplifier and an error amplifier. The main amplifier is optimised for gain while the error amplifier is optimised towards canceling the main amplifier's distortion tones. A general configuration of feedforward linearisation is shown in Fig. 2.14. This figure shows the important stages in the distortion characteristics in both the main and error amplifier. Note that the time delays and signal couplers can change depending on the amplifier topology.

Ideally, this technique does not reduce gain and is unconditionally stable leading to its operational bandwidth being high. This makes it an attractive

technique when compared with feedback systems. Unfortunately, this method suffers from some drawbacks. Amplifier designs are more complex and contain multiple components and amplifying stages. Therefore power efficiency is low due to the need for multiple amplifiers. The design must also account for gain and phase shift issues due to the input splitting of the signal. Finally, this technique can be sensitive to mismatches between the two amplifying stages potentially resulting in sub-optimal distortion and gain [4].

2.5.3 Predistortion

Predistortion is the creation of a complementary distortion characteristic to that of the main amplifier's distortion characteristic, without sampling the main amplifier's output. Consider two amplifying stages operating in series. The distortion components of each stage will constructively interfere. By inverting the phase of one of the amplifiers these distortion components now destructively interfere, resulting in reduction of the overall distortion component.

Predistortion has become a fundamental building block in PAs in the telecommunications industry. Designers aim to operate the PA with an optimal compromise between linearity and efficiency. Using predistortion allows a PA to operate at a higher power efficiency while maintaining close to the same linearity levels because they can operate close to the amplifier's compression point. Hence a predistorter stage is generally used to cancel distortion arising from compression, not distortion inherent to the amplifier topology. The effect is shown in Fig. 2.15.

This linearisation technique is relatively simple, requiring fewer components in its implementation and therefore lowering manufacturing costs. It easily translates into higher frequencies and can maintain a wide linearisation bandwidth. Predistortion is best employed after the amplifier has been designed and its distortion characterised. The predistorter circuit can then be tuned to cancel the amplifier's distortion. The disadvantages of predistortion include having only a modest improvement compared with other techniques, and having problems reducing multiple orders of distortion components. However, modern systems employ complex techniques to reduce the impact of these disadvantages [4].

Commonly both a predistorting stage and feedforward are used together. For this reason, definitions of predistortion can become blurred with that of feedfor-

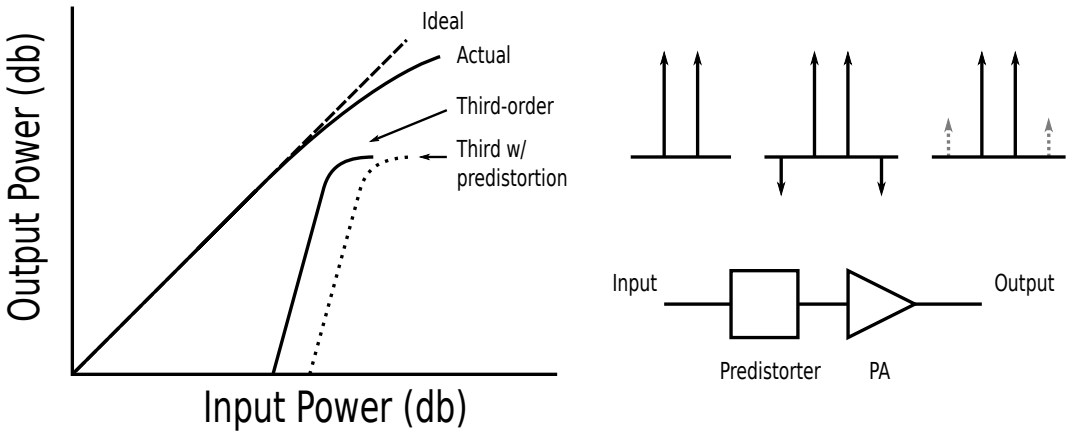


Figure 2.15: *Left:* Power input vs. power output plot for a generic amplifier. Shows the original amplifier third-order relative to the fundamental. *Right:* Shows the stages of predistortion. The three frequency spectrums show each stages contribution leading to cancellation of the third-order components in the final output.

ward. One example is implementing an extra control loop to adaptively adjust the predistorter. The predistorter samples the output distortion components of the main amplifier and adjusts the predistorter accordingly. This is the dominant method of linearisation in modern RF PAs. Adaptive control of the predistorter can be employed such that variation in the main amplifiers operating conditions can be accurately compensated [31].

2.5.4 Harmonic Termination

Since distortion components occur at differing frequencies, they can also experience different impedances at an amplifier output. This means amplifiers can be terminated on their load or source ends such that their harmonic output components are suppressed. This is essentially filtering or bandpassing the output signal such that the higher frequency components experience a higher impedance path. This method is generally employed at higher frequency levels where source and load impedances require impedance matching regardless of distortion reduction.

Utilizing this requires a process called load pull. This process consists of tuning the source and load impedances at each individual harmonic frequency and mapping the performance of the device. The correct optimisation between

source and load impedances can then be selected.

This process is generally employed on most RF amplifiers, alongside other distortion reduction methods, however it is not specifically a linearisation technique of interest to this work. Nevertheless, it is commonly used in RF amplifiers and hence is worth identifying.

2.6 General Literature Review

Due to the structure of this project, where three works are loosely related under the theme of distortion, parts of the literature review are contained within each chapter. Therefore, the reviewed literature that is specific to a certain work is located in that chapter. Specifically, this section reviews the theoretical and mathematical basis for describing linearity and techniques to increase linearity while maintaining gain. The need for optimisation between these two parameters demands a strong understanding of its fundamental causes and the methods used to model distortion components in amplifying stages.

Academic literature yields many insights into describing linearity in transistor devices. One well-known contribution to the literature is [32] who first presents a Volterra series as a method of analysis for amplifier circuits. He further develops this theory in a later paper [33]. This method follows a similar procedure to the common Maclaurin series expansion. Furthermore, it allows signal delay to be accounted for which is beneficial for amplifier systems with memory. Another recent well-known work in understanding bipolar device distortion is [21] who eloquently describes a mathematical basis for distortion in bipolar and MOS devices, and also extends into distortion in differential amplifier topologies. This work is often cited in literature when dealing with linearity.

High frequency distortion has also been well researched. Poon in [34] first proposed grading the width of the collector in a bipolar device to increase linearity at higher frequencies. Transistor layout techniques for low distortion at high frequencies are presented in [35] which describes device parameters that affect distortion and gain. In particular, the parasitic capacitance from base to collector must be minimised for low distortion at higher frequencies. This is done by optimising the epitaxial layer characteristics, to influence parameters such as the Kirk effect, breakdown voltage, collector depletion region, and device

gain. More modern work in [36] shows it is possible to link a device's distortion characteristics to its cutoff frequency. This work describes the underlying mathematics for high-frequency harmonic cancellation effects due to feedback from distortion currents also acting upon the input impedance.

In recent times within area of distortion in bipolar devices, there has been a significant amount of work regarding linearity in HBT devices. As shown in [16, 17] these devices outperform BJTs to a significant degree. Hence these devices get more attention in the literature regarding their inherent distortion characteristics and distortion reduction methods in HBT amplifiers. One well-known analysis is [37] which describes a fundamental basis for intermodulation distortion in HBT devices. This follows the well-known Volterra series expansion presented previously in [32] and derives the coefficients (kernels) for the second and third-order distortion components based on HBT transfer functions. It is noted in this work that distortion cancellation effects arise due to a HBT's base-emitter junction capacitance interacting with junction resistances. It is expanded on in detail in [38] which describes the distortion components while considering many extra device non-idealities.

Distortion reduction techniques which take different approaches in bipolar devices also appear in the literature. Yoshimasu presents a linearizing bias circuit for a HBT power amplifier [39]. This utilizes a second diode-connected HBT as bias circuitry that slightly increases DC bias voltage as RF input power increases. This results in a decreased gain compression as the DC bias adjusts dynamically with input power. Other authors expand on this bias technique [40].

Today, there exists a wide variety of commercial amplifiers, all designed to fit specific applications. Generally, the trade-off between gain and linearity is always optimised, alongside frequency range, noise and other parameters. A good example of a two products optimising for gain and linearity is the Maxim MAX2601 [41] and MAX2232 [42]. The MAX2601 is a silicon bipolar transistor aimed at delivering 1 Watt of RF power with a high degree of linearity for 900MHz cellular applications. The topology is a single bipolar device with simple bias circuitry used to control temperature variation. To contrast, a topology can become vastly more complex when further specifications are required. The Maxim MAX2232 is a narrow-band nonlinear 250mW linear power amplifier with gain/thermal control, aimed at higher power gain for the 900MHz cellular range.

The output amplifier stage is still a single silicon bipolar transistor, however the package now contains three amplifying and conditioning stages with additional circuitry to maintain the transistors bias conditions.

3

Third-Order Distortion Null

An interesting characteristic of the exponential transfer function of BJTs is a local minima (or null) occurring in its third-order distortion product. The phenomenon has been well documented by several authors and is described as interesting, but not many references identifying its use in a practical application have been found. The most probable reason for this is that the emitter resistance, defined by device manufacturing considerations, positions the null at low bias currents in comparison with those possible for a given device. This deprecates its usage in most applications in favour of some other alternative. If one can force the minima to occur at higher bias currents, then this characteristic becomes more feasible as a distortion reduction technique. This is the motivation for this chapter.

On a fundamental level, this characteristic extends into HBT devices as well. This is based on the fact that the device physics of an HBT mimic BJTs rather precisely up until device capacitances start to have a non-negligible impact [17]. HBTs operating frequency can easily reach 1-10 GHz before this starts to occur. Because of these two factors, one can safely assume that low-frequency analysis

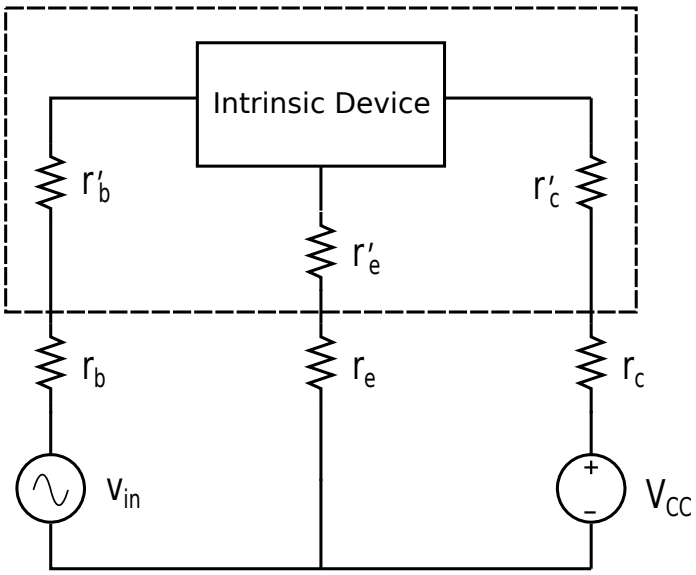


Figure 3.1: A simple BJT amplifier showing the combination of intrinsic and extrinsic resistances associated with series resistance.

is useful in the literature, up until extremely high frequencies are needed.

In this chapter the circuit conditions for a single transistor's third order distortion minima are outlined. Firstly, a review of the current literature surrounding third-order distortion minima in bipolar devices is presented. The currently accepted mathematical proof of a single BJT common-emitter amplifier is described, and then this is extended to propose a novel proof of the same phenomena in Darlington transistors. The new theory allows a prediction to be made about Darlington common-emitter amplifiers, in that its distortion null occurs at double that of a single BJT. The new theory is applied to a discrete amplifier design to review its performance in a practical situation. Measurement data are presented which confirm the relationship between a single BJT null and a Darlington null.

3.1 Introduction

The third-order distortion null of a single BJT amplifier is a position in the transistor's DC bias where the magnitude of third-order harmonics and distortion products tend towards zero. The exact physical mechanism as to why the null occurs is not clear in the literature. However the mathematical theory is rather

rigorous. Detailed insight is provided by Reynolds [43], one of the first authors of the phenomena, who states;

> "An insight can be obtained, however, if one lets $v_r = i_e r_1$. This voltage appears across the emitter-base junction in series with, but in opposition to v_s. It appears that when the nonlinearities are acted on by these two voltages they produce two components of third-order diffusion currents which are opposed to one another. When r_1 is properly adjusted these two currents cancel. With r_1 above or below this critical value one component or the other dominates."

In other words, when a series resistance voltage component, v_r, (created by the emitter current, i_e, across the series resistance r_1) matches a condition related to the input source voltage, v_s, acting across the transistor input impedance (represented in the text as admittance, y_{12}), a cancellation of the two resulting third-order currents occurs. Generally, the series resistance is defined as the resistance seen by the emitter current, which includes parasitic resistances and the base resistance reflected through the base current of the transistor. An equivalent circuit is represented in Fig. 3.1 where the series resistance is defined as

$$R_{EE} = R_E(1+\frac{1}{\beta}) + \frac{R_B}{\beta} \tag{3.1}$$

where $R_E = r_e + r_e'$ and $R_B = r_b + r_b'$. These show the intrinsic parasitic resistor combined with external resistors in the circuit. β is the mid-range current gain of the transistor.

Reynolds is stating that, by analysing the third-order intermodulation products and including intrinsic resistances, it becomes clear a distortion null occurs and is dependent on the transistor's series resistance. Practically this means it is possible to make single BJT amplifiers with reduced third-order distortion components by either varying the emitter or base resistances.

3.2 Literature Review

From the prior introduction, we see that the theoretical third-order null is proven to exist in early electronics literature such as [43]. This effect was actually cited

earlier in time by [44] and [45]. However, these were brief analytical derivations and did not go into depth as Reynolds did. There has been little research into this characteristic until recently. [46] is the only other literature entry found in that time period. This paper examines the same characteristic and its effects on cross-modulation.

More recently, [21] presents an elegant review of distortion characteristics where the nulling effect is again unveiled from analytical mathematics of distortion in a bipolar device. Practical usage of the characteristic are presented in [47] and [19]. The first shows analytical and simulated data of intermodulation characteristics in bipolar common-emitter amplifiers. This is done at a frequency of 100 MHz and shows at higher frequencies, more error is introduced into the null position in terms of collector current. The second paper shows similar work done at a frequency of 50 MHz. The third-order intercept point of the amplifier was shown to increase by more than 10dB in theory, and 7dB in experiment.

Aside from using the null as a distortion reduction method, there has also been interest in using it as an accurate technique to measure the emitter resistance of a BJT. One of the common methods requires forcing base current into a single BJT, and measuring the collector voltage while holding the collector current at zero [48]. This is commonly called the DC flyback method. It is a simple and quick method of measuring emitter resistance, but can suffer from temperature related errors in some transistor devices due to the high currents required to make the measurement. The common alternative to the DC Flyback method is high-frequency measurements of the H-parameters of the device, which requires a more complex setup to make the measurements [49, 50, 51]. Estimating the series resistance using a bipolar device's third-order null has been shown to be accurate to one-tenth of an ohm [52], when compared with a more complex impedance measurement using VNA extraction technique [37].

Considering the drawback of a distortion null requiring a low DC bias current, a technique which increases the null to occur at higher bias currents would be interesting and potentially valuable in designing an amplifier with optimal linearity.

3.3 Theoretical Proof

The proof for a null in a single BJT amplifier's third-order distortion current can be obtained by simple algebraic manipulation, which is reflected many times in the literature [43]-[19]. From these works we find the condition for nulling can be stated as

$$I_C = \frac{V_T}{2R_{EE}} \tag{3.2}$$

where I_C is the DC collector current, V_T is the thermal voltage and R_{EE} is the equivalent series resistance of the transistor. This can be approximated to not include the source resistance R_B if the current gain β of the BJT is large, leading to the $\frac{R_B}{\beta}$ term being removed from the series resistance in Eq. 3.1. Using a transistor's bias position as a distortion reduction technique is rarely used practically in the literature, most probably because the null in a BJT occurs at a small collector current. Modern amplifiers focus on efficiency as well as linearity, leading to the DC bias current having a strictly defined value for maximum power transfer to the load, or for maximum conversion efficiency for the amplifying device. As an example, most commercial discrete BJTs have an emitter resistance around 1 ohm. Taking V_T as 0.0258 V we can calculate the IM3 null to occur at an approximate collector current of 13 mA. This is too low for many applications which will benefit from distortion reduction. Another obvious drawback is the null condition's dependence on temperature through the parameter, V_T.

The upcoming novel work is heavily based on the mathematics of the single BJT null. It seems appropriate to cover this proof in depth, such that it elegantly leads into the following work. To begin the derivation, we define the circuit in Fig. 3.2. The goal is to prove a local minima occurs in the third-order component of the transistor's transfer function. The general method is to use the transfer function of the transistor, apply a power series expansion, and view the harmonic coefficients which directly relate to the harmonic magnitudes in the output signal. Note that all resistors contain both the internal and external components of resistance for these derivations.

Firstly, a Kirchoff's voltage loop is performed around the base-emitter loop

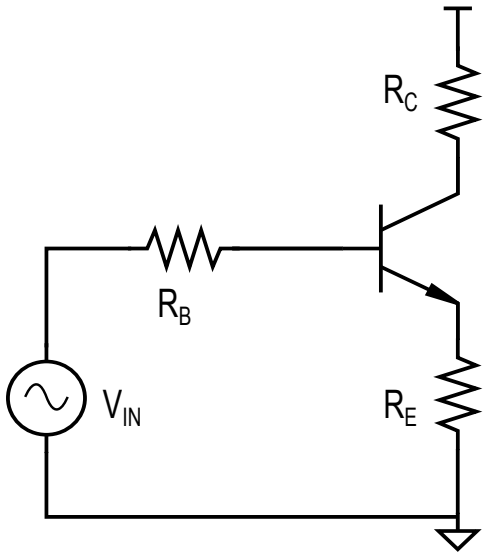


Figure 3.2: A typical single BJT transistor common-emitter amplifier used for transfer analysis. Each shown resistor is the total combination of internal and external resistances.

of the circuit in Figure 3.2 such that,

$$V_{IN} = \frac{I_C}{\beta}(R_B + R_E) + V_{BE} + I_C R_E, \tag{3.3}$$

$$V_{IN} = I_C(\frac{R_B + R_E}{\beta} + R_E) + V_{BE}. \tag{3.4}$$

It is known from the Ebers-Moll model that,

$$V_{BE} = V_T \, ln(\frac{I_C}{I_Q}) \tag{3.5}$$

From our previous definitions, the base-width modulation effect is considered to be contained inside I_C. Substituting Eq. 3.5 into Eq. 3.4 and rearranging gives

$$\frac{V_{IN}}{V_T} = \frac{I_C R_{EE}}{V_T} + \ln(\frac{I_C}{I_Q}) \tag{3.6}$$

where the series resistance term is defined as $R_{EE} = \frac{R_B + R_E}{\beta} + R_E$.

Using Eq. 3.6, one can rearrange to create a form suitable for deriving the series coefficients of the transfer function. Placing an $\frac{I_Q}{I_Q}$ term into the R_E term

allows us to define the equation W as a function of X,

$$W\{X\} = FX + \ln(X) \tag{3.7}$$

where W = $\frac{V_{IN}}{V_T}$, F = $\frac{I_Q R_{EE}}{V_T}$ and X = $\frac{I_C}{I_Q}$. This transfer function for the BJT amplifier is now in a form where we can compute the condition for first, second and third order distortion components. Differentiating Eq. 3.7 gives these distortion components as coefficients for a Maclaurin series. The series is of the form below, up to the third order only as we assume that fourth order and higher terms are negligible.

$$f\{X\} = A_1 X + A_2 X^2 + A_3 X^3. \tag{3.8}$$

A_1, A_2, and A_3 are the first, second and third order current gain coefficients respectively. By differentiating Eq. 3.7 and inverting to make V_{IN} (contained in X) the subject, the coefficients are found to be

$$\frac{dX}{dW} \rightarrow \frac{1}{\frac{1}{X} + F} \tag{3.9}$$

$$\frac{d^2X}{dW^2} \rightarrow \frac{X}{X^2(\frac{1}{X} + F)^3} \tag{3.10}$$

$$\frac{d^3X}{dW^3} \rightarrow \frac{X(1-2XF)}{(1+XF)^5}. \tag{3.11}$$

This inversion is required to make the derivatives of the form $\frac{I}{V}$, making them transconductance terms. By considering each transconductance term as the magnitude factor of each distortion component, one can evaluate any interesting features of the distortion. The third order term in Eq. 3.11 contains $(1-2XF)$, and clearly if $2XF = 1$, a theoretical condition is reached in which the third order distortion term equals zero. This is the cancellation condition that leads to the third-order null occurring in BJT devices. One can manipulate the term in Eq. 3.2 to arrive at the condition commonly stated in the literature. Substituting in the parameters for X and F results in Eq. 3.14, the nulling condition of interest.

$$2XF = 1, \tag{3.12}$$

$$2\frac{I_Q R_{EE}}{V_T}\frac{I_C}{I_Q} = 1, \tag{3.13}$$

$$I_C = \frac{V_T}{2R_{EE}}. \tag{3.14}$$

It is important to note that this condition is temperature dependent through V_T, and is process variation dependent through the parasitic resistances contained in R_{EE}. This is addressed in the next chapter. Other circuit effects that can change the null position are base-width modulation and the non-linear current gain at high or low operating currents. We have assumed these negligible in this derivation and are quantified later in the text. Including separating base-width modulation from I_C modifies the condition to be

$$I_C = \frac{V_T}{2R_{EE}}\left(1-\frac{V_{CE}}{V_A}\right). \tag{3.15}$$

Justification for the assumption that base-width modulation is negligible is based on the large value of Early voltage for general transistors. The bracketed term added in Eq. 3.15 shows the effect base-width modulation will have on the null position. For commercial general-purpose BJTs the value of V_A is in the range of 75-100 V. A good example is the CA3083 [53] which claims $V_{AF} = -100$ V. The value of collector-emitter voltage, V_{CE} varies with the supply voltage, amplifier topology and device type. For an amplifier operating with a 5V supply, a conservative estimate of V_{CE} is 2.5V. Using these two values one would obtain an error of 2.5% in the null position in terms of collector current compared with the ideal case. Furthermore, specialised devices tend to have better performance. A good example is the NXP BFU580G silicon RF transistor which claims $V_{AF} = -184$ V [54]. This would decrease the null position in terms of collector current to have an error of 1.3% compared with the ideal case.

3.4 Darlington BJT Null

One idea to increase the bias current at which this null occurs is to use a Darlington transistor. A Darlington is essentially two cascaded transistors in an emitter follower configuration. It can be proven mathematically that a Darlington operates effectively the same as a single transistor, but with increased current gain

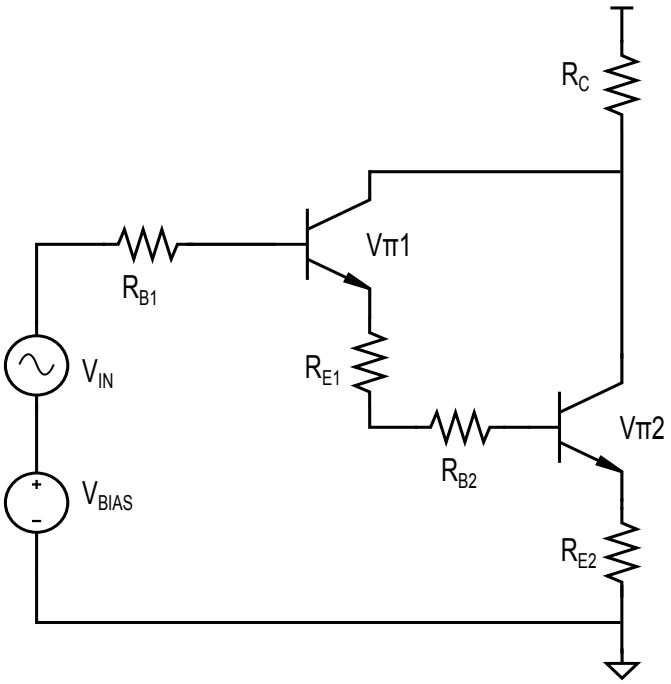


Figure 3.3: Typical single Darlington transistor amplifier circuit used for small signal analysis. Each shown resistor is the total combination of internal and external resistances.

traded for higher base-emitter voltage and lower switching speed [55].

Figure 3.3 shows a Darlington configuration which will, once again, be used as the definition for a derivation. The derivation of the Darlington nulling condition follows the same method. Firstly, the currents through the transistors are defined as

$$I_C = I_{C1} + I_{C2}, \tag{3.16}$$

$$I_{C2} = (I_{C1} + \frac{I_{C1}}{\beta_1})\beta_2 = I_{C1}(\beta_2 + \frac{\beta_2}{\beta_1}), \tag{3.17}$$

$$I_{B2} = I_{C1}(1 + \frac{1}{\beta_1}), \tag{3.18}$$

where β_n, I_{Bn} and I_{Cn} refer the the current gain, base current and collector current of the n^{th} transistor respectively. These equations describe and account for the base currents of each device. Due to this complexity, it makes the definition of series resistance more complex in a Darlington as the base and emitter currents differ greatly as they travel through each node and the associated circuit resistance.

Kirchoff's voltage law can be applied around the input loop to derive the following equation

$$V_{IN} = I_C R_{EE} + V_{\pi 1} + V_{\pi 2} \tag{3.19}$$

where

$$R_{EE} = R_{E2}(1 + \frac{1}{\beta_2}) + R_{E1}\frac{1 + \frac{1}{\beta_1}}{\beta_2 + \frac{\beta_2}{\beta_1}} + \frac{R_{B2}}{\beta_2} + \frac{R_{B1}}{\beta_1(\beta_2 + \frac{\beta_2}{\beta_1})}. \tag{3.20}$$

Note that the first term R_{E2} is the significant term and all other terms are suppressed by a factor related to $\frac{1}{\beta}$. Using the Ebers-Moll equation for transistors and the same steps presented for the single BJT case, we obtain the following transfer function for a Darlington amplifier.

$$W\{X\} = FX + \ln(X^2) \tag{3.21}$$

where W = $\frac{V_{IN}}{V_T}$, F = $\frac{I_Q R_{EE}}{V_T}$ and X = $\frac{I_{C2}}{I_Q}$. R_{EE} is defined above in Eq. 3.20.

Again, differentiation is used to find the current gain terms, for the first, second, and third order coefficients.

$$\frac{dX}{dW} \rightarrow \frac{1}{\frac{2}{X} + F}, \tag{3.22}$$

$$\frac{d^2X}{dW^2} \rightarrow \frac{2X}{(2 + XF)^3}, \tag{3.23}$$

$$\frac{d^3X}{dW^3} \rightarrow \frac{4X(1 - XF)}{(2 + XF)^5}. \tag{3.24}$$

Observing Eq. 3.24, one can see that the third order term will cancel completely if XF = 1, which can be written in the form below.

$$XF = 1 \tag{3.25}$$

$$\frac{I_Q R_{EE}}{V_T}\frac{I_{C2}}{I_Q} = 1 \tag{3.26}$$

$$I_{C2} = \frac{V_T}{R_{EE}} \tag{3.27}$$

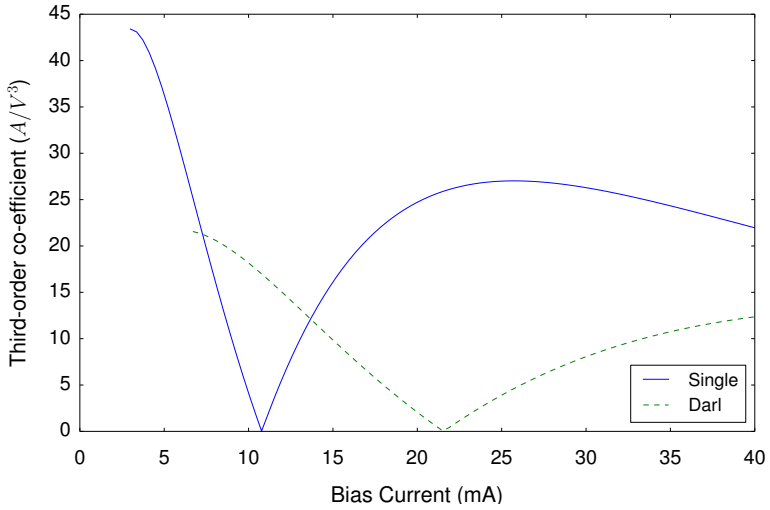


Figure 3.4: Theoretical plot of third-order magnitude vs. collector current for a single BJT/Darlington common-emitter amplifiers.

Eq. 3.27 gives a third-order nulling condition equation for a Darlington amplifier. This condition doubles the total collector current at the point of nulling for a given BJT, or equivalently permits twice the series resistance, R_{EE}, for a given operating current when in the third-order distortion null. To the best of the author's knowledge, this is a novel result which has yet to be published in the literature. The full derivation can been seen in Appendix B.

3.4.1 Theoretical Plotting

The single BJT and Darlington third-order coefficients can be plotted to indicate where the minima occur relative to each other. This is shown in Fig. 3.4. The data for this graph is obtained through python scripts incrementally plotting data points using Eq. 3.11 for the single BJT and Eq. 3.24 for the Darlington. This script can be seen in Appendix B. In this case the position is the only point of interest as the magnitude depends on many other factors such as input signal level, load conditions, etc. The magnitude data in these plots is abstract and scaled for graphical aesthetics only. The minima positions will be useful to compare with measurements in the next section. This theoretical data uses the assumptions that $V_T = 0.0258\,V$ (occurring at 300.15 Kelvin) and R_{EE}= 1.2Ω. R_{EE} is chosen as such because this value is used later on in measurements.

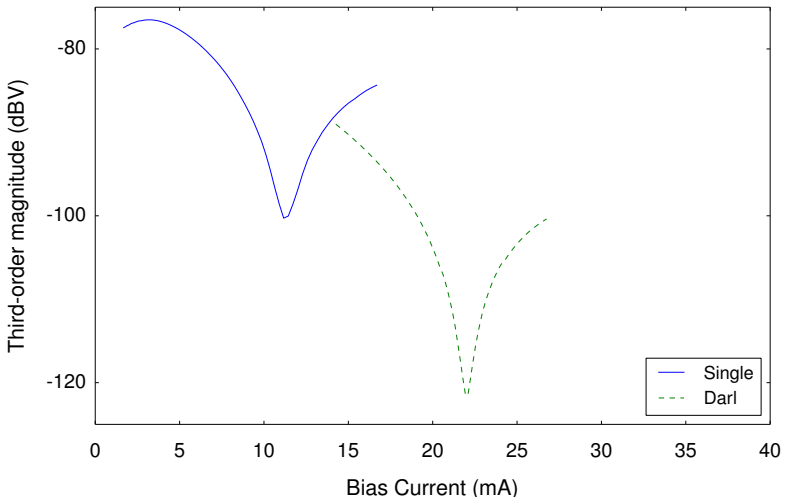


Figure 3.5: Simulated third-order magnitude vs. collector current for a single BJT/Darlington common-emitter amplifiers.

3.5 Simulation

The single BJT and Darlington common-emitter amplifiers are now simulated using LTSpice. These follow the same circuit specifications as measurements to keep the results consistent. SPICE models are used from the Intersil CA3083 datasheets [53]. The input tones are set to 15 kHz and 17 kHz, and 0.005 mV peak respectively.

Unfortunately, the CA3083 SPICE model does not state any value for emitter resistance [53], hence it was necessary to measure emitter resistance. This transistor's internal emitter resistance was measured as 1.2 Ω, using the Flyback method [51]. Error in this measurement is accounted for by considering the measurement instrumentation in the measurement setup. Error calculation suggests the worst case potential error of the emitter resistance is ±0.2 Ω. While this is rather large, the goal of this chapter is a proof that the nulling characteristic is positioned approximately where the new proof suggests it should be. We can tolerate this error given the measured null positions fall within these bounds. Further measurement methods exist which would also account for the base resistances, allowing the measurement of series resistance [56]. However, it requires further unavailable transistor parameters, such as the intrinsic base resistance, R_{BI}, to obtain the measurement values.

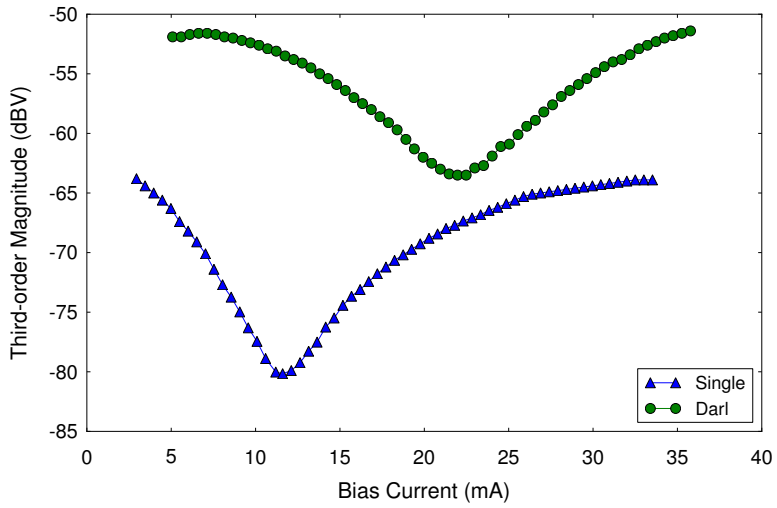


Figure 3.6: Measured third-order magnitude vs. collector current for a single BJT/Darlington common-emitter amplifiers.

Figure 3.5 shows the simulated null positions in terms of IM3 for a given collector current range. The exact current values for the null position are 11.2mA and 22.1mA for the single and Darlington configurations respectively. These two null position have a worst case error of ±0.2mA.

3.6 Measurement

In order to confirm theory and simulation, measurements are made using a common CA3083 transistor array. The integrated array allows the devices to be matched when a Darlington configuration is tested, meaning current gain, saturation current and internal resistances should all be well-matched. An Agilent E5270 is used to supply and measure the circuit currents and voltages for the circuit. A two-tone input signal is produced by a function generator and an Agilent 3561A Signal Analyzer is used to measure the harmonic components of the output signal for each amplifier. These are set to 15 kHz and 17 kHz, and 0.005 mV peak respectively..

This setup allows the measurement of IM3 components created by both a single BJT and Darlington amplifiers. Figure 3.6 shows the measured null positions in terms of IM3 for a given collector current range.

3.7 Discussion

The errors of the theoretical, simulated and measured stages are summarised in Tables 3.1 and 3.2. 'Theoretical Ideal' is the null position calculated using the idealised null condition in Eq. 3.14 and 3.27 for the single BJT and the Darlington respectively. 'Theoretical Corrected' is found from the same equations, adjusted for second-order effects. The single BJT is adjusted for base-width modulation and in the Darlington case, base-width modulation and base current loss due to Eq. 3.28. 'Simulated CA3083 Model' is the simulated null position and 'Measured' is the found from the measured data.

We observe in the measured data that the Darlington null indeed occurs at close to double the measured single BJT null position (22.3 mA and 11.6 mA respectively). There is some error in these values due to the dynamic range being limited in the test setup and hence the resolution of a more exact null position is masked by the noise floor in the IM3 measurements. However, the measured null position is accurate enough to conclude that the presented theory accurately matches measured results.

We also observe an absolute offset in null position from that predicted by theory. Theory predicts the nulls should occur at approximately 21.5 mA and 10.8 mA for the Darlington/single BJT respectively for an emitter resistance of 1.2 Ω. In the measured cases these are shifted positively. This is not a surprising result as the theory still does not account for base resistance effects. The measurement of the 1.2 Ω emitter resistance also introduces inaccuracy into the comparison. Considering the previously stated emitter resistance error of ±0.2 Ω, we find the measurements fall well within these limits. The measured collector currents 22.3 mA and 11.6 mA suggest a series resistance of 1.16 Ω and 1.11 Ω respectively. This suggests a 3.7% and 7.4% error respectively in the measured values compared with the theoretical ideal values.

While this technique with a Darlington transistor makes third-order distortion nulling look more appealing, other factors should be considered such as the drawbacks of second-order effects. The transistor datasheets state this parameter, V_{AF} = -100 V, which can have a minor impact on the measurements. If we assume the V_{CE} in the amplifier is 2.5 V, the Early effect will have an impact of +2.5% on the null positions in terms of collector current. A small current gain

	Single BJT	Uncertainty	Comparative Error
Theoretical Ideal	10.8 mA	-	0%
Theoretical Corrected	11.1 mA	-	2.5%
Simulated CA3083 Model	11.2 mA	±0.2mA	3.7%
Measured	11.6 mA	±0.5mA	7.4%

Table 3.1: Summary of error calculations and measurements for the single BJT configuration. Comparative error percentage is relative to 'Theoretical Ideal'.

	Darlington	Uncertainty	Comparative Error
Theoretical Ideal	21.5 mA	-	0%
Theoretical Corrected	22.2 mA	-	3.3%
Simulated CA3083 Model	22.1 mA	±0.2mA	2.8%
Measured	22.3 mA	±0.5mA	3.7%

Table 3.2: Summary of error calculations and measurements for the Darlington configuration. Comparative error percentage is relative to 'Theoretical Ideal'.

value will also effect the null positions through the base currents of the BJTs. This is stated to be reasonably high in the device SPICE model, approximately 112.8, but it is still worthwhile to consider because on the non-linearity of the beta at higher currents. Using Eqs. 3.16-3.18 a correction factor can be applied to the null condition. Including this factor and the Early effect modifies the null condition to be

$$I_C = \frac{V_T}{2R_{EE}}\left(1-\frac{V_{CE}}{V_A}\right)\left(1+\frac{1}{\beta+1}\right). \tag{3.28}$$

Beta effects introduce error in Eq. 3.15 through R_{EE}, where R_{EE} was defined in Eq. 3.1. Normally a transistor will have a large beta, for example the CA3096 SPICE model claims that $\beta = 467$ [53]. Like these general transistors, specialised RF transistors will vary depending on many factors. The NXP BFU580G silicon RF transistor states $\beta = 134$ [54]. Conservatively, one could take a beta value of 100 as a nominal value for a transistor. One can take this value and quantify its impact on series resistance R_{EE}. In a BFU580G device, this beta value would account for $0.0088\,\Omega$ of a total of $0.304\,\Omega$ (2.8%) of the total series resistance (where the BFU590G SPICE model states $R_E = 0.295\,\Omega$ and $R_B = 0.585\,\Omega$).

Absolute variation of the beta is due to process variation in differing fabrica-

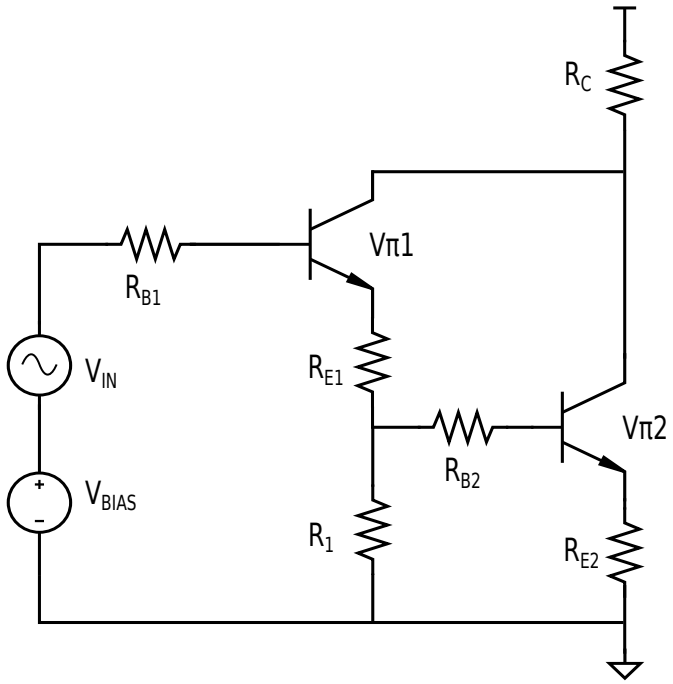


Figure 3.7: Typical single Darlington transistor amplifier circuit used for small signal analysis. Each shown resistor is the total combination of internal and external resistances.

tion runs. For a conservative absolute beta variation of ±50% (hence the worst case is $\beta = 67$ in the BFU580G), these numbers would shift to 0.0176 Ω of a total of 0.3126 Ω or 5.6% of the total series resistance. With this vastly overestimated beta mismatch variation the null position will still only experience a 5.6% shift in collector current. Considering process variation of the beta is more important when a practical circuit is being prepared for a commercial product. Firstly, one can make an assumption that the transistor devices are well matched, such that current gain and thermal voltage coefficients are equal in each semiconductor device. This is justified by assuming the amplifier is built using on an integrated circuit, in which the mismatch variation between devices is minimised. In this work, we are focused on proving the condition for the particular null holds, given reasonable circuit conditions such as accurately knowing the current gain. Hence, we have not included further analysis of the process variation of beta.

3.7.1 Practical implementation

It is well known that a Darlington cell has a slow switching speed due to the second transistor's collector-base capacitance having no direct discharge path to ground. Hence, a Darlington is almost always used with a 'flushout' resistor from the first emitter connection to ground. Usage of this resistor turns the configuration into a common-collector–common-emitter cascade amplifier and hence it can be analysed as such [55]. This can been seen in Fig. 3.7 where R_1 is the flushout resistor. The value of this resistor is a direct trade-off in overall current gain for increased switching speed.

In-depth theoretical analysis of the impact that this resistor will have on the Darlington configuration is beyond the scope of this chapter, however one can make qualitative observations as to its effect on the position of the null. The resistor, R_1, is in parallel with the second transistor in the Darlington and its associated resistances. If $R_1$is infinitely high, it has no impact. As R_1 decreases, it reduces the base-emitter junction voltage of the second transistor. In turn, this reduces the collector current, I_{C2}, while increasing the collector current I_{C1}. Hence, the series resistance would become more reliant on the first stage resistances, R_{E1} and R_{B1}. R_1 also begins to act as a partial series resistor for the first stage through the base current, I_{B1}. As R_1 approaches zero, the amplifier turns into a single BJT common-emitter amplifier, as the base junction of the second transistor is now grounded.

From these observations, it appears as the null condition for a Darlington will approach the single BJT null condition as the value of R_1 is reduced from a high impedance.

3.8 Conclusions

The chapter outlines a case study into a single BJT third-order distortion null, presenting the general proof already established in the literature. This proof is expanded upon to predict that the distortion null will occur at double the bias current in an Darlington amplifier. This is assuming the transistors used are matched. The prediction is proven mathematically and then confirmed with simulation and measurements made on a CA3083 transistor.

By comparing the simulated null positions with theoretical null positions corrected for second-order effects, we obtain an error of 1.2% and <1% error in the single BJT and Darlington cases respectively. By comparing measurements with the corrected theoretical null positions the error obtained is 6.9% and <1% in the single BJT and Darlington cases respectively. These errors are small enough to conclude second-order effects do not have a significant impact, and confirm the new null position model is accurate.

While the extended model of distortion nulling for a Darlington does double the null position in terms of bias current, this still occurs at a low current compared to the complete range of DC bias points available in a bipolar device. As mentioned previously, an amplifier designer will often be required to push the DC current as high as possible in order to maximise parameters like cutoff frequency. Therefore, the characteristic will still find little application in most amplifiers. However, the work is interesting as it could form a basis for analysis of the characteristic in more complex topologies. The nulling effect could also prove useful for low-frequency applications which do not require high bias currents. For example, distortion reduction in audio amplifiers, low-noise amplifiers, or mixers.

Two limitations that are not addressed in this work are the temperature and series resistance variation of the bias current, which will shift the true null position away from the predicted null position. These variations provide motivation for the following chapter, leading to investigation into maintaining a constant bias current in a transistor over temperature and series resistance circuit variations which can shift the bias current.

4

Translinear Extraction

As shown in the previous chapter, distortion cancellation using a transistor's series resistance (defined in the previous chapter) is limited by temperature and series resistance variation. If a large variation occurs, a transistor's inherent third-order null is shifted to a different position in bias current. This means the technique does not provide rigorous distortion cancellation. A method of suppressing the temperature and series resistances effects is required.

In this chapter, a method for extracting the series resistance of a BJT is presented. This method is based on invoking the translinear principle in a structure of bipolar transistors and extracting currents which are directly related to the series resistance. This method leads to the description and design of a bias circuit which can theoretically be used to bias a single BJT amplifier independent of temperature and parasitic emitter resistance. We develop a standalone circuit to achieve this goal, describing its operation through theory and simulations. Measurements are presented to support the theoretical and simulated data.

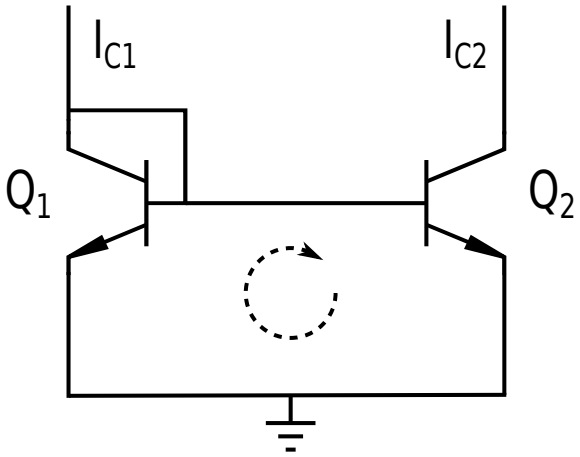


Figure 4.1: Simple current mirror circuit, showing the transistor's base-emitter junctions in closed loop.

4.1 Translinear Principle

The translinear principle is a fundamental law that addresses a simplified relationship between multiple semiconductor junctions in a closed loop. This was first introduced by Gilbert in 1975 [57]. A very simple example of a common translinear circuit is the current mirror where a closed loop is formed through the two base connections of the transistors. Consider Fig. 4.1 which is a simple current mirror. If Kirchoff's voltage law (KVL) is applied around the base-emitter loop created by Q_1 and Q_2 we find that

$$V_{BE1} - V_{BE2} = 0. \tag{4.1}$$

By considering these base-emitter voltages and their fundamental relationship to collector current through the Ebers-Moll model, and assuming the semiconductor devices are identical, their junction currents must be equal as well. This leads to the conclusion that the collector currents of each transistor must be equal in this circuit (assuming non-idealities of the transistors are negligible) due to the base-emitter voltages being forced equal. A current mirror circuit has the well-known idealistic property that $I_{C1} = I_{C2}$, which agrees with the translinear principle. Of course there are other circuits in which the translinear principle describes useful relationships between base-emitter junctions such as current multipliers, current dividers, and current conveyors.

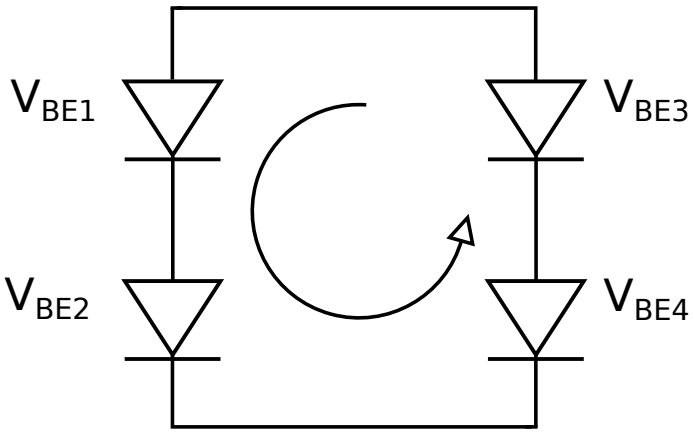


Figure 4.2: Fundamental circuit used to describe the translinear principle.

To describe the principle more comprehensively, the translinear principle is a specific application of Kirchoff's voltage law (KVL) for multiple transistor elements in a closed loop. It states that in a closed loop containing an even number of transistor elements, the product of the currents calculated clockwise through the closed loop is equal to the product of the currents calculated anti-clockwise through the closed loop. This can be described more practically as the sum of the base-emitter junction voltages anti-clockwise (ACW) around a closed loop is equal to the sum of the base-emitter junction voltages clockwise (CW) around the closed loop, assuming the relative transistor sizes are accounted for and that the transistors are otherwise identical.

This law is represented by Eq. 4.2 below,

$$\sum V_{BEj-acw} = \sum V_{BEk-cw}. \tag{4.2}$$

If a simple translinear loop with two NPN base-emitter junctions is considered, as seen in Fig. 4.2, the translinear principle can be stated as

$$\prod_{h}^{top} \frac{I_{j-cw}}{A_{j-cw}} = \prod \frac{I_{k-acw}}{A_{k-acw}} \tag{4.3}$$

where I is the current through the junction and A is the unit area of the junction. This principle can be used to implement multiplication, division and power-law circuits using the exponential current-voltage relationship in a BJT.

4.1.1 Nonideal Translinear Principle

The definition of the translinear principle can be modified to include the major sources of nonideality that affect the operation of a translinear circuit. Firstly, area mismatch will directly add error into the translinear circuit. This is caused by the process error of the technology when creating the emitters of the transistors. Integrated circuit layout techniques can minimise this process error. Symmetrical and common centroid layouts are good examples of this [18].

Beta effects will also introduce error to a translinear circuit. This is caused by the base current in the bipolar transistor junction being taken out of the main junction current resulting in an error through the translinear loop. This error can be avoided by certain circuit designs which either replace or cancel the lost base current from the main junction current. Because of the finite beta value, the error then manifests itself in the exponential current-voltage relationship as an extra voltage at the base junction of the transistor. This is stated as

$$V_{BE} = V_T \ln(\frac{I_c}{I_s}) + r_{bb}(\frac{I_c}{\beta}) \tag{4.4}$$

where V_T is the thermal voltage, I_c is the junction current, I_s is the transistor saturation current, r_{bb} is the intrinsic base resistance and β is the current gain.

One last error consideration is base-width modulation. Using the standard exponential current-voltage equation coupled with the Early voltage component, the effect can be modeled as a second area mismatch, γ. Using Eq. 54 above this can be stated as

$$V_{BE} = V_T \ln(\frac{I_c}{\gamma I_s}) + r_{bb}(\frac{I_c}{\beta}) \tag{4.5}$$

where $\gamma = 1 + \frac{V_{ce}}{V_A}$, V_A is the Early voltage and V_{ce} is the collector-emitter voltage.

So far the presented non-idealities can generally be neglected if they are present. Modern process errors and logical circuit design techniques can push these error limits to be negligible. However, resistances in the translinear loop can have a large impact. Resistive components added externally into the circuit can be used to control and measure voltages in the translinear loop. Since the value of an external resistor is known it can be theoretically accounted for. Parasitic resistance in the transistor is usually not known, as it varies moderately between fabrication runs. It presents the largest challenge in producing accurate

currents from translinear circuits. This is generally known as log-conformance error [58, 22].

4.2 Literature Review

The third-order null at a particular bias condition is a fundamental property of a degenerated BJT amplifier structure as discussed in the previous chapter. Recall that a third-order null requires a constant collector current to be applied with minimum variation over temperature and or circuit variations. The condition governing this is given by Eq. 3.15. Maintaining a bias current for an amplifier independent of series resistance variations has been established in the literature, albeit only sparingly.

In an integrated circuit process, modern process variation limits for series resistances can be cited as 20% for absolute process variation, and 2% for mismatch process variation [27, 28]. These are the variations one would expect to occur in the null position parameters and the bias circuitry.

Klimovitch briefly describes a bias circuit which maintains a constant bias current for a single BJT amplifier [19]. This is done using a current mirror with base current compensation. It is stated the bias current is independent of temperature and component variations. However it does not account for parasitic resistance variation, which will shift the actual null position in the amplifying transistor.

Huang utilises the translinear principle in CMOS devices to develop a logarithmic amplifier [59]. The translinear principle is invoked using an embedded resistive element, allowing the cancellation of temperature effects and resistive nonlinearities. One drawback is the complexity required to implement this cancellation.

The sensitivity of a BJT's third-order null to the parasitic resistances is large enough that it can be used as a sensitive method for extracting the resistance value for a particular device layout [52]. This work shows the sensitivity, and implies that tracking is required to utilise this IM3 characteristic.

Series resistance compensation in BJT circuits is more common in the literature as it finds use in other applications. The paper by Opris [22] forms a basis for this chapter's research. It shows that series resistance effect is proportional

to absolute temperature (PTAT) and bandgap translinear circuits can be compensated for by manipulating the transistor ratios in a translinear loop. This is based in the general field of log-conformance error and has been understood in the literature for some time [58].

Considering these literature entries, it appears one can manipulate the inherent relationship between resistive elements and the semiconductor junctions in a translinear loop. The following work builds on this idea, attempting to resolve a model which identifies an unknown resistive element in a translinear loop. If an unknown resistive element can be found, it becomes possible to account for and compensate unwanted effects from said unknown resistive elements.

4.3 Series Resistance Compensation

A useful property of translinear circuits is their suppression of temperature variation effects which otherwise contribute error into a measurement system. This suppression comes from the cancellation of the thermal voltage, V_T, due to its equal and opposite effect in the translinear loop of a circuit. This makes use of the assumption that the BJTs are monolithic and co-located so their temperature is identical. This leads to many useful circuits such as temperature sensors and band-gap references.

Certain translinear circuit configurations also allow compensation of the effect of base and emitter resistances intrinsic to the BJT structure. This combined with the inherent translinear circuit property of non-dependence on temperature variations can lead to more useful circuits and new applications. One example is the translinear circuit presented by [22], which produces an output temperature-independent current, along with any series resistance effects removed from the output.

To understand this technique, a unique version of a translinear circuit is presented. Consider the circuit in Fig. 4.3. In this circuit we impose a translinear condition by forcing equal voltages across the top of each branch of diode-connected transistors. This is done using current sources driven by a high-gain op amp, which forces the equal currents in each branch. This allows the translinear principle to be invoked around the loop containing the four BJT base-emitter junctions. Therefore, a series of equations describing the current

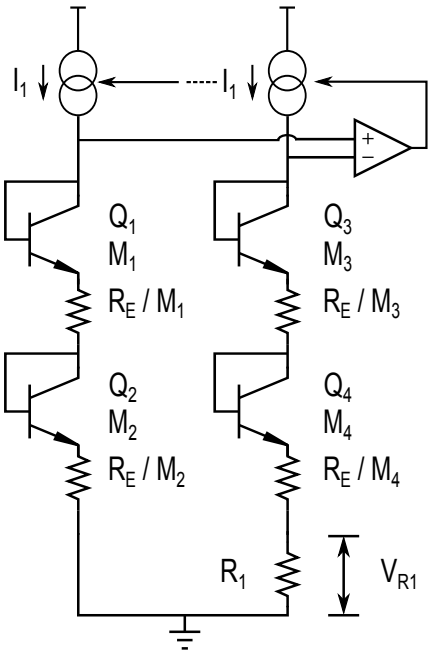


Figure 4.3: A two-transistor translinear stack circuit with the translinear condition forced around the two branches.

through the loop can be stated based on this principle.

Since we are interested in removing the effects of series resistance and temperature, the following maths aims to describe the voltages in the circuit with these variables in mind. Firstly, the voltages around the loop are summed as

$$V_{BE1} + V_{BE2} + I\left(\frac{R_E}{M_1} + \frac{R_E}{M_2}\right) = V_{BE3} + V_{BE4} + I\left(\frac{R_E}{M_3} + \frac{R_E}{M_4}\right) + IR_1 \tag{4.6}$$

where R_E is the intrinsic emitter resistance, M_n is the unit area size for transistor n, and I is the current through the stack (equal in each branch). Note that practically, this translinear condition can be forced by using other configurations at the top of the branches. For example, by sweeping the current sources and measuring the voltage until they converge on a single value. By substituting the Ebers-Moll model for the base-emitter voltages, one can expand and collect terms to give

$$\begin{aligned} &\tfrac{nkT}{q}\ln\left(\tfrac{I}{I_s M_1}\right) + \tfrac{nkT}{q}\ln\left(\tfrac{I}{I_s M_2}\right) - \tfrac{nkT}{q}\ln\left(\tfrac{I}{I_s M_3}\right) - \tfrac{nkT}{q}\ln\left(\tfrac{I}{I_s M_4}\right) \\ &\qquad = IR_1 + IR_E\left(\tfrac{1}{M_3} + \tfrac{1}{M_4} - \tfrac{1}{M_1} - \tfrac{1}{M_2}\right), \end{aligned} \tag{4.7}$$

$$\frac{nkT}{q}\ln\left(\frac{M_3M_4}{M_1M_2}\right) = IR_1 + IR_E\left(\frac{1}{M_3}+\frac{1}{M_4}-\frac{1}{M_1}-\frac{1}{M_2}\right). \tag{4.8}$$

For simplicity the substitutions below can be made.

$$A = \frac{M_3M_4}{M_1M_2}. \tag{4.9}$$

$$x = \frac{1}{M_3}+\frac{1}{M_4}-\frac{1}{M_1}-\frac{1}{M_2}. \tag{4.10}$$

These substitutions lead to a final descriptive equation for the presented translinear stack circuit. This is stated as

$$V_{R1} = IR_1 = \frac{nkT}{q}\ln A + IR_E x. \tag{4.11}$$

The terms A and x allow for some interesting observations regarding Eq. 4.11. The IR_E term can be canceled by setting x to zero while ln A is non-zero. This particular condition means all series resistance effects associated with the transistors are canceled from the voltage measurements across R_1, assuming theoretically ideal circuit conditions. Example values for this condition are $M_1 = 4$, $M_2 = 6$, $M_3 = 3$, $M_4 = 12$. This gives $A = 1.5$ and $x = 0$, and simplifies the describing equation to be

$$V_{R1} = IR_1 = \frac{nkT}{q}\ln A. \tag{4.12}$$

This derivation shows that it is possible to cancel the effects of series resistance from the translinear stack itself. However temperature effects still remain and more importantly the magnitude of series resistance still remains unknown.

4.3.1 Expansion of the Translinear Loop

By studying the practicality of Eq. 4.11 one can see that certain A and x combinations will give very small current and voltage values. This could lead to limitations in measuring the circuit or using it for another purpose. More flexibility in the transistor ratios can be obtained by increasing the number of transistors used in the stack. Fig. 4.4 shows three transistors used in the each branch of the stack.

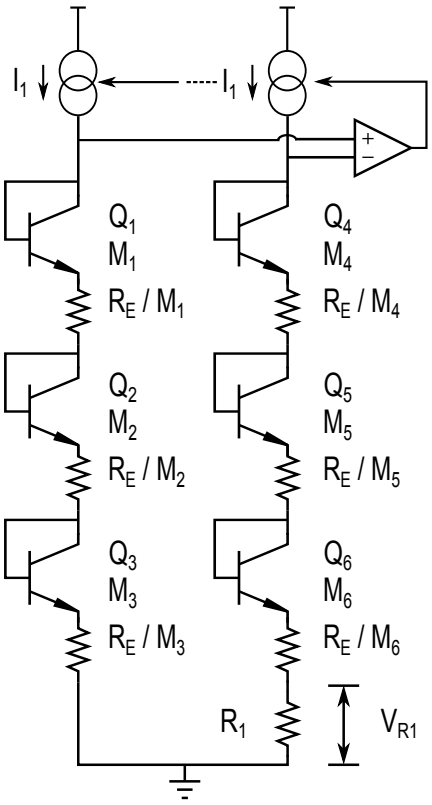


Figure 4.4: A three-transistor translinear stack circuit with the translinear condition forced around the two branches.

Hence the equation for the voltage across R_1 becomes

$$\begin{aligned} V_{R1} &= IR_1 \\ &= \frac{nkT}{q}\ln\left(\frac{M_4M_5M_6}{M_1M_2M_3}\right) \\ &\quad -IR_E\left(\frac{1}{M_4}+\frac{1}{M_5}+\frac{1}{M_6}-\frac{1}{M_1}-\frac{1}{M_2}-\frac{1}{M_3}\right), \end{aligned} \tag{4.13}$$

with the A and x terms becoming

$$A = \frac{M_4M_5M_6}{M_1M_2M_3}, \tag{4.14}$$

$$x = \frac{1}{M_4}+\frac{1}{M_5}+\frac{1}{M_6}-\frac{1}{M_1}-\frac{1}{M_2}-\frac{1}{M_3}. \tag{4.15}$$

This results in Eq. 4.11 holding true for the expanded translinear loop, but with A and x modified to be Eq. 4.14 and 4.15 respectively.

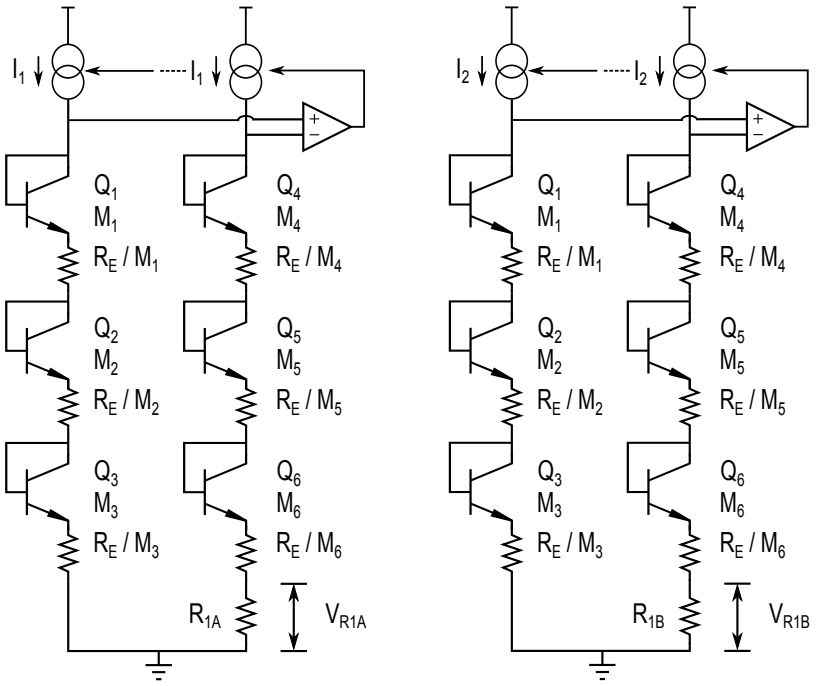


Figure 4.5: Two three-stack translinear circuits which allow series resistance to be resolved, due to the known difference in emitter area ratios.

4.3.2 Series Resistance Extraction

When using only one stack we can compensate series resistance, but not quantify it. Temperature effects also still remain in the describing equations. This section shows that manipulating two translinear stacks allows the series resistance to be measured and temperature effects to be suppressed, by using one stack as a reference. This original result forms the basis for a bias circuit which will solve series resistance and temperature variation issues as previously described.

This is achieved by using two translinear stacks which are identical, expect for different x values. Choosing one to have a non-zero x value and the other to have x equal to zero while both stacks have the same A value, allows the derivation of the following equations describing the transistor's series resistance.

Now, an equation which describes the difference in the current through each circuit is required. Firstly, two stacks in Fig. 4.5 are presented showing the proposed dual stacks arrangement. A voltage difference between the two external resistors is defined as V_3, seen below in Eq. 4.18. These resistors are set

as $R_1 = R_{1A} = R_{1B}$ such that

$$V_{R1A} = I_1 R_{1A} = \frac{kT}{q} \ln A, \tag{4.16}$$

$$V_{R1B} = I_2 R_{1B} = \frac{kT}{q} \ln A - x I_2 R_E. \tag{4.17}$$

$$V_3 = V_{R1A} - V_{R1B} = x I_2 R_E. \tag{4.18}$$

Further manipulation shows the series resistance R_E is calculated using

$$R_E = \frac{R_1(I_1 - I_2)}{x I_2} = \frac{R_1(V_1 - V_2)}{x V_2} \tag{4.19}$$

Eq. 4.19 presents an equation which provides the magnitude of the series resistance. This requires measurements of the current or voltage from both stacks operating at their respective equilibrium points (equal voltages at the top of each pair of transistor branch).

4.3.3 Application to Amplifier Biasing

As mentioned beforehand, the biasing in the natural IM3 null of a single BJT amplifier is set by the series resistance through the transistor's base-emitter junction, and is susceptible to process variation of the internal resistances. Extracting the emitter resistance using the translinear technique described in Eq. 4.19 offers a solution to process variations in the apparent emitter resistance. By extracting the value from accurately matched transistors, a bias current can be created and maintained to accurately bias in the amplifier's IM3 null independent of temperature and process variations. To implement this technique, the equations which describe the required amplifier bias current must be derived.

Firstly, a reference current is defined which can later be scaled to the appropriate value. In the interest of simplicity, an already existing current I_1 is used, defined below as

$$I_1 = \frac{1}{R_1} \frac{kT}{q} \ln A. \tag{4.20}$$

The condition for the IM3 null is defined back in Eq. 3.14 which requires $V_T/2$ dropped across the total series resistance. Hence, the following mathematics aims to develop a set of equations which will apply exactly $V_T/2$ across

the amplifying transistor's series resistance. Using this we define the required reference current as

$$I_{Bias} = \frac{V_T}{2R_1} = \frac{I_1}{2\ln A}, \tag{4.21}$$

where the total emitter resistance only consists of R_1. This needs to be scaled by the magnitude of the effect R_E has on the voltage dropped across the emitter resistance. This is achieved by looking at the ratio of R_1 to R_E. This is represented mathematically below in Eq. 4.23, with I_{Bias} now scaled by Eq. 4.22 which applies the correction for series resistance.

$$\frac{R_1}{R_e + R_1} = \frac{x I_2}{x I_2 + I_1 - I_2}. \tag{4.22}$$

$$I_{Bias} = \frac{I_1}{2\ln A} \frac{x I_2}{x I_2 + I_1 - I_2}. \tag{4.23}$$

For simplicity, the bias current is defined below using I_{OUT} to represent the scale for the current as

$$I_{Bias} = \frac{I_{OUT}}{2\ln A}, \tag{4.24}$$

$$I_{OUT} = I_1 \frac{x I_2}{x I_2 + I_1 - I_2}. \tag{4.25}$$

I_{OUT} now describes the theoretical bias current that will position a transistor in its IM3 null, assuming it also has R_1 as an emitter resistor. It does this while canceling series resistance effects and being independent of any temperature variables in the describing equation.

4.4 Extraction Circuit Design

To utilize this technique, a three-stage design is developed in order to extract the series resistance value and then bias a common-emitter amplifier in its IM3 null. The circuit blocks can be seen in Fig. 4.6. The first stage contains the two translinear stack circuits used for compensation and extraction. The two equilibrium currents from stack A and B are fed into the second stage where algebraic operations occur to create a scaled bias current. The third stage combines the scale current and reference current and uses it to bias the single transistor amplifier.

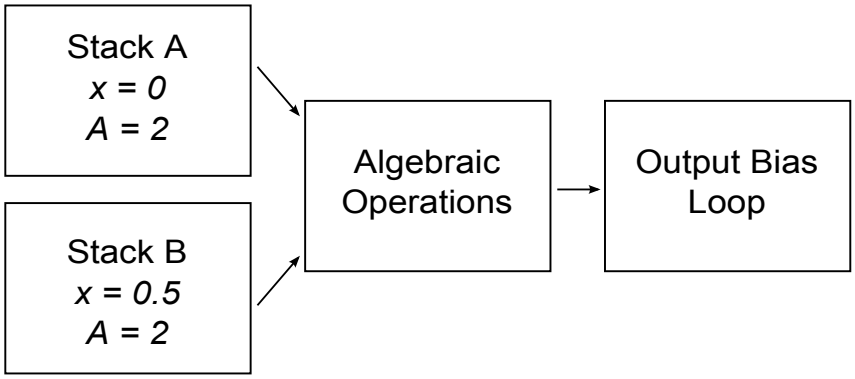


Figure 4.6: Bias circuit blocks showing the three main stages of the circuit.

4.4.1 Translinear Stack Ratios

Under further investigation, the selection of parameters A and x become rather complex. The two fundamental conditions for this Eq. 4.23 to hold are:

1. $\ln A$ must be equal in both stacks and be non-zero.
2. x must be zero in one stack and non-zero in the other stack.

The stacks can break condition two and have two different non-zero x values at the cost of more complex algebra to describe the bias currents, but in the interest of simplicity this is not utilised.

Python scripts were used to calculate all possible combinations of transistor area ratios, along with the associated A and x values. The code can be seen in Appendix C. This approach shows area ratios that give x = 0 values are quite rare with approximately 1002 combinations for a 3 stack translinear circuit with unit transistors sizes ranging between 1 and 16 (with a total of 2.9 million possible combinations). Again, in the interest of simplicity we choose $A = 2$ and with $x = 0$, $x = 0.5$ in the first and second stack respectively. This is formed by the combinations below.

$$Stack1 \rightarrow M_{1-6} = 2,2,2,1,4,4 \tag{4.26}$$

$$Stack2 \rightarrow M_{1-6} = 4,4,8,1,16,16 \tag{4.27}$$

The numerical computations done in Python show that this combination is the smallest collective transistor array size which allows a $x = 0.5$ scale factor in

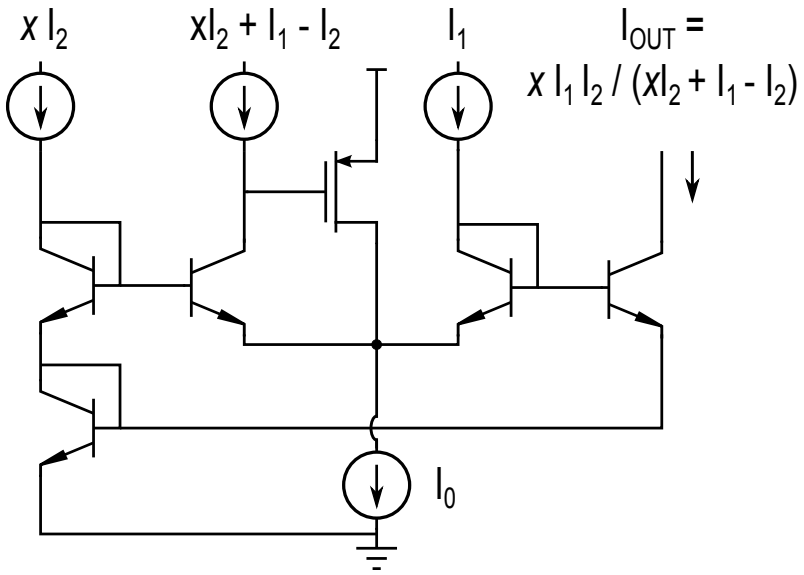


Figure 4.7: Translinear multiplier used to perform algebraic operations required by the second circuit block.

Stack B. This factor is appealing as it allows the design of scaled current mirrors with the simple task of dividing a current by half.

4.4.2 Multiplier Divider design

In order to create the scale current I_{OUT}, a translinear multiplier configuration is used, as presented by [60]. The circuit can be seen in Fig. 4.7 showing how its operation fits in well with the required operations of Eq. 4.25. It is a conventional multiplier/divider circuit modified to produce smaller error between the output and input currents, due to the base current compensation by the PMOS device.

4.4.3 Bias Driver Circuit

The bias driver scheme can be seen in Fig. 4.8. The main amplifying transistor Q_1 has R_1 added to its emitter resistance. Both sides of the current mirror are balanced with the same resistances. R_{2A} and R_{2B} isolate the signal from the input side of the current mirror. The input current to the mirror is driven through R_1 giving a voltage of

$$V_{R1} = \frac{V_T}{2} - V_{RE}, \tag{4.28}$$

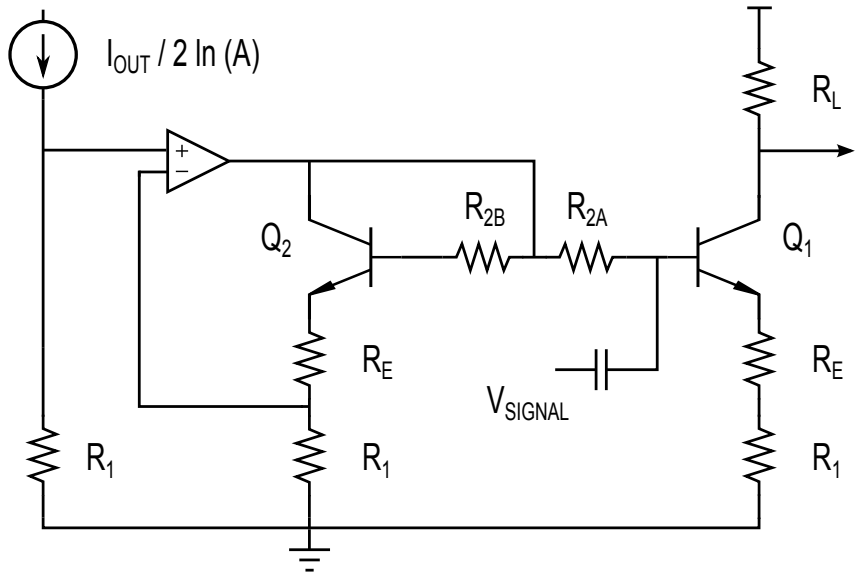


Figure 4.8: Output bias loop used to set the bias current in the output transistor such that it operates at the third order null.

and consequently the current mirror forces $V_T/2$ across the total emitter resistance of the single BJT amplifier.

The input to the driver circuit comes from a scaled current mirror attached between the multiplier circuit's output and the driver circuit's input. This current mirror applies the scale of $1/2\,ln(A)$ to the current I_{OUT}.

4.5 Simulation

The complete system has been simulated using parameters from a commercial 0.5 μm 27GHz BiCMOS process [61], typical for such applications, with a nominal 3.3V supply. Note that the system implementation is not specific to this technology, but the availability of NMOS and PMOS transistors is useful in the construction of the amplifiers and mirroring functions needed. Hence, the target application is this BiCMOS process. Simulations are done in SPICE with nominal circuit values chosen as $R_1 = 60.000\,\Omega$, ambient temperature = 27 °C, and supply voltage = 3.3 V. The theoretical target bias current required in the amplifier is 134 μA. This is calculated using Eq. 3.14 where $R_E = 32.376\,\Omega + 60.000\,\Omega + 3.7200\,\Omega$, contains both the external and internal emitter resistances. The full circuit can be seen in Appendix C.

	Stack A	Stack B	Series Resistance	% Error
Calculated	298.63 μA	229.20 μA	36.1 Ω	0%
Ideal Model	298.30 μA	229.30 μA	36.1 Ω	<1%
BiCMOS Model	298.15 μA	226.02 μA	38.3 Ω	5.36%

Table 4.1: Initial simulations of the translinear stack output currents versus the calculated values. This shows the simulated current values and the resulting series resistances when using these values. The percentage error is the error when compared with theoretical series resistance values.

Error sensitivity is a major consideration in this design for two reasons. Firstly, the IM3 null is sharply defined so a small change in the target emitter voltage can lead to a large change in the IIP3 magnitude and secondly it is a moderately large circuit in which there is the potential for errors to accumulate.

SPICE simulation data is shown in Table 4.1 which defines the nominal values of equilibrium current expected in the translinear stacks. The translinear stack ratios are kept the same as stated in Eqs. 4.26–4.27 from the previous section. 'Calculated' shows the currents expected using Eq. 4.19, and the expected series resistance. 'Ideal Model' shows the error in simulation when using an idealised transistor model. This shows negligible error compared with the expected theoretical result in 'Calculated'. 'BiCMOS Model' outlines the error in simulation using practical BiCMOS transistor models, and the data shows this impact. This larger error stems from beta mismatches between the different transistor sizes in each branch, something which can potentially be minimized with the optimization of the parameters A and x. The base-width modulation effect also contributes to this error through the limited V_{AF} of the practical transistor model used.

4.5.1 Multiplier Output Error

Analysis of the error at the multiplier output is done to quantify the total error from the first two circuit blocks (the translinear stacks and current multiplier). The error from the input stage to the amplifier can then be quantified as well. Table 4.2 shows the calculated and simulated currents expected from the multiplier output. Again, 'Calculated' shows the current calculated by using the theoretical values from Table 4.1 with Eq. 4.23. The 'Simulated' values shows the

	Output Current	Series Resistance % Error
Calculated	134.61 μA	0%
Simulated Ideal Model	139.05 μA	3.68%
Simulated BiCMOS Model	136.59 μA	1.85%

Table 4.2: Calculations of multiplier output current with ideal and non-ideal circuit models. This shows the simulated current values and the resulting series resistances when using these values. The percentage error is the error when compared with theoretical series resistance values.

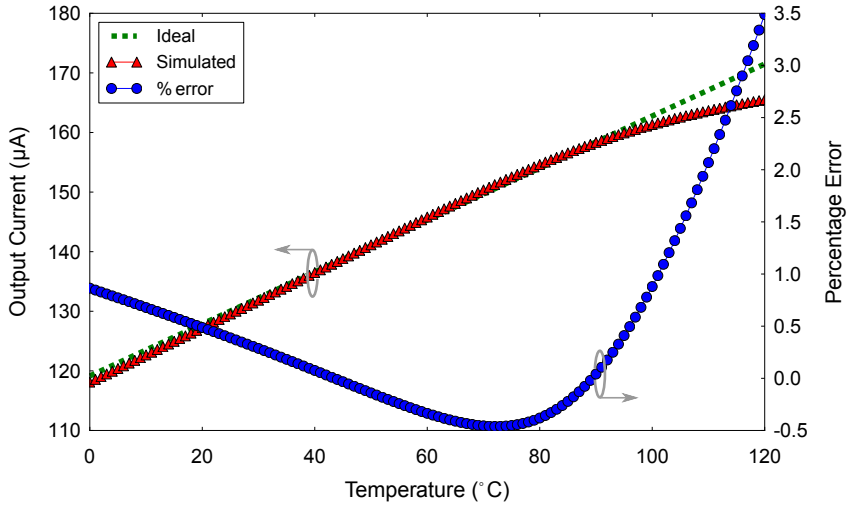


Figure 4.9: Bias current vs. temperature variation compared with the ideal bias current, at the multiplier output.

same current obtained from simulations in SPICE with a non-ideal and idealized transistor model. Note the error is still small in all cases.

Fig. 4.9 shows the variations of temperature as well as the resulting percentage error compared to the ideal calculated bias current, and it suggests the entire circuit is relatively unaffected by temperature variation. The data shows that in the temperature range of 0-100 °C the expected variation in bias current is ≤0.8%. The error increases steadily at values higher than 100 °C, e.g. 3.5% at 120 °C.

Similar data for the supply voltage shows the worst case sensitivity is ≤3.1%, obtained by varying the supply by ±20%, seen in Fig. 4.10. Note that the bottom limit is the saturation of the transistors in the multiplier as the supply voltage gets too low.

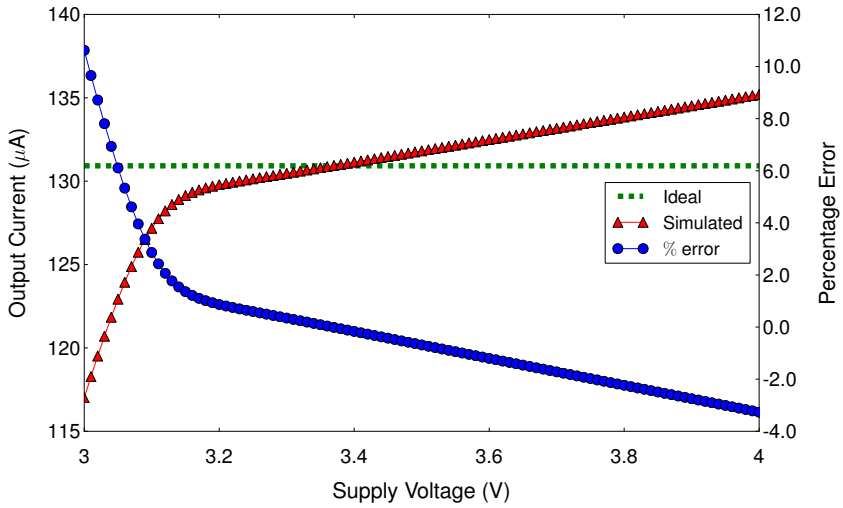


Figure 4.10: Bias current vs. supply voltage variation compared with the ideal bias current at the multiplier output.

4.5.2 Amplifier Bias Current Error

Fig. 4.11 shows the simulated IM3 null of the amplifier with the full BiCMOS model. The bias current through the emitter of the BJT is swept and the output signal's third-order component is captured at 13kHz. This shows the approximate placement of the IM3 null in the simulation with the BiCMOS model, which occurs at 140.5 μA.

4.5.3 IM3 Null Error

We can simulate the impact of these accumulated errors on the IM3 null tracking in the amplifier. Fig. 4.12 shows the position of the simulated circuit relative to the simulated IM3 null in the amplifier. This null is shown by varying both R_1 and R_E within the amplifier circuit (not globally in the complete tracking circuit), which gives a good visual representation of how the null position varies due to process errors in the tracking circuit. It also gives a good indication of where the circuit biases relative to the centre of the IM3 null. This data shows, as expected, the simulation has some error associated with it and therefore the amplifier is not placed directly in the IM3 null.

The effect of absolute and mismatch process error on the IIP3 of the amplifier, in the resistors R_1 and R_E, is shown in Fig. 4.13. These simulations also show

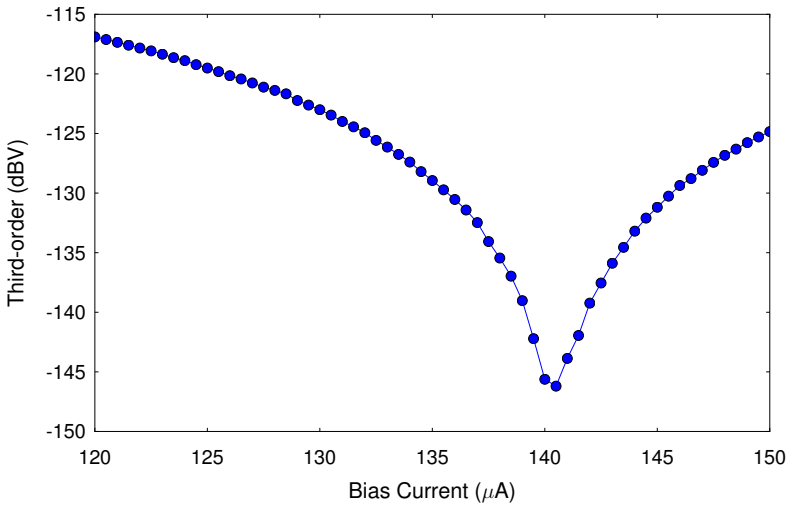


Figure 4.11: Simulated IM3 null of the amplifier showing the null position in bias current. Simulation uses the full BiCMOS transistor models.

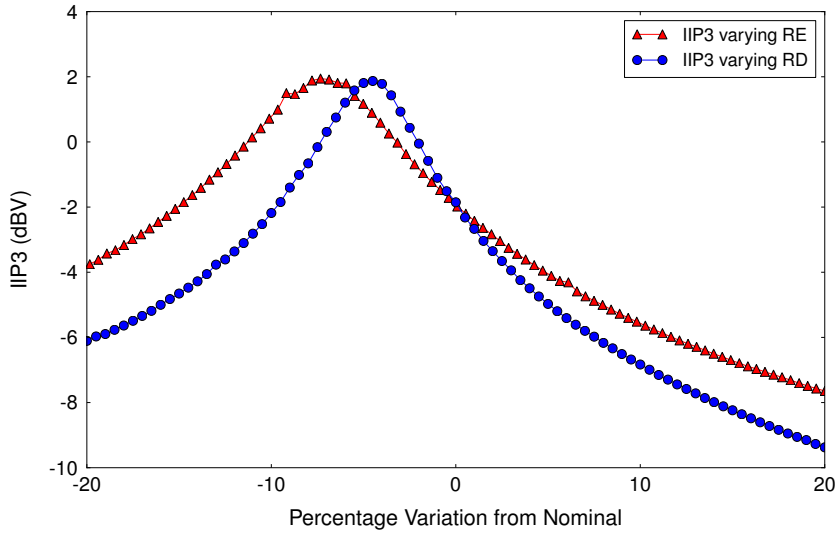


Figure 4.12: Variation of R_E and R_1 from the nominal values and the resulting position in the IM3 null.

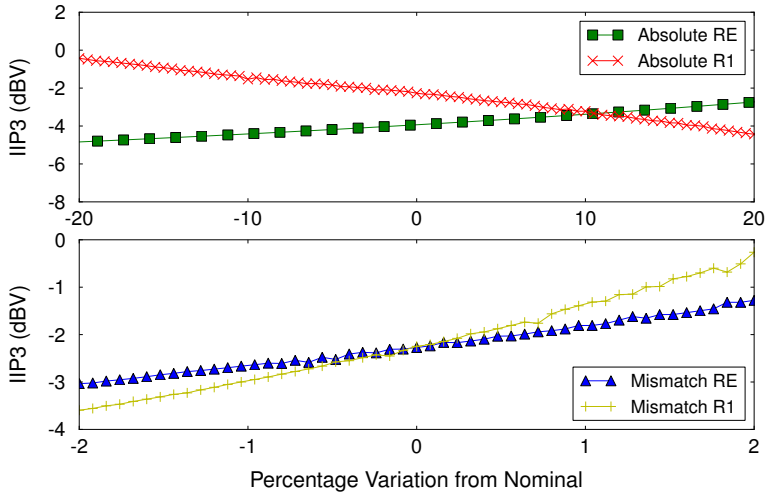


Figure 4.13: Absolute and mismatch process variations of R_E and R_1 and their impact on the current position in the IM3 null.

	Component	Error Limits
Absolute (±20%)	R_1	-1.90%, -0.63%
	R_E	+0.42%, -1.95%
Mismatch (±2%)	R_1	<0.1%, -1.97%
	R_E	-0.42%, -1.5%

Table 4.3: Summary of process error impact on position in the IM3 null, at the amplifier output.

minimal variation of the position in the null relative to the instantaneous bias position, showing the circuit is tracking the selected position in the null over these process errors. These errors are summarised in Table 4.3.

4.6 Measurements

This project does not have the resources available to manufacture an IC and test the circuit using a BiCMOS process. However, the bias circuit has been built and verified using transistor arrays. This circuit will obviously suffer from a much higher error due to beta and parasitic mismatches between transistor arrays and temperature differences. However this work does yield a modest result and hence adds some value to this research.

The circuit was built using Ferranti 2G004E/1U004E BJT transistor arrays.

These arrays are rare in the fact that they contain 8 transistor cells with varying sizes which accommodate for the selection of A and x in the translinear stacks. The datasheets can be seen in Appendix C. The datasheets do not state the emitter resistance size for comparison with the translinear circuits output so further measurements were undertaken to detail the magnitude of the series resistance. Each translinear stack was driven by an Agilent E5270 DC analyzer which forced equal voltages on the top of each branch, allowing the translinear condition to hold. This removes the need for high-gain amplifiers at the top of each branch. The E5270 also allowed accurate reading of the current sourced into each stack, and measurement of the voltage drop across R_1. The available transistors in the arrays still limit the choice of combinations of transistor sizes, hence the setup is restricted to only a few different area combinations. The values used for A and x are chosen to be 2 and 0.5 respectively, using the sizes (6, 8, 4, 24) and (1, 4, 2, 4) for Stack 1 and 2 respectively. As mentioned previously, large transistor size differences lead to beta differences in the transistors and hence error in the measurements. The sizes used are the best available using this setup. Measurements showed the current in the stacks 1 and 2 converged at 1.468V, 899 μA and 1.572V, 1.189mA respectively. Using these values gives the series resistance as 26.9 Ω. This has a worst case measurement error of $\pm$2.7 Ω.

4.6.1 Series Resistance Measurements

The first method used to clarify the series resistance of the Ferranti transistors was the flyback method [51]. This method only measures the emitter resistance, rather than the series resistance. The Agilent E5270 was used to force a base current into a single 1 unit-sized transistor, while the collector current was held at zero amperes. These measurements resulted in an average emitter resistance of 13.7 Ω with a worst case measurement error of $\pm$0.2 Ω. Note that this is a measure of emitter resistance only, and gives no indication of base resistance effects.

The second method used was the method proposed by [52], which is essentially a measurement of the transistor's IM3 null position as a function of series resistance. An HP 3561A Digital Signal Analyzer was used to analyze an output signal's third-order component, as the bias current was swept using a Agilent E3849A DC supply. These measurements resulted in an average series resistance of 16.9 Ω with a worst case measurement error of $\pm$0.3 Ω. This measurement is ex-

pected to be higher than the flyback measurement as it measures the total series resistance rather than just emitter resistance, hence it contains base resistance effects.

One issue with these measurements is that there is still no solid reference to compare this measurements with, or known parameters like R_{BI} such that base resistance can be disentangled. Therefore, no solid conclusions can be made about their accuracy or error. However, they give the only comparative resistance measurement that the stack measurements can be compared against. A second issue which affects this comparison, is the nature of the stack measurements. These were done under unmatched circuit conditions, where the transistor arrays aren't contained to one integrated circuit. Hence, there is an unquantified device mismatch error in the measurement.

4.7 Discussion

The primary goal of this work is to obtain a method of guaranteeing the bias of an amplifier in the device's distortion minima over process, supply variations, and temperature (PVT) and so the sensitivity of the complete system to IM3 is a critical measure. This sensitivity is reflected in the presented simulations and plots. From the nominal IIP3 value set by the nominal component values, these variations lead to a maximum IIP3 variation of ±6.0 dBV, reflecting the bias current error of where the circuit sits in the IM3 null. Including temperature and supply variations of 20% (based on the same percentage variations justified previously), the maximum IIP3 variation increases to approximately ±9.5 dBV. These simulations show good agreement with theory and the error is within the bounds expected from parasitics and transistor process errors.

The discrete measurements show a weak agreement with theory as they vary approximately 10Ω from the stack resistance measurement. When the measurement circuit is considered, we expect a large error to be introduced into the equilibrium current of the stack circuits. Most notably the transistor arrays used are not necessarily suited for the application, only in the fact that they allow for the transistor size ratios. We can further quantify this error by directly measuring the non-ideal parameters of the Ferranti devices. In this case using a 1 unit-sized Ferranti transistor, measurements result in V_{AF} = -27.65 V, $\beta = 75$, and

$I_{KF} = 5.0\,\text{mA}$. Re-simulating a BiCMOS modeled circuit with V_{AF}, β, and I_{KF} adjusted to these values shows a large increase in the measured series resistance. These parameter values give a much closer measured series resistance value of $23.9\,\Omega$. This aids in showing how the non-ideal parameters of the Ferranti transistors will drastically increase the equilibrium current in the stacks, and hence the measured series resistance will be different from the alternative series resistance measurements.

Unfortunately, we cannot make strong conclusions from these stack measurements. The project requires either better transistor arrays, or more practically, access to an integrated circuit process. Nevertheless, the theory and simulations give a strong indication that this circuit will be accurate in measuring series resistance.

One further limitation associated with this work is the intermediate circuitry between the stack circuits and the amplifier. As seen in Fig. 4.10, the error due to low supply voltage becomes large. This is due to a transistor saturating from a lack of supply voltage. This saturation point is not a direct error source in this work as the target supply voltage and supply variation is chosen to not include the effects of this saturation point. However, this is an important point to note as it could limit future work. The intermediate circuitry also includes multiple current mirrors. These areas of the circuit were not analysed in depth, and some insight into their contribution to bias current error would be valuable information.

4.8 Conclusion

This work has derived a translinear proof for a bias circuit which produces a temperature-independent current with series resistance compensation. The series resistance is quantified inherently in the translinear stack circuits and can be used to either measure the parameter, or produce a bias current. The IM3 null of a single BJT (which is series resistance dependent) is used as a test case for the implementation of the translinear stack circuit. Results of simulations confirm that the translinear stack circuit along with a multiplier circuit can track the IM3 null with an accuracy of $\pm 6.0\,\text{dBV}$ when realistic process and circuit variations are considered. Hence, the circuit accurately tracks changes in series resistance

of a BJT process. While measurements do not perfectly confirm theoretical and simulated data, they show to the limit possible with monolithic arrays, that the theory and simulations can be transferred to practical circuits.

This circuit largely solves two major limitations with the work presented in Chapter 3, namely temperature and series resistance variation which moves the null position in terms of collector current. The bias circuit performs this task to an acceptable standard with the figures shown above. Further work on the bias circuit's limitations could decrease this IM3 variation even further.

One interesting outcome of this research is the technique of extracting and quantifying series emitter resistance. Similar techniques are required in device fabrication for commercial products, where a process control monitor (PCM) is used to measure and compare device parameters from wafer to wafer. Common parameters monitored for a BJT device include series resistance. Hence, the technique presented in this work offers a solution to parameter monitoring in device fabrication.

5

Cascoded Compensation

A Cascomp circuit (shorthand for Cascoded Compensation) is a differential amplifier configuration which offers theoretically-perfect distortion cancellation. The term 'Cascomp' is perhaps more generally encompassed by the 'emitter-coupled' or 'cross-coupled' differential pair configuration and operates based on similar principles.

The authors originally became interested in this amplifier through contact with Agilent Technologies, who were interested in improving its performance. Agilent have a particular focus on designing wide-band HBT amplifiers for use up to 20GHz. A performance increase of a few dB in gain or IP3 in the Cascomp circuit would be valuable enough for Agilent to investigate developing an HBT Cascomp amplifier. However, their designers could not achieve this with their current analysis of the amplifier's nonlinearity.

In this chapter, the mathematical theory of this circuit's transfer characteristics will be explored. Firstly the literature's mathematical theory to date along with relevant background on the topic is presented. The current theory is then improved upon to include the non-idealities of the error amplifier by analysing

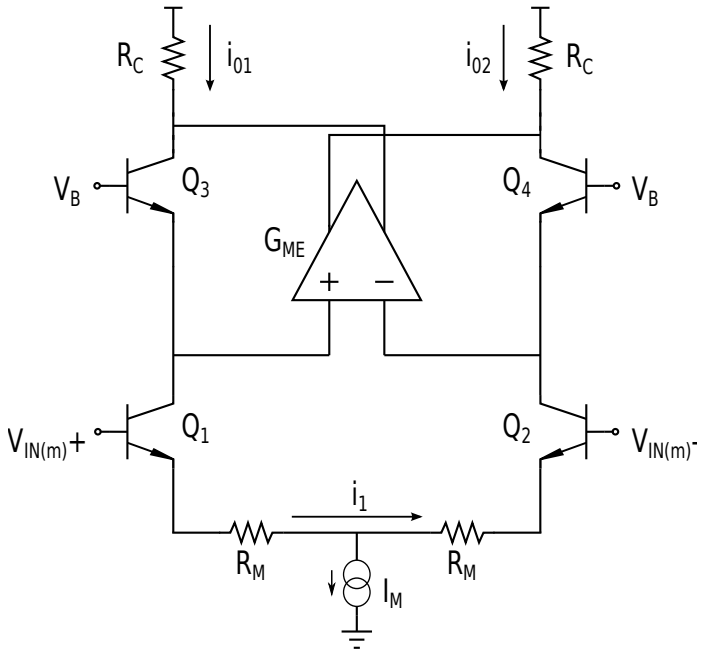


Figure 5.1: Cascomp circuit with an ideal transconductance error amplifier, G_{ME}.

transfer functions of both stages in the Cascomp. This improvement leads to the revelation of more effective bias points that maximise gain and linearity in the Cascomp. Simulation and measurement data is presented that confirms these new bias points exist and an optimum bias point is presented to take advantage of the new theory. Furthermore, the circuit's limitations in a practical situation are discussed, most notably the circuit parameter variations due to process errors. This chapter is not focused on any specific application for a Cascomp circuit but rather a generalised improvement for the topology which can be used where it is beneficial.

5.1 Background

A major theme of this work so far has been distortion reduction in amplifiers and the Cascomp amplifier does not deviate from this topic. Thus far, literature has shown that an idealised circuit model cancels all harmonic distortion at its output. The Cascomp employs feedfoward error correction, where the output signal is amplified and added back into the output again.

The classic depiction of a Cascomp circuit is seen in Figure 5.1. The outside differential pair, formed by Q_1 and Q_2, is referred to as the main amplifier. The inside amplifier is referred to as the error amplifier, in this case represented by an ideal transconductance amplifier, G_{ME}. In practice, the error amplifier is usually another differential pair. Ignoring circuit mismatches which cause each transistor's V_{CE} to be unequal, any distortion components created across the bases of transistors Q_1 and Q_2 are replicated across the respective transistors Q_3 and Q_4. This occurs due to transistors sharing collector current in each side of the amplifier. The error amplifier senses and amplifies the main amplifier's output signal. It is then inverted by the error amplifier's cross-coupled collectors and subtracted from the Cascomp's total output signal. This leads to theoretically-perfect third-order harmonic and intermodulation cancellation (which is the type of distortion reduction we are focused on) but also thermal distortion cancellation as well. The latter is sufficiently covered in the literature and is not analysed in-depth in this work.

5.2 Literature Review

The Cascomp amplifier first appeared in the literature in a patent filing in 1977 [20], followed by the first technical report in 1981 [62]. Both of these publications used a basic algebraic proof to show non-linearity in the main amplifier was canceled due to the replication of the input signal (across transistors Q_{1-4}) and summation of currents at the output. The first reviews did not cover non-idealities in detail but suggested that beta effects and base currents losses would remove the amplifier from its cancellation bias point. Other effects considered are thermal mismatch of the transistors and uncompensated phase delays in the error amplifier compared to the main amplifier [63].

Many improvements to the topology followed, including thermal mismatch distortion correction [64], and simple corrections for beta effects using base resistors on the cascoded pair [65]. Development of the error amplifier to more complex topologies also appear in patent filings. One shown in [66] allows control of frequency response of the error amplifier, so it can be tuned correctly without losing gain and dynamic range. Practical designs also appeared in the literature, such as [67], showing a Cascomp amplifier working at 600 MHz as a 2-stage

CRT amplifier. More recent literature shows the circuit technique being used in CMOS circuits under the title 'cross-coupled pairs'. One example, [68, 69], shows a basic Cascomp topology used in ultra-wideband distributed CMOS amplifier. It achieves a 20 dB reduction in IM3 distortion, or -78 dBc IM3 at 1 GHz at optimum bias conditions. Another example, [70], shows a basic Cascomp topology manufactured in a $0.18\mu m$ TSMC RF CMOS process. It achieves a 6.6 dB improvement in IIP3 at approximately 2 GHz. Similar results are achieved by [71] and [72], showing a manufactured Cascomp in CMOS processes.

One early patent, filed in 1989 by Garuts [73], presents an interesting analysis of a similar topology to the Cascomp. The major difference is the error amplifier's inputs are taken from the same input as the main amplifier. In the Cascomp topology the error amplifier input is taken from the main amplifier output. This patent presents an elegant derivation of the amplifier's overall transconductance and helps form a foundation for the derivation methods used in this text.

5.3 Current Theory

The original Cascomp papers by Quinn [20, 62], show a simple proof for distortion cancellation in a Cascomp circuit as seen in Figure 5.1. Here, this proof is replicated as a starting point for this work. From this circuit, the small-signal input voltage loop is defined as

$$V_{IN(m)} = V_{BE1} - V_{BE2} + 2V_{R_M}, \tag{5.1}$$

where $V_{IN(m)}$ is the applied input signal, V_{BE1} and V_{BE2} are the base-emitter voltages of Q_1 and Q_2 respectively, and V_{R_M} is the voltage across each emitter degeneration resistor of the main amplifier. This equation expresses the linear portion of the input voltage being across R_M and the non-linear portion being across the base-emitter junctions. As expected from basic theory, increasing R_M increases the voltage across this resistance, and hence the amplifier output signal becomes more linear. Compensation of the non-linear portion occurs when a term is introduced to cancel the non-linear term $\triangle V_{BE12} = V_{BE1} - V_{BE2}$. Indeed this is what Quinn states, showing the error amplifier senses this cancellation term by using the replicated non-linear term across Q_3 and Q_4, stated as $\triangle V_{BE34}$

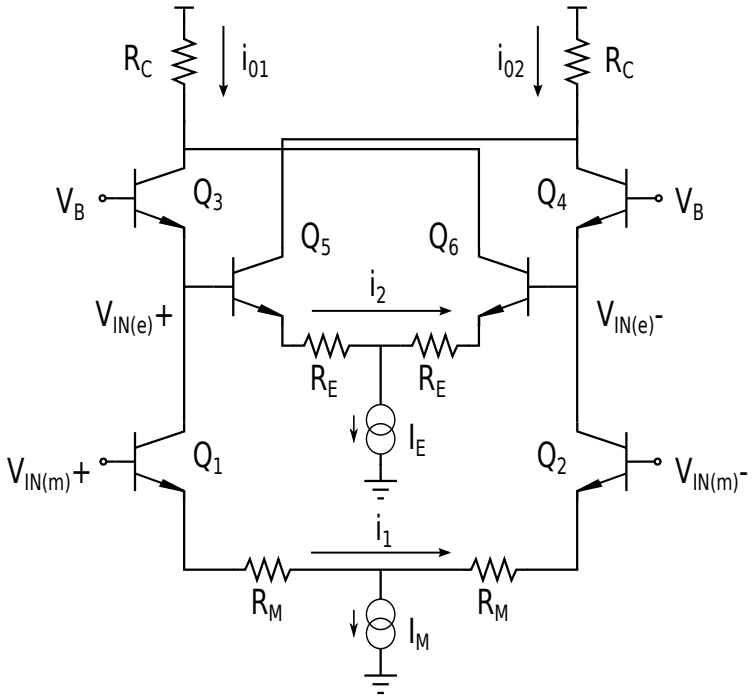


Figure 5.2: Cascomp amplifier with a differential pair used as the non-ideal error amplifier.

(such that ideally $\triangle V_{BE12} = \triangle V_{BE34}$). This is amplified by the G_{ME} of the error amplifier and added to the amplifier output to create the corrected output current as

$$\triangle i_{01} = \frac{V_{IN}}{2R_M} - \frac{\triangle V_{BE12}}{2R_M} + \triangle V_{BE34} G_{ME}. \tag{5.2}$$

This transfer function makes it obvious that, in order for cancellation of the non-linear term to occur, the transconductance of the error amplifier must be

$$G_{ME} = \frac{1}{2R_M}. \tag{5.3}$$

In practice, the error amplifier is not an ideal transconductance amplifier, and will not only amplify the $\triangle V_{BE34}$ term but will also add its own distortion through its own transfer function. Quinn's condition for cancellation is reliant on the error amplifier being highly linear, meaning its own distortion must be assumed negligible. This assumption means information is lost regarding the cancellation points the Cascomp can use. To study this in the following subsections, a practical bipolar Cascomp amplifier is established in Figure 5.2. This figure

defines the output differential current of both amplifiers, i_1 and i_2 for the main and error amplifiers respectively, as well as the input voltage loops for the main and error amplifiers, $V_{IN(m)}$ and $V_{IN(e)}$ respectively, such that

$$\triangle i_{01} = i_1 - i_2 \tag{5.4}$$

$$\triangle i_{02} = i_2 - i_1 \tag{5.5}$$

$$V_{IN(m)} = \triangle V_{BE12} + 2R_M i_1. \tag{5.6}$$

Equation 5.6 can be considered a simple transfer function for the main amplifier's contribution to the output current in terms of $V_{IN(m)}$. One can find a similar transfer function for the error amplifier contribution in terms of the $V_{IN(m)}$. Equation 5.7 shows the input voltage loop summation for the error amplifier.

$$V_{IN(e)} = \triangle V_{BE34} = -\triangle V_{BE56} - 2R_E i_2. \tag{5.7}$$

With the assumption that non-idealities are negligible, the transistor pairs (Q_{12} and Q_{34}) must share the same collector-emitter currents, such that

$$\triangle V_{BE12} = \triangle V_{BE34}. \tag{5.8}$$

A transfer function for the entire circuit defining $V_{IN(m)}$ in terms of i_2 and i_1 using Eq. 5.8 and Eq. 5.7 is found as,

$$V_{IN(m)} = 2R_M i_1 - \triangle V_{BE56} - 2R_E i_2. \tag{5.9}$$

To analyse the output distortion of the amplifier, we need to use a series expansion but this equation is multi-variable, making this format significantly more complex to expand. It contains linear terms with i_1 and i_2, as well as the term $\triangle V_{BE56}$ which is a function of transistors Q_{5-6} and Q_{1-2}, making separation of the amplifier distortion components complex. Instead we employ an elegant solution that first appeared in [73]. Here, the separate distortion contributions from the main and error amplifiers are calculated, and then added together after a series expansion.

5.4 Full Theory

This section aims to analyze the coefficients of a series expansion of the transfer functions for the main and error amplifiers respectively. This leads into a full non-ideal proof of the Cascomp transfer function. Firstly however, since the literature has never shown a full proof of the Cascomp transfer function with an *ideal* error amplifier, we derive this case and prove Quinn's theory. This derivation ignores circuit non-idealities, which are addressed later in the chapter.

5.4.1 Main Amplifier

Again using the circuit in Fig. 5.2, the input voltage loop for this amplifier can be taken as Eq. 5.6 and the V_{BE} terms for transistors Q_1 and Q_2 can be substituted for the Ebers-Moll equation such that

$$V_{BE} = V_T \ln \frac{i_{DC} + i_1}{i_0}, \tag{5.10}$$

where V_T is the thermal voltage, i_{DC} is the emitter bias current (equal to $\frac{I_M}{2}$ for this differential topology), and i_0 is the saturation current of the transistors. Substituting this into Eq. 5.6 gives

$$V_{IN(m)} = V_T \ln \frac{i_{DC} + i_1}{i_0} - V_T \ln \frac{i_{DC} - i_1}{i_0} + 2R_M i_1. \tag{5.11}$$

The logarithmic terms are collected and simplified to

$$V_{IN(m)} = 2R_M i_1 + V_T \ln \left(\frac{1 + 2\frac{i_1}{I_M}}{1 - 2\frac{i_1}{I_M}} \right). \tag{5.12}$$

This describes $V_{IN(m)}$ as a function of i_1. It is the inverted form of the common tanh transfer function for a single differential pair. In the literature it is commonly presented with i_1 as the subject of the equation [23].

The Cascomp output current is the summation of the main and error amplifier's current through the connected and cross-coupled collectors. This means a similar equation for the ideal error amplifier case is required, such as $V_{IN(m)}$ as a function i_2.

5.4.2 Ideal Error Amplifier

The ideal error amplifier is essentially modeled as an ideal transconductance G_{ME}, as seen in Fig. 5.1, with i_2 being the output current from the error amplifier. The input transfer function for the ideal error amplifier is defined as,

$$i_2 = G_{ME} V_{IN(e)}. \tag{5.13}$$

Eq. 5.8 and Eq. 5.7 can be used to form a substitution for $V_{IN(e)}$, the goal being to find $V_{IN(e)}$ in terms of i_2. Using this, the error amplifier input voltage is

$$V_{IN(e)} = \triangle V_{BE12} = \triangle V_{BE34}. \tag{5.14}$$

Substituting Eq. 5.14 and the Ebers-Moll equation into Eq. 5.13 gives,

$$i_2 = G_{ME} V_T \ln\left(\frac{\frac{I_M}{2} + i_1}{\frac{I_M}{2} - i_1}\right). \tag{5.15}$$

By rearranging this equation we can find i_1 as a function of i_2, and this then is substituted into Eq. 5.12 to obtain an equation describing the error amplifier transfer function. Eq. 5.15 is rearranged to be

$$i_1 = \frac{I_M}{2}\left(\frac{e^{\frac{i_2}{V_T G_{ME}}} - 1}{e^{\frac{i_2}{V_T G_{ME}}} + 1}\right), \tag{5.16}$$

and substitute into Eq. 5.12 to obtain the ideal error amplifier transfer function,

$$V_{IN(m)} = 2R_M \frac{I_M}{2}\left(\frac{e^{\frac{i_2}{V_T G_{ME}}} - 1}{e^{\frac{i_2}{V_T G_{ME}}} + 1}\right) + V_T \ln\left(\frac{1 + \left(\frac{e^{\frac{i_2}{V_T G_{ME}}} - 1}{e^{\frac{i_2}{V_T G_{ME}}} + 1}\right)}{1 - \left(\frac{e^{\frac{i_2}{V_T G_{ME}}} - 1}{e^{\frac{i_2}{V_T G_{ME}}} + 1}\right)}\right). \tag{5.17}$$

5.4.3 Amplifier Coefficients

Eq. 5.12 and Eq. 5.17 describe the Cascomp's total output current. Performing a series expansion on both yields the respective harmonic components. For

these expansions we make the assumption that higher order terms are negligible. It is important to note that, because Eq. 5.12 and Eq. 5.17 are non-invertible for i_1 or i_2, instead the first derivative of the series expansion is inverted which allows the coefficients to describe transconductance terms ($\frac{i}{V_{IN}}$). This is the elegant solution to non-invertible functions suggested by [73]. The main and error amplifier series expansions will be

$$i_1 = A_{m0} + A_{m1} V_{IN(m)} + A_{m3} V_{IN(m)}^3, \tag{5.18}$$

$$i_2 = A_{e0} + A_{e1} V_{IN(m)} + A_{e3} V_{IN(m)}^3, \tag{5.19}$$

where A_{mn} and A_{en} describe the nth-order derivative of the transfer function with respect to V_{IN}. The output of both amplifiers are summed together, out of phase at their respective collectors, so it follows that the gain coefficients of the Cascomp output are,

$$i_1 - i_2 = (A_{m0} - A_{e0}) + (A_{m1} - A_{e1}) V_{IN(m)} + (A_{m3} - A_{e3}) V_{IN(m)}^3. \tag{5.20}$$

From basic circuit theory we expect the second-order term $(A_{m2} - A_{e2})$ to be zero, as an inherent property of differential amplifiers is the cancellation of second-order terms [6]. This leaves the overall fundamental gain term $(A_{m1} - A_{e1})$, and the overall third-order gain term $(A_{m3} - A_{e3})$. To find the coefficients one can differentiate and invert the transfer functions with the use of the chain rule for the second and third-order calculations. Equating i_1 and i_2 to zero for each respective differentiated function gives us the particular expansion coefficient. For the main amplifier we obtain the coefficients

$$A_{m1} = \frac{I_M}{2R_M I_M + 4V_T}, \tag{5.21}$$

$$A_{m2} = 0, \tag{5.22}$$

$$A_{m3} = \frac{-2I_M V_T}{(I_M R_M + 2V_T)^4}. \tag{5.23}$$

As expected, the second-order gain term is zero. Similarly for the error amplifier, using Eq. 5.17, the coefficients of the gain terms can be derived as

$$A_{e1\_Ideal} = \frac{2G_{ME}V_T}{R_M I_M + 2V_T}, \tag{5.24}$$

$$A_{e2\_Ideal} = 0, \tag{5.25}$$

$$A_{e3\_Ideal} = \frac{2G_{ME}I_M R_M V_T}{(I_M R_M + 2V_T)^4}. \tag{5.26}$$

By using the third-order coefficients along with the summation in Eq. 5.20, a condition can be found which will lead to the third-order term equating to zero. This is derived to be

$$A_{m3} - A_{e3\_Ideal} = -\frac{2I_M V_T}{(I_M R_M + 2V_T)^4} - \frac{2G_{ME}I_M R_M V_T}{(I_M R_M + 2V_T)^4}. \tag{5.27}$$

Rearranging and canceling terms results in the condition in Eq. 5.28. This is the same condition presented by Quinn and hence confirms his theory under ideal error amplifier assumptions. Note the G_{ME} is negative due to the cross-coupled collectors.

$$G_{ME} = -\frac{1}{2R_M}. \tag{5.28}$$

5.4.4 Non-Ideal Error Amplifier

The same mathematical process is applied for the error amplifier, but now with a non-ideal transfer function. A differential amplifier with resistive degeneration can be accurately described by the tanh function [23]. Note that this is the same result obtained from inverting, Eq. 5.12, which is the transfer function for a differential amplifier. In terms of the error amplifier, this can be expressed as

$$i_2 = -I_E \tanh\left(\frac{V_{IN(e)} - R_E i_2}{2V_T}\right), \tag{5.29}$$

where i_2 is again the error amplifier's differential current, and $V_{IN(e)}$ is the input voltage to the error amplifier. We apply the same process, finding $V_{IN1} = f(i_1)$ and $V_{IN1} = f(i_2)$, noting that the main amplifier case has not changed as it is only a function of i_1. However, the latter requires finding $i_1 = f(i_2)$ and

substituting into $V_{IN1} = f(i_1)$, giving $V_{IN1} = f(i_2)$. Substituting in the general differential amplifier equation gives $i_1 = f(i_2)$ as

$$i_2 = -I_E \tanh\left(\frac{V_T \ln\left(\frac{\frac{I_M}{2}+i_1}{\frac{I_M}{2}-i_1}\right) - R_E i_2}{2V_T}\right), \tag{5.30}$$

$$i_1 = \frac{-I_M}{2}\frac{(2i_2 - I_E) + (2i_2 + I_E)\, e^{\left(\frac{2i_2 R_E}{V_T}\right)}}{(-2i_2 + I_E) + (2i_2 + I_E)\, e^{\left(\frac{2i_2 R_E}{V_T}\right)}}. \tag{5.31}$$

Eq. 5.31 can be substituted into Eq. 5.12 to give an equation of the form $V_{IN1} = f(i_2)$ as,

$$V_{IN(m)} = 2R_M X_2 + V_T \ln\left(\frac{1+2\dfrac{X_2}{I_M}}{1-2\dfrac{X_2}{I_M}}\right), \tag{5.32}$$

where X_2 is the full expression for $i_1 = f(i_2)$ given by Eq. 5.31. The same method of differentiation is followed as in the ideal case, to find the non-ideal gain coefficients. The main amplifier gain coefficients remain the same in Eq. 5.21 - 5.23. The non-ideal error amplifier gain coefficients are calculated as,

$$A_{e1} = -\frac{I_E V_T}{(R_E I_E + 2V_T)(R_M I_M + 2V_T)} \tag{5.33}$$

$$A_{e2} = 0 \tag{5.34}$$

$$A_{e3} = -\frac{2I_E V_T R_M\left(I_E^3 I_M R_E^3 + 6I_E^2 I_M R_E^2 V_T + 12 I_E I_M R_E V_T^2 - \frac{16V_T^4}{R_M}\right)}{(I_E R_E + 2V_T)^4 (I_M R_M + 2V_T)^4}. \tag{5.35}$$

These gain coefficients are proportional to the magnitude of their respective output harmonic components. Therefore, any coefficient minima show conditions for IM3 cancellation. Of course, Eq. 5.35 is reasonably complicated and further algebra will not be helpful. We instead will rely on describing any minima graphically in the next section. Note that full derivations of all gain coefficients can be found in Appendix D.

5.5 Cascomp Biasing

In this section the proposed theory is used to find bias points that maintain overall gain while maximizing linearity. The overall fundamental and third-order gain coefficients are expressed graphically and these are varied with respect to circuit variables. Generally, the main amplifier variables R_M and I_M are held constant for this section, and the error amplifier variables R_E and I_E are varied to express the coefficient relationships. Note that this research focuses on these resistors and currents but we could also just as easily vary the transconductance of each amplifier and show similar results. However, this would mask some subtle differences that R_M and I_M have on the BJT Cascomp amplifier.

5.5.1 Fundamental Gain

The first-order gain coefficients of the full Cascomp amplifier can be plotted. This will show the relative size of fundamental gain of the Cascomp, for both ideal and non-ideal error amplifier cases. The ideal overall fundamental gain coefficient is given by,

$$A_{1\_Ideal} = A_{m1} - A_{e1\_Ideal} = \left(\frac{I_M}{2R_M I_M + 4V_T}\right) - \left(\frac{2G_{ME} V_T}{R_M I_M + 2V_T}\right). \quad (5.36)$$

For the ideal error amplifier case, a small-signal approximation for G_{ME} is made as

$$G_{ME} = \frac{1}{\left(\frac{V_T}{I_E} + R_E\right)}. \quad (5.37)$$

This approximation is utilised in order to draw a strong comparison between the ideal and non-ideal cases of the Cascomp amplifier (Fig. 5.1 and Fig. 5.2 respectively). These equations produce traces showing how sweeping I_E and R_E affects the output signal's fundamental gain A_{1_Ideal} relative to static I_M and R_M values. Both cases use set values of $I_M = 20\,\text{mA}$ and $R_M = 10\,\Omega$, for varying values of I_E with R_E swept. The equation to describe the non-ideal overall fundamental gain coefficient A_1 is given by

$$A_1 = A_{m1} - A_{e1} = \left(\frac{I_M}{2R_M I_M + 4V_T}\right) - \left(\frac{-I_E V_T}{(R_E I_E + 2V_T)(R_M I_M + 2V_T)}\right). \quad (5.38)$$

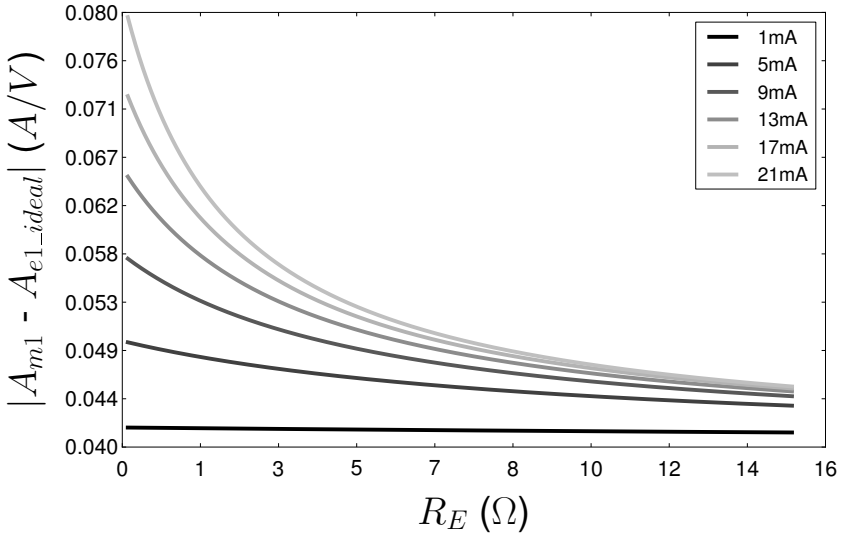


Figure 5.3: Ideal theoretical fundamental coefficient cancellation of a Cascomp amplifier for fixed R_M and I_M. R_E is swept for values of I_E. The y-axis reflects the magnitude of the gain.

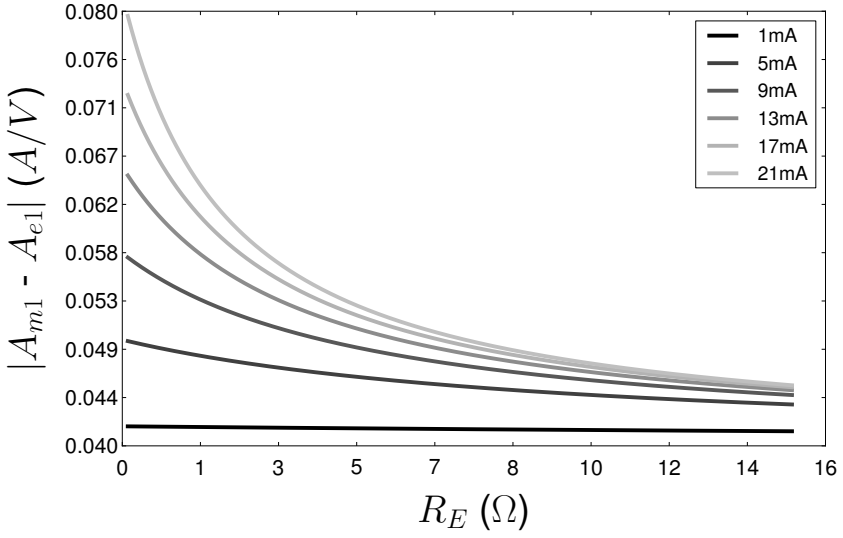


Figure 5.4: Non-ideal theoretical fundamental coefficient cancellation of a Cascomp amplifier for fixed R_M and I_M. R_E is swept for values of I_E. The y-axis reflects the magnitude of the gain.

In the ideal and non-ideal error amplifier case, both graphs (and equations) are equivalent as we have assumed higher order effects on first-order components are negligible. Hence Fig. 5.3 and 5.4 represent both fundamental output cases. The fundamental gain is improved when R_E tends to zero and I_E tends towards large values, but the amplifier becomes more nonlinear. This is in agreement with circuit theory which states degenerating a differential amplifier will reduce gain while increasing linearity [23]. We can confirm similar effects with I_M and R_M through the same theoretical simulations. Increasing I_M will decrease the peak gain value the plot approaches (where R_E tends to zero), but does not drastically change gain values when R_E is high. Increasing R_M will decrease the surface's overall gain across the surface for any given error amplifier variables. This is analysed with more depth later in the chapter.

5.5.2 Third-Order Gain

The same process is applied to the third-order gain coefficients for the ideal and non-ideal cases. In this case, the theoretical third-order cancellation occurs when the amplifier's overall third-order coefficient (A_3) equals zero. Firstly, the ideal case equation is given in Eq. 5.39, where G_{ME} is again substituted by the approximation given in Eq. 5.37 below. This is expressed graphically in Figure 5.5 showing how the single null positions change with the circuit variables.

$$A_{3\_Ideal} = A_{m3} - A_{e3\_Ideal} = \left(\frac{2I_M V_T}{(I_M R_M + 2V_T)^4}\right) - \left(\frac{4G_{ME} I_M R_M V_T}{(I_M R_M + 2V_T)^4}\right). \quad (5.39)$$

The non-ideal case is given by

$$A_3 = A_{m3} - A_{e3} = \left(\frac{2I_M V_T}{(I_M R_M + 2V_T)^4}\right) - \left(\frac{-2I_E V_T R_M \left(I_E^3 I_M R_E^3 + 6I_E^2 I_M R_E^2 V_T + 12 I_E I_M R_E V_T^2 - \frac{16V_T^4}{R_M}\right)}{(I_E R_E + 2V_T)^4 (I_M R_M + 2V_T)^4}\right). \quad (5.40)$$

Fig. 5.6 shows a significant variation in shape of the overall third-order component from the ideal case and hence a change in the possible IM3 cancellation

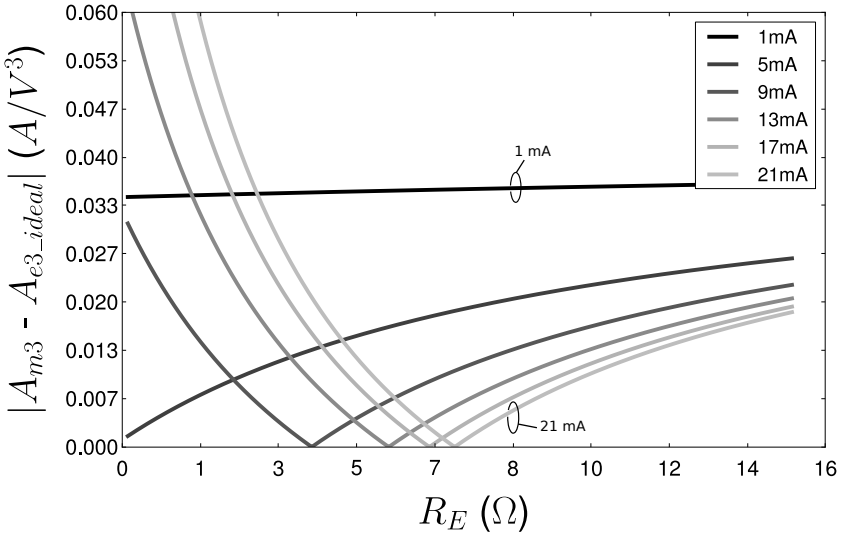


Figure 5.5: Ideal theoretical third-order coefficient cancellation of a Cascomp amplifier for fixed R_M and I_M. R_E is swept for values of I_E. The y-axis reflects the magnitude of the total IM3 product and the nulls indicate IM3 cancellation.

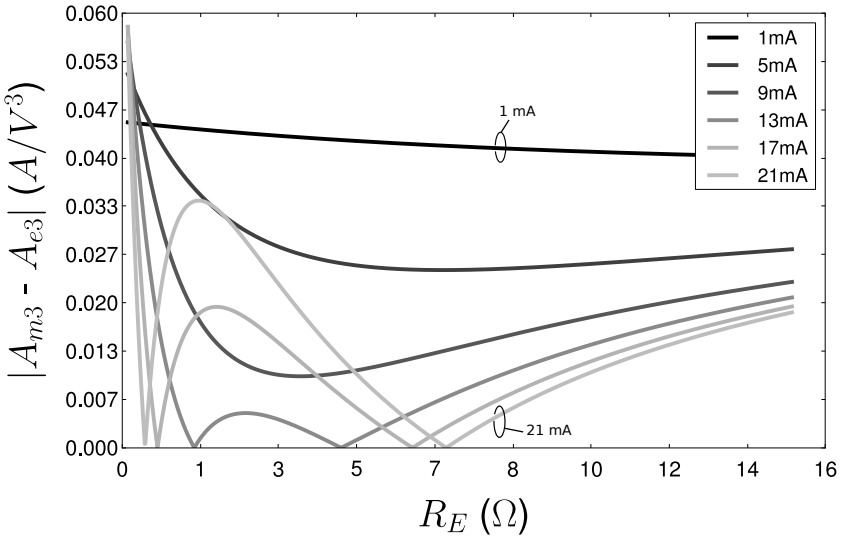


Figure 5.6: Non-ideal theoretical third-order coefficient cancellation of a Cascomp amplifier for fixed R_M and I_M. R_E is swept for values of I_E. The y-axis reflects the magnitude of the total IM3 product and the nulls indicate IM3 cancellation.

points. In the ideal case the cancellation points are singular for a given I_E value. In the non-ideal case two cancellation points occur at certain variable combinations. A new null now appears at lower values of R_E for given I_E values (herein referred to as the 'second' null or minima). As shown previously, lower values of emitter degeneration lead to higher fundamental gain and the second null position is occurs at lower R_E values. This insight is potentially very useful as it will increase IP3 in the amplifier. This bifurcation of the non-ideal IM3 minima is exposed because the proposed non-ideal theory now considers the error amplifier transfer function to be a function of the main amplifier transfer function. The main amplifier third-order distortion is now considered to be amplified through the error amplifier as well.

5.6 Simulation

In order to bridge this new theory with a real world circuit, this section presents SPICE simulations of a Cascomp circuit using NPN bipolar transistor models from an IBM 0.5 μm BiCMOS process. These simulations aim to validate the proposed theoretical model and prove the newly observed IM3 nulls exist in practice. The bipolar models used can be seen in [61], and it assumed they can be scaled to give reasonably low parasitic resistances.

5.6.1 Circuit Schematic

LTspice was used to build the SPICE netlist and NGSpice was used to simulate the circuit through Python scripts. Fig. 5.7 below shows the LTspice schematic. Circuit values were kept consistent with theory calculations with R_E and I_E swept, with $R_M = 10\,\Omega$ and $I_M = 20\,\text{mA}$. Fig. 5.8 shows the circuit's IM3 magnitude. This data yields a result consistent with the non-ideal theoretical third-order plot. For the same circuit values, a cancellation locus is obtained equivalent to the non-ideal theoretical third-order gain plot predicted by Eq. 5.23 - 5.35 and implied by Fig. 5.6. As an example, theory predicts at $I_E = 20\,\text{mA}$ when R_E equal to $7\,\Omega$ and $0.5\,\Omega$, IM3 nulls will occur. Simulation results show nulls occurring at approximately 6Ω and 1Ω. This variation is expected due the parasitic resistance (approximately $1.0\,\Omega$ for the used scaled transistors) of the bipolar models which

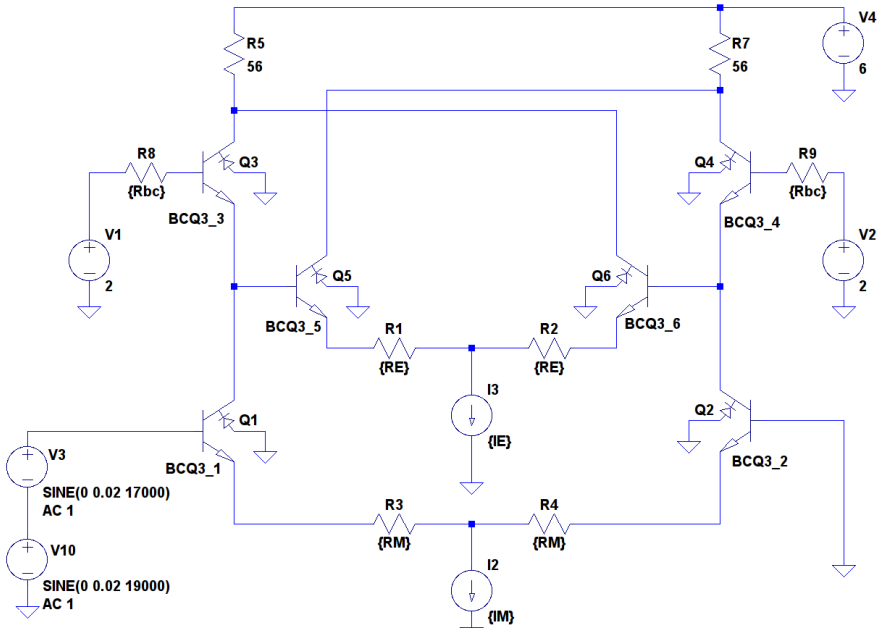


Figure 5.7: Cascomp circuit as built in LTspice.

effectively shifts the R_M value. The result of both R_E and R_M being shifted by this parasitic resistance is that the cancellation locus is 'squeezed', and the two nulls occur closer together in R_E. This is largely due to R_M being shifted rather than R_E.

5.6.2 Optimisation

Fig. 5.8 shows that circuit components R_E, I_E set the bias point of the circuit. It is obvious that R_E and I_E optimal values are those which set the circuit in an IM3 null. However, there is now a choice between IM3 nulls that fall at higher or lower R_E values. Furthermore, varying R_M also shifts these nulls and changes the overall fundamental gain of the circuit. This makes the circuit values which give an optimal bias point (in terms of gain and IM3) less obvious. To analyse the effects of R_M simulations are run similar to those done in the previous section, but instead varying R_M instead of I_E. I_E is now fixed at 20 mA.

Fig. 5.9 shows the simulated OIP3 of a Cascomp amplifier with R_E and R_M swept, while I_E and I_M are fixed are at 20 mA each. Note that the observed locus of cancellation in this plot is not comparable to the IM3 plot in Fig. 5.8. Observation of this plot data suggests that as R_M increases it both shifts the nulls

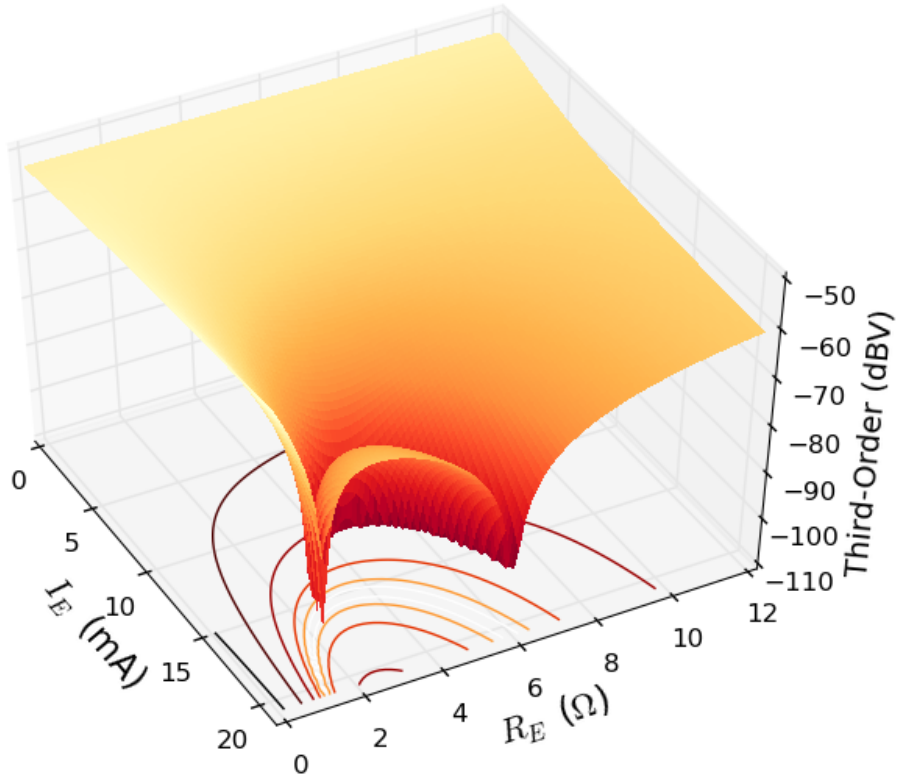


Figure 5.8: Simulated third-order output (dBV) of a non-ideal Cascomp amplifier for fixed R_M and I_M over a 56Ω load. Note that the z-axis values have been clipped (at -105 dBV) in the null positions to allow for readability.

to occur at lower values of I_E, but it also separates the two nulls (on any given I_E value) to occur further apart in terms of R_E and vice versa. This suggests we can optimise the shape of the cancellation locus. By decreasing R_M the two nulls can be moved closer together in terms of R_E and potentially make IP3 larger and/or make a more robust bias point in terms of circuit variation.

The proposed optimum bias point for the circuit conditions $I_E = I_M = 20\,\text{mA}$ are shown in Fig. 5.10. Three different R_M values are chosen around this point. At $R_M = 8.4\,\Omega$, the region between the two nulls produces a minimum OIP3 of 30dBV for the simulated circuit. This bias point maximises IP3 in terms of the degeneration resistors and may be of use if process variation is a problem. Fig. 5.11 shows the same optimum bias point except with $I_E = 30\,\text{mA}$ and hence the optimum cancellation occurring at lower R_M values.

Fig. 5.12 compares the proposed optimum bias point (where R_M has been

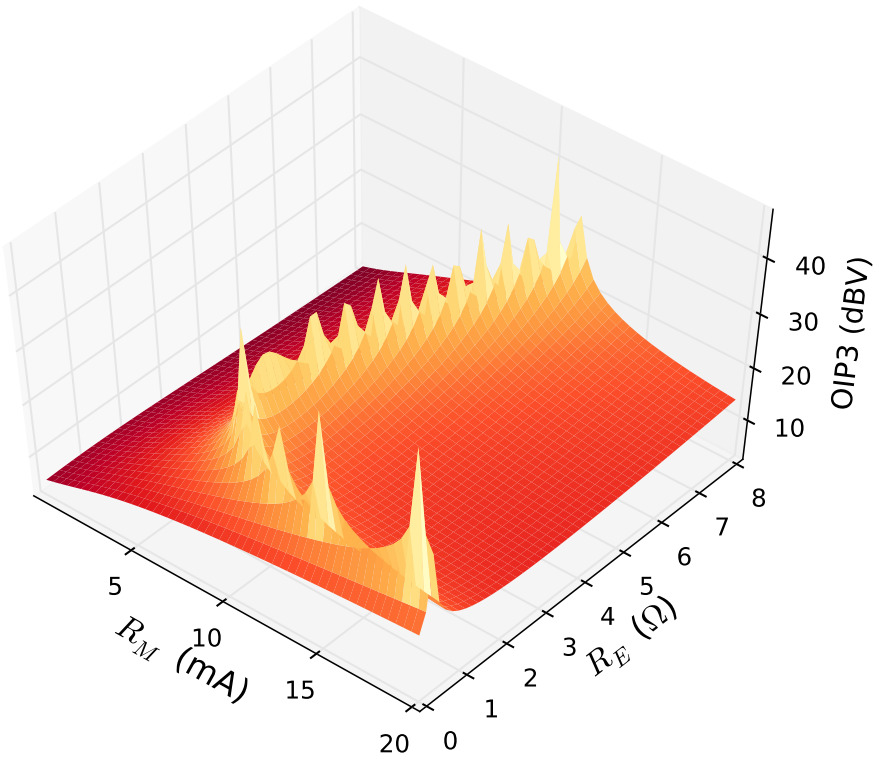


Figure 5.9: Simulated OIP3 of a Cascomp circuit with R_E and R_M swept. I_E and I_M are fixed are at 20 mA each. Note the peaks are points that fall deep into the IM3 null.

increased to move the two nulls very close together) with a bias point where R_M is smaller (and therefore its nulls are further separated). This clearly shows the benefit of the optimised case as the region between the two nulls has relatively low IM3 compared with each null of the nominal case. This results in a wide range in which IM3 is consistently very small. To provide some form of benchmark, this figure also includes the simulated IM3 of a differential pair. These simulations were performed such that the fundamental output levels are as close as possible as well as the emitter current densities being equal in each circuit. While this is still not a completely fair comparison because of the differences in topology and emitter degeneration between the Cascomp and differential pair, it does highlight the improvement in IP3 when using a Cascomp and the benefit of optimising R_M in a Cascomp circuit.

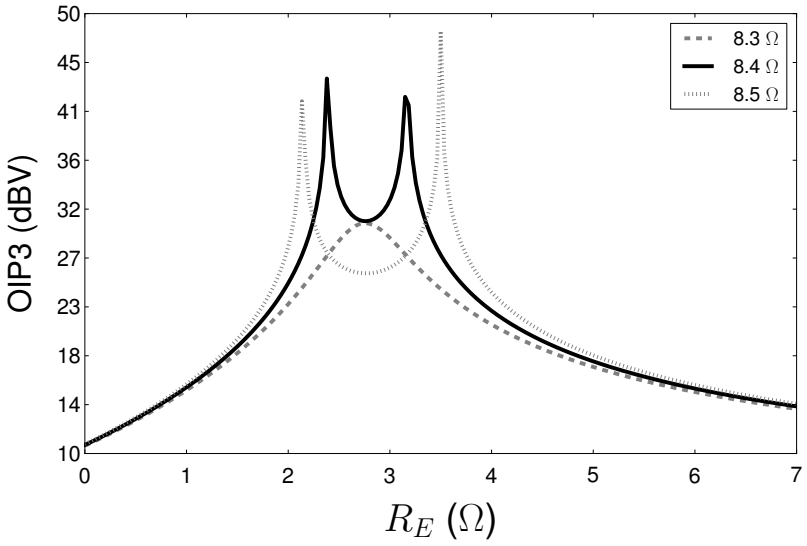


Figure 5.10: Optimum bias point for a Cascomp circuit with R_E swept with R_M varied.

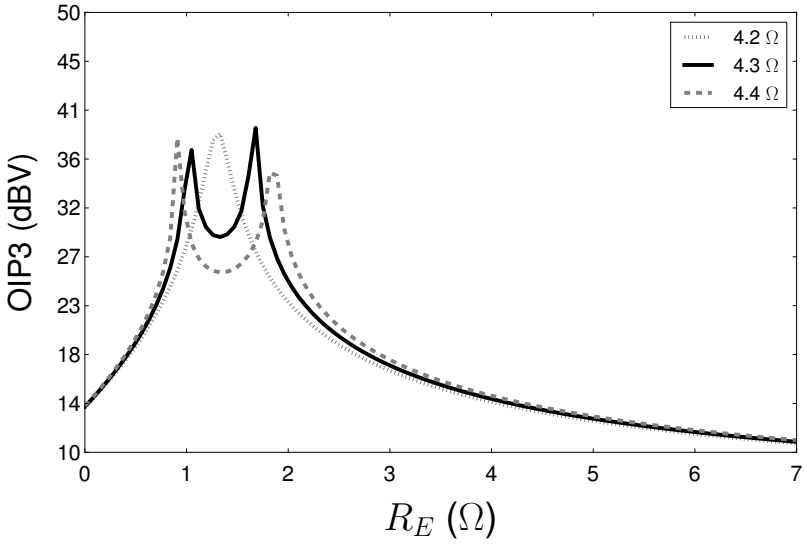


Figure 5.11: Optimum bias point for a Cascomp circuit with R_E swept with smaller R_M values for comparison.

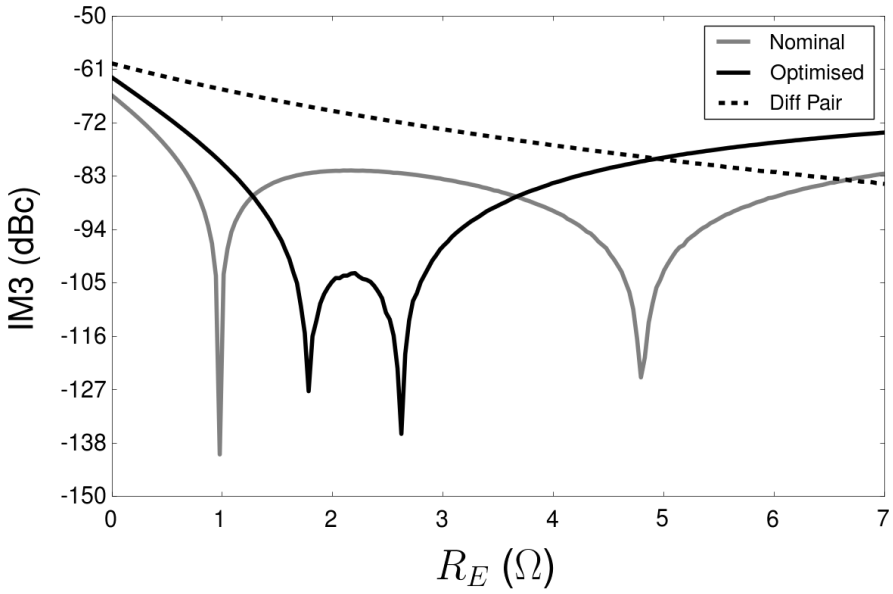


Figure 5.12: Optimum bias point in R_E compared against a conventional Cascomp (Nominal) and differential pair.

5.7 Process Errors

The Cascomp topology is susceptible to variations in circuit parameters which shift the circuit's operation from the optimal bias point. This section shows the effects of all the major circuit parameters and components in the circuit.

The data presented in this section is obtained from SPICE simulations using Monte-Carlo simulations to find the worst case variations in the circuit. Variation percentages for a BJT process are assumed to be ±20% for absolute process variation from wafer to wafer, and ±2% mismatch variation in each wafer [27, 28]. These limits are chosen to get greater than what we expect from commercial processes.

5.7.1 Transistor Parameters

The transistor parameter with the largest effect on the null position is the current gain, β. If we assume absolute process variation to be 20% for transistor parameters, the bias point can be completely removed out of the IM3 null. However this

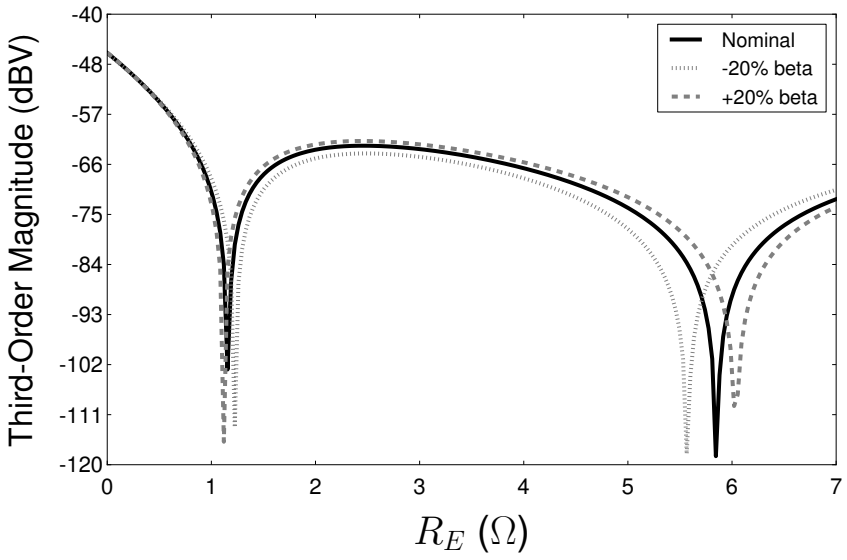


Figure 5.13: Simulated third-order output (dBV) of a non-ideal Cascomp amplifier. 'Nominal' is the normal circuit parameters. '±20% beta' show absolute process variation of β parameters in the circuit. R_E is swept for fixed R_M , I_M and I_E.

can effectively be corrected by using a cascoded transistor pair at the output.

Fig. 5.13 shows the worst case effects of absolute 20% variation of current gain and early voltage (V_{AF}) on the normal circuit presented in Fig. 5.2, and the circuit with an extra cascoded pair at the Cascomp output. We observe a significant improvement due to absolute variation in these parameters, and its null position shift is no longer significant. Other transistor parameters including saturation current, I_S, have relatively minimal impact with absolute variation. Mismatch process errors in the transistor parameters are assumed to be 2% at worst. Simulations show these again have minimal impact.

Mismatch process errors in the transistor parameters β, V_{AF}, and I_S are assumed to be ±2% at worst. Monte-Carlo simulations (done over 1000 iterations) showed that in general, these transistor parameter variations were not a significant problem compared with absolute variations. These results are seen in Fig. 5.14.

In general, these simulations showed transistor parameter variations were not a significant problem with the exception of absolute current gain variation. Furthermore, if β is large then its effects are significantly reduced. These obser-

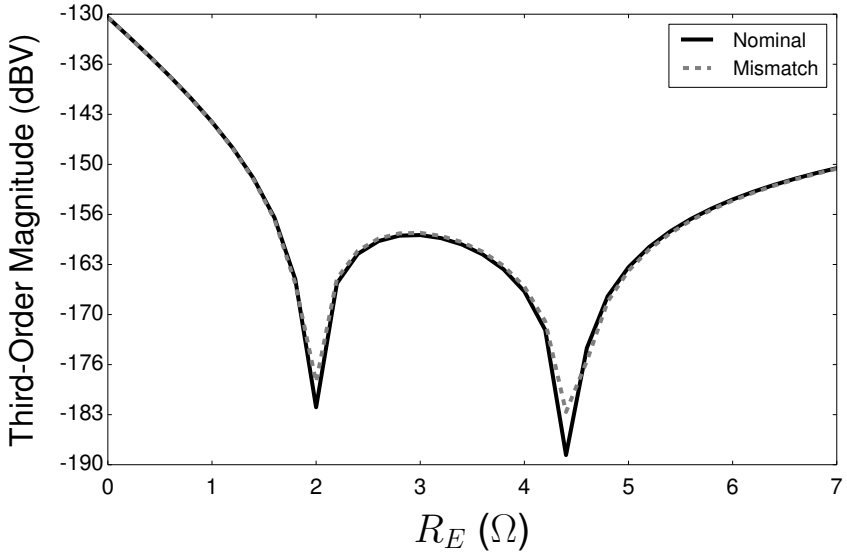


Figure 5.14: Simulated third-order output (dBV) of a non-ideal Cascomp amplifier. 'Nominal' is the normal circuit parameters. 'Mismatch' show the ±2% mismatch process variation of β, V_{AF}, and I_S parameters in the circuit. R_E is swept for fixed R_M , I_M and I_E.

vations also indicate that the assumption of $\triangle V_{BE12} = \triangle V_{BE34}$ in the derivation of the non-ideal theory is indeed reasonable provided β is large.

The greatest variations in the null positions are due to process errors affecting the total degeneration resistance at the emitters of the main and error amplifiers. Fig. 5.15 shows the impact on distortion nulls with absolute variations of ±5% in the emitter resistors R_M. When R_M varies both nulls move to occur at different R_E values. In comparison to variations in β, there is a much larger shift in the null positions. In high precision applications manufacturing tolerances are a common problem. There are many well established techniques for post-fabrication circuit trimming to address these problems, (usually after packaging to minimise stress effects) involving some form of programming to select incremental component elements or injecting small currents [74][75]. Externally trimming the bias current I_E would allow for full correction back into the distortion null. The need for trimming would clearly be dependent on the application, but the author considers it a reasonable solution to address resistance variations in a Cascomp.

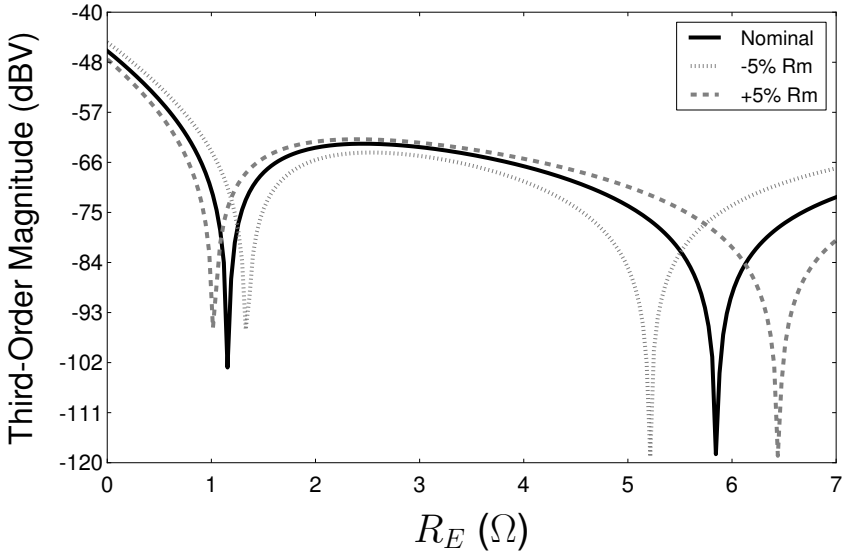


Figure 5.15: Simulated third-order output (dBV) of a non-ideal Cascomp amplifier. 'Nominal' is the normal circuit parameters. '±5% RM ' indicates respective 5% absolute variation of the main amplifier emitter resistance. R_E is swept for fixed R_M , I_M and I_E.

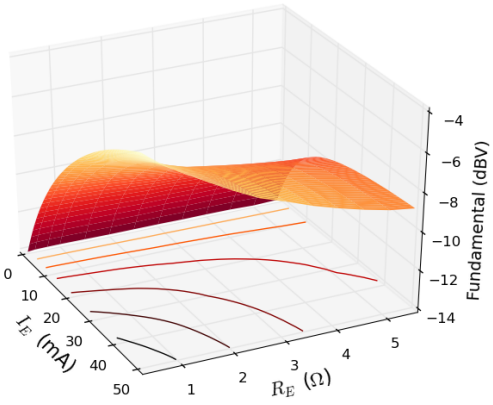
5.8 Experimental Results

Measurements were made to confirm this theory using the circuit shown in Fig. 5.2. While they are done using discrete devices, each differential pair is contained in the same IC, which minimises process and temperature variations between paired transistors. Therefore, the measurements should be comparable to what would be expected in a single IC.

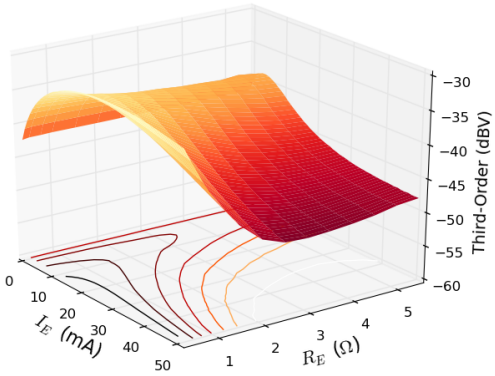
5.8.1 Measurements

The circuit was constructed using discrete components and CA3083 transistor arrays. The values I_E and R_E in the error amplifier were swept and the output current of the circuit was captured using an Agilent 3561A. Current sources were controlled and swept using an Agilent E5270. The main amplifier's current I_M was held at 20 mA (10 mA per side) and measurements were taken at three values of R_M at 5.6 Ω , 10.4 Ω and 15.2 Ω respectively. The amplifier was driven with a two-tone signal at 11 kHz and 13 kHz at input levels of -22.25 dBV per tone. The

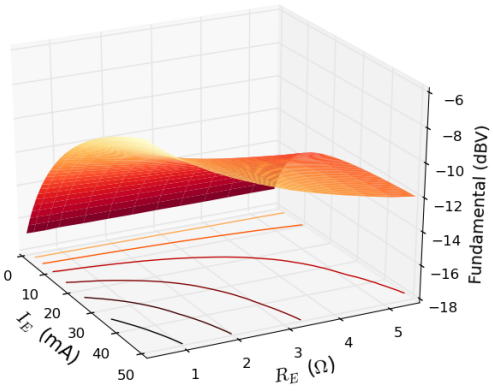
load resistors were chosen to be 56Ω, meaning the amplifier was operated well below compression. The results can be seen in Figs. 5.16a–5.16f which show the cancellation loci created at each R_M–I_M point. As R_M is increased, the loci changes, following what would be expected from theory. As R_M increases, smaller distortion components are required from the error amplifier for cancellation, so the distortion nulling starts to occur at lower values of I_E. When R_M is at low values there are no cancellation points for the shown I_E range (Fig. 5.16b) but rather they are occurring at much higher I_E values. A locus of cancellation is produced when R_M is increased (Fig. 5.16d). When R_M is further increased, this locus moves further to lower I_E values at higher R_E values (Fig. 5.16f).



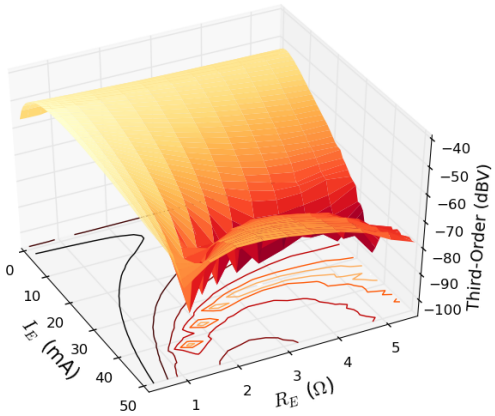
(a) Fundamental output for R_M=5.6 Ω and I_M=20 mA



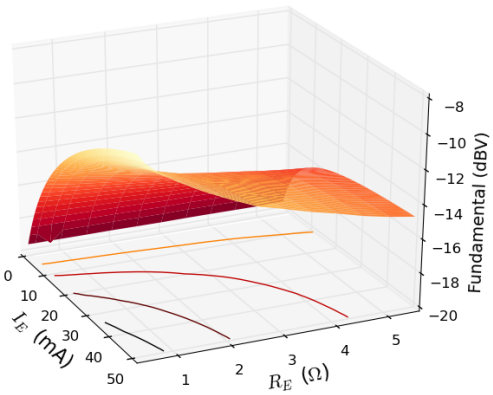
(b) Third-order output for R_M=5.6 Ω and I_M=20 mA



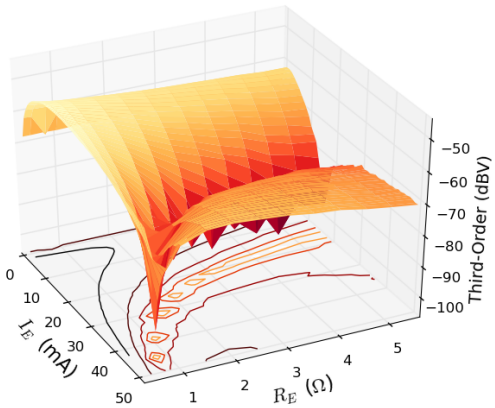
(c) Fundamental output for R_M=10.4 Ω and I_M=20 mA



(d) Third-order output for R_M=10.4 Ω and I_M=20 mA



(e) Fundamental output for R_M=15.2 Ω and I_M=20 mA



(f) Third-order output for R_M=15.2 Ω and I_M=20 mA

Figure 5.16: Measured experimental results of the Cascomp circuit's fundamental and third-order outputs.

In these measurements cancellation occurs at larger than expected values of R_M. Theory and simulation both predict cancellation loci will begin to appear at $I_E = 20\,\text{mA}$, at approximately $R_M = 3\,\Omega$. These measurements show cancellation still has not occurred when $R_M = 5.6\,\Omega$. This is attributed to the value of internal emitter resistances in the transistors used. The derived theory does not separate the internal versus the external emitter resistor contributions, but this should not affect the nulling effects and actual shape of the cancellation loci. Figs. 5.16a, 5.16c and 5.16e show improved overall fundamental gain at lower values of R_M which is to be expected. All of these surfaces follow theory showing further increased fundamental gain when R_E is low and I_E is high.

5.8.2 Verification of Optimisation Benefits

Estimates can be made as to how effective this optimisation of a Cascomp circuit will be. The exact increase in gain and IP3 is dependent on the technology used and the accuracy of fabricated emitter resistors and/or the parasitic base and emitter resistances of the specific transistor cell layout, as well as the circuit's bias variation with temperature and supply voltage. These are the factors that can shift third-order cancellation to different bias points if they have significant impact. As seen from the simulation and measurement plots, cancellation at smaller values of R_E is more sharply defined and variations that change the effective emitter resistance will move the bias point from the null.

Using the measurement data obtained, if a conventional Cascomp bias point is taken (the literature assumes I_M is about double I_E [73]) and is compared against a bias point chosen with a reasonably small R_E and large I_E, a measure of the achievable increase in gain and IP3 is obtained. Referring to the cases enumerated in Fig. 5.1, the 'Conventional' bias point is similar to that cited in the original literature, which has a large R_M and R_E. The 'New' bias point has taken the same R_M value as the 'Conventional' but with optimised R_E and I_E to obtain the best gain and IM3 null. The 'Optimised' bias point also varies R_M to an estimation of the best possible bias point for the Cascomp circuit derived from the foregoing theory. This is the proposed optimised bias point shown in a previous section. The example measurements suggest that this bias point will yield an improvement of 4 dB in gain and an increase of over 10 dBV in OIP3 in a practical situation.

Bias	R_M	R_E	I_E	**Gain (dB)**	**OIP3 (dBV)**
Conventional	15.2Ω	8.0Ω	20 mA	1.50	26.46
New	15.2Ω	2.0Ω	35 mA	2.02	30.18
Optimised	8.0Ω	4.1Ω	40 mA	5.78	38.95

Table 5.1: Comparison of bias points for a Cascomp at $I_M = 20\,\text{mA}$.

5.9 Conclusion

This chapter presents a novel analysis of a BJT Cascomp amplifier transfer function and identifies a bias point which yields gain and linearity benefits. Previous literature on the Cascomp circuit has suggested that the most effective bias point, in terms of gain and IP3, can be found by assuming its error amplifier is ideal. This work shows that when an ideal error amplifier is considered, the equations do not accurately represent the cancellation of distortion components contributed by the error amplifier. An improved nonlinear analysis of the Cascomp circuit is presented, including the non-linearity of the error amplifier. This analysis has identified a point of bifurcation in the conditions that allow an IM3 null. By analysing the theoretical IM3 coefficients of the non-ideal main and error amplifiers, theory suggested a more effective bias point at lower values of R_E where gain and IP3 are increased.

Simulation and measurements are presented confirming the theoretical analyses. By considering the plots of the measured variation in the optimum R_E and I_E values for a given $I_M - R_M$ point, the predicted gain and IP3 effects were observed. Since gain is increased in an amplifier with low degeneration and high bias current, we are able to find the IM3 null which is at optimum for these conditions. Using the predicted optimum bias values we can obtain an increase in gain of 4.3 dB and increase in OIP3 of 12.5 dBV compared with a traditional Cascomp circuit using the conventional bias point.

This work has revealed performance increases that would warrant further investigation by Agilent Technologies into developing a HBT Cascomp amplifier. With a large increase in the gain and linearity of the Cascomp amplifier through

the new nonlinearity analysis, the original motivation for this work has been fulfilled.

6

Conclusions and Future Work

Three works related to distortion reduction in bipolar transistor circuits have been presented in this thesis. Each one includes a novel mathematical proof describing circuit operation and is confirmed using simulations and measurements. Important aspects of these analyses result in some original circuit characteristics which have not appeared in the literature before. This chapter summarises the findings and explores potential future work in the author's opinion.

6.1 Third-Order Distortion Null

This chapter presented a theoretical description of a bipolar transistor's third-order distortion null. The analysis was extended to Darlington transistors which showed the nulling effect occurs at double the collector current. Data from simulations and measurements was gathered and proved consistent with that predicted by theory.

As discussed previously, third-order distortion nulling in single BJTs is not common practice in amplifier design because it occurs at inconvenient bias

currents. A Darlington null occurs at double the bias current compared to that of a single BJT. This opens the possibility for an amplifier which does not trade-off performance to achieve a third-order distortion reduction through this null. As previously justified in chapter 2, the models and distortion analyses used will transfer accurately to HBT device models that are operating below their input frequency compression point. Using HBTs would allow the work to be directly comparable to leading commercial products. A good example is the Agilent TC218 and HMMC5200 Power amplifiers [76, 77], both built using Darlington configurations. Optimisation of the Darlington configuration's emitter and ballast resistors could prove useful in further increasing the amplifier's performance.

High frequency analysis of this effect in both single and Darlington transistors is perhaps the most pertinent research to follow on from this work. Both device types require Volterra analysis applied with appropriate equivalent circuit models, in order to analyse how the third-order null changes with increasing frequency. The junction capacitors and device impedances would begin to factor into the nulling condition. In order for this work to be rigorous at high frequencies, a nulling condition accounting for these high frequency effects needs to be derived.

Another research path leading from this work is to analyse the nulling condition of Darlington transistor with an emitter shunt resistor, as discussed previously. As it stands, in low-distortion amplifiers a shunt resistor is almost always used to optimise the gain-bandwidth of the amplifier. Describing this shunt resistor's effect on a Darlington configuration and its inherent third-order null would allow a more rigorous prediction when attempting a practical application of the nulling effect.

As a final point-of-interest, Darlington transistors are not the only type of compound bipolar device. Sziklai pairs are one example of a different configuration. Another example would be the use of a collector to base feedback resistor between the Darlington's output and input terminals. Further configurations could be explored which may yield previously unknown characteristics.

6.2 Translinear Extraction

A circuit has been presented that can produce a bias current independent of temperature and series resistance in a bipolar device. The circuit inherently measures series resistance and adjusts the bias current accordingly. This circuit is used with a common-emitter amplifier such that the amplifier is biased in its third-order IM3 null, accounting for the BJT device's series resistance and operating temperature. This means that the amplifier is independent of the variables that might shift its bias current away from the null. Theoretical analysis of the circuit is provided, and simulations and measurements help confirm the operation of the translinear bias circuit.

Perhaps the most interesting phenomena in this circuit is its ability to measure series resistance of the BJT devices it contains. Foundries which operate semiconductor fabrication processes require methods of monitoring device parameters for each fabrication run. So called Process Control Monitors (PCMs) and pre-process measurements are used to do this. Typically, the stated parasitic resistances on a bipolar devices datasheet are vague because of absolute process variation. This technique for series resistance measurement could find some application as a monitor for semiconductor fabrication. Even general use in series resistance independent bias circuit design could be a useful contribution to the literature.

Now that a working bias circuit has been presented, a more rigorous evaluation of an amplifier using the inherent null for distortion reduction could be undertaken. This would have to tie back in with the work in chapter 3 and consider other things mentioned in the previous section (for instance, considering the common use of a shunt resistor in a Darlington configuration).

Finally, the translinear bias circuit's operation is based on a simplified method of operation. The structure of each stack is such that the application of the translinear principle is relatively straight-forward. While the presented bias circuit works well, considering the circuit topologies in other similar work [22], it appears a more elegant circuit topology could be found. For example, the work used a external resistor to measure the equilibrium current in each stack. The resistor presents an issue that it itself contributes to process variation error. A topology that removed this resistor would perhaps have better performance and

contribute less error into the output bias current.

6.3 Cascomp

This chapter has presented a new nonlinear analysis for the Cascomp topology. Previous analyses relied upon an assumption of high linearity in the error amplifier. The analysis revealed a characteristic in the third-order intermodulation distortion in a Cascomp amplifier that was previously masked by the assumption of an ideal error amplifier. The new theoretical analysis was confirmed with simulation and measurements. It was shown that this new characteristic can improve a Cascomp amplifier's IP3 and further analysis showed how this can be optimised for increased performance.

The literature does contain some FET implementations of the Cascomp circuit accompanied by measurements of IP3 [68, 69]. However, they are vague in terms of the theory behind a FET Cascomp amplifier and do not explore the characteristics as this work has. An interesting research path would be to replicate this work in FETs. Attempting to find similar characteristics using FET models could potentially yield similar optimisations to the topology as shown in this work. A theoretical analysis of a FET Cascomp has not been shown in the literature to the best of the author's knowledge.

Fabrication of an IC containing a Cascomp would give valuable results. Coupling this with the proposed optimisation in this work would yield an interesting result for comparison of the Cascomp amplifier with other similar amplifier topologies. The comparison would give an estimate of how impactful the proposed optimisations have been on a Cascomp amplifier's performance. Furthermore, this would give good measurements on the impact of process variations in a Cascomp. One could assess the proposed optimal bias point presented in this work and conclude on its usefulness in reducing the impact of process variation.

A

Series Expansion Coefficients

This appendix presents the well-known derivations of distortion components for single and two-tone input signals exciting a BJT's input junction. The transfer function used is the Ebers-Moll equation from Eq. 2.12 with the assumption that unity gain factor, $\alpha_f = 1$. This assumption is made for simplicity, and can be added into the final derivation at any point.

Single Tone Expansion

Here, the common derivation for a single tone input function exciting a generic transfer function is presented. Mathematica scripts were used to confirm all derivations[1].

[1]Overall, this work implemented some very complex derivations, so much so that hand derivations became near impossible (especially for the Cascomp work). Hence the author adopted the use of Mathematica scripts early on in the project. They clearly don't hold the same elegance that hand-typed latex derivations give but this was deemed a necessary evil by the author. All scripts can be copied or obtained from the author and run again for confirmation in Mathematica.

```
ClearAll["Global`*"]
ClearAll[Evaluate[$Context <> "*"]]
```

```
(*** Initial definition of a Maclaurin series expanding a function of x,
f[x], around zero. The f^n[0] terms are the series expansion coefficients. ***)
y = Series[f[x], {x, 0, 5}]
```

$$f[0] + f'[0]\,x + \frac{1}{2} f''[0]\,x^2 + \frac{1}{6} f^{(3)}[0]\,x^3 + \frac{1}{24} f^{(4)}[0]\,x^4 + \frac{1}{120} f^{(5)}[0]\,x^5 + O[x]^6$$

```
(*** Here we take the Ebers-
 Moll function and expand it using a Maclaurin series. ***)
y = Ic * Series[(Exp[v_IN / V_T]), {v_IN, 0, 5}]
```

$$Ic + \frac{Ic\,v_{IN}}{V_T} + \frac{Ic\,v_{IN}^2}{2\,V_T^2} + \frac{Ic\,v_{IN}^3}{6\,V_T^3} + \frac{Ic\,v_{IN}^4}{24\,V_T^4} + \frac{Ic\,v_{IN}^5}{120\,V_T^5} + O[v_{IN}]^6$$

```
(*** Applying a defined input signal to
 the Maclaurin series yeilds the following. ***)
v_IN = A * Cos[wt]
```

$$A\,Cos[wt]$$

```
y
```

$$Ic + \frac{Ic\,A\,Cos[wt]}{V_T} + \frac{Ic\,(A\,Cos[wt])^2}{2\,V_T^2} + \frac{Ic\,(A\,Cos[wt])^3}{6\,V_T^3} + \frac{Ic\,(A\,Cos[wt])^4}{24\,V_T^4} + \frac{Ic\,(A\,Cos[wt])^5}{120\,V_T^5} + O[A\,Cos[wt]]^6$$

```
(*** Analysing each order term individually and separating
 out the sinusoidal terms such that they are at multiples of the
 fundamental frequency. In order to better compare this with the
 generalised versions of the Maclaurin series of an amplifier
 (presented in Chapter 2) we simplify the above result. The factorial
 constant is factored out for each term (That is constants of 1, 1/2, 1/6,
  1/24, 1/120 for first-order through fifth-order respectively. ***)
```

$$\text{second} = \text{TrigReduce}\left[\frac{\text{Ic}\,(\text{A}\,\text{Cos}[\text{wt}])^2}{2\,\text{V}_\text{T}^2}\right]$$

$$\frac{\text{A}^2\,\text{Ic} + \text{A}^2\,\text{Ic}\,\text{Cos}[2\,\text{wt}]}{4\,\text{V}_\text{T}^2}$$

$$\text{third} = \text{TrigReduce}\left[\frac{\text{Ic}\,(\text{A}\,\text{Cos}[\text{wt}])^3}{6\,\text{V}_\text{T}^3}\right]$$

$$\frac{3\,\text{A}^3\,\text{Ic}\,\text{Cos}[\text{wt}] + \text{A}^3\,\text{Ic}\,\text{Cos}[3\,\text{wt}]}{24\,\text{V}_\text{T}^3}$$

$$\text{fourth} = \text{TrigReduce}\left[\frac{\text{Ic}\,(\text{A}\,\text{Cos}[\text{wt}])^4}{24\,\text{V}_\text{T}^4}\right]$$

$$\frac{3\,\text{A}^4\,\text{Ic} + 4\,\text{A}^4\,\text{Ic}\,\text{Cos}[2\,\text{wt}] + \text{A}^4\,\text{Ic}\,\text{Cos}[4\,\text{wt}]}{192\,\text{V}_\text{T}^4}$$

$$\text{fifth} = \text{TrigReduce}\left[\frac{\text{Ic}\,(\text{A}\,\text{Cos}[\text{wt}])^5}{120\,\text{V}_\text{T}^5}\right]$$

$$\frac{10\,\text{A}^5\,\text{Ic}\,\text{Cos}[\text{wt}] + 5\,\text{A}^5\,\text{Ic}\,\text{Cos}[3\,\text{wt}] + \text{A}^5\,\text{Ic}\,\text{Cos}[5\,\text{wt}]}{1920\,\text{V}_\text{T}^5}$$

(*** *Collecting terms into frequency bins.* ***)

```
total = Collect[
  Collect[Collect[Collect[Ic + (Ic A Cos[wt])/V_T + (A^2 Ic + A^2 Ic Cos[2 wt])/(4 V_T^2) +
       (3 A^3 Ic Cos[wt] + A^3 Ic Cos[3 wt])/(24 V_T^3) +
       (3 A^4 Ic + 4 A^4 Ic Cos[2 wt] + A^4 Ic Cos[4 wt])/(192 V_T^4) +
       (10 A^5 Ic Cos[wt] + 5 A^5 Ic Cos[3 wt] + A^5 Ic Cos[5 wt])/(1920 V_T^5),
     Cos[4 wt]], Cos[3 wt]], Cos[2 wt]], Cos[wt]]
```

$$Ic + \cos[3\,wt]\left(\frac{A^5\,Ic}{384\,V_T^5} + \frac{A^3\,Ic}{24\,V_T^3}\right) + \cos[2\,wt]\left(\frac{A^4\,Ic}{48\,V_T^4} + \frac{A^2\,Ic}{4\,V_T^2}\right) + \cos[wt]\left(\frac{A^5\,Ic}{192\,V_T^5} + \frac{A^3\,Ic}{8\,V_T^3} + \frac{A\,Ic}{V_T}\right) + \frac{A^5\,Ic\cos[5\,wt]}{1920\,V_T^5} + \frac{A^4\,Ic}{64\,V_T^4} + \frac{A^4\,Ic\cos[4\,wt]}{192\,V_T^4} + \frac{A^2\,Ic}{4\,V_T^2}$$

```
(*** Final equation with the separated terms. This shows the fully expanded
  collection of series coefficients in front of each frequency term. ***)
y = (Ic + (Ic A^4)/(40 V_T^4) + (Ic A^2)/(4 V_T^2)) + ((Ic A^5)/(192 V_T^5) + (Ic A^3)/(8 V_T^3) + (Ic A)/V_T) Cos[wt] +
  ((Ic A^2)/(4 V_T^2) + (Ic A^4)/(48 V_T^4)) Cos[2 wt] + ((Ic A^3)/(24 V_T^3) + (Ic A^5)/(384 V_T^5)) Cos[3 wt] +
  ((Ic A^4)/(192 V_T^4)) Cos[4 wt] + ((Ic A^5)/(1920 V_T^5)) Cos[5 wt]
```

```
(*** These can be made to match
   generalised terms (such as those in Equation 2.6)
   by factoring out the nth-order factorial term. ***)
DC_ = (Ic + (Ic A^4)/(40 V_T^4) + (Ic A^2)/(4 V_T^2))
```

$$\text{fundamental\_} = \left(\frac{\text{Ic}\,A^5}{192\,V_T^5} + \frac{\text{Ic}\,A^3}{8\,V_T^3} + \frac{\text{Ic}\,A}{V_T}\right)\text{Cos}[\text{wt}]$$

$$\text{second\_order} = \left(\frac{\text{Ic}\,A^2}{4\,V_T^2} + \frac{\text{Ic}\,A^4}{48\,V_T^4}\right)\text{Cos}[2\,\text{wt}]$$

$$\text{third\_order} = \left(\frac{\text{Ic}\,A^3}{24\,V_T^3} + \frac{\text{Ic}\,A^5}{384\,V_T^5}\right)\text{Cos}[3\,\text{wt}]$$

$$\text{fourth\_order} = \left(\frac{\text{Ic}\,A^4}{192\,V_T^4}\right)\text{Cos}[4\,\text{wt}]$$

$$\text{fifth\_order} = \left(\frac{\text{Ic}\,A^5}{1920\,V_T^5}\right)\text{Cos}[5\,\text{wt}]$$

Two Tone Expansion

Here, the common derivation for a two tone input function exciting a generic transfer function is presented. Mathematica scripts were used to confirm all derivations.

```
ClearAll["Global`*"]
ClearAll[Evaluate[$Context <> "*"]]
```

```
(*** Initial definition of a Maclaurin series expanding a function of x,
f[x], around zero. The f^n[0] terms are the series expansion coefficients. ***)
y = Series[f[x], {x, 0, 5}]
```

$$f[0] + f'[0]\,x + \frac{1}{2} f''[0]\,x^2 + \frac{1}{6} f^{(3)}[0]\,x^3 + \frac{1}{24} f^{(4)}[0]\,x^4 + \frac{1}{120} f^{(5)}[0]\,x^5 + O[x]^6$$

```
(*** Here we take the Ebers-
 Moll function and expand it using a Maclaurin series. ***)
y = Ic * Series[(Exp[V_IN / V_T]), {V_IN, 0, 5}]
```

$$Ic + \frac{Ic\,V_{IN}}{V_T} + \frac{Ic\,V_{IN}^2}{2\,V_T^2} + \frac{Ic\,V_{IN}^3}{6\,V_T^3} + \frac{Ic\,V_{IN}^4}{24\,V_T^4} + \frac{Ic\,V_{IN}^5}{120\,V_T^5} + O[V_{IN}]^6$$

```
(*** Applying a defined input signal to the Ebers-Moll model and expanding it
  using a Maclaurin series. The input signal have amplitude A_1 and A_2,
and frequencies w_1 and w_2 respectively. ***)
```

$$f[0] + f'[0]\,x + \frac{1}{2} f''[0]\,x^2 + \frac{1}{6} f^{(3)}[0]\,x^3 + \frac{1}{24} f^{(4)}[0]\,x^4 + \frac{1}{120} f^{(5)}[0]\,x^5 + O[x]^6$$

```
V_IN = A_1 * Cos[w_1 t] + A_2 * Cos[w_2 t]
Cos[t w_1] A_1 + Cos[t w_2] A_2
```

```
y
```

$$Ic + \frac{Ic\,(Cos[t\,w_1]\,A_1 + Cos[t\,w_2]\,A_2)}{V_T} + \frac{Ic\,(Cos[t\,w_1]\,A_1 + Cos[t\,w_2]\,A_2)^2}{2\,V_T^2} +$$
$$\frac{Ic\,(Cos[t\,w_1]\,A_1 + Cos[t\,w_2]\,A_2)^3}{6\,V_T^3} + \frac{Ic\,(Cos[t\,w_1]\,A_1 + Cos[t\,w_2]\,A_2)^4}{24\,V_T^4} +$$
$$\frac{Ic\,(Cos[t\,w_1]\,A_1 + Cos[t\,w_2]\,A_2)^5}{120\,V_T^5} + O[Cos[t\,w_1]\,A_1 + Cos[t\,w_2]\,A_2]^6$$

```
(*** Analysing each order term individually and separating
 out the sinusoidal terms such that they  are at multiples of the
 fundamental frequency. In order to better compare this with the
 generalised versions of the Maclaurin series of an amplifier
 (presented in Chapter 2) we simplify the above result. The factorial
 constant is factored out for each term (That is constants of 1, 1/2, 1/6,
  1/24, 1/120 for first-order through fifth-order respectively. ***)
```

```
second = TrigReduce[ Ic (Cos[t w1] A1 + Cos[t w2] A2)^2 / (2 V_T^2) ]
```

$$\frac{1}{4\,V_T^2}\left(Ic\,A_1^2 + Ic\,Cos[2\,t\,w_1]\,A_1^2 + 2\,Ic\,Cos[t\,w_1 - t\,w_2]\,A_1\,A_2 + 2\,Ic\,Cos[t\,w_1 + t\,w_2]\,A_1\,A_2 + Ic\,A_2^2 + Ic\,Cos[2\,t\,w_2]\,A_2^2\right)$$

```
third = TrigReduce[ Ic (Cos[t w1] A1 + Cos[t w2] A2)^3 / (6 V_T^3) ]
```

$$\frac{1}{24\,V_T^3}\left(3\,Ic\,Cos[t\,w_1]\,A_1^3 + Ic\,Cos[3\,t\,w_1]\,A_1^3 + 6\,Ic\,Cos[t\,w_2]\,A_1^2\,A_2 + 3\,Ic\,Cos[2\,t\,w_1 - t\,w_2]\,A_1^2\,A_2 + 3\,Ic\,Cos[2\,t\,w_1 + t\,w_2]\,A_1^2\,A_2 + 6\,Ic\,Cos[t\,w_1]\,A_1\,A_2^2 + 3\,Ic\,Cos[t\,w_1 - 2\,t\,w_2]\,A_1\,A_2^2 + 3\,Ic\,Cos[t\,w_1 + 2\,t\,w_2]\,A_1\,A_2^2 + 3\,Ic\,Cos[t\,w_2]\,A_2^3 + Ic\,Cos[3\,t\,w_2]\,A_2^3\right)$$

$$\text{fourth} = \text{TrigReduce}\left[\frac{\text{Ic}\,(\text{Cos}[t\,w_1]\,A_1 + \text{Cos}[t\,w_2]\,A_2)^4}{24\,V_T^4}\right]$$

$$\frac{1}{24\,V_T^4}\left(\frac{3\,\text{Ic}\,A_1^4}{8} + \frac{1}{2}\,\text{Ic}\,\text{Cos}[2\,t\,w_1]\,A_1^4 + \frac{1}{8}\,\text{Ic}\,\text{Cos}[4\,t\,w_1]\,A_1^4 + \right.$$
$$\frac{3}{2}\,\text{Ic}\,\text{Cos}[t\,w_1 - t\,w_2]\,A_1^3\,A_2 + \frac{1}{2}\,\text{Ic}\,\text{Cos}[3\,t\,w_1 - t\,w_2]\,A_1^3\,A_2 +$$
$$\frac{3}{2}\,\text{Ic}\,\text{Cos}[t\,w_1 + t\,w_2]\,A_1^3\,A_2 + \frac{1}{2}\,\text{Ic}\,\text{Cos}[3\,t\,w_1 + t\,w_2]\,A_1^3\,A_2 +$$
$$\frac{3}{2}\,\text{Ic}\,A_1^2\,A_2^2 + \frac{3}{2}\,\text{Ic}\,\text{Cos}[2\,t\,w_1]\,A_1^2\,A_2^2 + \frac{3}{2}\,\text{Ic}\,\text{Cos}[2\,t\,w_2]\,A_1^2\,A_2^2 +$$
$$\frac{3}{4}\,\text{Ic}\,\text{Cos}[2\,t\,w_1 - 2\,t\,w_2]\,A_1^2\,A_2^2 + \frac{3}{4}\,\text{Ic}\,\text{Cos}[2\,t\,w_1 + 2\,t\,w_2]\,A_1^2\,A_2^2 +$$
$$\frac{1}{2}\,\text{Ic}\,\text{Cos}[t\,w_1 - 3\,t\,w_2]\,A_1\,A_2^3 + \frac{3}{2}\,\text{Ic}\,\text{Cos}[t\,w_1 - t\,w_2]\,A_1\,A_2^3 +$$
$$\frac{3}{2}\,\text{Ic}\,\text{Cos}[t\,w_1 + t\,w_2]\,A_1\,A_2^3 + \frac{1}{2}\,\text{Ic}\,\text{Cos}[t\,w_1 + 3\,t\,w_2]\,A_1\,A_2^3 +$$
$$\left.\frac{3\,\text{Ic}\,A_2^4}{8} + \frac{1}{2}\,\text{Ic}\,\text{Cos}[2\,t\,w_2]\,A_2^4 + \frac{1}{8}\,\text{Ic}\,\text{Cos}[4\,t\,w_2]\,A_2^4\right)$$

$$\text{fifth} = \text{TrigReduce}\left[\frac{\text{Ic}\,(\text{Cos}[t\,w_1]\,A_1 + \text{Cos}[t\,w_2]\,A_2)^5}{120\,V_T^5}\right]$$

$$\begin{aligned}
&\frac{1}{120\,V_T^5}\left(\frac{5}{8}\,\text{Ic}\,\text{Cos}[t\,w_1]\,A_1^5 + \frac{5}{16}\,\text{Ic}\,\text{Cos}[3\,t\,w_1]\,A_1^5 + \frac{1}{16}\,\text{Ic}\,\text{Cos}[5\,t\,w_1]\,A_1^5 +\right.\\
&\quad\frac{15}{8}\,\text{Ic}\,\text{Cos}[t\,w_2]\,A_1^4\,A_2 + \frac{5}{4}\,\text{Ic}\,\text{Cos}[2\,t\,w_1 - t\,w_2]\,A_1^4\,A_2 +\\
&\quad\frac{5}{16}\,\text{Ic}\,\text{Cos}[4\,t\,w_1 - t\,w_2]\,A_1^4\,A_2 + \frac{5}{4}\,\text{Ic}\,\text{Cos}[2\,t\,w_1 + t\,w_2]\,A_1^4\,A_2 +\\
&\quad\frac{5}{16}\,\text{Ic}\,\text{Cos}[4\,t\,w_1 + t\,w_2]\,A_1^4\,A_2 + \frac{15}{4}\,\text{Ic}\,\text{Cos}[t\,w_1]\,A_1^3\,A_2^2 +\\
&\quad\frac{5}{4}\,\text{Ic}\,\text{Cos}[3\,t\,w_1]\,A_1^3\,A_2^2 + \frac{15}{8}\,\text{Ic}\,\text{Cos}[t\,w_1 - 2\,t\,w_2]\,A_1^3\,A_2^2 +\\
&\quad\frac{5}{8}\,\text{Ic}\,\text{Cos}[3\,t\,w_1 - 2\,t\,w_2]\,A_1^3\,A_2^2 + \frac{15}{8}\,\text{Ic}\,\text{Cos}[t\,w_1 + 2\,t\,w_2]\,A_1^3\,A_2^2 +\\
&\quad\frac{5}{8}\,\text{Ic}\,\text{Cos}[3\,t\,w_1 + 2\,t\,w_2]\,A_1^3\,A_2^2 + \frac{15}{4}\,\text{Ic}\,\text{Cos}[t\,w_2]\,A_1^2\,A_2^3 +\\
&\quad\frac{5}{4}\,\text{Ic}\,\text{Cos}[3\,t\,w_2]\,A_1^2\,A_2^3 + \frac{5}{8}\,\text{Ic}\,\text{Cos}[2\,t\,w_1 - 3\,t\,w_2]\,A_1^2\,A_2^3 +\\
&\quad\frac{15}{8}\,\text{Ic}\,\text{Cos}[2\,t\,w_1 - t\,w_2]\,A_1^2\,A_2^3 + \frac{15}{8}\,\text{Ic}\,\text{Cos}[2\,t\,w_1 + t\,w_2]\,A_1^2\,A_2^3 +\\
&\quad\frac{5}{8}\,\text{Ic}\,\text{Cos}[2\,t\,w_1 + 3\,t\,w_2]\,A_1^2\,A_2^3 + \frac{15}{8}\,\text{Ic}\,\text{Cos}[t\,w_1]\,A_1\,A_2^4 +\\
&\quad\frac{5}{16}\,\text{Ic}\,\text{Cos}[t\,w_1 - 4\,t\,w_2]\,A_1\,A_2^4 + \frac{5}{4}\,\text{Ic}\,\text{Cos}[t\,w_1 - 2\,t\,w_2]\,A_1\,A_2^4 +\\
&\quad\frac{5}{4}\,\text{Ic}\,\text{Cos}[t\,w_1 + 2\,t\,w_2]\,A_1\,A_2^4 + \frac{5}{16}\,\text{Ic}\,\text{Cos}[t\,w_1 + 4\,t\,w_2]\,A_1\,A_2^4 +\\
&\quad\left.\frac{5}{8}\,\text{Ic}\,\text{Cos}[t\,w_2]\,A_2^5 + \frac{5}{16}\,\text{Ic}\,\text{Cos}[3\,t\,w_2]\,A_2^5 + \frac{1}{16}\,\text{Ic}\,\text{Cos}[5\,t\,w_2]\,A_2^5\right)
\end{aligned}$$

```
(*** Collecting terms into frequency bins. For obvious
 reasons this is trucated to the third order. However the same
 process could be followed to find higher order components. ***)
```

$$\text{total} = \text{Collect}\left[\text{Ic} + \frac{\text{Ic}\,(\text{Cos}[t\,w_1]\,A_1 + \text{Cos}[t\,w_2]\,A_2)}{V_T} + \text{second} + \text{third},\ \text{Cos}[t\,w_2]\right]$$

$$\text{Ic} + \text{Cos}[t\,w_2]\left(\frac{\text{Ic}\,A_1^2\,A_2}{4\,V_T^3} + \frac{\text{Ic}\,A_2^3}{8\,V_T^3} + \frac{\text{Ic}\,A_2}{V_T}\right) + \frac{\text{Ic}\,\text{Cos}[t\,w_1]\,A_1^3}{8\,V_T^3} + \frac{\text{Ic}\,\text{Cos}[3\,t\,w_1]\,A_1^3}{24\,V_T^3} +$$

$$\frac{\text{Ic}\,\text{Cos}[2\,t\,w_1 - t\,w_2]\,A_1^2\,A_2}{8\,V_T^3} + \frac{\text{Ic}\,\text{Cos}[2\,t\,w_1 + t\,w_2]\,A_1^2\,A_2}{8\,V_T^3} + \frac{\text{Ic}\,\text{Cos}[t\,w_1]\,A_1\,A_2^2}{4\,V_T^3} +$$

$$\frac{\text{Ic}\,\text{Cos}[t\,w_1 - 2\,t\,w_2]\,A_1\,A_2^2}{8\,V_T^3} + \frac{\text{Ic}\,\text{Cos}[t\,w_1 + 2\,t\,w_2]\,A_1\,A_2^2}{8\,V_T^3} + \frac{\text{Ic}\,\text{Cos}[3\,t\,w_2]\,A_2^3}{24\,V_T^3} +$$

$$\frac{1}{4\,V_T^2}\left(\text{Ic}\,A_1^2 + \text{Ic}\,\text{Cos}[2\,t\,w_1]\,A_1^2 + 2\,\text{Ic}\,\text{Cos}[t\,w_1 - t\,w_2]\,A_1\,A_2 + \right.$$

$$\left. 2\,\text{Ic}\,\text{Cos}[t\,w_1 + t\,w_2]\,A_1\,A_2 + \text{Ic}\,A_2^2 + \text{Ic}\,\text{Cos}[2\,t\,w_2]\,A_2^2\right) + \frac{\text{Ic}\,\text{Cos}[t\,w_1]\,A_1}{V_T}$$

(*** *The harmonic content is separated from the intermodulation content by grouping and collecting terms using the above equation and varying the second parameter for the frequency component of interest. One final simplification is made that* $A = A_1 = A_2$. ***)

(*** *HARMONICS* ***)

$$\text{fundamental\_w1} = \left(\frac{\text{Ic}\,A}{V_T} + \frac{3\,\text{Ic}\,A^3}{8\,V_T^3}\right)\text{Cos}[t\,w_1]$$

$$\text{fundamental\_w2} = \left(\frac{\text{Ic}\,A}{V_T} + \frac{3\,\text{Ic}\,A^3}{8\,V_T^3}\right)\text{Cos}[t\,w_2]$$

$$\text{second\_w1} = \left(\frac{\text{Ic}\,A^2}{4\,V_T^2}\right)\text{Cos}[2\,t\,w_1]$$

$$\text{second\_w2} = \left(\frac{\text{Ic}\,A^2}{4\,V_T^2}\right)\text{Cos}[2\,t\,w_2]$$

$$\text{third\_w1} = \left(\frac{\text{Ic}\,A^3}{24\,V_T^3}\right)\text{Cos}[3\,t\,w_1]$$

$$\text{third\_w2} = \left(\frac{\text{Ic}\,A^3}{24\,V_T^3}\right)\text{Cos}[3\,t\,w_2]$$

(*** INTERMODULATION ***)

$$w1 + w2 = \left(\frac{Ic\, A^2}{2\, V_T^2}\right) \mathrm{Cos}[t\, w_1 + t\, w_2]$$

$$w1 - w2 = \left(\frac{Ic\, A^2}{2\, V_T^2}\right) \mathrm{Cos}[t\, w_1 - t\, w_2]$$

$$2\, w1 + w2 = \left(\frac{Ic\, A^3}{8\, V_T^3}\right) \mathrm{Cos}[2\, t\, w_1 + t\, w_2]$$

$$2\, w1 - w2 = \left(\frac{Ic\, A^3}{8\, V_T^3}\right) \mathrm{Cos}[2\, t\, w_1 - t\, w_2]$$

$$w1 + 2\, w2 = \left(\frac{Ic\, A^3}{8\, V_T^3}\right) \mathrm{Cos}[t\, w_1 + 2\, t\, w_2]$$

$$w1 - 2\, w2 = \left(\frac{Ic\, A^3}{8\, V_T^3}\right) \mathrm{Cos}[t\, w_1 - 2\, t\, w_2]$$

```
(*** These can be made to match generalised terms (such as those in Figure 2.2)
  by factoring out the nth-order factorial term. ***)
```

B

Transistor Nulling Derivations

This appendix presents the derivations for inherent nulling of third-order distortion in different transistor configurations. Overall, this work implemented some very complex derivations, so much so that hand derivations became near impossible (especially for the Cascomp work). Hence the author adopted the use of Mathematica scripts early on in the project. They clearly don't hold the same elegance that hand-typed latex derivations give but this was deemed a necessary evil by the author. All scripts can be copied or obtained from the author and run again for confirmation in Mathematica.

Single BJT Third-Order Null

Using the configuration in Chapter 2 (presented again below), the full mathematical derivation for a Single BJT amplifier is found. A Mathematica script is again used to present the derivation.

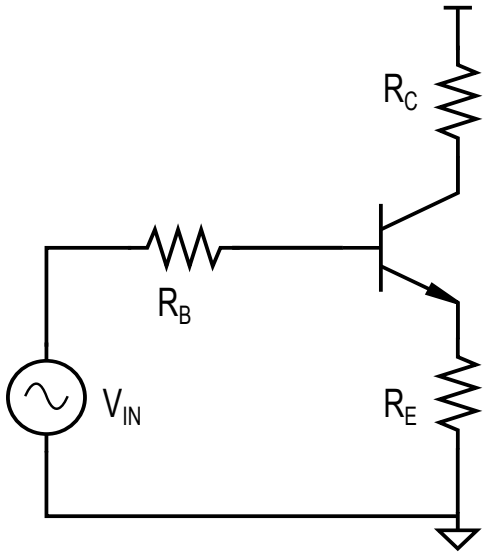


Figure B.1: A typical single BJT transistor common-emitter amplifier used for transfer analysis. Each shown resistor is the total combination of internal and external resistances.

```
Remove["Global`*"]
```

```
(*** Using the Equivalent model of a Single BJT (as shown in Chapter 2)
 we apply Kirchoff's voltage law on the input loop of the
 amplifier. b1 is the current gain for the device. Vbe is the  ***)
```

In[17]:=
```
VIN = VBE + IC * (RE + ((RE + RB) / b1) )
```

Out[17]=
$$IC\left(RE + \frac{RB + RE}{b1}\right) + VBE$$

```
(*** This form allows the substitutioin of the first bracketed term for a
 constant REE. This is the series resistance for this Single BJT circuit. ***)
```

In[3]:=
```
REE = (RE + (RB + RE) / b1)
```

Out[3]=
$$RE + \frac{RB + RE}{b1}$$

```
(*** Therefore,
one can simply state the following as the transfer function for the Single
  BJT amplifier. Also including is the substitution of VBE for the Ebers-
 Moll equation describing the voltage across the transistor junction. ***)
```

In[4]:=
```
VIN = IC2 * REE + VT * Log[IC / IS]
```

```
(*** Further simplifications are made to make
 the derivations of the series coefficients tidy. ***)
```

```
W = VIN / VT
X = IC / IS
F = (IS * REE) / VT

W = FX + Log[X]
```

```
(*** First derivative of W with respect to X. ***)
```

In[5]:=
```
D[W = F * X + Log[X] , X]
```

Out[5]=
$$F + \frac{1}{X}$$

```
(*** We are interested in transconductance terms in our resulting coefficients,
so the first derivative is inverted such that it has the form of Current over
 Voltage (dW/dF becomes dF/dW). This gives the first gain coefficient. ***)
```

In[6]:=
```
1 / (F + 1/X)
```

Out[6]=
$$\frac{1}{F + \frac{1}{X}}$$

```
(*** Second derivative gives the second order
 term. Note the chain rule needs to be applied. ***)
```

In[8]:=
```
D[1/(F + 1/X), X]
```

Out[8]=
$$\frac{1}{\left(F + \frac{1}{X}\right)^2 X^2}$$

```
(*** Application of the chain rule ***)
```

In[11]:=
```
(1/(F + 1/X)^2 X^2) * (1/(F + 1/X))
```

Out[11]=
$$\frac{1}{\left(F + \frac{1}{X}\right)^3 X^2}$$

```
(*** Simplifying results in the second-order term ***)
```

In[12]:=
```
Simplify[1/(F + 1/X)^3 X^2]
```

Out[12]=
$$\frac{X}{(1 + F X)^3}$$

```
(*** The same process is applied again. Derivation of the final second-
  order term → Apply chain rule → simplify. ***)
```

In[13]:=
```
D[X/(1 + F X)^3, X]
```

Out[13]=
$$-\frac{3 F X}{(1 + F X)^4} + \frac{1}{(1 + F X)^3}$$

```
(*** Application of the chain rule. ***)
```

In[14]:=
$$\left(-\frac{3\,F\,X}{(1+F\,X)^4}+\frac{1}{(1+F\,X)^3}\right)*\left(\frac{1}{F+\frac{1}{X}}\right)$$

Out[14]=
$$\frac{-\frac{3\,F\,X}{(1+F\,X)^4}+\frac{1}{(1+F\,X)^3}}{F+\frac{1}{X}}$$

(*** *Simplifying.* ***)

In[15]:=
$$\text{Simplify}\left[\frac{-\frac{3\,F\,X}{(1+F\,X)^4}+\frac{1}{(1+F\,X)^3}}{F+\frac{1}{X}}\right]$$

Out[15]=
$$\frac{X-2\,F\,X^2}{(1+F\,X)^5}$$

(*** *Summary of the coefficients.* ***)

$$\text{First} = \frac{1}{F+\frac{1}{X}}$$

$$\text{Second} = \frac{X}{(1+F\,X)^3}$$

$$\text{Third} = \frac{X-2\,F\,X^2}{(1+F\,X)^5}$$

Darlington Third-Order Null

Using the configuration in Chapter 2 (presented again below), the full mathematical derivation for a Darlington pair without a flushout resistor is found. A Mathematica script is again used to present the derivation.

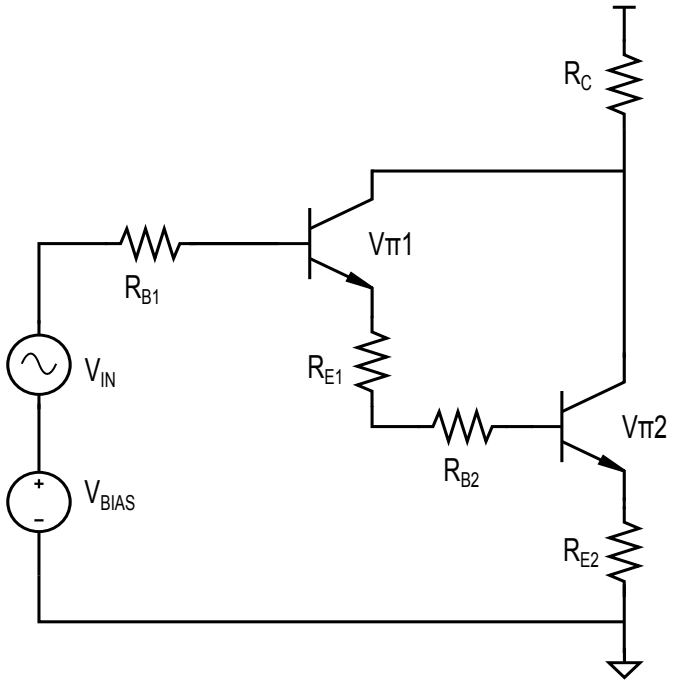


Figure B.2: Typical single Darlington transistor amplifier circuit used for small signal analysis. Each shown resistor is the total combination of internal and external resistances.

In[1]:=
```
Remove["Global`*"]
```
```
Remove::rmnsm : There are no symbols matching "Global`*". >>
```

```
(*** Using the equivalent model of a Darlington pair (as shown in Chapter 2)
 we apply Kirchoff's voltage law on the input loop of the
 amplifier. b1 and b2 are the current gains for each device. ***)
```

```
VIN = VBE1 + VBE2 + (IC2 + IB2) * RE2 +
  IB2 * RB2 + IC1 * (1 + 1 / b1) * RE1 + (IC1 / b1) * RB1
```

$$\frac{IC1\ RB1}{b1} + IB2\ RB2 + \left(1 + \frac{1}{b1}\right) IC1\ RE1 + (IB2 + IC2)\ RE2 + VBE1 + VBE2$$

```
(*** The definitions of each of the currents are listed below,
decribing the currents in the transistors Q1 and Q2. ***)
```

```
IB2 = IC1 + IC1 / b1
IB2 = IC2 / b2
IC = IC1 + IC2
```

```
(*** Using these three equations,
one can rearrange and state the following ***)
```

```
IC2 / b2 = IC1 (1 + 1 / b1)
IC1 = (IC2) / (b2 + b2 / b1)
IC = (IC2) / (b2 + b2 / b1) + IC2    (** IC in terms of IC2 **)
IC = IC1 + IC1 * (b2 + b2 / b1)      (** IC in terms of IC1 **)
```

In[2]:=
```
Reduce[IC == (IC2) / (b2 + b2 / b1) + IC2 , IC2]
```

Out[3]=
$$IC2 == \frac{(1 + b1)\ b2\ IC}{b1 + b2 + b1\ b2}$$

In[7]:=
```
Reduce[IC == IC1 + IC1 * (b2 + b2 / b1) , IC1]
```

Out[9]=
$$IC1 == \frac{b1\ IC}{b1 + b2 + b1\ b2}$$

```
(*** These equations can be replaced into the original
 input loop to make VIN depedant on only one current, IC,
which is the main collector current in the Darlington ***)
```

```
VIN = VBE1 + VBE2 + (IC2 + IB2) * RE2 +
  IB2 * RB2 + IC1 * (1 + 1 / b1) * RE1 + (IC1 / b1) * RB1
```

In[10]:=
```
VIN = VBE1 + VBE2 + (((1 + b1) b2 IC)/(b1 + b2 + b1 b2) + ((1 + b1) b2 IC)/(b1 + b2 + b1 b2) * (1 / b2)) * RE2 +
  (((1 + b1) b2 IC)/(b1 + b2 + b1 b2) * (1 / b2)) * RB2 + ((b1 IC)/(b1 + b2 + b1 b2)) * (1 + 1 / b1) * RE1 + (((b1 IC)/(b1 + b2 + b1 b2))/ b1) * RB1
```

Out[10]=
$$\frac{\text{IC RB1}}{\text{b1} + \text{b2} + \text{b1 b2}} + \frac{(1 + \text{b1})\ \text{IC RB2}}{\text{b1} + \text{b2} + \text{b1 b2}} + \frac{\left(1 + \frac{1}{\text{b1}}\right)\ \text{b1 IC RE1}}{\text{b1} + \text{b2} + \text{b1 b2}} + \left(\frac{(1 + \text{b1})\ \text{IC}}{\text{b1} + \text{b2} + \text{b1 b2}} + \frac{(1 + \text{b1})\ \text{b2 IC}}{\text{b1} + \text{b2} + \text{b1 b2}}\right) \text{RE2} + \text{VBE1} + \text{VBE2}$$

(*** *We simplify by collecting the collector current terms and reducing the beta terms.* ***)

In[13]:=
```
Collect[IC RB1/(b1 + b2 + b1 b2) + ((1 + b1) IC RB2)/(b1 + b2 + b1 b2) +
  ((1 + 1/b1) b1 IC RE1)/(b1 + b2 + b1 b2) + ((1 + b1) IC/(b1 + b2 + b1 b2) + ((1 + b1) b2 IC)/(b1 + b2 + b1 b2)) RE2 + VBE1 + VBE2, IC]
```

Out[13]=
$$\text{IC}\left(\frac{\text{RB1}}{\text{b1} + \text{b2} + \text{b1 b2}} + \frac{(1 + \text{b1})\ \text{RB2}}{\text{b1} + \text{b2} + \text{b1 b2}} + \frac{\left(1 + \frac{1}{\text{b1}}\right)\ \text{b1 RE1}}{\text{b1} + \text{b2} + \text{b1 b2}} + \frac{(1 + \text{b1})\ \text{RE2}}{\text{b1} + \text{b2} + \text{b1 b2}} + \frac{(1 + \text{b1})\ \text{b2 RE2}}{\text{b1} + \text{b2} + \text{b1 b2}}\right) + \text{VBE1} + \text{VBE2}$$

(*** *By further simplifying the bracketed term this equation gives the series resistance of the Darlington amplifier.* ***)

In[18]:=
```
Simplify[RB1/(b1 + b2 + b1 b2) + ((1 + b1) RB2)/(b1 + b2 + b1 b2) + ((1 + 1/b1) b1 RE1)/(b1 + b2 + b1 b2) + ((1 + b1) RE2)/(b1 + b2 + b1 b2) + ((1 + b1) b2 RE2)/(b1 + b2 + b1 b2)]
```

Out[18]=
$$\frac{\text{RB1} + (1 + \text{b1})\ (\text{RB2} + \text{RE1} + \text{RE2} + \text{b2 RE2})}{\text{b1} + \text{b2} + \text{b1 b2}}$$

```
REE = (RB1 + (1 + b1) (RB2 + RE1 + RE2 + b2 RE2))/(b1 + b2 + b1 b2)
```

(*** *Therefore, one can simply state the following as the transfer function for the Darlington.* ***)

In[19]:=
```
VIN = IC REE + VBE1 + VBE2
```

Out[19]=
$$\text{IC REE} + \text{VBE1} + \text{VBE2}$$

(*** *Introducing the Ebers-Moll equations for the base-emitter junction also introduces different currents IC1 and IC2. This needs to be simplified to contain only IC terms again using the same process.* ***)

In[20]:=
```
VIN = IC * REE + VT * Log[IC1 / IS] + VT * Log[IC2 / IS]
```

Out[20]=
$$\text{IC REE} + \text{VT Log}\left[\frac{\text{IC1}}{\text{IS}}\right] + \text{VT Log}\left[\frac{\text{IC2}}{\text{IS}}\right]$$

In[21]:=

$$\mathbf{VIN = IC * REE + VT * Log\left[\frac{b1\ IC}{b1 + b2 + b1\ b2} \Big/ IS\right] + VT * Log\left[\frac{(1 + b1)\ b2\ IC}{b1 + b2 + b1\ b2} \Big/ IS\right]}$$

Out[21]=

$$\mathrm{IC\ REE + VT\ Log\left[\frac{b1\ IC}{(b1 + b2 + b1\ b2)\ IS}\right] + VT\ Log\left[\frac{(1 + b1)\ b2\ IC}{(b1 + b2 + b1\ b2)\ IS}\right]}$$

$$\mathbf{a1 = \frac{b1}{(b1 + b2 + b1\ b2)}}$$

$$\mathbf{a2 = \frac{(1 + b1)\ b2}{(b1 + b2 + b1\ b2)}}$$

(*** *We see that each logarithmic term has different constants contained inside. We use fundamental logarithmic identities to seperate out the constant portion as its own constant term in the transfer function.* ***)

$$\mathbf{VT\ Log\left[\frac{a1 * IC}{IS}\right] + VT\ Log\left[\frac{a2 * IC}{IS}\right]}$$

$$\mathbf{VT\ Log\left[\frac{IC}{IS}\right] + VT\ Log\left[\frac{IC}{IS}\right] + VT\ Log[a1] + VT\ Log[a2]}$$

$$\mathbf{VT\ Log\left[\frac{IC}{IS}\right] + VT\ Log\left[\frac{IC}{IS}\right] + VT\ Log[a1 * a2]}$$

In[30]:=

$$\mathbf{Simplify\left[\left(\frac{b1}{(b1 + b2 + b1\ b2)}\right) * \left(\frac{(1 + b1)\ b2}{(b1 + b2 + b1\ b2)}\right)\right]}$$

Out[30]=

$$\mathrm{\frac{b1\ (1 + b1)\ b2}{(b1 + b2 + b1\ b2)^2}}$$

$$\mathbf{C = VT\ Log\left[\frac{b1\ (1 + b1)\ b2}{(b1 + b2 + b1\ b2)^2}\right]}$$

(*** *Finally, this results in a transfer function which is a function of only one current IC. A simple application of a series expansion is now possible.* ***)

In[31]:=
```
VIN = IC * REE + VT * Log[IC / IS] + VT * Log[IC / IS] + C
```

Out[31]=
$$C + IC\ REE + 2\ VT\ Log\left[\frac{IC}{IS}\right]$$

```
(*** Further simplifications are made to make
 the derivations of the series coefficients tidy. ***)
W = VIN / VT
X = IC / IS
F = (IS * REE) / VT
C = Log[a1 * a2] / VT

W = FX + Log[X^2] + C

(*** First derivative of W with respect to X. ***)
D[W = F * X + Log[X^2] + C, X]
```

$$F + \frac{2}{X}$$

```
(*** We are interested in transconductance terms in our resulting coefficients,
so the first derivative is inverted such that it has
 the form of Current over Votlage (dW/dF becomes dF/dW). ***)
1 / (F + 2 / X)
```

$$\frac{1}{F + \frac{2}{X}}$$

```
(*** Simplifying results in the first order transconductance term,
which is the same thing as our first order gain coefficient. ***)

Simplify[1 / (F + 2 / X)]
```

$$\frac{X}{2 + F\ X}$$

```
(*** Second derivative gives the second order
 term. Note the chian rule needs to be applied. ***)
```

```
D[X/(2 + F X), X]
```

$$-\frac{F X}{(2+F X)^2}+\frac{1}{2+F X}$$

```
(*** Application of the Chain rule ***)
```

```
(-F X/(2 + F X)^2 + 1/(2 + F X)) * (1/(F + 2/X))
```

$$\frac{-\frac{F X}{(2+F X)^2}+\frac{1}{2+F X}}{F+\frac{2}{X}}$$

```
(*** Simplifying results in the second-order term ***)
```

```
Simplify[(-F X/(2+F X)^2 + 1/(2+F X))/(F + 2/X)]
```

$$\frac{2 X}{(2+F X)^3}$$

```
(*** The same process is applied again. Derivation of the final second-
  order term → Apply chain rule → simplify. ***)
```

```
D[2 X/(2 + F X)^3, X]
```

$$-\frac{6 F X}{(2+F X)^4}+\frac{2}{(2+F X)^3}$$

```
(*** Application of the Chain rule. ***)
```

```
(-6 F X/(2 + F X)^4 + 2/(2 + F X)^3) * (1/(F + 2/X))
```

$$\frac{-\frac{6 F X}{(2+F X)^4}+\frac{2}{(2+F X)^3}}{F+\frac{2}{X}}$$

```
(*** Simplifying. ***)
```

```
Simplify[(-6 F X/(2+F X)^4 + 2/(2+F X)^3)/(F + 2/X)]
```

$$-\frac{4X(-1+FX)}{(2+FX)^5}$$

```
(*** Summary of the coefficients. ***)
First = X/(2 + F X)
Second = 2 X/(2 + F X)^3
Third = 4 X (1 - F X)/(2 + F X)^5
```

Theoretical Calculation Scripts

This python script was used to calculate the theoretical data for the single and Darlington nulls using the theoretical coefficients found in the mathematical derivation. This is the basis for the theoretical plots shown.

```
import re
import pylab
from pylab import
import numpy as np
import string

def Darl_theoryplot():

    ### File handle for simulated values of a single and Darlington####
    i = open('Nulldata3rd_Darlplot.xlsx', 'r')

    ### Definition of variables
    current_steps, IM3_darl, IM3_sing = [], [], []
    darl_ic, sing_ic, darl_3rd, sing_3rd = [], [], [], []

    ### Loop extrecting csv values ###
    count = 0
    for line in i:
        if count > 0:
            line_tmp = line.split(',')
            darl_ic.append(line_tmp[3])
            darl_3rd.append(line_tmp[5])
            sing_ic.append(line_tmp[12])
            sing_3rd.append(line_tmp[14])
        count += 1
    i.close()

    ### Console print ###
    print darl_ic
    print darl_3rd
    print sing_ic
    print sing_3rd

    ### Manual X axis labels for upcoming theoretical data
    current_steps = np.linspace(0.003, 0.040, 101)
    ### Theoretical definitions and values for use in the IM3 coeffcient equations. ###
    Vt = ((1.380648e-23   (300.15)) / (1.6021766e-19))
        iq = 10.0(10 -9)
    beta = 76
    re = 1.2
    rb = re 10
    Ree_sing = ((re rb)/beta)+re
    Ree_darl = re(1+1/beta)+re((1+1/beta)/
              (beta+1))+(rb/beta)+rb (1/(beta beta+beta))
```

```
### Loops calculating the coefficient value at each current step value ###
for ic in current_steps[10:]:
    F = (iq Ree_darl)/Vt
    X =ic/iq
    IM3_darl.append(abs((4 X(1-X F))/(2+X F) 5)/1300)
for ic in current_steps:
    F = (iq Ree_darl)/Vt
    X =ic/iq
    IM3_sing.append(abs((X(1-2 X F))/(1+X F) 5)/2600)

### Console print ###
print Vt
print Ree_sing
print Ree_darl
print current_steps
print IM3_sing
print IM3_darl
```

C

Translinear Extraction Data

This section presents scripts and files used in the translinear extraction work. This work was mainly done in Python, and circuit simulations were done in LTSpice.

Translinear Conditions

This script computes all possible emitter area ratios and hence all possible A and x values for a translinear stack. This was extremely useful for optimising and minimising the stack ratios used. The script was built and executed in Python.

```
import numpy as np
import collections as cl

### Loop computing the A  and x values for a two-stack translinear ###
### loop with emitter area ratios from 1 to 32 ###
def Looptwo():

    ### Open files for dump data in ###
    f = open('Loop2data_xgt0.txt', 'w')
    f1 = open('Loop2data_xeq0.txt', 'w')
```

```
    ### Four loops for each of the possible emitter ratios of the ###
    ### junctions in the loop. ###
    for i in range(1, 32):
        m1 = i
        for j in range (1, 32):
            m2 = j
            for k in range (1, 32):
                m3 = k
                for l in range (1, 32):
                    m4 = l

                    ### Calculation of a and A ###
                    x = (1/float(m3))+(1/float(m4))-(1/float(m1))-(1/float(m2))
                    A = (float(m3) float(m4))/(float(m1) float(m2))

                    m1to3 = m1 + m2
                    m4to6 = m3 + m4

                    ### Filtering of tiny x and A values ###
                    if (x > 0.01) and (A > 1):
                        fileout = repr(x) + ' ' + repr(A) + ' ' + repr(i) + ' '
                                + repr(j) + ' ' + repr(k) + ' ' + repr(l) + '\n'
                        f.write(fileout)

                    if ( -0.000001 < x < 0.000001) and (A != 1):
                        fileout1 = repr(x) + ' ' + repr(A) + ' ' + repr(i) + ' '
                                 + repr(j) + ' ' + repr(k) + ' ' + repr(l) + '\n'
                        f1.write(fileout1)

### Loop computing the A and x values for a three-stack translinear ###
### loop with emitter area ratios from 1 to 32 ###
def Loopthree():

    f = open('Loop3data_xgt0.txt', 'w')
    f1 = open('Loop3data_xeq0.txt', 'w')

    for i in range(1, 32):
        m1 = i
        for j in range (1, 32):
            m2 = j
            for k in range (1, 32):
                m3 = k
                for l in range (1, 32):
                    m4 = l
                    for m in range (1, 32):
                        m5 = m
                        for n in range (1, 32):
                            m6 = n

                            x = (1/float(m4))+(1/float(m5))+(1/float(m6))
                                -(1/float(m1))-(1/float(m2))-(1/float(m3))
                            A = (float(m4) float(m5) float(m6))/
```

```
                    (float(m1) float(m2) float(m3))

                m1to3 = m1 + m2 + m3
                m4to6 = m4 + m5 + m6

                if (x > 0.01) and (A > 1):
                    fileout = repr(x) + ' ' + repr(A) + ' '
                            + repr(i) + ' ' + repr(j) + ' '
                            + repr(k) + ' ' + repr(l) + ' '
                            + repr(m) + ' ' + repr(n) + '\n'
                    f.write(fileout)

                if ( -0.000001 < x < 0.000001) and (A != 1):
                    fileout1 = repr(x) + ' ' + repr(A) + ' '
                             + repr(i) + ' ' + repr(j) + ' '
                             + repr(k) + ' ' + repr(l) + ' '
                             + repr(m) + ' ' + repr(n) + '\n'
                    f1.write(fileout1)

### Loop computing the A and x values for a three-stack translinear ###
### loop with emitter area ratios from 1 to 16 and with the condition ###
### of A equal to 1 ###
def Loopthree_Aequal1():

    f = open('Loop3data_Aequal1.txt', 'w')
    f1 = open('Loop3data_showBill_xeq0.txt', 'w')

    for i in range(1, 16):
        m1 = i
        for j in range (1, 16):
            m2 = j
            for k in range (1, 16):
                m3 = k
                for l in range (1, 16):
                    m4 = l
                    for m in range (1, 16):
                        m5 = m
                        for n in range (1, 16):
                            m6 = n

                            x = (1/float(m4))+(1/float(m5))+(1/float(m6))
                              -(1/float(m1))-(1/float(m2))-(1/float(m3))
                            A = (float(m4) float(m5) float(m6))/
                                (float(m1) float(m2) float(m3))

                            m1to3 = m1 + m2 + m3
                            m4to6 = m4 + m5 + m6

                            if (-1 < x < 1) and (A == 1.0):
                                fileout = repr(x) + ' ' + repr(A) + ' '
                                        + repr(i) + ' ' + repr(j) + ' '
                                        + repr(k) + ' ' + repr(l) + ' '
```

```
                    + repr(m) + ' ' + repr(n) + '\n'
                f.write(fileout)
            #if ( -0.000001 < x < 0.000001) and (A != 1):
                #fileout1 = repr(x) + ' ' + repr(A) + ' '
                #        + repr(i) + ' ' + repr(j) + ' '
                #        + repr(k) + ' ' + repr(l) + ' '
                #        + repr(m) + ' ' + repr(n) + '\n'
                #f1.write(fileout1)

### Loop computing the A and x values for a four-stack translinear ###
### loop with emitter area ratios from 2 to 16 with condtions
### A > 1.5 and x being negitive ###
def Loopfour():

    f = open('Loop4_xgt0.txt', 'w')
    f1 = open('Loop4_xeq0.txt', 'w')

    for i in range(2, 16):
        m1 = i
        for j in range (2, 16):
            m2 = j
            for k in range (2, 16):
                m3 = k
                for l in range (2, 16):
                    m4 = l
                    for m in range (2, 16):
                        m5 = m
                        for n in range (2, 16):
                            m6 = n
                            for o in range (2, 16):
                                m7 = o
                                for p in range (2, 16):
                                    m8 = p
                            x = (1/float(m5))+(1/float(m6))+(1/float(m7))
                              +(1/float(m8))-(1/float(m1))-(1/float(m2))
                              -(1/float(m3))-(1/float(m4))
                            A = (float(m5) float(m6) float(m7) float(m8))
                                /(float(m1) float(m2) float(m3) float(m4))


                            if ( x < -0.2) and (A > 1.5):
                                fileout = repr(x) + ' ' + repr(A) + ' '
                                        + repr(i) + ' ' + repr(j) + ' '
                                        + repr(k) + ' ' + repr(l) + ' '
                                        + repr(m) + ' ' + repr(n) + '\n'
                            if ( -0.000001 < x < 0.000001) and (A != 1):
                                fileout1 = repr(x) + ' ' + repr(A) + ' '
                                         + repr(i) + ' ' + repr(j) + ' '
                                         + repr(k) + ' ' + repr(l) + ' '
                                         + repr(m) + ' ' + repr(n) + '\n'
                                f1.write(fileout1)
```

```
### Loop computing the A and x values for a two-stack translinear ###
### loop with emitter area ratios from 2 to 18. In this case the ###
### parameters are forced to be considered floats.  ###
def Looptwo_2ndAttempt():

    f = open('Loop2data_2ndAttempt_xgt0.txt', 'w')
    f1 = open('Loop2data_2ndAttempt_xeq0.txt', 'w')

    for i in range(2, 18):
        m1 = i
        for j in range (2, 18):
            m2 = j
            for k in range (2, 18):
                m3 = k
                for l in range (2, 18):
                    m4 = l

                    if (m3!=0): x3 = (1/float(m3))
                    else: x3 = 0
                    if (m4!=0): x4 = (1/float(m4))
                    else: x4 = 0
                    if (m1!=0): x1 = (1/float(m1))
                    else: x1 = 0
                    if (m2!=0): x2 = (1/float(m2))
                    else: x2 = 0
                    x = x3+x4-x1-x2

                    if (m3!=0): a3 = (float(m3))
                    else: a3 = 1
                    if (m4!=0): a4 = (float(m4))
                    else: a4 = 1
                    if (m1!=0): a1 = (float(m1))
                    else: a1 = 1
                    if (m2!=0): a2 = (float(m2))
                    else: a2 = 1
                    A = (a3 a4)/(a1 a2)

                    m1to3 = m1 + m2
                    m4to6 = m3 + m4

                    if ( x < -0.1) and (A > 1.5):
                        fileout = repr(x) + ' ' + repr(A) + ' '
                                + repr(i) + ' ' + repr(j) + ' '
                                + repr(k) + ' ' + repr(l) + ' '
                                + '\n'
                        f.write(fileout)
                    if ( -0.000001 < x < 0.000001) and (A > 1.5):
                        fileout1 = repr(x) + ' ' + repr(A) + ' '
                                + repr(i) + ' ' + repr(j) + ' '
                                + repr(k) + ' ' + repr(l) + ' '
                                + '\n'
```

```
                    f1.write(fileout1)

### Loop computing the A and x values for a four-stack translinear ###
### loop with emitter area ratios from 6 to 32. This removes small ratioed
### junction (M < 6) to evaluate the effect on the stacks. ###
def Looptwo_MinimizeBeta():

    f = open('Loop2data_MinimizeBeta_xgt0.txt', 'w')
    f1 = open('Loop2data_MinimizeBeta_xeq0.txt', 'w')

    for i in range(6, 32):
        m1 = i
        for j in range (6, 32):
            m2 = j
            for k in range (6, 32):
                m3 = k
                for l in range (6, 32):
                    m4 = l

                    if (m3!=0): x3 = (1/float(m3))
                    else: x3 = 0
                    if (m4!=0): x4 = (1/float(m4))
                    else: x4 = 0
                    if (m1!=0): x1 = (1/float(m1))
                    else: x1 = 0
                    if (m2!=0): x2 = (1/float(m2))
                    else: x2 = 0
                    x = x3+x4-x1-x2

                    if (m3!=0): a3 = (float(m3))
                    else: a3 = 1
                    if (m4!=0): a4 = (float(m4))
                    else: a4 = 1
                    if (m1!=0): a1 = (float(m1))
                    else: a1 = 1
                    if (m2!=0): a2 = (float(m2))
                    else: a2 = 1
                    A = (a3 a4)/(a1 a2)

                    m1to3 = m1 + m2
                    m4to6 = m3 + m4

                    if (x > 0.01) and (A > 1):
                        fileout = repr(x) + ' ' + repr(A) + ' '
                                + repr(i) + ' ' + repr(j) + ' '
                                + repr(k) + ' ' + repr(l) + ' '
                                + '\n'
                        f.write(fileout)
                    if ( -0.000001 < x < 0.000001) and (A != 1):
                        fileout1 = repr(x) + ' ' + repr(A) + ' '
                                + repr(i) + ' ' + repr(j) + ' '
                                + repr(k) + ' ' + repr(l) + ' '
```

```
                                + '\n'
                        f1.write(fileout1)

#Ferrantiloop()
#Looptwo_showBill()
#Looptwo_2ndAttempt()
#Loopthree_showBill()
#Looptwo_MinimizeBeta()
Loopfour()
```

Ferranti Datasheets

Here, the Ferranti transistor datasheets are shown. These are discontinued products and hence the datasheet is not easily available, so they are included here for convenience.

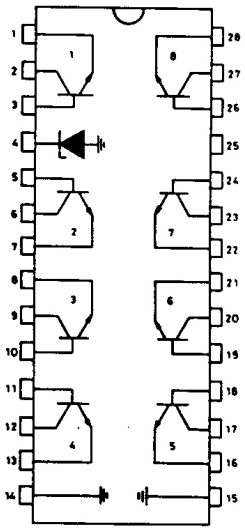
ULA* 1U009

Evaluation Part for Digilin* Design. Transistors/Bandgap Reference.

DESCRIPTION

- Evaluation part for Digilin designs
- Package: 28 pin plastic dual-in-line
- Operating temperature range −55 to +125°C
- Peripheral cell transistors
  - type 4A
- Bandgap reference (Pin 4)

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage V_{CC}	+7.0V max. −0.5V min.
Input Voltage V_{IN}	+5.5V max. −0.5V min.
Operating Temperature Range . .	−55 to +125°C
Storage Temperature Range . .	−65 to +150°C



Pin Layout

ELECTRICAL CHARACTERISTICS at 25°C

Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CB}/V_{CS}		7.5			V
V_{EB}		6.0			V
V_{CEO}		4.5			V
H_{FE} forward	$I_C = 1\mu A$ to 1mA	70	150	300	
H_{FE} matching	$I_C = 1\mu A$ to 1mA			10	%
V_{BE}	$I_E = 10\mu A$		0.608		V
V_{BE} matching	$I_E = 1\mu A$		±0.5	4	mV
I_{CBO}	$V_{CB} = 1V$		0.01		nA
I_{CEO}	$V_{CE} = 1V$		0.5		nA
R_{SAT}	$I_C = 1mA$, $I_B = 100mA$		30		Ω
V_{REF}	$I_{REF} = 40\mu A$	1.25	1.30	1.35	V

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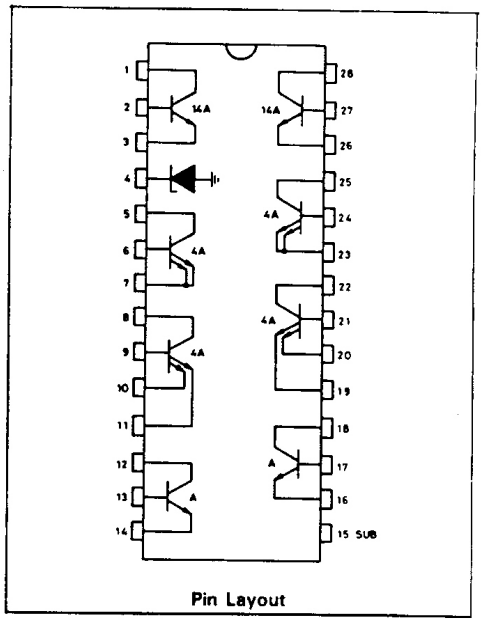
*Digilin is a registered trademark of Ferranti plc for semiconductor devices

ULA* 2G004

Evaluation Part for Digilin* Design. Transistor/Bandgap Reference.

FEATURES

- Evaluation part for Digilin designs
- Package: 28 pin plastic dual-in-line
- Operating temperature range 0 to +70°C
- Peripheral cell transistors
  - 2 × 14A
  - 4 × 4A
  - 2 × A
- Bandgap reference (pin 4)



Pin Layout

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage V_{CC}	+7.0V max. −0.5V min.
Input Voltage V_{IN}	+5.5V max. −0.5V min.
Operating Temperature Range	−55 to +125°C
Storage Temperature Range	−65 to +150°C

ELECTRICAL CHARACTERISTICS at 25°C

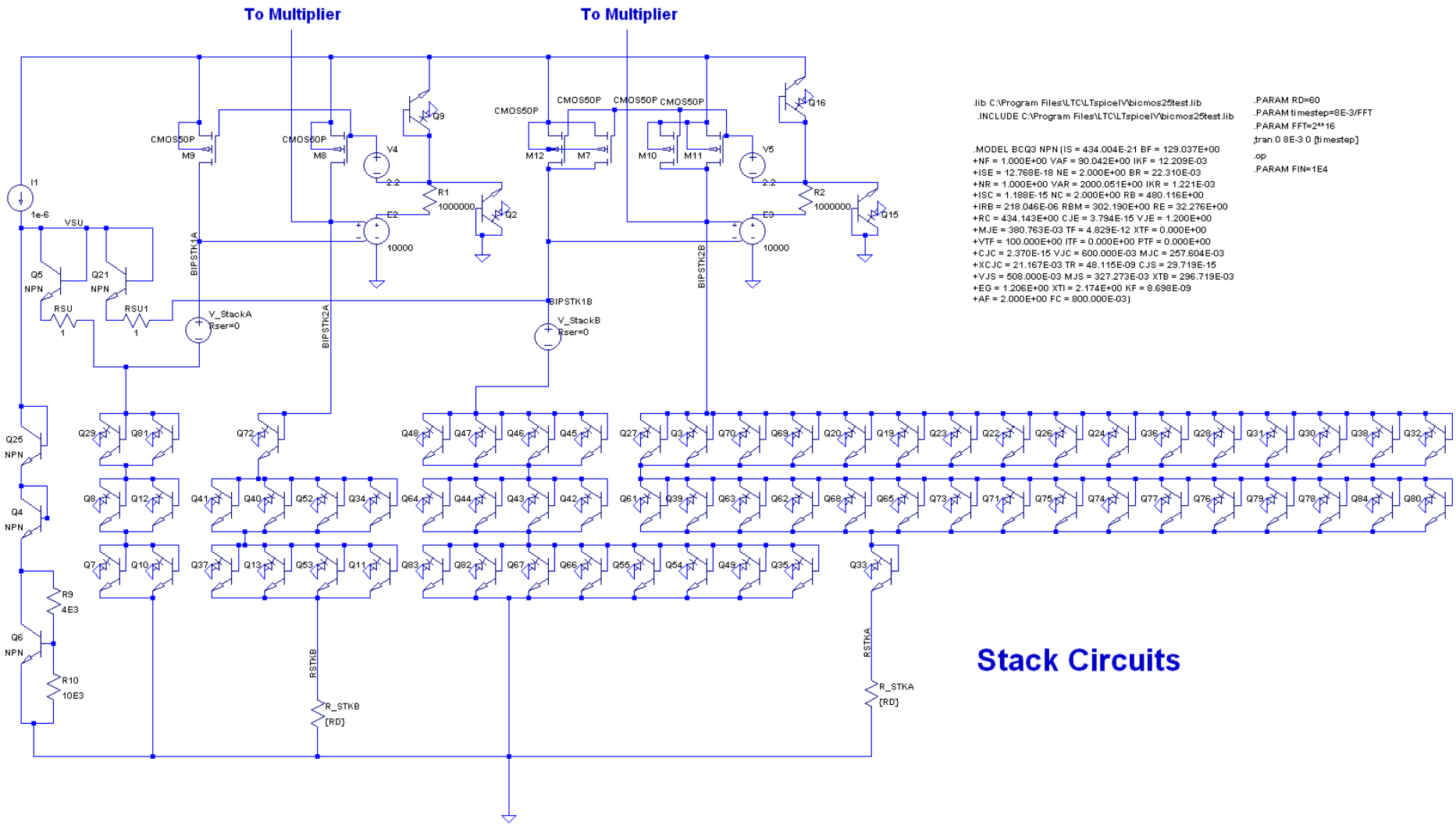
Parameter	Conditions		Min.	Typ.	Max.	Unit
(a) Transistors						
h_{FE} forward	$I_E = 1\mu A$ - 1mA		70	150	300	
h_{FE} reverse	$I_E = 1\mu A$ - 1mA	A		8		
		4A		20		
		14A		40		
I_{CBO}	$V_{CB} = 1V$			0.01		nA
I_{CEO}	$V_{CE} = 1V$			0.5		nA
V_{BE}	$I_E = 10\mu A$	A		644		mV
		4A		608		mV
		14A		575		mV

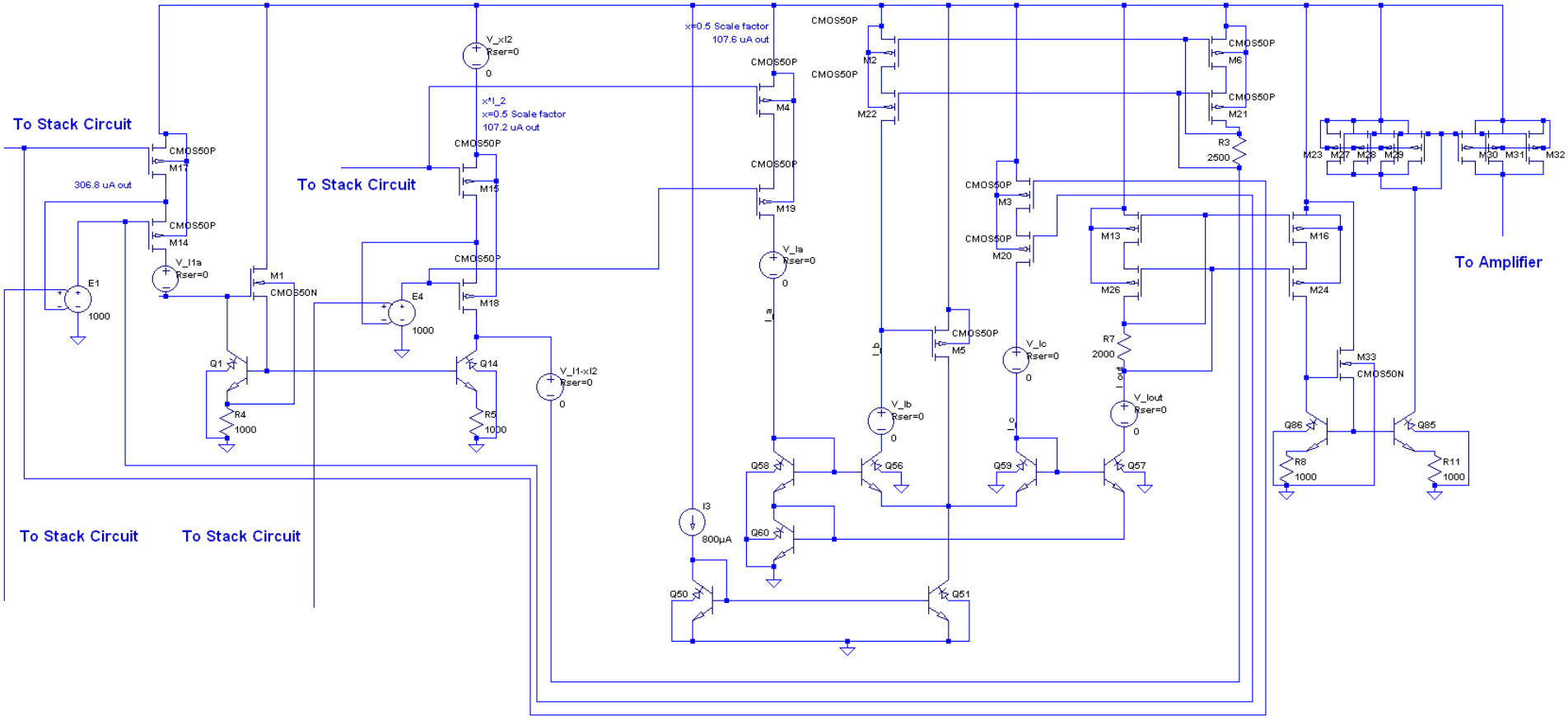
*ULA is a registered trademark of Ferranti plc for semiconductor devices.
*Digilin is a registered trademark of Ferranti plc for semiconductor devices.

Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BE} matching	Between adjacent transistors, $I_E = 1\mu A$	A		±2		mV
		4A		±0.5		mV
		14A		±0.3		mV
V_{OFFSET}	$I_C = 10\mu A$, $I_B = 30\mu A$	A		3.0		mV
		4A		1.5		mV
		14A		0.8		mV
V_{OFFSET} matching	Between adjacent pairs of transistor $I_C = 10\mu A$, $I_B = 30\mu A$	A		50		μV
		4A		10		μV
		14A		10		μV
R_{SAT}	$I_C = 1mA$, $I_B = 100\mu A$	A		55		Ω
		4A		30		Ω
		14A		25		Ω
V_{CBO}			7.5			V
V_{EBO}			6.0			V
V_{CEO}			4.5			V
Collector slope resistance				10		kΩ/mA
(b) Bandgap Reference						
V_{REF}				1.30		V
Stability				100		ppm/°C
Bias current			20	40	80	μA

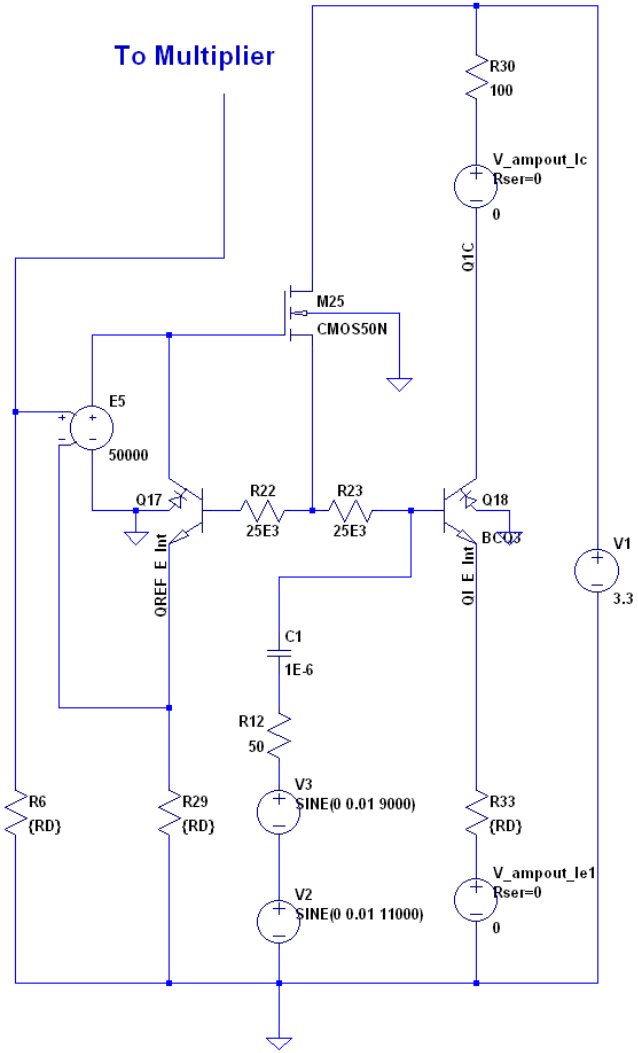
Full Translinear Bias Circuit SPICE model

Here, the full SPICE model circuit is shown for the translinear bias circuit developed. It is large and therefore split between three pages.


To Multiplier
To Multiplier
CMOS50P
M9
M8
M12
M7
M10
M11
Q9
Q16
V4
V5
2.2
R1
1000000
R2
Q2
Q15
E2
E3
10000
I1
1e-6
VSU
Q5
Q21
NPN
RSU
RSU1
1
V_StackA
V_StackB
Rser=0
BIPSTK1A
BIPSTK2A
BIPSTK1B
BIPSTK2B
Q25
Q4
Q6
R9
4E3
R10
10E3
RSTKB
R_STKB
{RD}
RSTKA
R_STKA
.lib C:\Program Files\LTC\LTspiceIV\bicmos25test.lib
.INCLUDE C:\Program Files\LTC\LTspiceIV\bicmos25test.lib
.MODEL BCQ3 NPN (IS = 434.004E-21 BF = 129.037E+00
+NF = 1.000E+00 VAF = 90.042E+00 IKF = 12.209E-03
+ISE = 12.768E-18 NE = 2.000E+00 BR = 22.310E-03
+NR = 1.000E+00 VAR = 2000.051E+00 IKR = 1.221E-03
+ISC = 1.188E-15 NC = 2.000E+00 RB = 480.116E+00
+IRB = 218.046E-06 RBM = 302.190E+00 RE = 32.276E+00
+RC = 434.143E+00 CJE = 3.784E-15 VJE = 1.200E+00
+MJE = 380.763E-03 TF = 4.829E-12 XTF = 0.000E+00
+VTF = 100.000E+00 ITF = 0.000E+00 PTF = 0.000E+00
+CJC = 2.370E-15 VJC = 600.000E-03 MJC = 257.604E-03
+XCJC = 21.167E-03 TR = 48.115E-09 CJS = 29.719E-15
+VJS = 508.000E-03 MJS = 327.273E-03 XTB = 296.719E-03
+EG = 1.206E+00 XTI = 2.174E+00 KF = 8.698E-09
+AF = 2.000E+00 FC = 800.000E-03)
.PARAM RD=60
.PARAM timestep=8E-3/FFT
.PARAM FFT=2**16
.tran 0 8E-3 0 {timestep}
.op
.PARAM FIN=1E4
Stack Circuits


To Stack Circuit
306.8 uA out
CMOS50P
M17
CMOS50P
M14
V_I1a
Rser=0
E1
1000
M1
CMOS50N
Q1
R4
1000
To Stack Circuit
V_xI2
Rser=0
0
x*I_2
x=0.5 Scale factor
107.2 uA out
CMOS50P
M15
CMOS50P
M18
E4
1000
Q14
R5
1000
V_I1-xI2
Rser=0
0
To Stack Circuit
To Stack Circuit
x=0.5 Scale factor
107.6 uA out
CMOS50P
M4
CMOS50P
M19
V_Ia
Rser=0
0
I_a
I3
800µA
Q50
Q51
Q58
Q60
Q56
CMOS50P
M2
CMOS50P
M22
CMOS50P
M5
V_Ib
Rser=0
0
I_b
CMOS50P
M6
CMOS50P
M21
R3
2500
CMOS50P
M3
CMOS50P
M20
V_Ic
Rser=0
0
I_c
Q59
Q57
M13
M26
R7
2000
V_Iout
Rser=0
0
I_o
M23
M27
M28
M29
M30
M31
M32
M16
M24
To Amplifier
M33
CMOS50N
Q86
R8
1000
Q85
R11
1000

Amplifier Circuit



D

Cascomp Derivations

This appendix presents the full derivations for the Cascomp circuit and its distortion products.

Ideal Cascomp Expansion Coefficients

Here, the series coefficients derivation for the Cascomp amplifier with an ideal error amplifier is shown. Due to the complex nature of the derivations, they were done using Mathematica scripts to avoid human error in the algebraic manipulations.

```
(*** The derivation in this script begins from the final transfer equation of
 an ideal Cascomp amplifier(found in Chapter 5, section 5.4). here we aim to
 derive the series expansion coefficients using the previously presented method
 of differentiating the transfer function. This will result in confirming
 current theory (error amplifier must be gme = -1/rm for cancellation)   ***)

(*** Firstly, we state the equation found for a non-ideal differential
  amplifier. This is the main amplifier equation stated in Eq. 5.12.   ***)

vin == (rm * 2 * i1) + vt * Log[(1 + 2 * i1 / im) / (1 - 2 * i1 / im)]
```

$$\text{vin} == 2\,\text{i1}\,\text{rm} + \text{vt}\,\text{Log}\left[\frac{1 + \frac{2\,\text{i1}}{\text{im}}}{1 - \frac{2\,\text{i1}}{\text{im}}}\right]$$

```
(*** We aim to find the series expansion coefficients
 for the main amplifier. This equation is differentiated and
 inverted to give the transconductance (dVin(m) / di1).  * **)

Simplify[
 D[(rm * 2 * i1) + vt * Log[(1 + 2 * i1 / im) / (1 - 2 * i1 / im)], {i1, 1}]]
```

$$\frac{8\,\text{i1}^2\,\text{rm} - 2\,\text{im}\,(\text{im}\,\text{rm} + 2\,\text{vt})}{4\,\text{i1}^2 - \text{im}^2}$$

$$1 \Big/ \left(\left(\frac{8\,\text{i1}^2\,\text{rm} - 2\,\text{im}\,(\text{im}\,\text{rm} + 2\,\text{vt})}{4\,\text{i1}^2 - \text{im}^2}\right)\right)$$

$$\frac{4\,\text{i1}^2 - \text{im}^2}{8\,\text{i1}^2\,\text{rm} - 2\,\text{im}\,(\text{im}\,\text{rm} + 2\,\text{vt})}$$

```
(*** The first order coefficient is found by making i2 tend to zero leaving
 the a term describing the magnitude of the first order transconductance.  ***)

Simplify[(4 i1^2 - im^2) / (8 i1^2 rm - 2 im (im rm + 2 vt)), i1 == 0]
```

$$\frac{\text{im}}{2\,\text{im}\,\text{rm} + 4\,\text{vt}}$$

```
(*** To find the second and third order coefficients, we defferentiate,
and apply the Chain rule. We expect the second order to be zero
  as this is a well-known property of differential amplifiers/  ***)
```

```
Simplify[D[(4 i1^2 - im^2)/(8 i1^2 rm - 2 im (im rm + 2 vt)), i1]]
```

$$-\frac{8\,i1\,im\,vt}{\left(-4\,i1^2\,rm+im\,(im\,rm+2\,vt)\right)^2}$$

```
(*** Chain rule ***)
Simplify[(-(8 i1 im vt)/(-4 i1^2 rm + im (im rm + 2 vt))^2) * ((4 i1^2 - im^2)/(8 i1^2 rm - 2 im (im rm + 2 vt)))]
```

$$\frac{4\,i1\,im\left(-4\,i1^2+im^2\right)vt}{\left(4\,i1^2\,rm-im\,(im\,rm+2\,vt)\right)^3}$$

```
(*** Second order coefficient. ***)
Simplify[(4 i1 im (-4 i1^2 + im^2) vt)/(4 i1^2 rm - im (im rm + 2 vt))^3, i1 == 0]
0

(*** The third order coefficient is found by the same process again.  ***)
Simplify[D[(4 i1 im (-4 i1^2 + im^2) vt)/(4 i1^2 rm - im (im rm + 2 vt))^3, i1]]
```

$$-\frac{4\,im\,vt\left(-48\,i1^4\,rm+8\,i1^2\,im\,(im\,rm-3\,vt)+im^3\,(im\,rm+2\,vt)\right)}{\left(-4\,i1^2\,rm+im\,(im\,rm+2\,vt)\right)^4}$$

```
Simplify[(-(4 im vt (-48 i1^4 rm + 8 i1^2 im (im rm - 3 vt) + im^3 (im rm + 2 vt)))/(-4 i1^2 rm + im (im rm + 2 vt))^4) *
  ((4 i1^2 - im^2)/(8 i1^2 rm - 2 im (im rm + 2 vt)))]
(2 im (-4 i1^2 + im^2) vt
    (-48 i1^4 rm + 8 i1^2 im (im rm - 3 vt) + im^3 (im rm + 2 vt))) /
 (4 i1^2 rm - im (im rm + 2 vt))^5
```

```
Simplify[(2 im (-4 i1^2 + im^2) vt
     (-48 i1^4 rm + 8 i1^2 im (im rm - 3 vt) + im^3 (im rm + 2 vt))) /
   (4 i1^2 rm - im (im rm + 2 vt))^5, i1 == 0]
```

$$-\frac{2\,\text{im}\,\text{vt}}{(\text{im}\,\text{rm}+2\,\text{vt})^4}$$

```
(*** Summary of a differential amplifiers
 (the main amplifier) series expansion coefficients. ***)
```

$$\text{First} = \frac{\text{im}}{2\,\text{im}\,\text{rm}+4\,\text{vt}}$$

$$\text{Second} = 0$$

$$\text{Third} = -\frac{2\,\text{im}\,\text{vt}}{(\text{im}\,\text{rm}+2\,\text{vt})^4}$$

```
(*** The same process is followed for the ideal error amplifier. We
  make the assumption that this is a perfect transconductance. Therefore
  we can state the following because Using the propety that Vbe12 =
 Vbe34 we can find an equation describing i1 in terms of i2.***)
Clear[i2]
(*** Statement of the error amplifiers input transfer function. Solving for i1. ***)
Solve[i2 == gme * (vt * Log[(1 + 2 * (i1 / im)) / (1 - 2 * (i1 / im))]), i1]
```

$$\left\{\left\{\text{i1} \to \frac{\left(-1+e^{\frac{\text{i2}}{\text{gme}\,\text{vt}}}\right)\text{im}}{2\left(1+e^{\frac{\text{i2}}{\text{gme}\,\text{vt}}}\right)}\right\}\right\}$$

```
(*** Now the exact same process as before is
 applied to find the series expasnion coefficients. ***)
```

```
Simplify[
 D[(rm * 2 * ((-1 + e^(i2/(gme vt))) im)/(2 (1 + e^(i2/(gme vt))))) + vt * Log[(1 + 2 * ((-1 + e^(i2/(gme vt))) im)/(2 (1 + e^(i2/(gme vt)))))/im]/
   (1 - 2 * ((-1 + e^(i2/(gme vt))) im)/(2 (1 + e^(i2/(gme vt))))/im), {i2, 1}]]
```

$$\frac{vt + e^{\frac{2\,i2}{gme\,vt}}\,vt + 2\,e^{\frac{i2}{gme\,vt}}\,(im\,rm + vt)}{\left(1 + e^{\frac{i2}{gme\,vt}}\right)^2\,gme\,vt}$$

$$1\Big/\left(\frac{vt + e^{\frac{2\,i2}{gme\,vt}}\,vt + 2\,e^{\frac{i2}{gme\,vt}}\,(im\,rm + vt)}{\left(1 + e^{\frac{i2}{gme\,vt}}\right)^2\,gme\,vt}\right)$$

$$\frac{\left(1 + e^{\frac{i2}{gme\,vt}}\right)^2\,gme\,vt}{vt + e^{\frac{2\,i2}{gme\,vt}}\,vt + 2\,e^{\frac{i2}{gme\,vt}}\,(im\,rm + vt)}$$

```
Simplify[(1 + e^(i2/(gme vt)))^2 gme vt/(vt + e^(2 i2/(gme vt)) vt + 2 e^(i2/(gme vt)) (im rm + vt)), i2 == 0]
```

$$\frac{2\,gme\,vt}{im\,rm + 2\,vt}$$

```
(*** The second-
 order follows the same processas the main amplifier's second order derivation. ***)
```

```
Simplify[D[(1 + e^(i2/(gme vt)))^2 gme vt/(vt + e^(2 i2/(gme vt)) vt + 2 e^(i2/(gme vt)) (im rm + vt)), i2]]
```

$$\frac{2\,e^{\frac{i2}{gme\,vt}}\left(-1 + e^{\frac{2\,i2}{gme\,vt}}\right)im\,rm}{\left(vt + e^{\frac{2\,i2}{gme\,vt}}\,vt + 2\,e^{\frac{i2}{gme\,vt}}\,(im\,rm + vt)\right)^2}$$

```
(*** Chain rule ***)
```

```
Simplify[
 (2 e^(i2/(gme vt)) (-1 + e^(2 i2/(gme vt))) im rm) /
   (vt + e^(2 i2/(gme vt)) vt + 2 e^(i2/(gme vt)) (im rm + vt))^2 *
  ((1 + e^(i2/(gme vt)))^2 gme vt) /
   (vt + e^(2 i2/(gme vt)) vt + 2 e^(i2/(gme vt)) (im rm + vt))]
```

$$\frac{2\, e^{\frac{i2}{gme\, vt}} \left(-1 + e^{\frac{i2}{gme\, vt}}\right) \left(1 + e^{\frac{i2}{gme\, vt}}\right)^3 gme\, im\, rm\, vt}{\left(vt + e^{\frac{2\, i2}{gme\, vt}}\, vt + 2\, e^{\frac{i2}{gme\, vt}} (im\, rm + vt)\right)^3}$$

```
Simplify[2 e^(i2/(gme vt)) (-1 + e^(i2/(gme vt))) (1 + e^(i2/(gme vt)))^3 gme im rm vt /
   (vt + e^(2 i2/(gme vt)) vt + 2 e^(i2/(gme vt)) (im rm + vt))^3, i2 == 0]
```

```
0
```

```
(*** Third order ***)
```

```
Simplify[D[2 e^(i2/(gme vt)) (-1 + e^(i2/(gme vt))) (1 + e^(i2/(gme vt)))^3 gme im rm vt /
   (vt + e^(2 i2/(gme vt)) vt + 2 e^(i2/(gme vt)) (im rm + vt))^3, i2]]
```

$$-\left(2\, e^{\frac{i2}{gme\, vt}} \left(1 + e^{\frac{i2}{gme\, vt}}\right)^2 im\, rm \left(e^{\frac{2\, i2}{gme\, vt}} (4\, im\, rm - 6\, vt) + vt + e^{\frac{4\, i2}{gme\, vt}}\, vt - 2\, e^{\frac{i2}{gme\, vt}} (2\, im\, rm + vt) - 2\, e^{\frac{3\, i2}{gme\, vt}} (2\, im\, rm + vt)\right)\right) \Big/ \left(vt + e^{\frac{2\, i2}{gme\, vt}}\, vt + 2\, e^{\frac{i2}{gme\, vt}} (im\, rm + vt)\right)^4$$

```
(*** Chain rule ***)
```

```
Simplify[
 (-(2 e^(i2/(gme vt)) (1 + e^(i2/(gme vt)))^2 im rm (e^(2 i2/(gme vt)) (4 im rm - 6 vt) + vt +
          e^(4 i2/(gme vt)) vt - 2 e^(i2/(gme vt)) (2 im rm + vt) - 2 e^(3 i2/(gme vt)) (2 im rm + vt)))/
    (vt + e^(2 i2/(gme vt)) vt + 2 e^(i2/(gme vt)) (im rm + vt))^4) *
  ((1 + e^(i2/(gme vt)))^2 gme vt)/(vt + e^(2 i2/(gme vt)) vt + 2 e^(i2/(gme vt)) (im rm + vt))]
 - (2 e^(i2/(gme vt)) (1 + e^(i2/(gme vt)))^4 gme im rm vt (e^(2 i2/(gme vt)) (4 im rm - 6 vt) + vt +
       e^(4 i2/(gme vt)) vt - 2 e^(i2/(gme vt)) (2 im rm + vt) - 2 e^(3 i2/(gme vt)) (2 im rm + vt)))/
  (vt + e^(2 i2/(gme vt)) vt + 2 e^(i2/(gme vt)) (im rm + vt))^5
```

```
Simplify[
 -(2 e^(i2/(gme vt)) (1 + e^(i2/(gme vt)))^4 gme im rm vt (e^(2 i2/(gme vt)) (4 im rm - 6 vt) + vt + e^(4 i2/(gme vt)) vt -
        2 e^(i2/(gme vt)) (2 im rm + vt) - 2 e^(3 i2/(gme vt)) (2 im rm + vt)))/
  (vt + e^(2 i2/(gme vt)) vt + 2 e^(i2/(gme vt)) (im rm + vt))^5, i2 == 0]
```

$$\frac{4\,\text{gme}\,\text{im}\,\text{rm}\,\text{vt}}{(\text{im}\,\text{rm}+2\,\text{vt})^4}$$

```
(*** Summary of the Cascomps ideal error
 amplifiers series expansion coefficients. ***)
```

$$\text{First} = \frac{2\,\text{gme}\,\text{vt}}{\text{im}\,\text{rm}+2\,\text{vt}}$$

$$\text{Second} = 0$$

$$\text{Third} = \frac{4\,\text{gme}\,\text{im}\,\text{rm}\,\text{vt}}{(\text{im}\,\text{rm}+2\,\text{vt})^4}$$

```
(*** This can be double checked by taking the
  third order coefficient and solving for gm of the error
  amplifier. THis should match current ideal-case literature.  ***)
```

```
Solve[(4 gme im rm vt)/(im rm + 2 vt)^4 == -(2 im vt)/(im rm + 2 vt)^4, gme]
```

$$\left\{\left\{\text{gme} \to -\frac{1}{2\,\text{rm}}\right\}\right\}$$

```
(*** Indeed this matches the Quinn condition for cancellation in a Cascomp circuit ***)
```

Nonideal Cascomp Expansion Coefficients

Here, the series coefficients derivation for the Cascomp amplifier with a non-ideal error amplifier is shown. Due to the complex nature of the derivations, they were done using Mathematica scripts to avoid human error in the algebraic manipulations.

```
(*** The derivation in this script begins from the final transfer equation
 of a nonideal Cascomp amplifier(found in Chapter 5, section 5.4). here
 we aim to derive the series expansion coefficients using the previously
 presented method of differentiating the transfer function.  ***)

(*** Firstly,
we state the equation found for a non-ideal differential amplifier.  ***)

Solve[vine == (re * 2 * i2) + vt * Log[(1 + 2 * i2 / ie) / (1 - 2 * i2 / ie)], i2]
```

```
(*** Using the propety that Vbe12 =
 Vbe34 in Eq. 5.14 we can find an equation describing i1 in terms of i2.  ***)

Solve[vt * Log[(1 + 2 * i1 / im) / (1 - 2 * i1 / im)] ==
   (re * 2 * i2) + vt * Log[(1 + 2 * i2 / ie) / (1 - 2 * i2 / ie)], i1]
```

$$\left\{\left\{i1 \to \frac{\left(2\,i2 + 2\,e^{\frac{2\,i2\,re}{vt}}\,i2 - ie + e^{\frac{2\,i2\,re}{vt}}\,ie\right)\,im}{2\left(-2\,i2 + 2\,e^{\frac{2\,i2\,re}{vt}}\,i2 + ie + e^{\frac{2\,i2\,re}{vt}}\,ie\right)}\right\}\right\}$$

```
Simplify[(2 i2 + 2 e^(2 i2 re / vt) i2 - ie + e^(2 i2 re / vt) ie) im /
  (2 (-2 i2 + 2 e^(2 i2 re / vt) i2 + ie + e^(2 i2 re / vt) ie))]
```

$$\frac{\left(2\left(1 + e^{\frac{2\,i2\,re}{vt}}\right)i2 + \left(-1 + e^{\frac{2\,i2\,re}{vt}}\right)ie\right)\,im}{2\left(2\left(-1 + e^{\frac{2\,i2\,re}{vt}}\right)i2 + \left(1 + e^{\frac{2\,i2\,re}{vt}}\right)ie\right)}$$

```
(*** This equation is substitued into Eq. 5.12 of the main amplifier,
making Vin(m) a function of only i2. This equation is then differentiated
 and inverted to give the transconductance (dVin(m) / di2).  ***)
```

$$\text{Simplify}\left[\text{D}\left[\left(\text{rm}*2*\left(\left(\left(2\,\text{i2}+2\,e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{i2}-\text{ie}+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{ie}\right)\,\text{im}\right)\Big/\left(2\left(-2\,\text{i2}+2\,e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{i2}+\text{ie}+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{ie}\right)\right)\right)\right)+\text{vt}*\text{Log}\left[\left(1+2*\left(\left(\left(2\,\text{i2}+2\,e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{i2}-\text{ie}+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{ie}\right)\,\text{im}\right)\Big/\left(2\left(-2\,\text{i2}+2\,e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{i2}+\text{ie}+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{ie}\right)\right)\right)\Big/\text{im}\right)\Big/\left(1-2*\left(\left(\left(2\,\text{i2}+2\,e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{i2}-\text{ie}+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{ie}\right)\,\text{im}\right)\Big/\left(2\left(-2\,\text{i2}+2\,e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{i2}+\text{ie}+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{ie}\right)\right)\right)\Big/\text{im}\right)\right],\ \text{i2}\right]\right]$$

$$\left(2\left((-2\,\text{i2}+\text{ie})^2\,\text{vt}+e^{\frac{4\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2}+\text{ie})^2\,\text{vt}-2\,e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\left(4\,\text{i2}^2-\text{ie}^2\right)(\text{im}\,\text{rm}+\text{vt})\right)\left(4\,\text{i2}^2\,\text{re}-\text{ie}\,(\text{ie}\,\text{re}+2\,\text{vt})\right)\right)\Big/\left(\left(2\left(-1+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\right)\text{i2}+\left(1+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\right)\text{ie}\right)^2\left(4\,\text{i2}^2-\text{ie}^2\right)\text{vt}\right)$$

$$\text{Simplify}\left[1\Big/\left(\left(2\left((-2\,\text{i2}+\text{ie})^2\,\text{vt}+e^{\frac{4\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2}+\text{ie})^2\,\text{vt}-2\,e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\left(4\,\text{i2}^2-\text{ie}^2\right)(\text{im}\,\text{rm}+\text{vt})\right)\left(4\,\text{i2}^2\,\text{re}-\text{ie}\,(\text{ie}\,\text{re}+2\,\text{vt})\right)\right)\Big/\left(\left(2\left(-1+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\right)\text{i2}+\left(1+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\right)\text{ie}\right)^2\left(4\,\text{i2}^2-\text{ie}^2\right)\text{vt}\right)\right)\right]$$

$$\left(\left(2\left(-1+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\right)\text{i2}+\left(1+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\right)\text{ie}\right)^2\left(4\,\text{i2}^2-\text{ie}^2\right)\text{vt}\right)\Big/\left(2\left((-2\,\text{i2}+\text{ie})^2\,\text{vt}+e^{\frac{4\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2}+\text{ie})^2\,\text{vt}-2\,e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\left(4\,\text{i2}^2-\text{ie}^2\right)(\text{im}\,\text{rm}+\text{vt})\right)\left(4\,\text{i2}^2\,\text{re}-\text{ie}\,(\text{ie}\,\text{re}+2\,\text{vt})\right)\right)$$

```
(*** The first order coefficient is found by making i2 tend to zero leaving
 the a term describing the magnitude of the first order transconductance.  ***)
```

```
Simplify[((2 (-1 + e^(2 i2 re/vt)) i2 + (1 + e^(2 i2 re/vt)) ie)^2 (4 i2^2 - ie^2) vt)/
   (2 ((-2 i2 + ie)^2 vt + e^(4 i2 re/vt) (2 i2 + ie)^2 vt -
       2 e^(2 i2 re/vt) (4 i2^2 - ie^2) (im rm + vt)) (4 i2^2 re - ie (ie re + 2 vt))), i2 == 0]
```

$$\frac{ie\ vt}{(ie\ re + 2\ vt)\ (im\ rm + 2\ vt)}$$

```
(*** The second order term is found by differentiating the first order term,
and applying the chani rule. This is expected to be zero as a well-
 known property of differential amplifiers is the rejection of the second-
 order component. ***)
Simplify[D[((2 (-1 + e^(2 i2 re/vt)) i2 + (1 + e^(2 i2 re/vt)) ie)^2 (4 i2^2 - ie^2) vt)/
   (2 ((-2 i2 + ie)^2 vt + e^(4 i2 re/vt) (2 i2 + ie)^2 vt - 2 e^(2 i2 re/vt) (4 i2^2 - ie^2)
       (im rm + vt)) (-4 i2^2 re + ie (ie re + 2 vt))), i2]]
```

$$\left(2\left(2\left(-1 + e^{\frac{2\,i2\,re}{vt}}\right) i2 + \left(1 + e^{\frac{2\,i2\,re}{vt}}\right) ie\right)\right.$$
$$\left(-4\,i2\,(2\,i2 - ie)^3\,ie\,vt^3 + 4\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2 + ie)^3\,vt^3 + e^{\frac{4\,i2\,re}{vt}}\,(2\,i2 - ie)\right.$$
$$(2\,i2 + ie)^2\,\left(16\,i2^4\,im\,re^2\,rm - 8\,i2^2\,ie\,im\,re\,rm\,(ie\,re + 2\,vt) + ie^2\,im\,rm\right.$$
$$\left.(ie\,re + 2\,vt)^2 - 4\,i2\,ie\,vt^2\,(2\,im\,rm + 3\,vt)\right) + e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2 + ie)^2$$
$$(2\,i2 + ie)\,\left(16\,i2^4\,im\,re^2\,rm - 8\,i2^2\,ie\,im\,re\,rm\,(ie\,re + 2\,vt) +\right.$$
$$\left.\left.\left.ie^2\,im\,rm\,(ie\,re + 2\,vt)^2 + 4\,i2\,ie\,vt^2\,(2\,im\,rm + 3\,vt)\right)\right)\right)\Big/$$
$$\left(\left((-2\,i2 + ie)^2\,vt + e^{\frac{4\,i2\,re}{vt}}\,(2\,i2 + ie)^2\,vt - 2\,e^{\frac{2\,i2\,re}{vt}}\,\left(4\,i2^2 - ie^2\right)\,(im\,rm + vt)\right)^2\right.$$
$$\left.\left(-4\,i2^2\,re + ie\,(ie\,re + 2\,vt)\right)^2\right)$$

```
(*** Chain Rule ***)
```

```
Simplify[(((2 (-1 + e^(2 i2 re/vt)) i2 + (1 + e^(2 i2 re/vt)) ie)^2 (4 i2^2 - ie^2) vt)/
    (2 ((-2 i2 + ie)^2 vt + e^(4 i2 re/vt) (2 i2 + ie)^2 vt -
        2 e^(2 i2 re/vt) (4 i2^2 - ie^2) (im rm + vt)) (-4 i2^2 re + ie (ie re + 2 vt)))) *
  ((2 (2 (-1 + e^(2 i2 re/vt)) i2 + (1 + e^(2 i2 re/vt)) ie) (-4 i2 (2 i2 - ie)^3 ie vt^3 +
      4 e^(6 i2 re/vt) i2 ie (2 i2 + ie)^3 vt^3 + e^(4 i2 re/vt) (2 i2 - ie) (2 i2 + ie)^2
       (16 i2^4 im re^2 rm - 8 i2^2 ie im re rm (ie re + 2 vt) + ie^2 im rm
          (ie re + 2 vt)^2 - 4 i2 ie vt^2 (2 im rm + 3 vt)) + e^(2 i2 re/vt) (-2 i2 + ie)^2
       (2 i2 + ie) (16 i2^4 im re^2 rm - 8 i2^2 ie im re rm (ie re + 2 vt) +
         ie^2 im rm (ie re + 2 vt)^2 + 4 i2 ie vt^2 (2 im rm + 3 vt)))))/
    (((-2 i2 + ie)^2 vt + e^(4 i2 re/vt) (2 i2 + ie)^2 vt - 2 e^(2 i2 re/vt) (4 i2^2 - ie^2)
        (im rm + vt))^2 (-4 i2^2 re + ie (ie re + 2 vt))^2))]
 (((2 (-1 + e^(2 i2 re/vt)) i2 + (1 + e^(2 i2 re/vt)) ie)^3 (4 i2^2 - ie^2) vt
    (-4 i2 (2 i2 - ie)^3 ie vt^3 + 4 e^(6 i2 re/vt) i2 ie (2 i2 + ie)^3 vt^3 + e^(4 i2 re/vt) (2 i2 - ie)
      (2 i2 + ie)^2 (16 i2^4 im re^2 rm - 8 i2^2 ie im re rm (ie re + 2 vt) + ie^2 im rm
        (ie re + 2 vt)^2 - 4 i2 ie vt^2 (2 im rm + 3 vt)) + e^(2 i2 re/vt) (-2 i2 + ie)^2
      (2 i2 + ie) (16 i2^4 im re^2 rm - 8 i2^2 ie im re rm (ie re + 2 vt) +
        ie^2 im rm (ie re + 2 vt)^2 + 4 i2 ie vt^2 (2 im rm + 3 vt))))/
  (((-2 i2 + ie)^2 vt + e^(4 i2 re/vt) (2 i2 + ie)^2 vt - 2 e^(2 i2 re/vt) (4 i2^2 - ie^2) (im rm + vt))^3
    (-4 i2^2 re + ie (ie re + 2 vt))^3))

(*** Simplifcation with i2 going to zero yeilds the second-
 order coefficient as zero. ***)
```

```
Simplify[
 (((2 (-1 + e^(2 i2 re/vt)) i2 + (1 + e^(2 i2 re/vt)) ie)^3 (4 i2^2 - ie^2) vt (-4 i2 (2 i2 - ie)^3 ie
        vt^3 + 4 e^(6 i2 re/vt) i2 ie (2 i2 + ie)^3 vt^3 + e^(4 i2 re/vt) (2 i2 - ie) (2 i2 + ie)^2
        (16 i2^4 im re^2 rm - 8 i2^2 ie im re rm (ie re + 2 vt) + ie^2 im rm
            (ie re + 2 vt)^2 - 4 i2 ie vt^2 (2 im rm + 3 vt)) + e^(2 i2 re/vt) (-2 i2 + ie)^2
        (2 i2 + ie) (16 i2^4 im re^2 rm - 8 i2^2 ie im re rm (ie re + 2 vt) +
          ie^2 im rm (ie re + 2 vt)^2 + 4 i2 ie vt^2 (2 im rm + 3 vt)))) /
  (((-2 i2 + ie)^2 vt + e^(4 i2 re/vt) (2 i2 + ie)^2 vt - 2 e^(2 i2 re/vt) (4 i2^2 - ie^2) (im rm + vt))^3
    (-4 i2^2 re + ie (ie re + 2 vt))^3), i2 == 0]
0

(*** The third-order coefficient is found by repeating
   the previous steps. Differentiate → Chain rule → simplify  ***)
Simplify[
 D[((2 (-1 + e^(2 i2 re/vt)) i2 + (1 + e^(2 i2 re/vt)) ie)^3 (4 i2^2 - ie^2) vt (-4 i2 (2 i2 - ie)^3 ie
        vt^3 + 4 e^(6 i2 re/vt) i2 ie (2 i2 + ie)^3 vt^3 + e^(4 i2 re/vt) (2 i2 - ie) (2 i2 + ie)^2
        (16 i2^4 im re^2 rm - 8 i2^2 ie im re rm (ie re + 2 vt) + ie^2 im rm
            (ie re + 2 vt)^2 - 4 i2 ie vt^2 (2 im rm + 3 vt)) + e^(2 i2 re/vt) (-2 i2 + ie)^2
        (2 i2 + ie) (16 i2^4 im re^2 rm - 8 i2^2 ie im re rm (ie re + 2 vt) +
          ie^2 im rm (ie re + 2 vt)^2 + 4 i2 ie vt^2 (2 im rm + 3 vt)))) /
  (((-2 i2 + ie)^2 vt + e^(4 i2 re/vt) (2 i2 + ie)^2 vt - 2 e^(2 i2 re/vt) (4 i2^2 - ie^2)
        (im rm + vt))^3 (-4 i2^2 re + ie (ie re + 2 vt))^3), i2]]
```

$$\left(\left(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\right)^2\right.$$
$$vt\left(24\,i2\left(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\right)\right.$$
$$\left(4\,i2^2-ie^2\right)re\left(\left(-2\,i2+ie\right)^2vt+e^{\frac{4\,i2\,re}{vt}}\left(2\,i2+ie\right)^2vt-\right.$$
$$\left.2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2-ie^2\right)\left(im\,rm+vt\right)\right)\left(-4\,i2\left(2\,i2-ie\right)^3ie\,vt^3+\right.$$
$$4\,e^{\frac{6\,i2\,re}{vt}}i2\,ie\left(2\,i2+ie\right)^3vt^3+e^{\frac{4\,i2\,re}{vt}}\left(2\,i2-ie\right)\left(2\,i2+ie\right)^2$$
$$\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+ie^2\,im\,rm\right.$$
$$\left.\left(ie\,re+2\,vt\right)^2-4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)+e^{\frac{2\,i2\,re}{vt}}\left(-2\,i2+ie\right)^2$$
$$\left(2\,i2+ie\right)\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+\right.$$
$$\left.\left.ie^2\,im\,rm\left(ie\,re+2\,vt\right)^2+4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)\right)+$$
$$8\,i2\left(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\right)\left(\left(-2\,i2+ie\right)^2vt+\right.$$
$$\left.e^{\frac{4\,i2\,re}{vt}}\left(2\,i2+ie\right)^2vt-2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2-ie^2\right)\left(im\,rm+vt\right)\right)$$
$$\left(-4\,i2^2\,re+ie\left(ie\,re+2\,vt\right)\right)\left(-4\,i2\left(2\,i2-ie\right)^3ie\,vt^3+\right.$$
$$4\,e^{\frac{6\,i2\,re}{vt}}i2\,ie\left(2\,i2+ie\right)^3vt^3+e^{\frac{4\,i2\,re}{vt}}\left(2\,i2-ie\right)\left(2\,i2+ie\right)^2$$
$$\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+ie^2\,im\,rm\right.$$
$$\left.\left(ie\,re+2\,vt\right)^2-4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)+e^{\frac{2\,i2\,re}{vt}}\left(-2\,i2+ie\right)^2$$
$$\left(2\,i2+ie\right)\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+\right.$$
$$\left.\left.ie^2\,im\,rm\left(ie\,re+2\,vt\right)^2+4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)\right)+$$
$$\frac{1}{vt}6\left(4\,i2^2-ie^2\right)\left(-vt+e^{\frac{2\,i2\,re}{vt}}\left(2\,i2\,re+ie\,re+vt\right)\right)$$
$$\left(\left(-2\,i2+ie\right)^2vt+e^{\frac{4\,i2\,re}{vt}}\left(2\,i2+ie\right)^2vt-\right.$$

$$2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2-ie^2\right)(im\,rm+vt)\Big)\left(-4\,i2^2\,re+ie\,(ie\,re+2\,vt)\right)$$
$$\Big(-4\,i2\,(2\,i2-ie)^3\,ie\,vt^3+4\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2+ie)^3\,vt^3+$$
$$e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\,(2\,i2+ie)^2\left(16\,i2^4\,im\,re^2\,rm-\right.$$
$$8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2-$$
$$\left.4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2$$
$$(2\,i2+ie)\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\right.$$
$$\left.ie^2\,im\,rm\,(ie\,re+2\,vt)^2+4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)\Big)-$$
$$\frac{1}{vt}\,12\left(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\right)\left(4\,i2^2-ie^2\right)$$
$$\left(-4\,i2^2\,re+ie\,(ie\,re+2\,vt)\right)$$
$$\Big((2\,i2-ie)\,vt^2+e^{\frac{4\,i2\,re}{vt}}\,(2\,i2+ie)\,vt\,(2\,i2\,re+ie\,re+vt)-$$
$$e^{\frac{2\,i2\,re}{vt}}\,(im\,rm+vt)\left(4\,i2^2\,re-ie^2\,re+4\,i2\,vt\right)\Big)$$
$$\Big(-4\,i2\,(2\,i2-ie)^3\,ie\,vt^3+4\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2+ie)^3\,vt^3+$$
$$e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\,(2\,i2+ie)^2\left(16\,i2^4\,im\,re^2\,rm-\right.$$
$$8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2-$$
$$\left.4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2$$
$$(2\,i2+ie)\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\right.$$
$$\left.ie^2\,im\,rm\,(ie\,re+2\,vt)^2+4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)\Big)+$$
$$\left(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\right)\left(4\,i2^2-ie^2\right)$$
$$\Big((-2\,i2+ie)^2\,vt+e^{\frac{4\,i2\,re}{vt}}\,(2\,i2+ie)^2\,vt-$$
$$2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2-ie^2\right)(im\,rm+vt)\Big)$$

$$\left(-4\,i2^2\,re+ie\,(ie\,re+2\,vt)\right)\left(24\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2+ie)^3\,re\,vt^2-4\,(2\,i2-ie)^3\,ie\,vt^3-24\,i2\,ie\,(-2\,i2+ie)^2\,vt^3+24\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2+ie)^2\,vt^3+4\,e^{\frac{6\,i2\,re}{vt}}\,ie\,(2\,i2+ie)^3\,vt^3+e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\,(2\,i2+ie)^2\left(64\,i2^3\,im\,re^2\,rm-16\,i2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)-4\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2\,(2\,i2+ie)\left(64\,i2^3\,im\,re^2\,rm-16\,i2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+4\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+4\,e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\,(2\,i2+ie)\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2-4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+2\,e^{\frac{4\,i2\,re}{vt}}\,(2\,i2+ie)^2\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2-4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+\frac{1}{vt}4\,e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\,(2\,i2+ie)^2\,re\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2-4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+2\,e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2+4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)-4\,e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)\,(2\,i2+ie)\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2+4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+\frac{1}{vt}2\,e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2\,(2\,i2+ie)\,re\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2+4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)\Big)\Big)\Big/\left(\left((-2\,i2+ie)^2\,vt+e^{\frac{4\,i2\,re}{vt}}\,(2\,i2+ie)^2\,vt-2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2-ie^2\right)(im\,rm+vt)\right)^4\left(-4\,i2^2\,re+ie\,(ie\,re+2\,vt)\right)^4\right)$$

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(*** Chain rule ***)
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$$\text{Simplify}\Big[\Big(\Big(\Big(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\Big)^2\left(4\,i2^2-ie^2\right)vt\Big)\Big/$$
$$\Big(2\left(\left(-2\,i2+ie\right)^2 vt+e^{\frac{4\,i2\,re}{vt}}\left(2\,i2+ie\right)^2 vt-\right.$$
$$\left.2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2-ie^2\right)\left(im\,rm+vt\right)\right)\left(-4\,i2^2\,re+ie\left(ie\,re+2\,vt\right)\right)\Big)\Big)*$$
$$\Big(\Big(\Big(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\Big)^2 vt$$
$$\Big(24\,i2\left(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\right)\left(4\,i2^2-ie^2\right)re\left(\left(-2\,i2+ie\right)^2\right.$$
$$\left.vt+e^{\frac{4\,i2\,re}{vt}}\left(2\,i2+ie\right)^2 vt-2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2-ie^2\right)\left(im\,rm+vt\right)\right)$$
$$\Big(-4\,i2\left(2\,i2-ie\right)^3 ie\,vt^3+4\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\left(2\,i2+ie\right)^3 vt^3+$$
$$e^{\frac{4\,i2\,re}{vt}}\left(2\,i2-ie\right)\left(2\,i2+ie\right)^2\left(16\,i2^4\,im\,re^2\,rm-\right.$$
$$\left.8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+ie^2\,im\,rm\left(ie\,re+2\,vt\right)^2-\right.$$
$$\left.4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)+e^{\frac{2\,i2\,re}{vt}}\left(-2\,i2+ie\right)^2\left(2\,i2+ie\right)$$
$$\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+\right.$$
$$\left.ie^2\,im\,rm\left(ie\,re+2\,vt\right)^2+4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)\Big)+$$
$$8\,i2\left(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\right)\left(\left(-2\,i2+ie\right)^2 vt+\right.$$
$$\left.e^{\frac{4\,i2\,re}{vt}}\left(2\,i2+ie\right)^2 vt-2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2-ie^2\right)\left(im\,rm+vt\right)\right)$$
$$\left(-4\,i2^2\,re+ie\left(ie\,re+2\,vt\right)\right)\left(-4\,i2\left(2\,i2-ie\right)^3 ie\,vt^3+\right.$$
$$4\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\left(2\,i2+ie\right)^3 vt^3+e^{\frac{4\,i2\,re}{vt}}\left(2\,i2-ie\right)\left(2\,i2+ie\right)^2$$
$$\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+\right.$$
$$\left.ie^2\,im\,rm\left(ie\,re+2\,vt\right)^2-4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)+$$
$$e^{\frac{2\,i2\,re}{vt}}\left(-2\,i2+ie\right)^2\left(2\,i2+ie\right)\left(16\,i2^4\,im\,re^2\,rm-\right.$$
$$\left.8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+\right.$$

$$\text{ie}^2\,\text{im}\,\text{rm}\,(\text{ie}\,\text{re} + 2\,\text{vt})^2 + 4\,\text{i2}\,\text{ie}\,\text{vt}^2\,(2\,\text{im}\,\text{rm} + 3\,\text{vt})\Big)\Big) +$$

$$\frac{1}{\text{vt}} 6\left(4\,\text{i2}^2 - \text{ie}^2\right)\left(-\text{vt} + e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2}\,\text{re} + \text{ie}\,\text{re} + \text{vt})\right)$$

$$\Big((-2\,\text{i2} + \text{ie})^2\,\text{vt} + e^{\frac{4\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2} + \text{ie})^2\,\text{vt} -$$

$$2\,e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\left(4\,\text{i2}^2 - \text{ie}^2\right)(\text{im}\,\text{rm} + \text{vt})\Big)\left(-4\,\text{i2}^2\,\text{re} + \text{ie}\,(\text{ie}\,\text{re} + 2\,\text{vt})\right)$$

$$\Big(-4\,\text{i2}\,(2\,\text{i2} - \text{ie})^3\,\text{ie}\,\text{vt}^3 + 4\,e^{\frac{6\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{i2}\,\text{ie}\,(2\,\text{i2} + \text{ie})^3\,\text{vt}^3 +$$

$$e^{\frac{4\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2} - \text{ie})\,(2\,\text{i2} + \text{ie})^2\,\Big(16\,\text{i2}^4\,\text{im}\,\text{re}^2\,\text{rm} -$$

$$8\,\text{i2}^2\,\text{ie}\,\text{im}\,\text{re}\,\text{rm}\,(\text{ie}\,\text{re} + 2\,\text{vt}) + \text{ie}^2\,\text{im}\,\text{rm}\,(\text{ie}\,\text{re} + 2\,\text{vt})^2 -$$

$$4\,\text{i2}\,\text{ie}\,\text{vt}^2\,(2\,\text{im}\,\text{rm} + 3\,\text{vt})\Big) + e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,(-2\,\text{i2} + \text{ie})^2\,(2\,\text{i2} + \text{ie})$$

$$\Big(16\,\text{i2}^4\,\text{im}\,\text{re}^2\,\text{rm} - 8\,\text{i2}^2\,\text{ie}\,\text{im}\,\text{re}\,\text{rm}\,(\text{ie}\,\text{re} + 2\,\text{vt}) +$$

$$\text{ie}^2\,\text{im}\,\text{rm}\,(\text{ie}\,\text{re} + 2\,\text{vt})^2 + 4\,\text{i2}\,\text{ie}\,\text{vt}^2\,(2\,\text{im}\,\text{rm} + 3\,\text{vt})\Big)\Big) -$$

$$\frac{1}{\text{vt}} 12\left(2\left(-1 + e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\right)\text{i2} + \left(1 + e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\right)\text{ie}\right)\left(4\,\text{i2}^2 - \text{ie}^2\right)$$

$$\left(-4\,\text{i2}^2\,\text{re} + \text{ie}\,(\text{ie}\,\text{re} + 2\,\text{vt})\right)$$

$$\Big((2\,\text{i2} - \text{ie})\,\text{vt}^2 + e^{\frac{4\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2} + \text{ie})\,\text{vt}\,(2\,\text{i2}\,\text{re} + \text{ie}\,\text{re} + \text{vt}) -$$

$$e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,(\text{im}\,\text{rm} + \text{vt})\left(4\,\text{i2}^2\,\text{re} - \text{ie}^2\,\text{re} + 4\,\text{i2}\,\text{vt}\right)\Big)$$

$$\Big(-4\,\text{i2}\,(2\,\text{i2} - \text{ie})^3\,\text{ie}\,\text{vt}^3 + 4\,e^{\frac{6\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{i2}\,\text{ie}\,(2\,\text{i2} + \text{ie})^3\,\text{vt}^3 +$$

$$e^{\frac{4\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2} - \text{ie})\,(2\,\text{i2} + \text{ie})^2\,\Big(16\,\text{i2}^4\,\text{im}\,\text{re}^2\,\text{rm} -$$

$$8\,\text{i2}^2\,\text{ie}\,\text{im}\,\text{re}\,\text{rm}\,(\text{ie}\,\text{re} + 2\,\text{vt}) + \text{ie}^2\,\text{im}\,\text{rm}\,(\text{ie}\,\text{re} + 2\,\text{vt})^2 -$$

$$4\,\text{i2}\,\text{ie}\,\text{vt}^2\,(2\,\text{im}\,\text{rm} + 3\,\text{vt})\Big) + e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,(-2\,\text{i2} + \text{ie})^2\,(2\,\text{i2} + \text{ie})$$

$$\Big(16\,\text{i2}^4\,\text{im}\,\text{re}^2\,\text{rm} - 8\,\text{i2}^2\,\text{ie}\,\text{im}\,\text{re}\,\text{rm}\,(\text{ie}\,\text{re} + 2\,\text{vt}) +$$

$$\text{ie}^2\,\text{im}\,\text{rm}\,(\text{ie}\,\text{re} + 2\,\text{vt})^2 + 4\,\text{i2}\,\text{ie}\,\text{vt}^2\,(2\,\text{im}\,\text{rm} + 3\,\text{vt})\Big)\Big) +$$

$$\left(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\right)\left(4\,i2^2-ie^2\right)$$
$$\left(\left(-2\,i2+ie\right)^2 vt+e^{\frac{4\,i2\,re}{vt}}\left(2\,i2+ie\right)^2 vt-\right.$$
$$\left.2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2-ie^2\right)\left(im\,rm+vt\right)\right)\left(-4\,i2^2\,re+ie\left(ie\,re+2\,vt\right)\right)$$
$$\left(24\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\left(2\,i2+ie\right)^3 re\,vt^2-4\left(2\,i2-ie\right)^3 ie\,vt^3-\right.$$
$$24\,i2\,ie\left(-2\,i2+ie\right)^2 vt^3+24\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\left(2\,i2+ie\right)^2 vt^3+$$
$$4\,e^{\frac{6\,i2\,re}{vt}}\,ie\left(2\,i2+ie\right)^3 vt^3+e^{\frac{4\,i2\,re}{vt}}\left(2\,i2-ie\right)\left(2\,i2+ie\right)^2$$
$$\left(64\,i2^3\,im\,re^2\,rm-16\,i2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)-\right.$$
$$\left.4\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)+e^{\frac{2\,i2\,re}{vt}}\left(-2\,i2+ie\right)^2\left(2\,i2+ie\right)$$
$$\left(64\,i2^3\,im\,re^2\,rm-16\,i2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+\right.$$
$$\left.4\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)+4\,e^{\frac{4\,i2\,re}{vt}}\left(2\,i2-ie\right)\left(2\,i2+ie\right)$$
$$\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+ie^2\,im\right.$$
$$\left.rm\left(ie\,re+2\,vt\right)^2-4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)+2\,e^{\frac{4\,i2\,re}{vt}}$$
$$\left(2\,i2+ie\right)^2\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+\right.$$
$$\left.ie^2\,im\,rm\left(ie\,re+2\,vt\right)^2-4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)+$$
$$\frac{1}{vt}4\,e^{\frac{4\,i2\,re}{vt}}\left(2\,i2-ie\right)\left(2\,i2+ie\right)^2 re\left(16\,i2^4\,im\,re^2\,rm-\right.$$
$$8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+ie^2\,im\,rm\left(ie\,re+2\,vt\right)^2-$$
$$\left.4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)+2\,e^{\frac{2\,i2\,re}{vt}}\left(-2\,i2+ie\right)^2$$
$$\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+\right.$$
$$\left.ie^2\,im\,rm\left(ie\,re+2\,vt\right)^2+4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)-$$
$$4\,e^{\frac{2\,i2\,re}{vt}}\left(-2\,i2+ie\right)\left(2\,i2+ie\right)\left(16\,i2^4\,im\,re^2\,rm-\right.$$
$$8\,i2^2\,ie\,im\,re\,rm\left(ie\,re+2\,vt\right)+ie^2\,im\,rm\left(ie\,re+2\,vt\right)^2+$$
$$\left.4\,i2\,ie\,vt^2\left(2\,im\,rm+3\,vt\right)\right)+\frac{1}{vt}2\,e^{\frac{2\,i2\,re}{vt}}\left(-2\,i2+ie\right)^2$$

$$(2\,i2 + ie)\,re\left(16\,i2^4\,im\,re^2\,rm - 8\,i2^2\,ie\,im\,re\,rm\,(ie\,re + 2\,vt) + ie^2\,im\,rm\,(ie\,re + 2\,vt)^2 + 4\,i2\,ie\,vt^2\,(2\,im\,rm + 3\,vt)\right)\Big)\Big)\Big/$$

$$\Big(\Big((-2\,i2 + ie)^2\,vt + e^{\frac{4\,i2\,re}{vt}}\,(2\,i2 + ie)^2\,vt - 2\,e^{\frac{2\,i2\,re}{vt}}\,\left(4\,i2^2 - ie^2\right)(im\,rm + vt)\Big)^4\left(-4\,i2^2\,re + ie\,(ie\,re + 2\,vt)\right)^4\Big)\Big)\Big]$$

$$\Big(\Big(2\left(-1 + e^{\frac{2\,i2\,re}{vt}}\right)i2 + \left(1 + e^{\frac{2\,i2\,re}{vt}}\right)ie\Big)^4 \left(4\,i2^2 - ie^2\right)vt^2\Big(24\,i2\left(2\left(-1 + e^{\frac{2\,i2\,re}{vt}}\right)i2 + \left(1 + e^{\frac{2\,i2\,re}{vt}}\right)ie\right)\left(4\,i2^2 - ie^2\right)re\Big((-2\,i2 + ie)^2\,vt + e^{\frac{4\,i2\,re}{vt}}\,(2\,i2 + ie)^2\,vt - 2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2 - ie^2\right)(im\,rm + vt)\Big)\Big(-4\,i2\,(2\,i2 - ie)^3\,ie\,vt^3 + 4\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2 + ie)^3\,vt^3 + e^{\frac{4\,i2\,re}{vt}}\,(2\,i2 - ie)\,(2\,i2 + ie)^2\left(16\,i2^4\,im\,re^2\,rm - 8\,i2^2\,ie\,im\,re\,rm\,(ie\,re + 2\,vt) + ie^2\,im\,rm\,(ie\,re + 2\,vt)^2 - 4\,i2\,ie\,vt^2\,(2\,im\,rm + 3\,vt)\right) + e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2 + ie)^2\,(2\,i2 + ie)\left(16\,i2^4\,im\,re^2\,rm - 8\,i2^2\,ie\,im\,re\,rm\,(ie\,re + 2\,vt) + ie^2\,im\,rm\,(ie\,re + 2\,vt)^2 + 4\,i2\,ie\,vt^2\,(2\,im\,rm + 3\,vt)\right)\Big) + 8\,i2\left(2\left(-1 + e^{\frac{2\,i2\,re}{vt}}\right)i2 + \left(1 + e^{\frac{2\,i2\,re}{vt}}\right)ie\right)\Big((-2\,i2 + ie)^2\,vt + e^{\frac{4\,i2\,re}{vt}}\,(2\,i2 + ie)^2\,vt - 2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2 - ie^2\right)(im\,rm + vt)\Big)\left(-4\,i2^2\,re + ie\,(ie\,re + 2\,vt)\right)\Big(-4\,i2\,(2\,i2 - ie)^3\,ie\,vt^3 + 4\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2 + ie)^3\,vt^3 + e^{\frac{4\,i2\,re}{vt}}\,(2\,i2 - ie)\,(2\,i2 + ie)^2\left(16\,i2^4\,im\,re^2\,rm - 8\,i2^2\,ie\,im\,re\,rm\,(ie\,re + 2\,vt) + ie^2\,im\,rm\,(ie\,re + 2\,vt)^2 - 4\,i2\,ie\,vt^2\,(2\,im\,rm + 3\,vt)\right) + e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2 + ie)^2\,(2\,i2 + ie)\left(16\,i2^4\,im\,re^2\,rm - 8\,i2^2\,ie\,im\,re\,rm\,(ie\,re + 2\,vt) +\right.$$

$$
\begin{aligned}
&\left. \text{ie}^2\,\text{im}\,\text{rm}\,(\text{ie}\,\text{re}+2\,\text{vt})^2+4\,\text{i2}\,\text{ie}\,\text{vt}^2\,(2\,\text{im}\,\text{rm}+3\,\text{vt})\right)+\\
&\frac{1}{\text{vt}}6\left(4\,\text{i2}^2-\text{ie}^2\right)\left(-\text{vt}+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2}\,\text{re}+\text{ie}\,\text{re}+\text{vt})\right)\\
&\quad\left((-2\,\text{i2}+\text{ie})^2\,\text{vt}+e^{\frac{4\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2}+\text{ie})^2\,\text{vt}-\right.\\
&\qquad\left.2\,e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\left(4\,\text{i2}^2-\text{ie}^2\right)(\text{im}\,\text{rm}+\text{vt})\right)\left(-4\,\text{i2}^2\,\text{re}+\text{ie}\,(\text{ie}\,\text{re}+2\,\text{vt})\right)\\
&\quad\left(-4\,\text{i2}\,(2\,\text{i2}-\text{ie})^3\,\text{ie}\,\text{vt}^3+4\,e^{\frac{6\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{i2}\,\text{ie}\,(2\,\text{i2}+\text{ie})^3\,\text{vt}^3+\right.\\
&\qquad e^{\frac{4\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2}-\text{ie})\,(2\,\text{i2}+\text{ie})^2\left(16\,\text{i2}^4\,\text{im}\,\text{re}^2\,\text{rm}-\right.\\
&\qquad\quad\left.8\,\text{i2}^2\,\text{ie}\,\text{im}\,\text{re}\,\text{rm}\,(\text{ie}\,\text{re}+2\,\text{vt})+\text{ie}^2\,\text{im}\,\text{rm}\,(\text{ie}\,\text{re}+2\,\text{vt})^2-\right.\\
&\qquad\quad\left.4\,\text{i2}\,\text{ie}\,\text{vt}^2\,(2\,\text{im}\,\text{rm}+3\,\text{vt})\right)+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,(-2\,\text{i2}+\text{ie})^2\\
&\qquad(2\,\text{i2}+\text{ie})\left(16\,\text{i2}^4\,\text{im}\,\text{re}^2\,\text{rm}-8\,\text{i2}^2\,\text{ie}\,\text{im}\,\text{re}\,\text{rm}\,(\text{ie}\,\text{re}+2\,\text{vt})+\right.\\
&\qquad\quad\left.\left.\text{ie}^2\,\text{im}\,\text{rm}\,(\text{ie}\,\text{re}+2\,\text{vt})^2+4\,\text{i2}\,\text{ie}\,\text{vt}^2\,(2\,\text{im}\,\text{rm}+3\,\text{vt})\right)\right)-\\
&\frac{1}{\text{vt}}12\left(2\left(-1+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\right)\text{i2}+\left(1+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\right)\text{ie}\right)\left(4\,\text{i2}^2-\text{ie}^2\right)\\
&\quad\left(-4\,\text{i2}^2\,\text{re}+\text{ie}\,(\text{ie}\,\text{re}+2\,\text{vt})\right)\\
&\quad\left((2\,\text{i2}-\text{ie})\,\text{vt}^2+e^{\frac{4\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2}+\text{ie})\,\text{vt}\,(2\,\text{i2}\,\text{re}+\text{ie}\,\text{re}+\text{vt})-\right.\\
&\qquad\left.e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,(\text{im}\,\text{rm}+\text{vt})\left(4\,\text{i2}^2\,\text{re}-\text{ie}^2\,\text{re}+4\,\text{i2}\,\text{vt}\right)\right)\\
&\quad\left(-4\,\text{i2}\,(2\,\text{i2}-\text{ie})^3\,\text{ie}\,\text{vt}^3+4\,e^{\frac{6\,\text{i2}\,\text{re}}{\text{vt}}}\,\text{i2}\,\text{ie}\,(2\,\text{i2}+\text{ie})^3\,\text{vt}^3+\right.\\
&\qquad e^{\frac{4\,\text{i2}\,\text{re}}{\text{vt}}}\,(2\,\text{i2}-\text{ie})\,(2\,\text{i2}+\text{ie})^2\left(16\,\text{i2}^4\,\text{im}\,\text{re}^2\,\text{rm}-\right.\\
&\qquad\quad\left.8\,\text{i2}^2\,\text{ie}\,\text{im}\,\text{re}\,\text{rm}\,(\text{ie}\,\text{re}+2\,\text{vt})+\text{ie}^2\,\text{im}\,\text{rm}\,(\text{ie}\,\text{re}+2\,\text{vt})^2-\right.\\
&\qquad\quad\left.4\,\text{i2}\,\text{ie}\,\text{vt}^2\,(2\,\text{im}\,\text{rm}+3\,\text{vt})\right)+e^{\frac{2\,\text{i2}\,\text{re}}{\text{vt}}}\,(-2\,\text{i2}+\text{ie})^2\\
&\qquad(2\,\text{i2}+\text{ie})\left(16\,\text{i2}^4\,\text{im}\,\text{re}^2\,\text{rm}-8\,\text{i2}^2\,\text{ie}\,\text{im}\,\text{re}\,\text{rm}\,(\text{ie}\,\text{re}+2\,\text{vt})+\right.\\
&\qquad\quad\left.\left.\text{ie}^2\,\text{im}\,\text{rm}\,(\text{ie}\,\text{re}+2\,\text{vt})^2+4\,\text{i2}\,\text{ie}\,\text{vt}^2\,(2\,\text{im}\,\text{rm}+3\,\text{vt})\right)\right)+
\end{aligned}
$$

$$\left(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\right)\left(4\,i2^2-ie^2\right)$$
$$\left((-2\,i2+ie)^2\,vt+e^{\frac{4\,i2\,re}{vt}}\,(2\,i2+ie)^2\,vt-\right.$$
$$\left.2\,e^{\frac{2\,i2\,re}{vt}}\left(4\,i2^2-ie^2\right)(im\,rm+vt)\right)$$
$$\left(-4\,i2^2\,re+ie\,(ie\,re+2\,vt)\right)\left(24\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2+ie)^3\,re\,vt^2-\right.$$
$$4\,(2\,i2-ie)^3\,ie\,vt^3-24\,i2\,ie\,(-2\,i2+ie)^2\,vt^3+$$
$$24\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2+ie)^2\,vt^3+4\,e^{\frac{6\,i2\,re}{vt}}\,ie\,(2\,i2+ie)^3\,vt^3+$$
$$e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\,(2\,i2+ie)^2\left(64\,i2^3\,im\,re^2\,rm-\right.$$
$$\left.16\,i2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)-4\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+$$
$$e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2\,(2\,i2+ie)\left(64\,i2^3\,im\,re^2\,rm-16\,i2\,ie\,im\,re\right.$$
$$\left.rm\,(ie\,re+2\,vt)+4\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+4\,e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)$$
$$(2\,i2+ie)\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\right.$$
$$\left.ie^2\,im\,rm\,(ie\,re+2\,vt)^2-4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+$$
$$2\,e^{\frac{4\,i2\,re}{vt}}\,(2\,i2+ie)^2\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\right.$$
$$\left.ie^2\,im\,rm\,(ie\,re+2\,vt)^2-4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+$$
$$\frac{1}{vt}\,4\,e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\,(2\,i2+ie)^2\,re$$
$$\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\right.$$
$$\left.ie^2\,im\,rm\,(ie\,re+2\,vt)^2-4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+2\,e^{\frac{2\,i2\,re}{vt}}$$
$$(-2\,i2+ie)^2\left(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\right.$$
$$\left.ie^2\,im\,rm\,(ie\,re+2\,vt)^2+4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)-$$
$$4\,e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)\,(2\,i2+ie)\left(16\,i2^4\,im\,re^2\,rm-\right.$$
$$\left.8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2+\right.$$
$$\left.4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\right)+\frac{1}{vt}\,2\,e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2\,(2\,i2+ie)$$

```
        re (16 i2^4 im re^2 rm - 8 i2^2 ie im re rm (ie re + 2 vt) +
          ie^2 im rm (ie re + 2 vt)^2 + 4 i2 ie vt^2 (2 im rm + 3 vt)))) /
 (2 ((-2 i2 + ie)^2 vt + e^(4 i2 re / vt) (2 i2 + ie)^2 vt - 2 e^(2 i2 re / vt) (4 i2^2 - ie^2) (im rm + vt))^5
   (-4 i2^2 re + ie (ie re + 2 vt))^5)

(**Third non-ideal differential**)

Simplify[((2 (-1 + e^(2 i2 re / vt)) i2 + (1 + e^(2 i2 re / vt)) ie)^4 (4 i2^2 - ie^2) vt^2
    (24 i2 (2 (-1 + e^(2 i2 re / vt)) i2 + (1 + e^(2 i2 re / vt)) ie) (4 i2^2 - ie^2) re ((-2 i2 + ie)^2
        vt + e^(4 i2 re / vt) (2 i2 + ie)^2 vt - 2 e^(2 i2 re / vt) (4 i2^2 - ie^2) (im rm + vt))
      (-4 i2 (2 i2 - ie)^3 ie vt^3 + 4 e^(6 i2 re / vt) i2 ie (2 i2 + ie)^3 vt^3 +
        e^(4 i2 re / vt) (2 i2 - ie) (2 i2 + ie)^2 (16 i2^4 im re^2 rm -
          8 i2^2 ie im re rm (ie re + 2 vt) + ie^2 im rm (ie re + 2 vt)^2 -
          4 i2 ie vt^2 (2 im rm + 3 vt)) + e^(2 i2 re / vt) (-2 i2 + ie)^2 (2 i2 + ie)
         (16 i2^4 im re^2 rm - 8 i2^2 ie im re rm (ie re + 2 vt) +
          ie^2 im rm (ie re + 2 vt)^2 + 4 i2 ie vt^2 (2 im rm + 3 vt))) +
     8 i2 (2 (-1 + e^(2 i2 re / vt)) i2 + (1 + e^(2 i2 re / vt)) ie) ((-2 i2 + ie)^2 vt +
        e^(4 i2 re / vt) (2 i2 + ie)^2 vt - 2 e^(2 i2 re / vt) (4 i2^2 - ie^2) (im rm + vt))
      (-4 i2^2 re + ie (ie re + 2 vt)) (-4 i2 (2 i2 - ie)^3 ie vt^3 +
        4 e^(6 i2 re / vt) i2 ie (2 i2 + ie)^3 vt^3 + e^(4 i2 re / vt) (2 i2 - ie) (2 i2 + ie)^2
         (16 i2^4 im re^2 rm - 8 i2^2 ie im re rm (ie re + 2 vt) +
```

$$
\begin{aligned}
&\quad ie^2\,im\,rm\,(ie\,re+2\,vt)^2-4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\big)+\\
&e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2\,(2\,i2+ie)\,\big(16\,i2^4\,im\,re^2\,rm-\\
&\quad 8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\\
&\quad ie^2\,im\,rm\,(ie\,re+2\,vt)^2+4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\big)\Big)+\\
&\frac{1}{vt}\,6\,\left(4\,i2^2-ie^2\right)\,\left(-vt+e^{\frac{2\,i2\,re}{vt}}\,(2\,i2\,re+ie\,re+vt)\right)\\
&\Big((-2\,i2+ie)^2\,vt+e^{\frac{4\,i2\,re}{vt}}\,(2\,i2+ie)^2\,vt-\\
&\quad 2\,e^{\frac{2\,i2\,re}{vt}}\,\left(4\,i2^2-ie^2\right)\,(im\,rm+vt)\Big)\,\left(-4\,i2^2\,re+ie\,(ie\,re+2\,vt)\right)\\
&\Big(-4\,i2\,(2\,i2-ie)^3\,ie\,vt^3+4\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2+ie)^3\,vt^3+\\
&\quad e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\,(2\,i2+ie)^2\,\big(16\,i2^4\,im\,re^2\,rm-\\
&\quad 8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2-\\
&\quad 4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\big)+e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2\,(2\,i2+ie)\\
&\quad \big(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\\
&\quad ie^2\,im\,rm\,(ie\,re+2\,vt)^2+4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\big)\Big)-\\
&\frac{1}{vt}\,12\,\left(2\,\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)\,i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)\,ie\right)\,\left(4\,i2^2-ie^2\right)\\
&\Big(-4\,i2^2\,re+ie\,(ie\,re+2\,vt)\Big)\\
&\Big((2\,i2-ie)\,vt^2+e^{\frac{4\,i2\,re}{vt}}\,(2\,i2+ie)\,vt\,(2\,i2\,re+ie\,re+vt)-\\
&\quad e^{\frac{2\,i2\,re}{vt}}\,(im\,rm+vt)\,\left(4\,i2^2\,re-ie^2\,re+4\,i2\,vt\right)\Big)\\
&\Big(-4\,i2\,(2\,i2-ie)^3\,ie\,vt^3+4\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2+ie)^3\,vt^3+\\
&\quad e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\,(2\,i2+ie)^2\,\big(16\,i2^4\,im\,re^2\,rm-\\
&\quad 8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2-
\end{aligned}
$$

$$
\begin{aligned}
&4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\Big)+e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2\,(2\,i2+ie)\\
&\Big(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\\
&ie^2\,im\,rm\,(ie\,re+2\,vt)^2+4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\Big)\Big)+\\
&\Big(2\left(-1+e^{\frac{2\,i2\,re}{vt}}\right)i2+\left(1+e^{\frac{2\,i2\,re}{vt}}\right)ie\Big)\,\left(4\,i2^2-ie^2\right)\,\Big((-2\,i2+ie)^2\,vt+\\
&e^{\frac{4\,i2\,re}{vt}}\,(2\,i2+ie)^2\,vt-2\,e^{\frac{2\,i2\,re}{vt}}\,\left(4\,i2^2-ie^2\right)\,(im\,rm+vt)\Big)\\
&\left(-4\,i2^2\,re+ie\,(ie\,re+2\,vt)\right)\,\Big(24\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2+ie)^3\,re\,vt^2-\\
&4\,(2\,i2-ie)^3\,ie\,vt^3-24\,i2\,ie\,(-2\,i2+ie)^2\,vt^3+\\
&24\,e^{\frac{6\,i2\,re}{vt}}\,i2\,ie\,(2\,i2+ie)^2\,vt^3+4\,e^{\frac{6\,i2\,re}{vt}}\,ie\,(2\,i2+ie)^3\,vt^3+\\
&e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\,(2\,i2+ie)^2\,\Big(64\,i2^3\,im\,re^2\,rm-\\
&16\,i2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)-4\,ie\,vt^2\,(2\,im\,rm+3\,vt)\Big)+\\
&e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2\,(2\,i2+ie)\,\Big(64\,i2^3\,im\,re^2\,rm-16\,i2\,ie\,im\,re\\
&rm\,(ie\,re+2\,vt)+4\,ie\,vt^2\,(2\,im\,rm+3\,vt)\Big)+4\,e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\\
&(2\,i2+ie)\,\Big(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\\
&ie^2\,im\,rm\,(ie\,re+2\,vt)^2-4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\Big)+2\,e^{\frac{4\,i2\,re}{vt}}\\
&(2\,i2+ie)^2\,\Big(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\\
&ie^2\,im\,rm\,(ie\,re+2\,vt)^2-4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\Big)+\\
&\frac{1}{vt}\,4\,e^{\frac{4\,i2\,re}{vt}}\,(2\,i2-ie)\,(2\,i2+ie)^2\,re\,\Big(16\,i2^4\,im\,re^2\,rm-\\
&8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2-\\
&4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\Big)+2\,e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)^2\\
&\Big(16\,i2^4\,im\,re^2\,rm-8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+\\
&ie^2\,im\,rm\,(ie\,re+2\,vt)^2+4\,i2\,ie\,vt^2\,(2\,im\,rm+3\,vt)\Big)-\\
&4\,e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2+ie)\,(2\,i2+ie)\,\Big(16\,i2^4\,im\,re^2\,rm-\\
&8\,i2^2\,ie\,im\,re\,rm\,(ie\,re+2\,vt)+ie^2\,im\,rm\,(ie\,re+2\,vt)^2+
\end{aligned}
$$

$$4\,i2\,ie\,vt^2\,(2\,im\,rm + 3\,vt)\Big) + \frac{1}{vt}\,2\,e^{\frac{2\,i2\,re}{vt}}\,(-2\,i2 + ie)^2\,(2\,i2 + ie)$$
$$re\,\Big(16\,i2^4\,im\,re^2\,rm - 8\,i2^2\,ie\,im\,re\,rm\,(ie\,re + 2\,vt) +$$
$$ie^2\,im\,rm\,(ie\,re + 2\,vt)^2 + 4\,i2\,ie\,vt^2\,(2\,im\,rm + 3\,vt)\Big)\Big)\Big)\Big/$$
$$\Big(2\,\Big((-2\,i2 + ie)^2\,vt + e^{\frac{4\,i2\,re}{vt}}\,(2\,i2 + ie)^2\,vt - 2\,e^{\frac{2\,i2\,re}{vt}}\,\left(4\,i2^2 - ie^2\right)$$
$$(im\,rm + vt)\Big)^5$$
$$\left(-4\,i2^2\,re + ie\,(ie\,re + 2\,vt)\right)^5\Big),\ i2 == 0\Big]$$
$$-\left(2\,ie\,vt\,\left(ie^3\,im\,re^3\,rm + 6\,ie^2\,im\,re^2\,rm\,vt + 12\,ie\,im\,re\,rm\,vt^2 - 16\,vt^4\right)\right)\Big/$$
$$\left((ie\,re + 2\,vt)^4\,(im\,rm + 2\,vt)^4\right)$$

```
(*** This is the coefficient describing the third order transconductance from
 the main amplifier input voltage to the error ampifier output current. ***)
```

```
(*** Summary of the coefficients for the non-ideal Error amplifier. ***)
```

$$First = -\frac{ie\,vt}{(ie\,re + 2\,vt)\,(im\,rm + 2\,vt)}$$

$$Second = 0$$

$$Third = -\frac{2\,ie\,vt\,\left(ie^3\,im\,re^3\,rm + 6\,ie^2\,im\,re^2\,rm\,vt + 12\,ie\,im\,re\,rm\,vt^2 - 16\,vt^4\right)}{(ie\,re + 2\,vt)^4\,(im\,rm + 2\,vt)^4}$$

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