Efficiency Improvement of LDO Output Based Linear Regulator With Supercapacitor Energy Recovery – A versatile new technique with an example of a 5V to 1.5V version

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By

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THE UNIVERSITY OF
WAIKATO
Te Whare Wānanga o Waikato

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To my parents

Zainul Abidin Ibrahim
Masenah Ibrahim

To my wife and son

Hazrina Ghazali

Ihtisham Akid

To our twins

Harzan Rayyan Juani
Hariez Rayyan Juani

Abstract

Supercapacitors are used in various industrial applications and the supercapacitors technology is gradually progressing into a mature state. Common applications of supercapacitors are in electric vehicles, hybrid electric vehicles, uninterruptible power supply (UPS) and in portable devices such as cellular phones and laptops. The capacitance values range from fractional Farads to few thousand Farads and their continuos DC voltage ratings are from 2V to 6V.

At University of Waikato, a team works on using supercapacitors for improving the efficiency of linear voltage regulators. In particular, this patented technique aims at combining off the shelfs LDO ICs and a supercapacitor array for improving end to end efficiency of linear regulator.

My work is aimed at developing the theoretical background and designing prototype circuitry for a voltage regulator for the case of unregulated input supply is more than 3 times of the minimum input voltage requirement of the LDO which is applicable for a 5V to 1.5V regulator. Experimental results are indicated with future suggestions for improvement

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Chapter 1 – Introduction

1.1 Background

With the high demand of worldwide portable electronic products such as notebooks, PDAs, camcorders, digital cameras, mobile phones and laptops, its boosts the needs for a compact, lightweight and powerful energy storage than ever. In these circumstances, time is very high. This is due to incorporation of more features required in mobile electronics product and also for a wireless network application. The manufacturers of these portable products have spent a lot of time and money towards research to optimize power usage and efficiency; including power management circuits and new battery technologies. The optimization in these two areas must be parallel with the environmental impact of the product as well.

1.2 DC-DC Converter

DC-DC converter is an electronic circuit that converts a source of direct current (DC) from one voltage level to another level, either lower or higher voltage than the input. There are two types of dc-dc converters: linear and switching regulator. A linear regulator has more advantages compared with switching regulator in terms of cost and output noise but it comes with low efficiency. Table 1 below is the comparison of basic differences between linear regulator and switching regulator.

Table 1.1 : Comparison basic differences between linear and switching regulator

	Linear	Switching
Function	Only steps down; input voltage must be greater than output.	Steps up, steps down, or inverts
Efficiency	*Low to medium, but actual battery life depends on load current and battery voltage over time; high if V_{IN}-V_{OUT} difference is small.*	*High, except at very low load currents (µA), where switch-mode quiescent current is usually higher.*
Waste Heat	High, if average load and/or input/output voltage difference are high	Low, as components usually run cool for power levels below 10W
Complexity	Low, which usually requires only the regulator and low-value bypass capacitors	Medium to high, which usually requires inductor, diode, and filter caps in addition to the IC; for high-power circuits, external FETs are needed
Size	Small to medium in portable designs, but may be larger if heatsinking is needed	Larger than linear at low power, but smaller at power levels for which linear requires a heat sink
Total Cost	Low	Medium to high, largely due to external components
Ripple/Noise	Low; no ripple, low noise, better noise rejection.	Medium to high, due to ripple at switching rate

From the table above, generally linear regulators have more advantages than switching regulators in term of simplicity and cost but not efficiency. Due to this factor, a study has been carried out to increase the efficiency of LDO linear regulator. The efficiency of the LDO is increased using supercapacitor energy recovery technique that has been successfully developed in 12V to 5V regulator.

1.3 Supercapacitor

As we know, capacitors are to store energy and normally in the range of microfarad to picofarad. The technology of supercapacitors (also known as ultracapacitors) came into wide usage in the industry a decade ago. The supercapacitors value had increase up from few Farads until 5000 Farads. This makes supercapacitors store more energy than the normal capacitor. Due to very large capacitance value in supercapacitors, if ideal, they can be used as lossless voltage droppers in the series path of a linear regulator circuit, without blocking the circuit for a reasonably longer time.

1.4 Low Dropout (LDO) Regulator

Low dropout regulator is a linear regulator that can operate even when the difference between input and output voltage is small. The advantages of low dropout regulators are including lower minimum operating voltage, high efficiency, noise sensitive, fast transient load and lower heat dissipation. The application of LDO is suitable to be applied to this technique because the minimum input of the LDO will be 1.6V and the output of the LDO 1.5V. This means very low dropout between the input/output voltages that is only 100mV.

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Chapter 2 – Literature Review

2.1 DC-DC Converter Fundamentals

In the world of electronics today, DC-DC converters are classified into two types: linear voltage regulators and switching voltage regulators; depending on the circuit implementation. Power losses are unavoidable in both types of voltage regulator and affect the lifetime of the battery; wasting about 10% to 40% of the total energy consumed by the system. Figure 2.1 indicates the typical current flow path and nontrivial power loss in the dc-dc converter results in a short battery life despite lower power dissipation of the digital system [1].

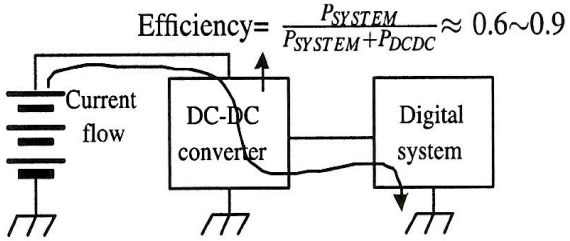


Figure 2. 1: Typical current flow path. Nontrivial power loss in the dc-dc converter results in a short battery life despite lower power dissipation of the digital system (Source: Yongseok et al [1])

It is known that switching regulators achieves better power efficiency than linear regulators, which have low efficiency due to the use of bulky heat sinks, cooling fans and isolation transformers. This makes linear regulators unfit for most modern compact electronic systems [2]. Linear voltage regulators can only step-down an input voltage to produce a lower output voltage and are available with either a fixed output voltage or a variable output voltage when using external biasing resistors. This is achievable by operating a bipolar transistor (current controlled, current source) or MOSFET (voltage controlled, current source) pass device in its linear operating mode. Control signal which drives the pass device is proportionally changed to maintain the required output voltage [3]. The

advantage of a linear regulator is its simple implementation, minimal parts (just the IC in case of fixed output) and low output ripple. A linear regulator is suitable when the difference between input and output voltage is minimal and converter efficiency is not a concern [4]. Despite the increasing use of switching regulators, linear regulators continue to enjoy widespread use because they are easily implemented and have much better noise and drift characteristic than switching regulators. In addition, linear regulators do not radiate RF, function with standard magnetics, and are easily frequency compensated and have a fast respond.

Excess energy is dissipated as heat and because of this, linear regulators are associated with excessive dissipation, inefficiency, high operating temperature and the need for large heat sinks. The major disadvantage of linear regulators is low efficiency that can be overcome by minimizing the input-to-output voltage across the regulator. The smaller the difference between input and output, the lower the power loss. The minimum input/output voltage required to support regulation is called 'dropout voltage' [5]. One way to improve efficiency is to apply a very low frequency supercapacitor circulation technique at the input side of a LDO regulator IC as developed by Kularatna et al [6].

For low-power or high-current converters, a switching regulator is mostly used except when low noise or low cost is particularly important. Increasing the efficiency of switching regulators is a problem that has been addressed by several studies that focused on more efficient circuit configuration, circuit modification, investigation of sources of power loss in DC-DC converters, and developing dissipation models of input/output characteristics and converter parameters. A simulation developed by Simunic et al [7] for cycle-accurate simulation of performance and energy consumption in an embedded system with a DC-DC converter showed that the regulator consumed a significant fraction of the total energy consumption.

2.1.1 Modes of Operation of Switching Regulator

Within the switching regulator, there are two major operational modes for DC-DC converter: forward mode and flyback mode. The modes differ in the way the magnetic component operates and each mode has its advantages and disadvantages.

2.1.1.1 Forward Mode Converters

A forward mode converter is identified by the L-C filters on its output that creates a DC output voltage which is essential for the volt-time average of the L-C filter input AC rectangular waveform. This can be expressed as:

$$Vout \approx Vin * dutycycle \tag{1}$$

The switching power supply controller varies the duty cycle of the input regulator voltage waveform and thus control the signal's volt-time average. The buck or step-down converter is the simplest forward mode converter as shown in Figure 2.2.

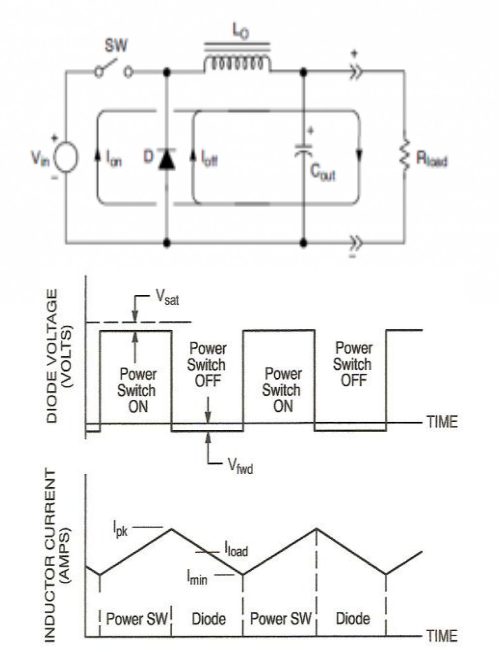


Figure 2. 2: Basic forward-mode converter and waveforms (Buck converter)

Its operation can be divided into two time periods, when the power is tuned on and turned off. When the switch is on, the input voltage is directly connected to the input of the L-C filter. Assuming the converter is in a steady-state, there is the output voltage on the filter's output. The inductor current begins a linear ramp from an initial current dictated by the remaining flux in the inductor. The inductor current is given by:

$$i_L(on) = \frac{(Vout - Vin)}{L} t + i_{init} \qquad 0 \le t \le t_{on} \qquad (2)$$

During this period, energy is stored as magnetic flux within the core of the inductor. When the switch is off, the core contains enough energy to supply the load during the following off period plus some reserve energy. The voltage on the input side of the inductor tries to fly below ground, but it clamped when the catch diode D become forward biased. The stored energy then continues flowing to the output through the catch diode and the inductor. The inductor current decreases from an initial value i_{pk} and is given by

$$i_L(off) = i_{pk} - \frac{Vout}{L} t \qquad 0 \le t \le t_{off} \qquad (3)$$

The off period continues until the controller turns the power switch back on and the cycle is repeated.

The buck converter is capable of over one kilowatt of output power but typically used for on-board regulator applications whose output power are less than 100 watts. Forward mode converter exhibits lower output peak-to-peak ripple voltage compare with the flyback converter. The disadvantage is that it is a step down topology only. Since it is not an isolated topology, for safety reason the forward converter cannot be used for input voltage greater than 42.5V DC [3].

2.1.1.2 Flyback Mode Converter

It is based on the same components as the forward mode converter but in a different arrangement. Consequently, it operates in a different way from the forward mode converter. The most elementary flyback mode converter, the boost or step-up converter is shown in Figure 2.3.

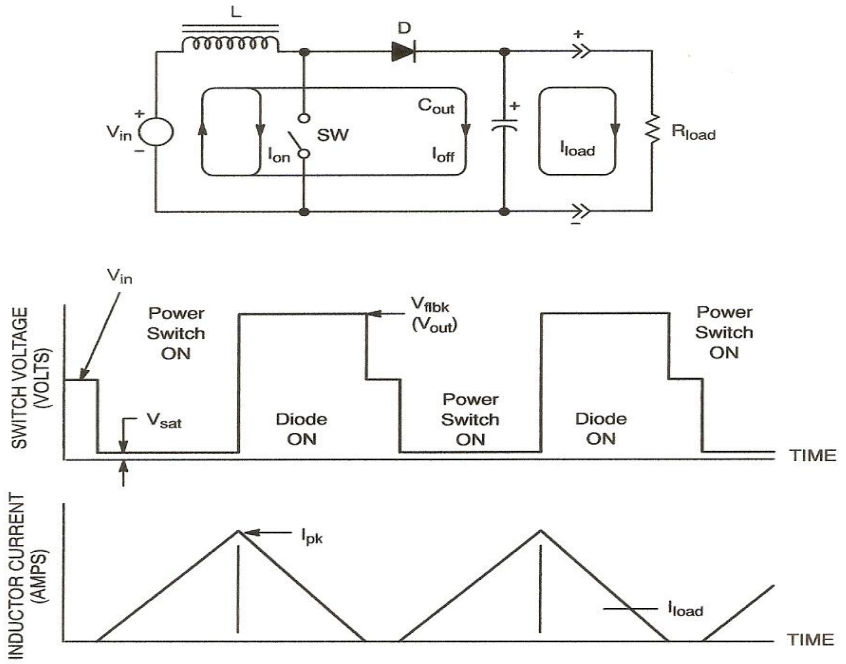


Figure 2. 3: Basic boost-mode converter with waveforms (Boost converter)

The operation is best understood by considering the `on' and `off' period separately. When the switch is on, the inductor is connected directly across the input voltage source. The inductor current then rises from zero and given by:

$$i_L(on) = \frac{Vin}{L}t \qquad 0 \le t \le t_{on} \tag{4}$$

Energy is stored within the flux in the core of the inductor. The peak current i_{pk} occurs at the instant the power switch is turned off and is given by :

$$i_{pk} = \frac{Vin}{L} t_{on} \tag{5}$$

When the switch is off, the switched side of the inductor wants to fly-up in voltage, but clamped by the output rectifier when its voltage exceeds the output voltage. The energy within the core of the conductor is then passed to the output capacitor. The inductor current during the off period has a negative ramp whose slope is given by:

$$i_L(off) = \frac{(Vin - Vout)}{L} \tag{6}$$

The energy is completely emptied into the output capacitor and the switched terminal of the inductor fall back to the level of the input voltage. Some ringing is evident during this time due to residual energy flowing through parasite element such as the stray inductances and capacitances in the circuit.

When there is some residual energy permitted to remain within the inductor core, the operation is called continuos-mode as in Figure 2.4.

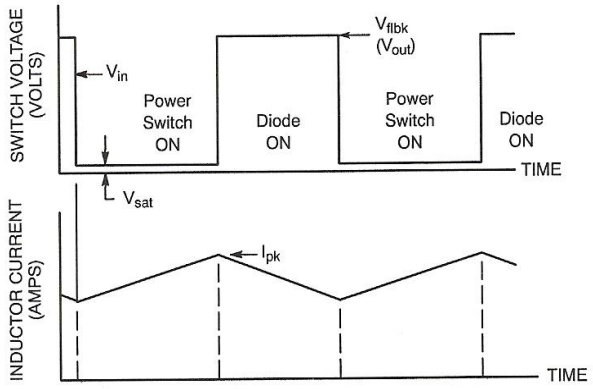


Figure 2. 4 : Waveforms of continuos-mode boost converter

Energy for the entire on and off time periods must be stored within the inductor. The stored energy is defined by:

$$E_L = 0..5L * i_{pk}^{\ 2} \quad (7)$$

The boost-mode inductor must store enough energy to supply the output load for the entire switching period (t_{on}+t_{off}), and typically limited to a 50 percent duty cycle. There must be a time period when the inductor is permitted to empty itself of its energy.

The boost converter is used in board-level (i.e non-isolated) step up application and its limited to less than 100-150 watts due to high peak currents. Being a non-isolated converter, it is limited also to input voltage less than 42.5V DC. Replacing the inductor with a transformer results in flyback converter, which may be step-up or step-down. The transformer also provides dielectric isolation from input to output [3].

2.1 2 DC-DC Converters & Associated Power Management

All electronic circuits required a clean and constant DC supply but in reality this energy source comes in terms of commercial AC supply, battery or combination of both. Sometimes the energy source maybe from other DC bus within the system or for a laptop it may be derived from the universal serial port (USB). During design stage of the system, the power supply should not be considered at the last stage. It is because for an excellent total system design exercise, power supply is the most important and vital part of the entire system beside consideration of the total weight and power management of the system.

Resources and limitations of components in the power supply and power management system are the most serious power supply design issues. Inadequate attention to all the possible worst case scenario at an early design stage such as limitation to allocate sufficient backup battery within the battery pack, unexpected surges and transient from the AC supply and fast load current transients by the load can create problems.

Nowadays, power management and digital control concepts were introduced in power supply and overall power management. There is four elements that must be fulfilled in the design of a low voltage power supply subsystem that is (i) isolation from mains, (ii) change of voltage level, (iii) conversion to a stable and precise DC value (DC-DC Converter) and (iv) energy storage [8].

Most of the digital systems today are equipped with the dc-dc converter to supply a multiple level of voltages from batteries to logic device as per Figure 2.5 below. DC-DC converter maintains the required voltage ranges regardless of the variation of the load current and at the same time the voltage drop of the battery. Even though the efficiency of DC-DC converter is changed by the output voltage level and the load current, this efficiency variation of dc-dc converters is simply ignored by the existing power management technique. Developing a true optimal power management is impossible without taking into consideration of these efficiency variations of the DC-DC converter [1].

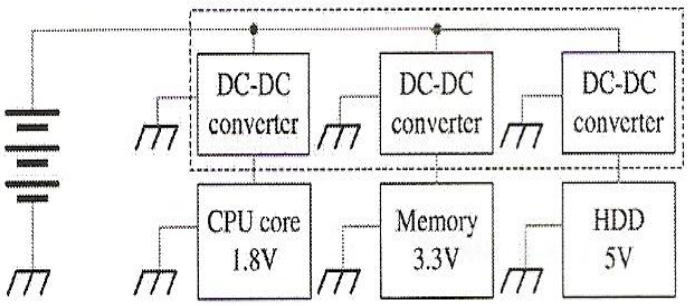


Figure 2. 5: DC-DC Converters generate different supply voltages for the CPU, memory and hard disc drive from a single battery (Source: Yongseok et al [1])

Until today, many proposed power management techniques are aiming to saving energy in the embedded system design. Also at the same time, not all of the proposals seriously take into consideration the efficiency of the dc-dc converter. The dc-dc converter's effect on the total energy consumption of the system can be ignored if the efficiency of a dc-dc converter was constant over its entire operating range. But in the real world, the efficiency of dc-dc converter has a close correlation with the level of output voltage and load current. Consequently,

when a power management scheme such as dynamic voltage scaling (DVS) that is also known as the most effective and well-studied power management technique; involves varying the DC supply voltage in an embedded system. It is also essential to properly schedule the output voltage of the dc-dc converter to minimize the overall energy consumption of the system. As the output voltage and power efficiency are the key element of the switching regulator that is affected by the load current, an effective power management is capable to reducing the power consumption of a device to a large extend. But by doing this, it doesn't means that it also reduces the power consumption of the DC-DC converter at minimum level where is some cases operating very inefficiently, resulting in a poor battery enhancement. In addition to that, it is necessary to solve the problem of output voltage scaling of DC-DC converter and problem of voltage scaling that is applied to the devices other than dc-dc converter in an integrated way, so that the total energy consumption can be minimized entirely. There are two major problems arising from DC-DC converter-aware power management that is the converter-aware voltage scaling and the application-driven converter optimization [1].

The increasing demand of high power application such as fast processors and pulsed loads require a new dimension of performance from DC-DC converters. The requirement of high slew rate of load current with minimal output voltage deviation together with high conversion efficiency, small size and low cost are all contradictory requirements of a DC-DC converters design. In order to have a high slew rate, it needs a small filter inductance but this will create high current ripple which increase the conduction and switching losses. New approaches have been introduced by Osama Abdel-Rahman [9] to efficiently limit the voltage overshoot and undershoot during load transient and reducing the number of capacitors. It is achieved without compromise on the efficiency, cost or size of the DC-DC converter by allowing to optimize the power stage efficiency for the dc operation with less concern on dynamic performance. Additional switching circuits that utilizes the output capacitor current to detect load transient; is activated during load step up to deliver the shortage charge from the output capacitor, and also

to pull out the extra charge from the output capacitor during load step down. Therefore, lower voltage deviation are achieved during the load transient.

Interleaved multiphase voltage regulator can reduce the input and output current ripples and have good distributed thermal capability which is regularly used in powering the central processing unit (CPU) of the desktop and laptop computer systems. In high slew transient, the voltage regulator current cannot catch up with the required load current immediately. The unbalanced current will be provided by filter and decoupling capacitor. Due to this, two transient voltage spikes occur in the voltage regulator output voltage. The first voltage spike is determined by ESR, ESL of capacitor and the second voltage spike is mainly determined by the energy stored in filter conductor related to the close-loop bandwidth. Large numbers of capacitor are mounted near to the processor on the motherboard in order to reduce the voltage spike for a lower ESRs and ESLs. Due to the limitation of space on the motherboard, it is difficult to add more capacitors for increasing the slew rate. Due to this, increased numbers of motherboard capacitors have limited effect on the voltage spike suppression and also to the existence of resistance and inductance of PCB traces and socket. The effective method to reduce the second voltage spike is to reduce the times delays in the controller, especially in large signal transients. There are three main delay times in a voltage regulator they are LC filter, compensation network and IC propagation delay times. The challenge is how to reduce those delay times in a simple way and to achieve tradeoffs between fast transient response and high efficiency. The voltage regulator equivalent inductance and its applied voltage is determined by the barrier of the output voltage regulator current slew rate. High switching frequency operation helps to reduce its LC for high bandwidth but also produce a higher switching loss.

Other studies have limiting the internal supply voltage spikes in the DC-DC converter by using a different spike reduction technique that have been presented by Rocha J et al [10]. The supply voltage spikes can be reduced in the resonant converter. This study is about original techniques that limit spikes in the internal supply voltage on a monolithic DC-DC converter. By applying monolithic

DC-DC converter for low power portable devices with a standard low voltage CMOS technology, it contributes to the saving on the production cost and higher reliability. Its also allows miniaturization by the integration of the two units in the same die that is the power management unit (PMU) that regulates the supply voltage for the second unit and a dedicated signal processor that performs the function required. The spikes mostly caused by the fast current variation in the path connecting the external power supply to the internal pads of the converter power block that includes the two parasitic inductances inbuilt in bond wires and in package pins. The small effect of relatively low values of the parasitic inductance cannot be ignored when switching high current at high switching frequency compared with the typical external inductance of DC-DC converter because these associated overvoltage frequently causes destruction, reliability problem and/or control malfunction.

The growth in portable devices has lead to the increasing level of integration in circuits, smaller in size and weight that integrate the power management unit (PMU) and signal processing unit that composed by analog and digital blocks in the same die that outlining the system-on-chip (SoC). In PMU with the step-down DC-DC converter, the components size of the off-chip LC filter should be small because the limited space on the printed circuit board (PCB) area. The reduction of inductor and capacitor value require a high switching frequency in order to maintain successful energy transferred from the battery to the load. At high switching frequency, DC-DC converter produces fast current variation in the path connecting external power source to the internal pads. When the switch is off, the fast current variation produces an internal supply voltage overshoot due to the parasitic inductances inbuilt in bond wires and the package pin on the serial path with the switches. Due to high switching frequency and high current, the effect of the low value of the parasitic inductances when compared with external inductor of the converter cannot be neglected since this is the main reason for spikes on internal supply voltage that cause overvoltage, which leads to device destruction, reliability problem or malfunction on the converter feedback control [10].

The class of resonant converters to reduce the supply voltage spike uses extra circuitry connected to the output load (load resonant) or to switches (switch-resonant) to force a sinusoidal shape of current and voltage in the switches. Beside to reduce the switching loss, the design of zero current switching (ZCS) or zero voltage switching (ZCS) is also to reduce supply voltage spike.

The increasing of interest on the green environment, pollution, global warming and energy conservation has triggered the research activity in the automotive sector to identify and develop alternatives to the internal combustion engine. Fuel cell vehicles (FCV) are among most interesting technical solution that are intensively studied today [11] and also an electric bus with supercapacitors as the only on-board power source that can realize fast and effective recuperation of energy in frequent braking and deceleration in the city. This bus is designed for operation over fixed routes no longer than 15km within the city [12]. Both technologies are using the bidirectional DC-DC converter that will be discussed separately based on the application of the converter. Basically, bidirectional converters are the combined configuration of battery charging circuits and DC-DC converter circuits. That allow power flow in either direction, i.e. towards battery or away from battery which been apply in DC UPS, battery charging circuits, stand by DC power supplies and also in aerospace applications [13].

The main functional electric scheme of the electric bus is shown in Figure 2.6 below.

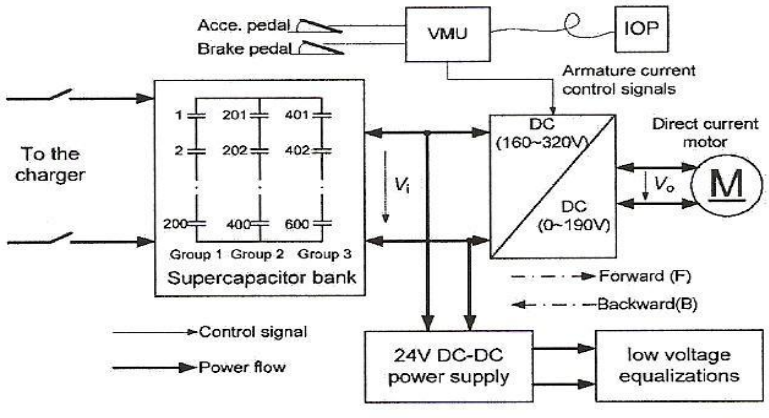


Figure 2. 6: Main functional electric scheme of electric bus (Source: Kong et al[12])

As we concentrate of the dc-dc converter part of the system, the DC motor is designed to work in two quadrants to realize regenerative braking and the DC-DC converter must be bidirectional. However, it is a difficult task to design a bidirectional dc-dc converter because of the wide voltage range and high current order of supercapacitor. For this system, the energy in the supercapacitor is transferred to the DC motor (motoring operation) through the DC-DC converter which is called the forward energy transmission. The recuperative braking energy of the DC motor is fed back to the supercapacitor bank in regenerative braking mode through the converter which is backward energy transmission. The converter exercises control of armature current with the signal from the vehicle management unit (VMU). VMU is the main controller in the electric bus and an input-output panel (IOP) to display all the information of the bus, the DC motor and the supercapacitor bank. Buck/Boost converter is used as a final choice for the DC-DC converter of this electric bus and the design specification is determined by the parameters of the supercapacitor bank and the DC motor[12].

In a new DC-DC converter structure for power flow management in fuel-cell electric vehicles that have fuel cell generator, batteries and supercapacitor, the batteries and supercapacitor guarantee load levelling, assuring braking energy recovery and good performance in transient operation. To this end, converters with bidirectional power flows are needed to connect the accumulator to the dc-link of the motor drive system, while a classical bidirectional DC-DC converter (typically with step-up function) is used to connect the fuel-cell generator. A possible connection that has been described by [14] is connected in parallel to provide voltage regulated dc power supply to the traction drive.

A new conversion solution proposed by [15] for interfacing fuel cell and supercapacitor with motor drive that only need two controllable power electronic switches to achieve 6 way power flow control and in other words, has halved the number of power electronic devices is needed to obtain the same performance in terms of power flow control with respect the solution described by [14].

2.2 Linear Regulator Advantages

The basic of linear regulator is as Figure 2.7 below. As we can observe from the figure below, linear regulator is nothing more than a electronically resistor in between the input and the regulated output. The resistance varies according to the load resulting in a constant output voltage. The capacitor is placed at the input of the linear regulator to help filter out the ripple. For example, if the input voltage is 24V, output voltage is 12V and load current is 10A, this regulator must dissipated heat energy of approximately 120W (12V voltage drop across variable resistor x 10A). This results in a mere 50% efficiency for the linear regulator for the linear regulator and a lot of wasted power which is normally transformed into heat.

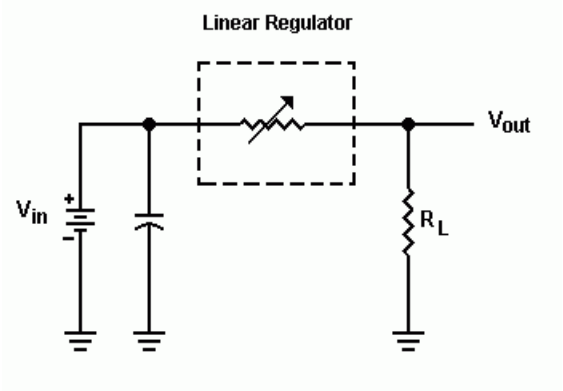


Figure 2. 7: Basic of linear regulator

Linear regulator is the basic building block of nearly every power supply used in electronics. The IC linear regulator is very easy to use that it is foolproof and the cheapest component is an electronic assembly. The operation of a linear regulator is to provides the constant DC output voltage and contains circuitry that holds the output voltage at the design value even when there is a change in the input voltage and load current (Input voltage and load current is also within the specified operating range). A modern linear regulator is developed using series MOSFETS (operates as a voltage controlled current source) to force a fixed voltage at the output terminal as in Figure 2.8.

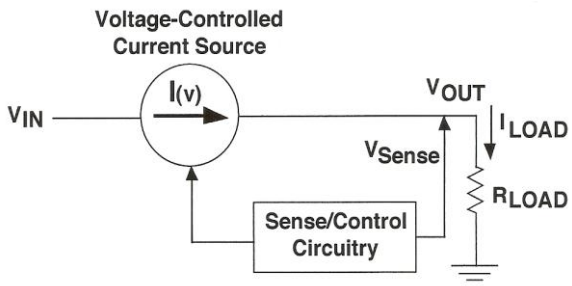


Figure 2. 8: Linear regulator functional diagram

The control circuitry monitor (sense) the output voltage and adjusts the voltage difference across the current source (as required by the load) to hold the output voltage at the desired value. The design limit of the current source defines the maximum load current the regulator can source and still maintain the regulation.

The output voltage is controlled by the feedback loop that requires some type of compensation to assure loop stability. Normally most of the linear regulators have built in compensation and they are completely stable without external components. However, some regulators like low dropout types requires some external capacitance at the output side to assure regulator stability.

The linear regulator also requires a finite amount of time to `correct' the output voltage after a change in load current demand. This `lag time' defines the characteristic called transient response which is a measure of how fast the regulator return to steady-state condition after a load change.

The operation of a control loop in a typical linear regulator based on a bipolar transistor is elaborated using the simplified schematic diagram in Figure 2.9.

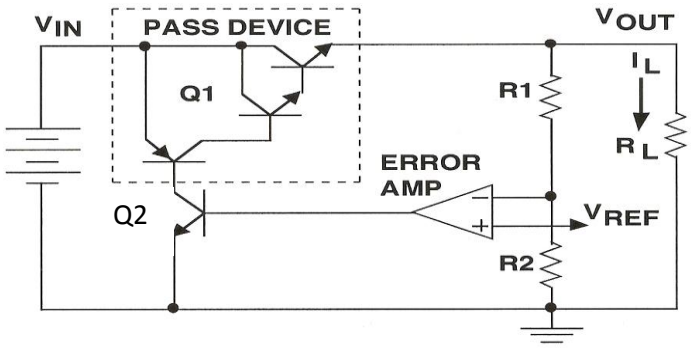


Figure 2. 9: Diagram of a typical linear regulator

The pass devices, Q1 is made up of an NPN Darlington driven by a PNP transistor and the current, I_L flowing out the emitter of the pass device is controlled by Q2 and the voltage error amplifier. The current through R1 and R2 resistor divider is assumed to be negligible (R1 & R2 is very big to make sure no load current through the resistor divider).

The feedback loop which controls the output voltage is obtained by using R1 and R2 to sense the output voltage and apply the sensed voltage to the inverting input of the voltage error amplifier. The non-inverting input is tied to a reference voltage which means the error amplifier will constantly adjust the output voltage and the current through Q1 to force the voltages at its input to be equal. The feedback loop continuously hold the regulated output at a fixed value which is a multiple of the reference voltage (as set by R1 and R2) regardless changes in the load current.

It is important that sudden changes in load current will cause the output voltage to change until the loop can correct and stabilize to the new level that is called transient response. The change in output voltage is sensed through the resistor divider R1 & R2 and appears as an `error signal' at the input of the error amplifier causing it to correct the current through Q1.

Linear regulator designs have three basic types that are (i) standard (NPN Darlington) regulator, (ii) LDO regulator and (iii) Quasi LDO regulator. The single most important difference between these three types is the dropout voltage which defined as the minimum voltage drop required across the regulator to

maintain output voltage regulation. A critical point to be considered is that the linear regulator that operates with the smallest voltage across it dissipates the least internal power and has the highest efficiency. The LDO requires the least voltage across it, while the standard regulator requires the most. The second important difference between the regulator types is the ground pin current required by the regulator when driving rated load current. The standard regulator has the lowest ground pin current, while the LDO generally has the highest. Increased ground pin current is undesirable since it is 'wasted' current, in that it must be supplied by the source but does not power the load. However, we are going to discussed only one type of linear regulator design that is Low Dropout or LDO Regulator.

Criteria of selecting a regulator that suitable for specific application is by evaluating the requirements such as maximum load current, type of input voltage source either battery of AC line, output voltage and quiescent current. The maximum load current required for the application must be carefully considered when selecting an LDO IC that it is capable to provide sufficient current to the load under worst-case operating conditions. The type of input voltage such as battery or AC line will contribute to the selection of the regulator. For battery powered application, LDO IC is the best solution because of the utilization of the fully available input voltage (and longer during the discharge cycle of the battery). For example, a '6V' lead-acid battery (a popular battery type) has a terminal voltage about 6.3V when fully charge and about 5.5V at the end-of discharge point. If a regulated 5V supply powered by the battery, an LDO is required with dropout between 0.5V to 1.3V. If DC voltage is regulated from a rectified AC source, the dropout voltage of the regulator is not as critical because additional regulator input voltage is easily obtained by increasing the secondary voltage of the AC transformer. For this application, standard regulators are the cheaper choice and also provide more load current. But, in some cases, additional features and better output voltage precision of some new LDO regulator will still be the best choice.

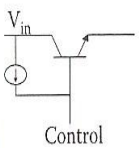
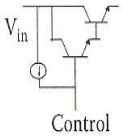
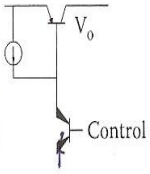
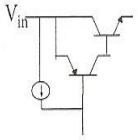
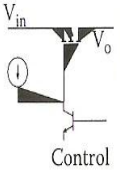
The other important aspect is the precision of output voltage which typical linear regulator will regulate output within 5% of nominal. This level of accuracy is adequate for most applications. Lastly, the quiescent current that a part drown from the source when idling (either shutdown or not delivering significant amount of load current) can be of critical importance in battery-powered applications. In some applications, a regulator may spent most of its life shut off (in standby mode) and only supply load current when there is failure of the main regulator. In this situation, the quiescent current determines the battery life. Many of the new low drop out (LDO) type linear regulators are optimized for low quiescent current like 75 to 150µA and provide significant improvement over typical regulators which draw several milliamps.

2.3 Low Drop-Out (LDO) regulators

LDO s are linear regulators where the input to output voltage differences are usually small so that dissipation in the series element is limited. They are developed using linear IC technology, in the form of single chip ICs where series transistor can have several different variation. Table 2.1 below compare those difference options for the series transistor and their advantages and disadvantages [8].

Table 2. 1: LDO series transistor configuration and their characteristic

(Source:Nihal Kularatna[8])

	Single NPN	Darlington NPN	Single PNP	PNP/NPN Combination	p-MOSFET
Configuration					
Minimum dropout voltage (minimum pass transistor drop)	≈1V	≈2V	≈0.1V	≈1.5V	$\approx R_{DS}(on) \times I_L$
Load current capability	<1A	>1A	<1A	>1A	>1A
Output impedance (Z_{out})	Low	Low	High	High	High
Bandwidth	Wide	Wide	Narrow	Narrow	Narrow
Effect of load capacitance (C_L)	Immune	Immune	Sensitive	Sensitive	Sensitive

These are used in many portable devices such as cellular handset, laptop and as well as in automotive environments.

For the regulator to regulate, it must fulfil these two characteristic that is the output voltage must be lower than the input voltage and the output impedance is low as to yield good performance. LDO can also be categorized as low power LDO where the maximum output current is normally less than 1A which is mostly used by portable electronic device and a high power LDO where the maximum output current are equal or more than 1A which are used by many automotive and industrial application. As one of the most important power management modules, LDO can provide regulated low-noise and precision supply voltage for noise sensitive block [4]. Also the manufacturers of low-voltage low dropout (LDO) linear regulators are competing to produce a high performance LDOs in smaller packages with excellent load transient response and stability. Additionally, LDO's being tailored to offer better noise performance that are capable to handle voltages at 1.2V or below that meets the increasing of power demands of new generation of microprocessor [16].

A LDO basically is a linear series regulator technique where the unregulated voltage from the rectifier after smoothing is buffered by series element such as NPN or PNP BJT or a MOSFET with a suitable feedback loop to maintain the output voltage at the required value which is normally in the order of 0.1V to 2V with the control circuit using very low power providing efficiencies around 65% and even higher for low dropout voltages [17]. LDO is made up by using only one pass device that is a single PNP transistor as Figure 2.10.

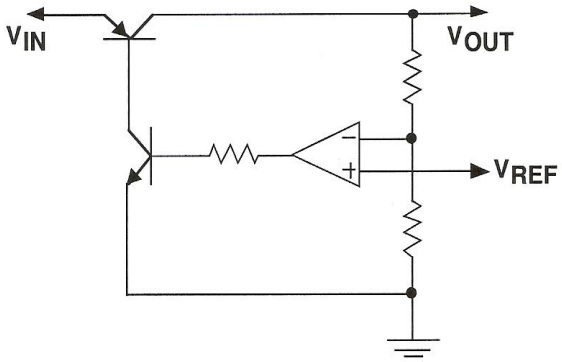


Figure 2. 10: LDO regulator

The minimum voltage drop required across LDO regulator to maintain regulate is the voltage that is across the PNP transistor.

$$V_{D(min)} = V_{CE} \tag{8}$$

The maximum specified dropout voltage of an LDO regulator is usually about 0.7 to 0.8V at full current with typical value of 0.6V. The dropout voltage is directly related to load current which means that at very low values of load current, the dropout voltage may be as little as 50mV. The lower dropout voltage is the reason LDO regulator dominates battery powered application since they maximize the utilization of the available input voltage and can operate in higher efficiency. The rapid growth of battery-powered consumer products in recent years has driven development in the LDO regulator [18].

Thus, LDO has been design to regulate according to the type of the input voltage. A regulation from stable inputs will results in significant power saving where the

input voltage is relatively constant. A regulation from unstable input, those are normally from AC line, SCR pre-regulator and DC pre-regulator input.

The nature of the LDO regulator makes it suitable for many applications such as automotive by powering up the digital circuit especially during cold crank condition where the battery terminal voltage is less than 6V [19], portable device, industrial and medical. In portable products, LDO suppliers are racing to deliver a high performance low-voltage LDO in smaller packages with excellent load transient response. In some applications require fast varying dynamic load with transients of 100A/µsec to 1000A/µsec at 3.3V output or lower [17]. LDO are also been tailored to offer better noise performance with the ability to have voltage 1.2V and below [20].

In the modern world today, portable devices are becoming very important and being used everyday in our life. There is a proposal to be very strict with the performance requirements of the LDO. The first proposal is that fast load transient response with little output voltage variation including overshoot and undershoot upon load switching, is critical to prevent an accidental turn off or resetting of the portable device. Secondly, low no-load quiescent current is required to reduce standby power. And finally, a need for a small compensation capacitor, that required to save the die size.

2.3.1 LDO Families and Applications

LDO is used coherently with dc-dc converter as well as standalone part. In power supply systems, they are normally cascaded onto switching regulators to suppress noise and provide a low noise output. The need of low voltage is innate to portable low power devices and corroborated by lower breakdown voltages resulting from reductions in feature size. Low quiescent current in a battery operated system is an intrinsic performance characteristic because it partially determines battery life. Rincon Mora et al [19] has discussed some techniques

that enable the practical realizations of low quiescent current LDOs at low voltages. The circuit proposed by Rincon-Mora et. al[19] in Figure 2.11 exploits the frequency response dependence on load-current to minimize quiescent current flow. Additionally, the output current capabilities of MOS power transistor are enhanced and dropout voltages are decreased for a given device size. Other application like DC-DC converter, can also reap the benefits of these enhanced MOS devices. An LDO prototype incorporating the aforementioned techniques was fabricated and operates down to input voltages of 1V with a zero-load quiescent current flow of 25A. Moreover, the regulator provide 10 to 50mA of output current at input voltages of 1V and 1.2V respectively [19].

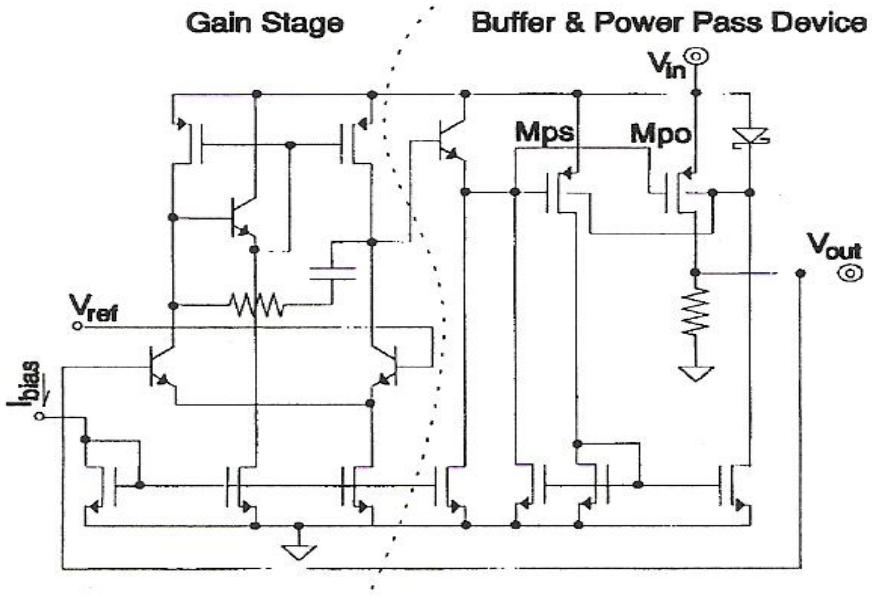


Figure 2. 11: Low voltage regulator by Rincon-Mora et al [19]

LDO based on a series-regulator is known to have adequate transient response for fast-varying load .Shunt regulator technique described by [17] has the added advantage of foldback-current limiting and this discretely implemented LDO, which need few components to implement will also provide a fast transient response. A simplified schematic for the concept described by [17] is shown in Figure 2.12 below.

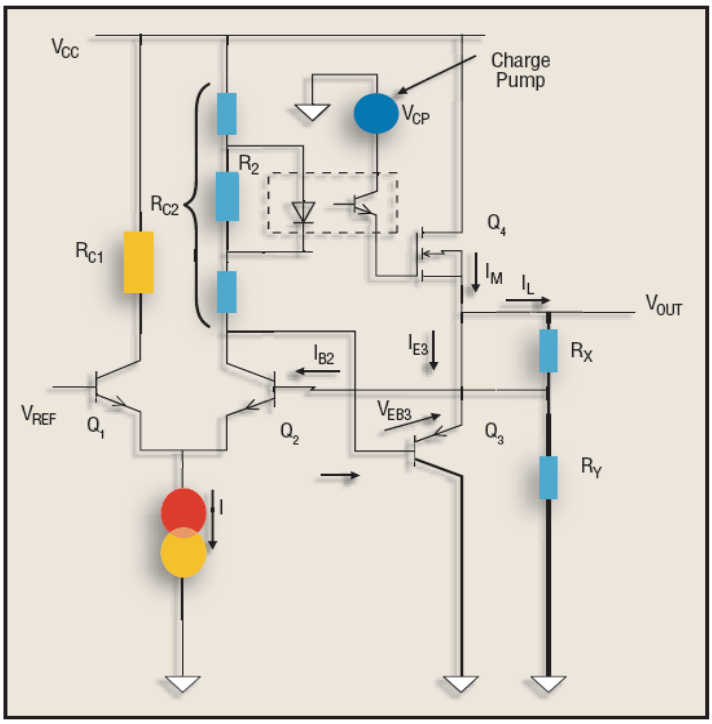


Figure 2. 12: A simplified schematic illustrates the concept of the shunt-type LDO regulator with foldback current limiting (Source: Kularatna and Thrimawithana[17])

The high current voltage regulator module above is developed using cheap discrete components with power MOSFET as a dropper and BJT for voltage regulator. It is suitable for 1.2V to 3.3V output rail that's delivering load current from few milliamps to over 10A and for application where the load frequently draws its maximum current and has a potential for short circuit or overloads.

The circuit above is based on a previously described shunt-regulated dc-power-supply technique by [17] which a reference voltage is compared with the sample of the power supply output voltage from the voltage divider. A series transistor acts as a constant-current source while shunt transistor acts as the regulating element. When the load current fluctuates, the shunt transistor acts as a current shunt that allowing output voltage regulation during fast transient. A bipolar transistor or a MOSFET is configured to act as a current source or a variable resistance, receives its control from the collector load path of a differential pair transistor. Under normal condition, within the set value of the output current

limit, the collector current of the differential pair transistor provide enough voltage at its collector to maintain the current source value, setting the maximum current limit of the regulator module. This configuration not only permits the setting of a maximum load current limit but also achieves foldback-current limiting. During overload conditions, foldback-current limiting is achieved by changing the voltage at the collector of the differential pair transistor. When the load tries to draw a current beyond the set regulation limit, such as short-circuited output, the voltage output drops below the regulation limit and the base voltage of the differential pair transistor drop, forcing it to operate in cut-off region [17].

2.3.2 – Commercial LDO ICs

There are many IC versions of LDOs in the marketplace. Many manufacturers such as Maxim, Linear Technology, National Semiconductor, Texas Instruments and Analog Devices have many families introduced over the past two decades. Increasing demand for higher efficiency portable electronic devices is a dominating factor in the power IC market.

In term of the new products available in the market today, two new products will be discussed below:

Today, most of the modern cars use automotive electronics modules that require very low ignition-off current. ON Semiconductor, a global leader of efficient power solutions has produce the new NCV86xx LDO, qualified to AEC-Q100 and operate across a wide temperature range and also to combine high levels on-board functionality with typical quiescent currents (Iq) as low as 22µA. This new LDOs are ideal for automotive system power modules that need to meet the voltage of 3.3V and 5.0V, up to 350mA output current and the new very low Iq. This LDOs has battery-connectable that feature on-board protection functions and include stringent criteria for current used while vehicle ignition is turned off with delivering precision output devices with power-on reset and delay time select capabilities. The quiescent current in the regulation portion of the module

can be minimized using this LDO. This means that the designer can allocate more current to higher level design elements including microprocessors and CAN and LIN network components.

For applications that need a precision output voltage of 3.3V and 5.0V with an output current capability of 150mA, this new LDO family also offers power-on reset and delay time select functionality with the typical I*q* of 22µA, 28µA and 30µA. The LDO with I*q* of 22µA is suitable to be used with the design where power-on reset is not required. While for the applications that required an output current up to 350mA, the new LDO families are also available with the 3V and 5.0V output options and respectively have an I*q* of 27µA and 34µA. They incorporate power-on reset functionality and are available with a choice of reset delay times. All the LDOs family operates with the output voltage accuracy of ±2.0 percent and incorporates a variety of on-board protection and other features like reverse battery, short circuit and thermal protection, while some of it, offer internal short circuit and thermal shutdown functions. These LDO can sustain input voltage transients inherent to direct battery connection, eliminating the need for intermediate conversion or protection devices. The wider operating range as lowest as -40°C and as highest as 150°C compared to other low I*q* LDOS that are currently available in the market [21].

The other one, a new family of low-power 200mA LDO has been produce by Toshiba Electronics Europe and is available in ultra-miniature wafer-level chip scale (WCPS). Measuring just 0.79mm x 0.79mm x 0.5mm, this LDO family just needs 8% of the board area from the SOT-25 device, while maintaining excellent ripple rejection and output noise performance. With a capability to have a fixed output voltage ranging from 1.2V to 3.6V with 100mV internal and output current up to 200mA, this LDO is a single output device with dropout voltages of only 90mV@2.5V output. It has incorporated overcurrent protection plus an on/off control function to minimize total system power consumption. Additionally, it has an auto discharge function for rapid discharge of the LDO when switched off using the control voltage. Designed for low power application, it has low I*q* bias current of 45µA while typical standby currents are down to just

1μA. Typical power supply ripple rejection ratio is a high 80dB (I_{OUT} = 10mA, f=1kHz) while output noise voltage is rated only 30μV_{rms}. All these specifications make it suitable for mobile phone, PDAs and other portable battery operated application that requiring high-density component mounting with low system power consumption. In addition to the small size, its also allows designers to use small ceramic input and output capacitors to further reduce board space requirement [22].

Low voltage LDO linear regulators have become the popular choice to power low voltage IC as these give the designer an option to implement a variety of power modes to minimize power consumption and maximize battery life. Due to this, several manufacturers have introduced a new member to their existing LDO family that bring optimal combinations of specification that were discussed above for the LDO from ON Semiconductor and Toshiba. The clear future is toward low V*in* and very low dropout to be used in many handheld or portable gear applications have contributed to the rapid growth of the LDOs manufacturing in order to fulfil the demand on this product. The development of CMOS also has encouraged the manufacturers to exploit the technology by transition from the bipolar to CMOS process to deliver a range of low-voltage regulator [20].

As LDO provide high current efficiency and clean power sources at a cheaper cost in comparison to the DC-DC converter, a novel topology for LDO regulators with load regulation improvement and very low quiescent current have been presented by [23] in Figure 2.13. LDO's have been used in almost every application and the managing circuitry to turn it on and off anytime to reduce system's power consumption, a fast transient response is needed to provide the required well regulated output current at the given voltage. The accuracy of the LDO is a must in sensitive application where any changes on the voltage source affect the performance severely. The core of the circuit presented by Gutierrez et al [23] is made by operating the pass transistor in the linear region., achieving an area reduction above 90%, reducing the gate capacitance and therefore improving loop response. The proposed structure to improve the load regulation

is based on transconductance cells and current mirrors, allowing it to sink the remaining energy on the compensation capacitor without affecting the battery lifetime. This design was developed in AMS 0.35µm technology and occupies only 0.025mm^2 with a quiescent current of 10µA. The proposed LDO can deliver 50mA@3.3V with 200mV dropout, a load regulation of 591nV/mA and is able to recover within 3s for any load transient [23].

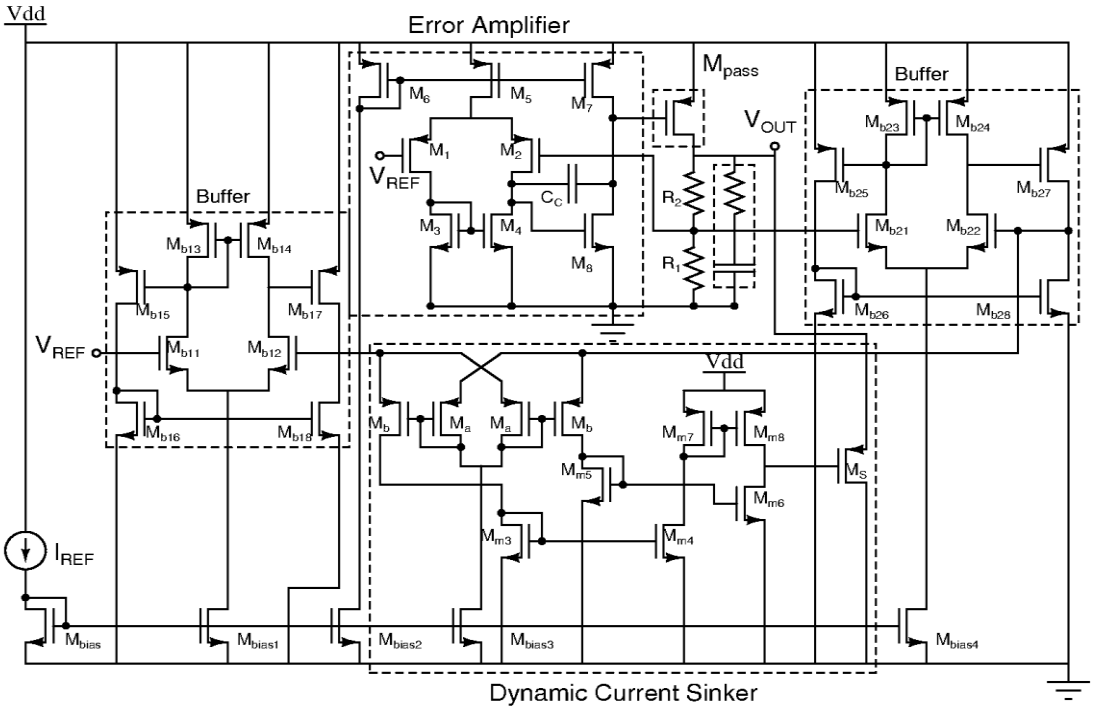


Figure 2. 13: Schematic of the new LDO Regulator (Source: Gutierrez et al [23]

An adaptive reference control (ARC) technique is proposed Chia-Hsiang et al [24] as in Figure 2.14 below for minimizing overshoot/undershoot voltage and settling time of low-dropout regulators. Linear operation provided by the ARC technique can dynamically and smoothly adjust the reference voltage so as to increase the slew rate of error amplifier thus forcing the output voltage back to its steady-state value rapidly. The amount of transient revision is proportional to transient state output voltage variation and load condition. In addition, a dynamic push–pull technique is used to enhance transient response. Experimental results demonstrate that the undershoot voltage, settling time, and

load regulation are improved by 31%, 68.5%, and 70%, respectively, when load current changes between 1 and 100mA [24].

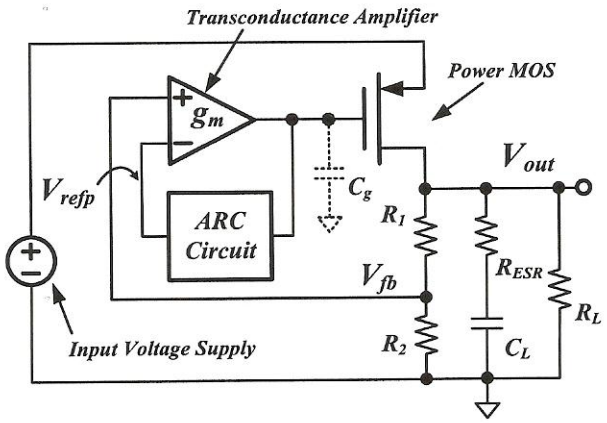


Figure 2. 14: LDO with ARC technique (Source: Chia-Hsiang et al[24])

2.4 Capacitor

Capacitor is the basic electrical components that stores energy in an electric field Microfarad or Farad is the unit of measuring capacitors. The use of capacitors are for energy storage and filtering or blocking the DC. Charging is acquiring energy into a capacitors and discharge is reuse of it. This happens in all capacitors in circuit. For filtering or blocking the DC, capacitors is applied to filter or extract particular frequency where this is dispensable to the circuits where excellent characteristic of frequency is required [25].

A physical capacitor is a device that stores energy in charge separation form when appropriately polarized by an electric field (i.e voltage) which can be simply a configuration of two parallel conducting plates of cross-sectional are *A*, separated by air (or other dielectric material such as mica or Teflon) as described in Figure 2.15 below.

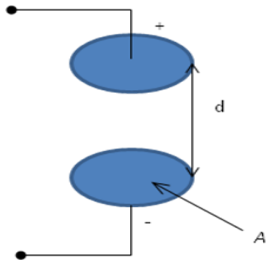


Figure 2. 15: Parallel-plate capacitor with airgap d (air is the dielectric)

The presence of an insulating material between the conducting plates does not allow the DC current flow thus the capacitor acts as an open circuit in the presence of DC current or DC analysis of the circuit. However, if the voltage present at the capacitor terminal changes as a function of time, so will the charge that accumulated at the two capacitor plates since the degree of polarization is a function of the applied electric field, which is time varying. In a capacitor, the charge separation caused by polarization of the dielectric is proportional to the external voltage, that is, to the applied electric field [26].

$$Q = CV \tag{9}$$

Where the parameter C is capacitance of the element and it is a measure of the ability of the device to accumulate, or store charge. The unit of capacitance is Coulomb per volt and is called farad (F), where farad is normally is microfarad or picofarad. From the equation (9) above, it becomes apparent that if the external voltage applied to the capacitor plates changes in time, so will the charge that is internally stored by the capacitor.

$$q(t) = Cv(t) \tag{10}$$

Thus, although no current can flow through a capacitor if the voltage across it is constant, a time-varying voltage will cause charge to vary in time. The change with time in the stored charge is analogous to current. Electric current is corresponding to the time rate of change or charge as given in equation (11) below

$$i(t) = \frac{dq(t)}{dt} \tag{11}$$

Differentiating equation (11), one can obtain a relationship between the current and voltage in a capacitor

$$i(t) = C\frac{dv(t)}{dt} \qquad i - v \text{ relation for capacitor} \tag{12}$$

Equation 12 above is the defining circuit law for a capacitor and if the differential equation that defines the $i - v$ relationship for a capacitor is integrated, one can obtain the following relationship for the voltage across a capacitor

$$vc(t) = \frac{1}{C}\int_{-\infty}^{t} ic(t')dt' \tag{13}$$

Equation 13 shows that capacitor voltage depends on the past current through the capacitor until the present time t. One do not usually accurate regarding the flow of capacitor current for all past time, and it is useful to define the initial voltage (or initial condition) for the capacitor according to the equation below, where t_o is an arbitrary initial time

$$Vo = vc(t = to) = \frac{1}{C}\int_{\infty}^{to} ic(t^{'})dt^{'} \tag{14}$$

The capacitor voltage is now given by the expression

$$vc(t) = \frac{1}{C}\int_{to}^{t} ic(t^{'})dt^{'} + Vo \qquad t \geq to \tag{15}$$

The significance of the initial voltage is simply that at time some charge is stored in the capacitor, giving rise to a voltage, based on relationship. The understanding of this initial condition is sufficient to account for the capacitor current [26].

After the capacitor, comes into commercialized the electrolytic capacitors which are similar to battery in cell construction but the anode and cathode material remain the same. They use aluminium, tantalum and ceramic capacitors which

use solid/liquid electrolytes with a separator between two symmetrical electrodes.

2.4.1 Types of Capacitors

There is different types of capacitors that are commercially available in the market. The common type of capacitors and their features are summarised below:

Paper and plastics capacitors use a variety of dielectric material that's include mylar, polystyrene and polyethylene for the plastic type, waxed or oiled paper for the older, less expensive paper type. Typically, the plates are long strip of tinfoil separated by the dielectric material. The foil and dielectric material are commonly rolled into a cylindrical component as in Figure 2.16 below. Because of this construction, each plate has two active surfaces and use twice area of the plate rather than only the area of one plate in order to calculate the area of the plate. This type of capacitor is normally range from 0.001µF to 1µF or more. Paper and plastic capacitors are normally used in low frequency application such as audio amplifier.

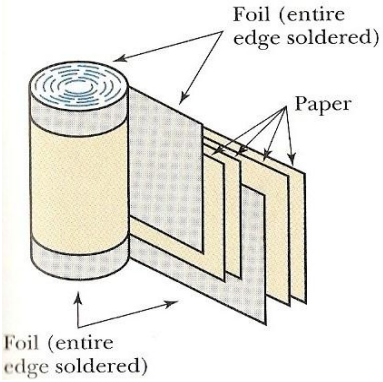


Figure 2. 16: Paper and plastic capacitor

Mica capacitor used mica for the dielectric material because its high breakdown voltage and low capacitance makes its mostly found in the high voltage circuit. Their construction is alternate layers of foil of mica that moulded into a plastic case as in Figure 2.17 below. Mica capacitor is compact, moisture-proof and

durable. The voltage rating in thousand of volts and capacitance value normally from 5 to 5000 picofarad.

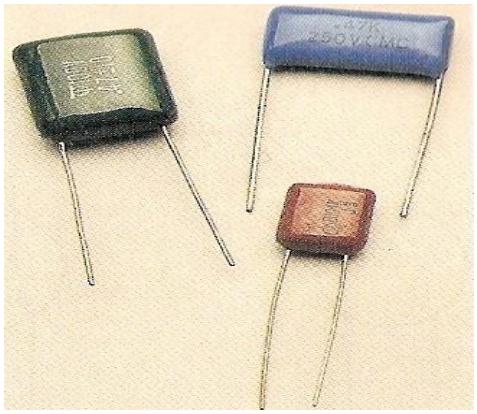


Figure 2. 17: Mica capacitor

Ceramic capacitors are typified by their small size and high dielectric strength and come shaped like a flat disc (disc-ceramics) or in cylindrical shapes as in Figure 2.18 below. It's compact, moisture-proof and durable. Typical available ranges having 1000 V rating are from 5pF to 5000pF and higher capacitance at low voltage rating. Both mica and ceramic capacitor are used in audio frequency range up to several hundred megahertz because they have good dielectric characteristic.

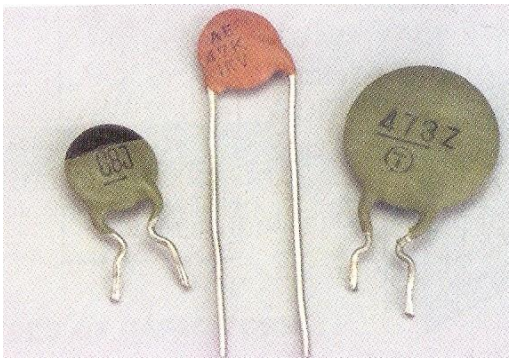


Figure 2. 18: Ceramic capacitor

Electrolytic capacitors have several prominent characteristic such as high capacitance-to-size ratio, polarity sensitive with terminal market + and -, allow more leakage current than other types and have their C value and voltage rating printed on the capacitor as shown in Figure 2.19. The external aluminium can or

housing is typically the negative plate (or electrode) The positive electrode external contact is generally aluminium foil immersed or in contact with an electrolyte of ammonium borate (or equivalent). If the electrolyte is a borax solution, the capacitor is called a wet electrolyte and if the electrolyte is a gauze material saturated with borax solution, its called dry electrolyte. To create the dielectric, a dc current is passed through the capacitor that causes a thin aluminium oxide film (about 10 micrometer thick) that is dielectric, to form on the foil surface. Due to the extremely thin dielectric, capacitor value per given plate area is very high as well as voltage breakdown levels are relatively low. The dielectric is very thin and made some leakage current occurs in a fraction of milliampere for each microfarad of capacitance. The main advantage of this type of capacitor is the large capacitance-per-size factor. Two obvious disadvantages are the polarity, which must be observed and higher leakage current feature. The electrolyte can dry out with age and depreciate the capacitor quality or render it useless. Due to the losses of the dielectric at the higher frequencies, electrolyte capacitor applications are limited to power-supply circuit and audio frequency.

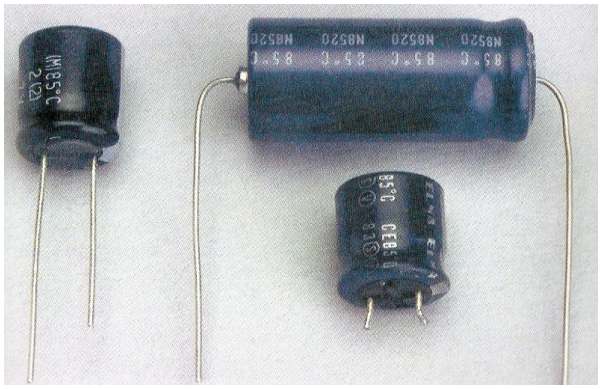


Figure 2. 19: Electrolytic capacitor

Tantalum capacitor as in Figure 2.20 is in the electrolyte capacitor family and used tantalum instead of aluminium because tantalum provides very high capacitance in small-sized capacitors and lower leakage current. Tantalum does not dry out as fast, thus they have a longer shelf life. Tantalum are normally

manufactured in a low-voltage rating that makes they been used in the semiconductor circuitry. Tantalum capacitor is expensive.

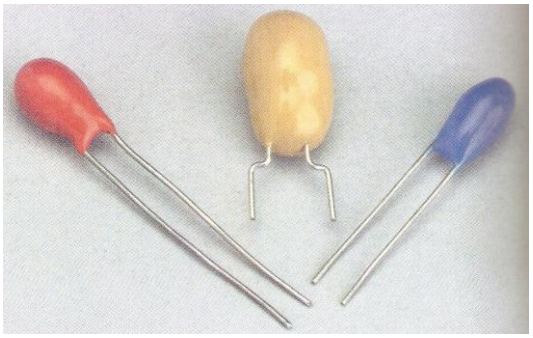


Figure 2. 20: Tantalum capacitor

Chip (SMPT) capacitors is very small in size and are suitable to be primarily used as compact components on PC board-type circuitry where space is limited as in Figure 2.21. The construction style, with virtually no lead length enables these components to have minimal stray inductance or capacitance that makes it useful in high frequency application. Ceramic as the dielectric between layers are the material commonly used in the construction of the type of capacitor including layers of conductive material. The general exterior portions of the chip capacitor are the ceramic type body and the metallic end contacts as shown in Figure 2.21. These metallic end pieces are the electrical contact points to the capacitor and their miniature size makes its difficult to mark their value. Therefore, they are typically marked with a two character code (which needs a magnifying glass to read it) [27].

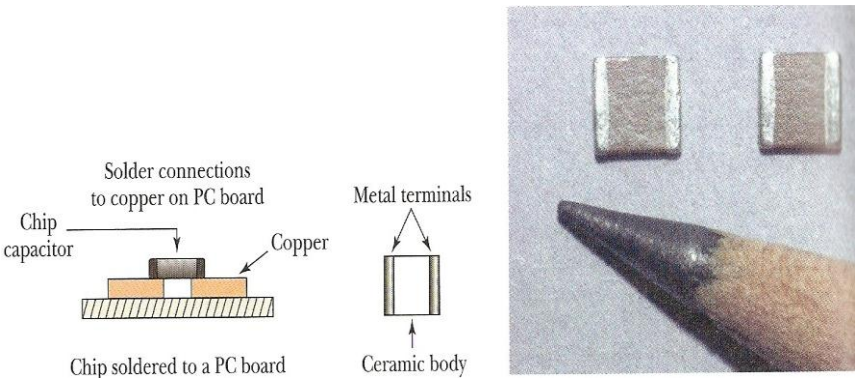


Figure 2. 21: Chip (SMT) capacitor

2.5 Supercapacitors

As the demand for lighter, compact wireless and portable devices with more features in a very small space had become compulsory in modern electronics. All of this cannot be achieved without the power supply innovations, good batteries and other energy storage devices. Current battery technology always compromises with the desired space and weight without properly satisfying peak power requirements.

Supercapacitors or as they are sometimes refer to ultracapacitors offer an alternative energy source that promises the green technology. Supercapacitors offer unlimited growth potential because its respond to key market and societal needs. It is environmental friendly, helps conserve energy, enhances the performance, portability of consumer devised and more importantly is free from characteristic battery problem such as limited life cycle, cold intolerance and critical charging rates [28]. Table 2.2 below is a summary of comparison between the batteries and supercapacitors [29].

Table 2. 2: Comparison between battery and supercapacitors:

Batteries	Supercapacitor
Store watt-hours energy	Store watts of power
Depend on chemical reaction with long time constants. Takes long time to charge and need a good profile of current to charge the battery	Charged by applying a voltage across the terminal and charge rate depends mostly on external resistance
Deliver power in form of more or less constant voltage over long time period	Discharge rapidly and the output voltage decay exponentially
Good for only a limited number of	Can be charged and discharged

charge and discharged cycle and the number of cycle depends on how deep the batteries is discharge	repeatedly for tens of millions of cycle.
Big and heavy	Small and light

Many of these differences can be illustrated in a Ragone plot as in Fig. 2.22 below. The Ragone plot helps illustrate the differences between different kinds of battery chemistry, clustered on the left, and capacitors on the right. Taken together as illustrated on the Ragone plot, those characteristics make batteries and ultracapacitors complementary to each other.

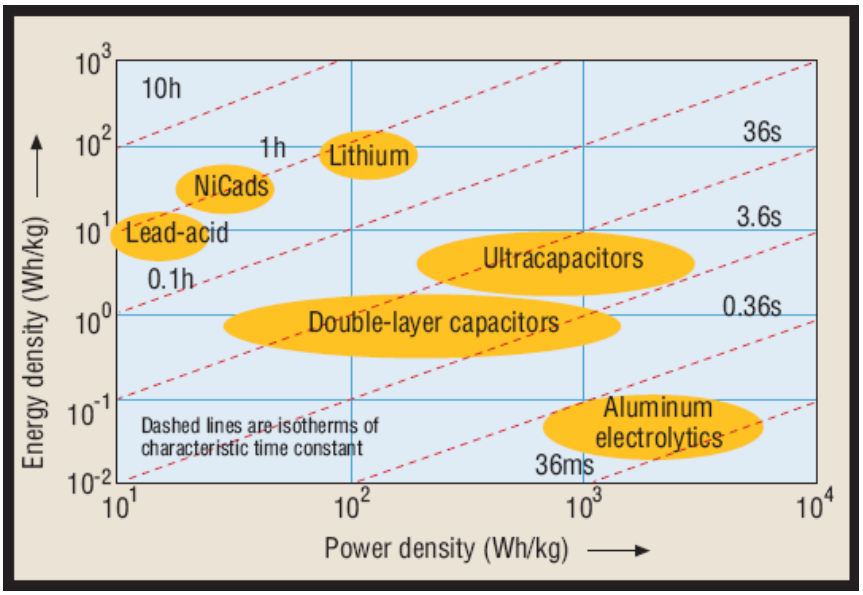


Figure 2. 22: Power vs energy characteristic of energy-storage devices

The development of double layer capacitor has rapidly evolved from the huge size to a small size with higher power (up to 100kW/kg for supercapacitor and 0.4kW/kg for the battery) but low energy density (5 Whr/kg for supercapacitor and 8 to 600Whr/kg for battery) [30]. This is because the significant of new electrochemical elements introduced in order to give great delivery of the desirable power and energy densities [25]. It is highly efficient and environmental friendly storage component that offers rapid charging and

discharging current and shows a good reliability and cycle capability [31]. Battery has higher energy density while supercapacitors have higher power density.

The third generation is the electric double layer capacitor (EDLC) which the charge stored at a metal/electrolyte interface is exploited to construct a storage device. The interface can store electrical charge in the order of ~10^6 Farad and activated carbon is the main component in the electrode construction. Even though this concept and idea had been initialized and industrialized in last 40 years ago, there was stagnancy in research until recent times. The increasing demands for the electrical energy storage in certain current applications such as digital electronic devices, implantable medical devices and start/stop operation in vehicle traction which need very short high power pulses that can be fulfilled by electric double layer capacitors. Compared to conventional capacitor, EDLCs have a longer life cycle than batteries and posse higher energy density. This had led to new concept of the so called hybrid charge storage devices electrochemical capacitor and it's interfaced with a fuel cell or battery. These electrochemical capacitors that use carbon as the main material for both anode and cathode electrode with organic electrolytes are commercialized and used in the daily life. The three different types of capacitors in terms of their construction and design are shown in Figure 2.23.

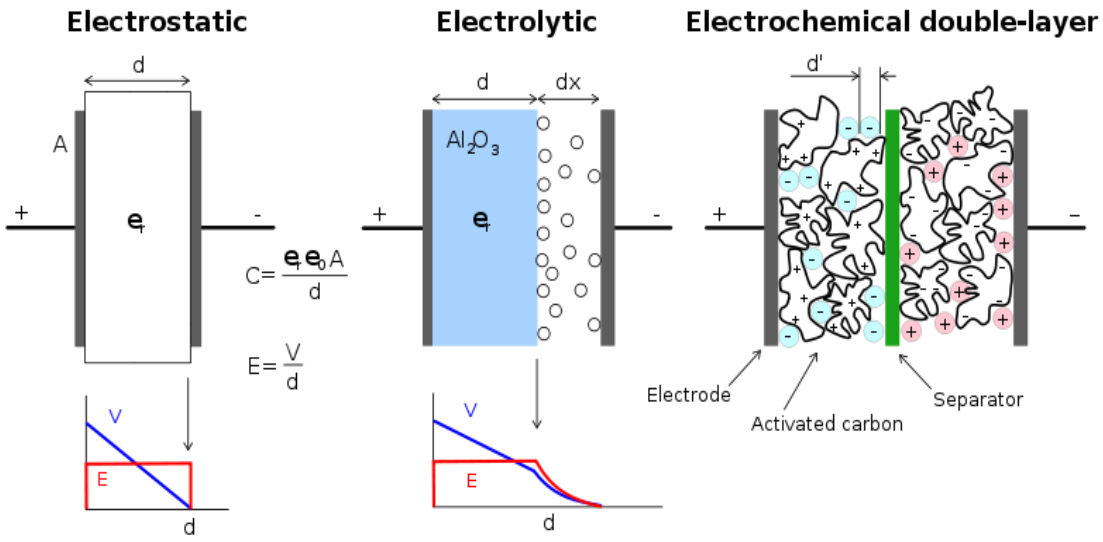


Figure 2. 23: Schematic presentation of electrostatic capacitor, electrolytic capacitor and electrical double layer capacitor

EDLC is known to be low energy density and researchers recently had to tackle this problem by incorporating transition metal oxides along with carbon in the electrode materials. When the electrode materials consists of transition, the electrosorption or redox process enhances the value of specific capacitance 10 – 100 times depending on the nature of oxides and when this happen, it is the fourth generation capacitor that is called supercapacitor or pseudocapacitor [25].

The energy storage mechanism inside the electrochemiocal double layer capacitor does not involved any chemical reaction and is highly reversible. It's allow the supercapacitor to be charge and discharge for hundreds of thousand times. It can be represented by two nonreactive porous plate suspended within an electrolyte, with a voltage applied across the plates. The applied potential on the positive plate attracts the negative ion and the potential of negative plates attracts the positive ion in the electrolyte that creates two layers of capacitor storage. Capacitors stores energy in the form of separated electric charges. The greater the area for storing charge and closer the separated charges, the greater the capacitance which is achieved inside the supercapacitor. The material is wound in great length and sometimes a texture is imprinted on it to increased its surface area. A supercapacitor gets its area from the porous carbon-based

electrode material that allows its surface area to approach 2,000 square meters per gram (m^2/g) much greater than can be achieved using flat or textured films and plates as in Figure 2.24. The charge separation distance of the supercapacitor is determined by the size of the ions in the electrolyte which are attracted to the charged electrode. The charge separation that is less than 10 angstroms (Å) is much smaller than can be achieved by conventional dielectric materials. The combination of enormous surface area and extremely small charge separation gives the supercapacitor their superb capacitances compare to conventional capacitors [26].

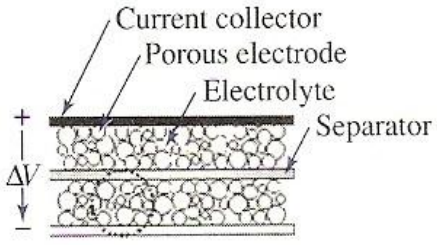
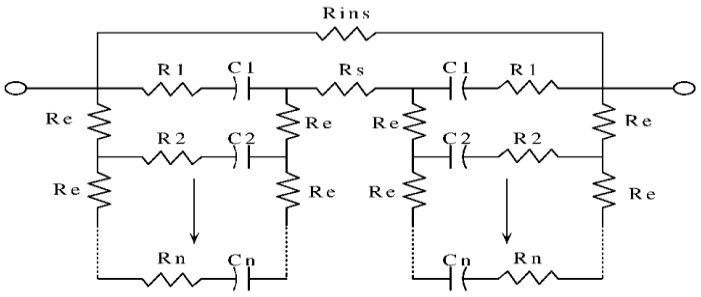


Figure 2. 24: Supercapacitor structure

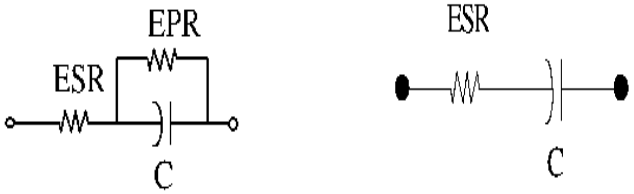
The rapid development in the area of energy storage had promise that the double-layer capacitor will become an important device for most electronic or digital applications. Their low voltage device and high power density gives it has more advantages in term of efficiency by reducing the peak load current [32] by half the average level [30] compare with the battery or an electrostatic devices [31]. Even though it is does not store quite as much as the battery but the charge and discharging in a second rather than a minute in a battery makes this combination of speed and energy supply suitable for example in regenerative braking where only have seconds to recharge if apply to a car that comes to stop. But seconds is still too long and with the new technology using nanometer-scale fins of graphene makes its possible for the researcher to built a supercapacitor that can charge in millisecond. With this new discovery, the devices could replace a bulky component to give free space in electronic portable products or computers. A recent development in graphene supercapacitor also makes it possible to do a filtering job as part of an AC rectifier when tested in such 120Hz

filtering circuit while the other commercial supercapacitor fail at the filtering role at 0.01Hz. This means that this supercapaitor can replace the big electrolytic capacitors and estimates that the commercial version of graphene supercapacitor that operate at 2.5V will be less than one-sixth of the prototype model [33].

The double–layer capacitor is best described by distributed parameter system because of its complex physical nature. Many model of double-layer capacitors have been proposed and lumped parameter equivalent circuit are the mostly used. The equivalent circuit in Figure 2.25a contains a resistance for the ion permeable separator and resistance and capacitance for individual activated carbons fibers in the electrode and with four resistance and four capacitance that represent the terminal behaviour of the double-layer capacitor [34].



(a)



(b) (c)

Figure 2. 25: Equivalent circuit for a supercapacitor (a) detailed version (b) simplified equivalent circuit inculding EPR (c) simplified equivalent circuit neglecting the EPR

In a slow discharge application on the order of few second, the simplified equivalent circuit as in Figure 2.25b is referred to as a classical equivalent circuit that may be used to predict the system performance. This model may be considered a first-order approximation to the actual capacitor behaviour in a slow discharge application.

The classical equivalent circuit as Figure 2.25b is comprised of three components that is capacitance (C), the ESR and the equivalent parallel resistance (EPR). The ESR is a loss term that models internal heating in the capacitor and discharging. It also will reduce terminal voltage during discharge into a small load resistance due to the resistive divider effect. The EPR models a current leakage effect and will therefore impact long-term energy storage performance [34].

The high densities of the supercapacitor depends on the voltage and internal resistance which focus more into the reduction of the equivalent series resistance (ESR) that can bring higher power.[30] The capacitance is governed by

$$C = \frac{A}{d} * \varepsilon_0 \varepsilon_r \qquad (16)$$

Where ε_0 is the permittivity of free space, ε_r the relative permittivity of the dielectric (one or several layer of electrolyte separation), *A* the plate surface area and *d* the plate separation. From the equation above, capacitance is inversely proportional to the electrode separation and proportional to area which means that the closer the electrodes and more surface area, the higher the capacitance [30].

2.5.1 Applications of Supercapacitors

The most basic applications for supercapacitor are in stabilizing dc bus voltages. It had been widely used in automobile industry to protect the various engine control units and other microcontrollers from voltage dips associated with the application of sudden transient loads. Those sudden loads often are associated with motors. But if the speaker output of the car's entertainment system is

sufficiently robust, the load could come from audio peaks. In lieu of simply putting a supercapacitor on the 12-V input to the entertainment system, an application note by Australian supercapacitor maker, Cap-XX shows a way of increasing the voltage for a class-D output amplifier's H-bridge as in Figure 2.26. It uses a small boost converter and stores the power needed for those occasional peaks in a pair of supercapacitor [29].

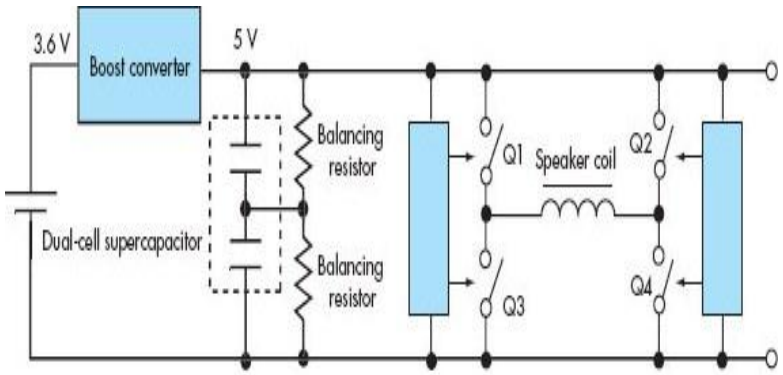


Figure 2. 26: New circuit to increase the voltage for a class-D output amplifier's H-bridge by Cap XX

In transportation, the supercapacitor's ability to absorb and discharge energy rapidly makes it far better than batteries for regenerative braking schemes. Most of these applications have been in public transportation as in Figure 2.27. The Bombardier rail cars in the light-rail system in Mannheim, Germany, use packs of 600 2600F supercapacitors for braking energy recapture. The stored energy is used to boost acceleration and to bridge non-powered sections and intersections. Operation there represents between 100,000 and 300,000 load cycles/year. This is an all-electric rail system, so recaptured braking energy reduces demand on the grid and the prototype has demonstrated a potential for energy savings of up to 30% [29].

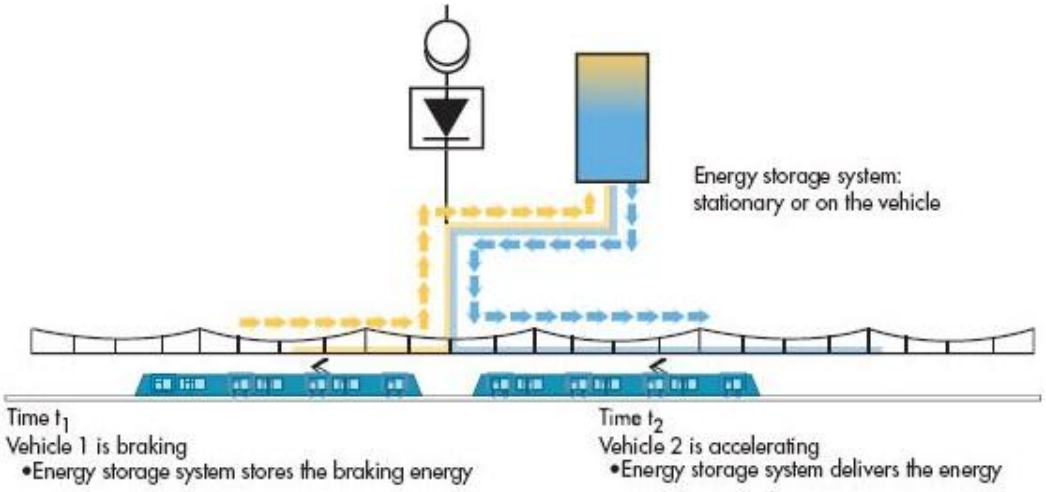


Figure 2. 27: Application of supercapacitor in a rail system

The supercapacitors has been installed on the rail cars themselves or for an alternative, alongside the tracks. Demonstrating this approach, Siemens Transportation Systems uses supercapacitors for regenerative braking in its Sitras SES system, which is used in Cologne's and Madrid's metro rail lines. In a typical trackside implementation, the supercapacitors absorb the braking energy from all trains within a 3-km radius [29].

Supercapacitors are being developed as an alternative to pulse batteries. In order to be an attractive alternative, supercapacitor must have at least one order of magnitude higher power and much longer shelf and life cycle than the battery. Supercapacitors have much lower energy density than batteries, and their low-energy density is the main factor that determines the feasibility of their use in a particular high-power application. For decades, a conventional electrolytic capacitor is an energy-storage device that can be compared to a container that gradually fills with electrical energy and then delivers it when needed in a sudden burst. A supercapacitor is a high-energy version of a conventional capacitor, holding hundreds of times more energy per unit volume or mass than the latter by using state-of-the-art materials and high-tech microscopic manufacturing processes. When fully charged, these robust devices deliver instant power in an affordable and compact package. The unit price of the supercapacitor is not economical to be implemented by the designer in the first place. But after a long

period innovation of inexpensive, compact supercapacitor, characterized by an exceptionally high surface area, excellent conductivity, superior chemical and physical stability, supercapacitor herald a new era of practical usage.

Supercapacitor has also been used in a power management architecture as a storage and hybrid storage element for energy harvesting in wireless sensor networks as in Figure 2.28 below This system had take advantages of supercapacitor capability of charge speed and instantaneous output power and also lithium cells for the store available energy The instantaneous power demand is supplied by supercapacitor if the power generated by the converter is less than the power required by the load and battery charge. The structure for this system can be simplified and only utilizes supercapacitor if the technologies of the supercapacitor improve the performance in terms of leakage current and energy density. By utilizing the dc-dc converter, the supercapacitor is connected in parallel without requiring an overvoltage protection system on each element that is needed in the serial connection [35].

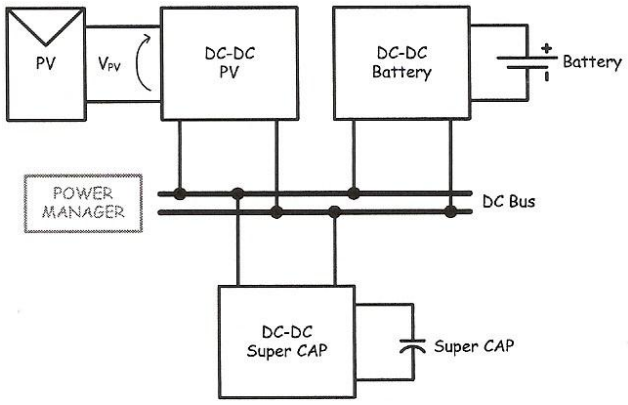


Figure 2. 28: Power Conversion system of the network with supercapacitor (Source: Saggini et al [35])

To date on-road electric vehicles (EV) and hybrid electric vehicles (HEV) make use of high-power density ac propulsion systems to provide comparable performance with vehicles using internal combustion engine (ICR) technology. But the need of speed, greater performance and vehicle variety of EVs plus the commitment to further reduce emission in HEVs has increased the appeal for combined on-board energy storage systems and generators. The technology for

the electric motor, inverter and associated control technology of the EVs and HEVs has been progressed substantially in past decade and it is not the limiting factor to either the performance or mass production of EVs and HEVs. The major problem to this mass production of EVs and HEVs is for the search for compact, lightweight and efficient energy storage (battery and/or combination of other emerging technologies including ultracapacitor, flywheel energy storage system, advanced battery and fuel cells) that are both low cost and reliable. Figure 2.29 below is a multiple input dc/dc power converter devoted to combine the power flowing from combined on-board energy sources.

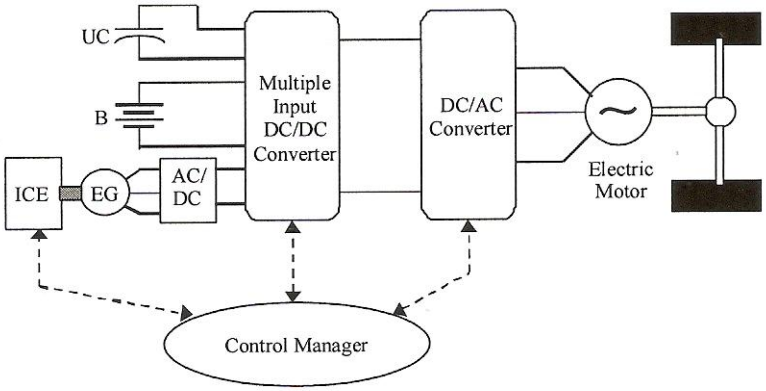


Figure 2. 29: Hybrid drive-train (Source: Di Napoli et al[36])

The arrangement for the propulsion system includes an electric generator (EG), ultracapacitor (UC) bank and battery system. The electric generator is directly driven by an internal combustion engine (IEC), the main energy source. However, IEC has a very poor efficiency at light load and in this condition; battery storage system is required to supply the traction power in order to save the total efficiency. As a result, the IEC+EG system is sized in order to supply the traction electric drive up to 3/5 of the cruising maximum power, where the storage battery should feed at least 2/5 of the cruising maximum power for the time calculated on the basis of selected driving cycles. Since ICE+EG system can neither recovers energy nor provides high dynamic response and to save efficiency and reduce emission, UC is used to satisfy acceleration and regenerative braking requirements complying with the load transients and improving the on-board battery life cycle. The configuration, design and sizing of

the multiple input power electronic converter (MI-PEC) as in Figure 2.30 below had been extensively carry out by Di Napoli et al [36].

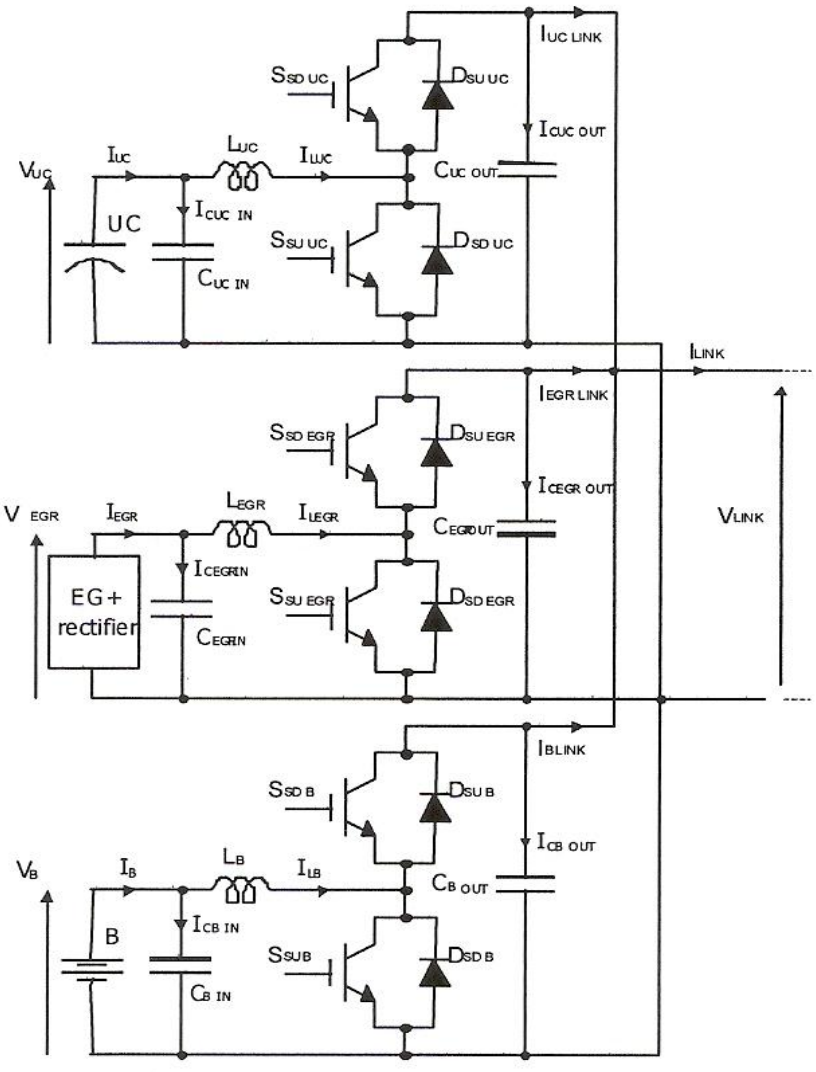


Figure 2. 30: Multi-Input Power Electronic Converter Layout (Source: Di Napoli et al[36])

Chapter 3 - Theoretical Framework

3.1 Basic Concept

A basic operation of basic LDO that consists of series pass element (where for this case, it is NPN transistor) can simply be configured in Figure 3.1 below.

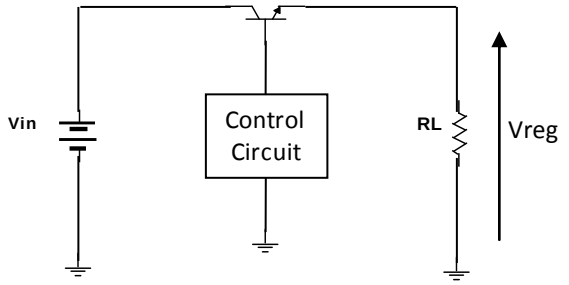


Figure 3. 1 : Basic concept of LDO

The approximate efficiency of the circuit could be given by V_{reg}/V_{in}, if the control circuit block diagram consumes only minimal power Therefore, the efficiency will be high if there is not much difference between the input and the output voltages. However, if there is a big difference between the input and the output voltages, for example, a circuit that has the following specification, V_{in} = 12V and V_{reg} = 5V, no matters how good the design of the circuit, the efficiency of circuit can only be as high as 42% approximately. And most of the losses will be dissipated at the transistor in the form of heat. This circuit is not practical since there is a need to use a bulky heat sink at the transistor. In order to reduce the wasted energy at the transistor, lets consider the circuit as shown in Figure 3.2 below.

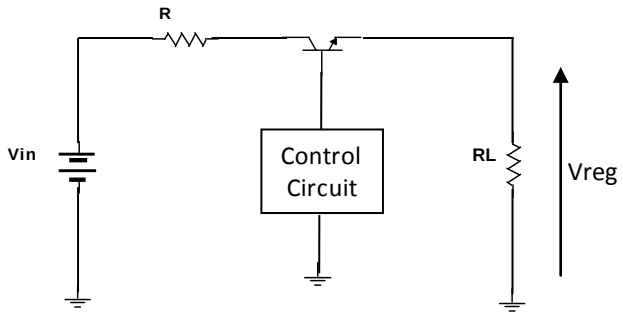


Figure 3. 2: Basic concept of LDO with a resistor in the series path

By using a resistor that is placed before the transistor, it will reduce the voltage drop across the V_{CE} of the transistor but again, part of the losses will be at the resistor and again the efficiency of the circuit will remain the same.

The energy wasted in this series path which in this case is in the resistor or transistor can be recovered and reused by using supercapacitor based energy recovery technique that has been develop by Kularatna and Fernando[6, 37, 38]. This patented technique [37] is suitable for LDO type linear regulators where a single supercapacitor or an array of supercapacitors are used to recover and reuse the energy wasted. In principal, this technique can be used for many different input and output voltages and is also easy to implement when the input unregulated voltage is higher than twice that of the regulated output voltage.

In general, a linear regulator, series or shunt type is inefficient except for its excellent load and line regulation, transient response and low output impedance. Meanwhile switching regulators that are regularly used in industry and meet the consumer product requirement because of its high efficiency despite its noisy and complex with poor transient response.

In a series regulator, the approximate efficiency (η) is given by $\eta = \frac{Vout}{Vin}$, where V_{in} is the unregulated input voltage and V_{out} is the regulated output voltage by assuming the power consumed by the control circuit is zero . This proves that the efficiency can be increased if the difference between the unregulated input

voltage and the regulated output voltage is not very high and kept closer to each other. This principle has been used in commercial low dropout (LDO) regulator families in the portable electronic devices.

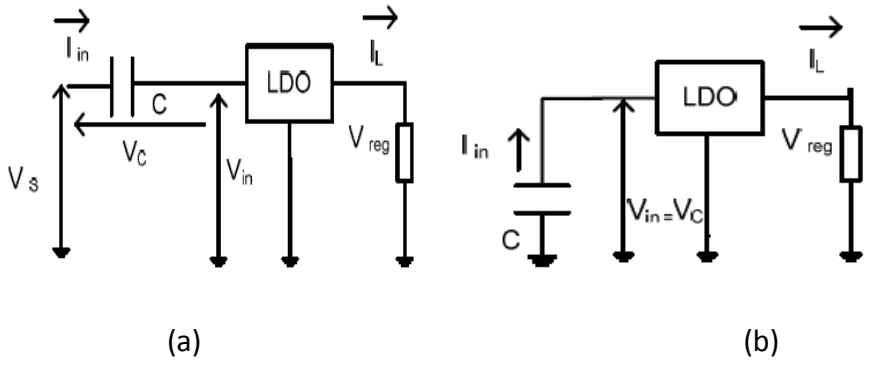
As discussed in an earlier in Chapter 2.3, the introduction of LDO is to address the requirement of noise-sensitive and fast transient response in the electronic portable devices. In many applications, the dropout voltage is between 0.1V to 2V with extremely low power control circuits, providing efficiencies around 65% at the lower end and much higher for lower dropout voltages. Combining LDO and switch-mode regulators is commonly used in a portable device and this concept is used in commercial systems which is called Point of Load (POL). LDO operates the same as the basic LDO discussed in Chapter 3.1.1 (that consists the standard NPN regulator except that the pass series transistor has been replaced by a single PNP or a PMOS transistor) which can hold the output voltage in regulation with much lower voltage differences across the series transistor. So, the efficiency of the LDO is good only when the difference between the input and output voltage is low. Meanwhile switch-mode power supplies offer substantial efficiency with the difference between input and output voltages is higher.

It can be hypothesised that the voltage change (*dv*) across a larger capacitance such as a supercapacitor is very small when a finite charge (or discharge) current *i(t)* flows during a finite time *d(t)*

$$dv = \int_0^t \frac{1}{C} i(t)dt \tag{17}$$

In a circuit if a pre-charged large capacitor is used as a voltage dropper, the effect of this (*dv*) can be neglected in terms of operational principals applicable to a circuit. For example, a large series capacitor will not act as a blocking element in a series circuit for a short time. Based on this principle, the supercapacitor based energy recovery technique that is suitable for linear regulator was developed using a single supercapacitor or an array of

supercapacitor in the series path to recover and reuse the wasted energy. Figure 3.3 below shows the simplified approach to this patent technique.



(a) (b)

Figure 3. 3: Concept of supercapacitor energy recovery (a) minimizing the series element dissipation, (b) reuse of stored energy (Source from Kularatna et al [6])

3.1.1 Possible Scenario Of Energy Recovery

In Figure 3.3 above, the supercapacitor is charged by the input current of the LDO are charged by supercapacitor and the stored energy in the supercapacitor is reused by the LDO in the next stage. Using this method, average efficiency of the overall circuit can be improved by a significant amount, while maintaining the useful characteristic of a linear regulator. The linear regulator in Figure 3.3(a) is designed with an LDO which operates with a low voltage difference between the input and output sides of the series pass element. A pre-charged supercapacitor is placed in series with the series pass element until the V_{in} reaches the lowest allowed input voltage value $V_{in,\ min}$. In the next stage, the capacitor is placed in parallel to the input of the linear regulator to discharge the supercapacitor energy into the regulator stage.

If the initial voltage across the supercapacitor is V_{CO} before placing it in series with the LDO, after a period of Δt , the instantaneous voltage across the capacitor, V_C is given by,

$$Vc = Vco + \frac{I_{L.}\Delta t}{C} \quad (18)$$

If the unregulated source voltage is *Vs,* and the instantaneous voltages across the supercapacitor and the LDO are V_C and V_{in} respectively,

$$V_S = V_C + V_{in} \quad (19)$$

Series supercapacitor charges until V_{in} reaches the $V_{in(min)}$ while the voltage across the capacitor reaches (V_s - $V_{in\ (min)}$) at the end of the charging time. In order to discharge this supercapacitor later up to $V_{in(min)}$, it should satisfy the criteria V_S>2 $V_{in(min)}$.

After the charging process of the supercapacitor, its stored energy can be reused until its terminal voltage drops back to $V_{in\ (min)}$ as shown in Fig. 33(b) satisfying the following equation.

$$V_S - 2V_{in(\min)} = \frac{I_L \Delta t}{C} \quad (20)$$

In this case, the circuit only draws power from the unregulated input supply only during half the time of its operating period. During charging the supercapacitor, its draws current from the unregulated supply and meanwhile during the discharging the supercapacitor itself, delivers the power to the circuit keeping the unregulated supply disconnected from the circuit. So, the average input current is $\frac{I_{in}}{2}$. In summary, the circuit operated with a net zero charge on capacitor over the total cycle.

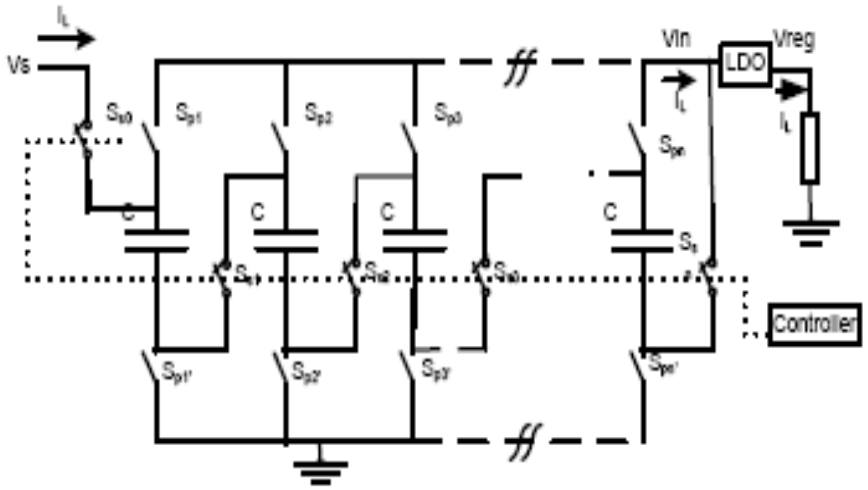
Therefore, considering ideal capacitors and switching elements, approximate end-to end efficiency of the case where $Vs > 2V_{in(\min)}$ is given by the following:

$$\eta = \frac{Output \quad power}{Input \quad power} = \frac{I_L V_{reg}}{V_S \frac{I_{in}}{2}} = \frac{2V_{reg}}{V_S} \tag{21}$$

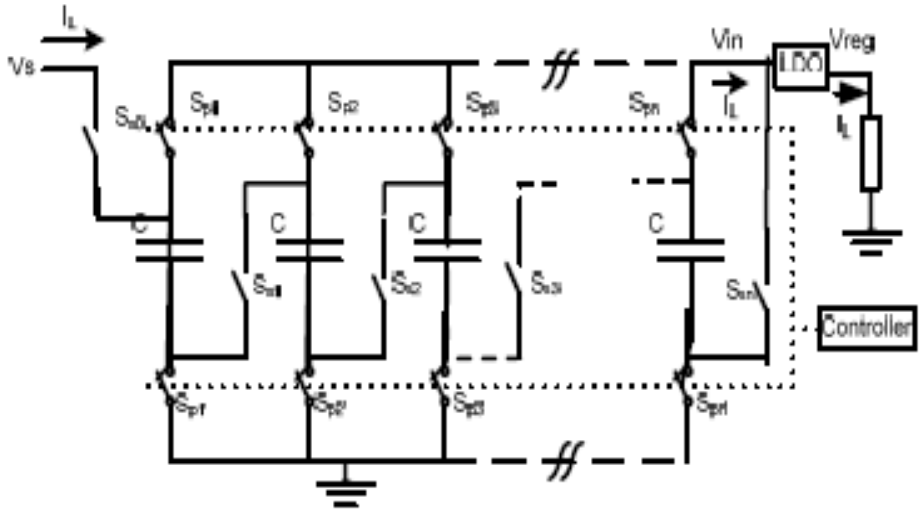
With a very low frequency of supercapacitor circulation, technique allows low current linear regulators based on a simple LDO output stage. Versatility of this technique allows a wide range of supercapacitor based linear DC power supply topologies, maintaining the advantages of linear power supplies, and eliminating the efficiency limitation.

It is important to note that in this case capacitors are not used for any DC-DC conversion purposes, as in the case of switched-capacitor type DC-DC converters such as voltage doublers and inverters. In these, capacitors are used as voltage droppers in the series path (during the first phase of the cycle) and storing energy, while during the second phase, the capacitor transferring energy to the load, maintaining the charge balance during the entire cycle.

For this report, we concentrate for the case where $V_S > 3V_{in(\min)}$ and applicable for situation 5V – 1.5V regulators and similar. For this configuration, a group of identical series supercapacitor are connected in series with the LDO shown in Figure 3.4(a). When the input voltage of the LDO, V_{in} reaches the $V_{in(min)}$, the controller will transfers the switch to parallel capacitor configuration as in Figure 3.4(b), reusing the accumulated charged in the supercapacitor until its terminal voltage drops back to $V_{in(min)}$[6].



(a)



(b)

Figure 3. 4: (a) Configuration suitable for (a) Charging (b) Discharging (Source from Kularatna, et al [6])

3.1.2 Theory Implementation of 5V to 1.5V configuration

For the application of 5V – 1.5V, two supercapacitors that are placed in series are charged up until to a maximum of 3.4V which give 1.7V for each supercapacitor when placed parallel to the input of the LDO. During the discharge phase, it could drops from 1.7V to 1.6V per supercapacitor.

For the application of $V_S > 3V_{in(\min)}$, it is assumed that all the supercapacitors and switches are identical and the ESR of the supercapacitor is r_s and the on-resistance of a switch is R_{on}. From the datasheet of PVN012, on-resistance of a switch, **R_{on} = 0.04Ω** (for C connection) and from the datasheet of Maxwell Supercapacitor, the ESR of the supercapacitor, **r_s = 0.4Ω**.

Table 3.1 below is the parameter and relationship for cases $V_S > 3V_{in(\min)}$ which has been derived by Kularatna et al [6] in the previous study. These parameters are used to calculate the theoretical value of the prototype.

Table 3. 1: Parameter and relationship for cases $V_S > 3V_{in(\min)}$ (Source: Nihal Kularatna et al [6])

Parameter	$V_S > 3V_{in(\min)}$
n	$n \le \dfrac{V_s - V_{in(\min)} - I_L(3R_{on} + r_s)}{V_{in(\min)} + \Delta V_{in} + I_L(R_{on} + r_s)}$
$V_{C(\max)}$	$\dfrac{I_L}{n}\{V_s - V_{in(\min)} - [(n+1)R_{on} + nr_s\}$
$V_{in(\max),dis}$	$\dfrac{1}{n}\left[(V_s - V_{in(\min)} - I_L\{(n+3)R_{on} + (n+1)r_s\}\right]$
$V_{in(\max),char}$	$\left[(V_s - nV_{in(\min)} - I_L\{(n+3)R_{on} + (n+1)r_s\}\right]$
Δt_{dis}	$C\left[\dfrac{V_s - (n+1)V_{in(\min)}}{I_L} - \{(n+3)R_{on} + (n+\_1)r_s\}\right]$
Δt_{dis}	$\dfrac{C}{n}\left[\dfrac{V_s - (n+1)V_{in(\min)}}{I_L} - \{(n+3)R_{on} + (n+\_1)r_s\}\right]$
η_r	$1+n$

From the above prediction, the $\mathbf{V_{in(max),dis}}$ **=1.7V** and the $\mathbf{V_{in(min)}}$ **= 1.6V**. Therefore, the expected minimum voltage fluctuation of V_{in} that is ΔV_{in} *:*

$$V_{in(\max),dis} \geq V_{in(\min)} + \Delta V_{in}$$

$$\Delta V_{in} \leq V_{in(\max),dis} - V_{in(\min)}$$

$$\leq \mathbf{0.1V}$$

Therefore, the number of supercapacitors (n) required for the design can be found as below with the unregulated voltage source, V_s = 5V

$$n \leq \frac{V_s - V_{in(\min)} - I_L(3R_{on} + r_s)}{V_{in(\min)} + \Delta V_{in} + I_L(R_{on} + r_s)} \leq \frac{5 - 1.6 - 200x10^{-3}[3(0.04) + 0.4]}{1.6 + 0.1 + 200x10^{-3}(0.04 + 0.4)}$$

$$\leq 1.84 \approx \mathbf{2}$$

With the use of a very low power controller, we can neglect its power consumption for approximate efficiency calculations. During the supercapacitor's charging, each capacitor leg carries a current of I_L = 200mA, and when the supercapacitors are placed in charging mode in series; the maximum allowed voltage of the supercapacitor is given by :

$$V_{C(\max)} = \frac{1}{n}\{V_s - V_{in(\min)} - I_L[(n+1)R_{on} + nr_s]\}$$

$$= \frac{1}{2}\{(5 - 1.6) - 200x10^{-3}[(2+1)0.04 + 2(0.4)]$$

$$= \mathbf{1.608V}$$

When V_{in} reaches $V_{in(min)}$ for the LDO, capacitor reaches its maximum voltage. Therefore the supercapacitor can be chosen with the rating,

$$V_{in} = V_C - \frac{I_L}{2}\left[(n+1)R_{on} + nr_S\right]$$

$$= 1.6 - \frac{200x10^{-3}}{2}[(2+1)0.04 + 2(0.4)]$$

= **1.508V**

Therefore the rating for the supercapacitors used in the prototype work is 2.5V.

And the maximum allowed input voltage of the LDO during charging is:

$$V_{in(\max),char} = \left[(V_s - nV_{in(\min)} - I_L\{(n+3)R_{on} + (n+1)r_s\}\right]$$

= [5 -2(1.6) – 200x10^{-3}[(2+3)0.04 + (2+1)0.4]]

= **1.52V**

Discharging process starts when the capacitor reaches its maximum allowed voltage $V_{C(max)}$. so that the above equation can be written as,

$$V_{in(\max),dis} = \frac{1}{n}\{V_{C(\max)} - I_L\left[(n+3)R_{on} + (n+1)r_s\right]\}$$

$$V_{in(\max),dis} = \frac{1}{n}\{(V_s - V_{in(\min)}) - I_L[(n+3)R_{on} + (n+1)r_s]\}$$

$$= \frac{1}{2}\left\{(5-1.6) - 200x10^{-3}[(2+3)0.04 + (2+1)0.4]\right\}$$

= **1.56V**

Capacitor discharges until the V_{in} reaches the lowest allowed input voltage value $V_{in,\ (min)}$. If the voltage across a capacitor is $V_{C(min),dis}$ at this stage,

$$V_{in(\min)} = V_{c(\min),disc} - \frac{I_L}{n}[(n+1)R_{on} + nr_s])$$

$$V_{c(\min),dis} = V_{in(\max),char} - \frac{I_L}{n}(2R_{on} + r_s)$$

= 1.52 – (200x10^{-3}/2)[2(0.04)+0.4]

= **1.472V**

Charging time of a capacitor

$$\Delta t_{char} = \frac{C}{n}\left\{\left[\frac{V_s - (n+1)V_{in(\min)}}{I_L}\right] - [(n+3)R_{on} + (n+1)r_s\right\}$$

$$= \frac{4}{2}\left\{\frac{[(5) - (2+1)1.6]}{200x10^{-3}} - [(2+3)0.04 + (2+1)0.18\right\}$$

= **0.52s = T**

Discharging time for a capacitor,

$$\Delta t_{dis} = C\left\{\left[\frac{V_s - (n+1)V_{in(\min)}}{I_L}\right] - [(n+3)R_{on} + (n+1)r_s]\right\}$$

$$= 4\left\{\frac{[5 - (2+1)1.6}{200x10^{-3}} - [(2+3)0.04 + (2+1)0.18\right\}$$

= **1.04s**

Therefore, $\Delta t_{dis} = \frac{T}{n}$

As the circuit draws current only from the supply only through the charging cycle, average current taken from the supply,

$$I = \frac{I_L T + 0.\frac{T}{n}}{T + \frac{T}{n}} = \frac{I_L}{1 + \frac{1}{n}}$$

End to end efficiency improvement factor, η_r is given by,

$$\eta_r = \frac{V_s\left[\frac{I_L}{1 + \frac{1}{n}}\right]}{I_L . V_s} = n + 1$$

$$= 3$$

3.1.3 Losses and Loss Minimization

In this technique losses are typically related to the following:

i. Dissipation in switches

ii. Dissipation in ESR of capacitors

iii. Losses due to switch transitions (frequency dependent)

iv. Losses due to paralleling capacitors with different voltages

Losses in item (i) and (ii) are device dependant. Item (iii) is a very minimal which in this case as capacitor switching frequency is very low, compared to a switch-mode power supply. Item (iv) is very specific to this technique [6].

3.2 Design Approach

Figure 3.5 below is the basic circuit during charging mode that consists of one PIC controller (MicroChip PIC16F684-I/P), seven solid-state relay (International Rectifier - PVN012), two supercapacitors rated at 4F 2.5V (Maxwell), LDO and (LP38842-National Semiconductor).

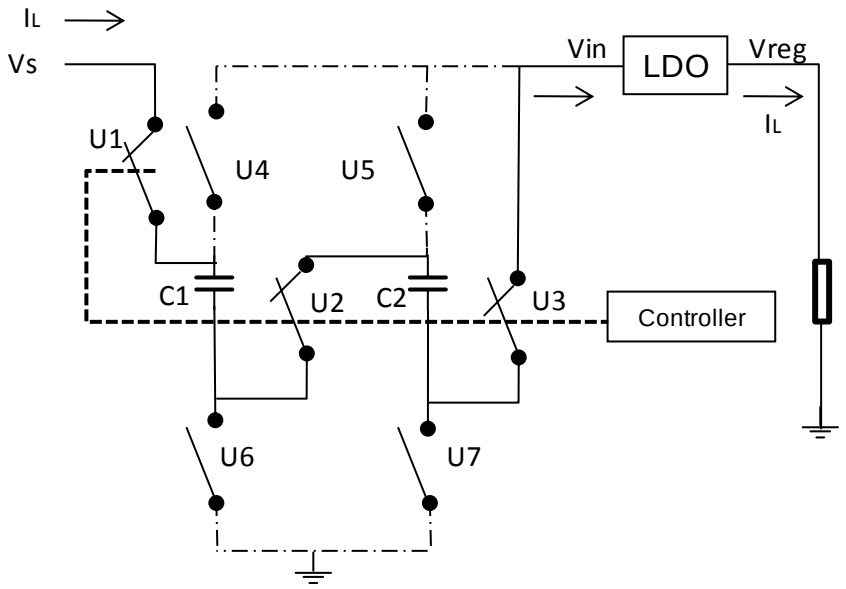


Figure 3. 5: Basic circuit during charging mode

During charging mode, the circuit is powered up by input voltage, V_s and solid-state relay (SSR) U1, U2 and U3 will be activated by the controller. The supercapacitors that are put in series will be charged up by Vs until the minimum input voltage, V_{in} for the LDO is reached. The Table 3.2 below shows state of the solid state relay when charging and discharging mode.

Table 3. 2: State of solid-state relay during charging and discharging mode

Mode	State of solid-state relay U1, U2 and U3	State of solid-state relay U4, U5, U6 and U7
Charging	ON	OFF
Discharging	OFF	ON

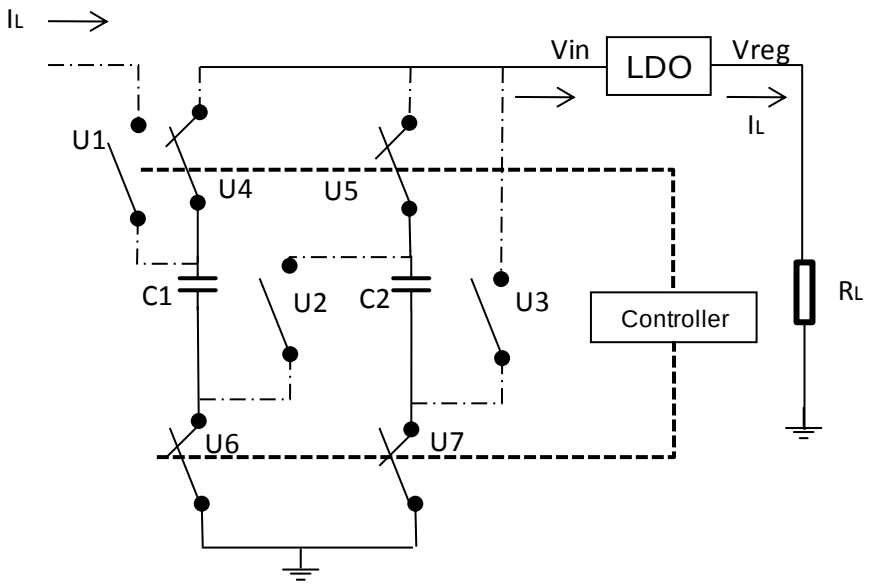


Figure 3. 6: Basic circuit during discharging mode

Figure 3.6 above is the basic circuit during discharging mode. Here Vs is disconnected from the circuit by solid-state relay U1. Solid-sate relay U4, U5, U6 and U7 connect C1 and C2 in parallel to discharge the energy stored to the LDO. The C programming of PIC controller is given in Appendix 3.

In the practical circuit, the solid-state relay is a single pole, open solid-state relay and it utilizes the output switch, driven by an integrated circuit power MOSFET photovoltaic relay. This output switch is controlled by radiation from a GaAIAs LED which is optically isolated from the photovoltaic generator. During charging mode, the practical circuit is shown in Figure 3.7 below:

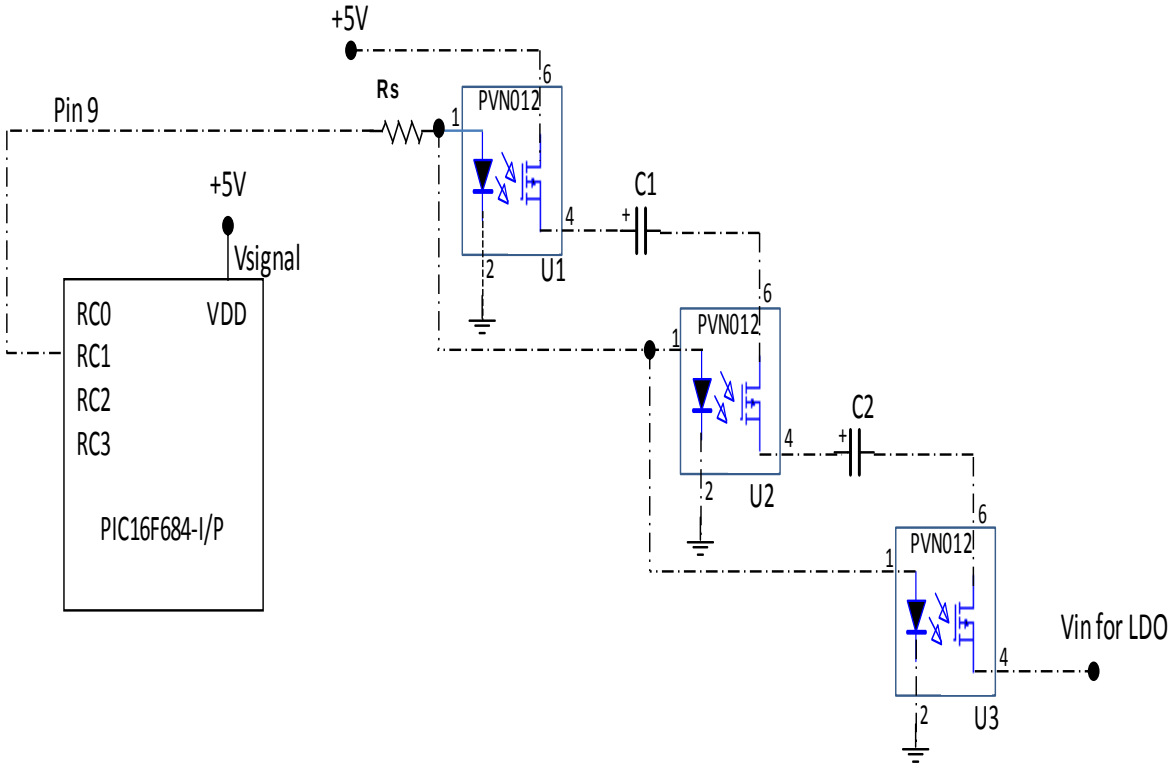


Figure 3. 7: Practical charging mode circuit

Resistor Rs is needed to limit the current through GaAIAs LEDs inside the solid-state relay. During the charging mode, RC1 of the PIC controller becomes high to solid-state relay on U1, U2 and U3. The total current taken from RC1 is about 5mA x 3 = 15mA (since the current taken by one LED is 5mA). The output high voltage of PIC controller is about 4.5V. The forward bias voltage of LED at 5mA can be also found in the datasheet PVN012 (Input Characteristic graph) to be 0.9V. Rs can be calculated as below:

$$R_S = \frac{V_{Pin9} - V_{Diode}}{I_{TotalU1,U2\&U3}} = \frac{4.5v - 0.9V}{15mA} = 240\Omega \approx 180\Omega$$

During discharging mode, the practical circuit is shown in Figure 3.8 below:

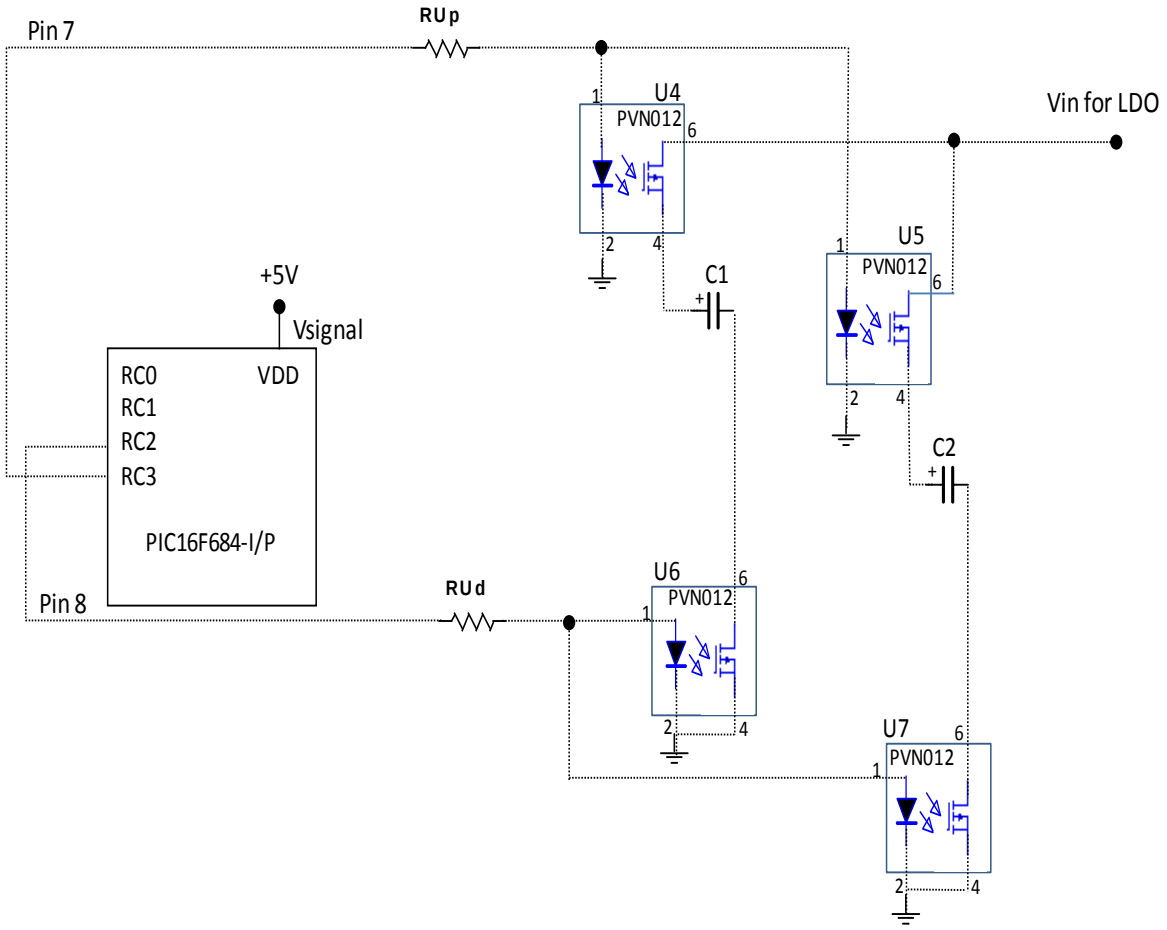


Figure 3. 8: Practical discharging mode circuit

During discharging mode, RC2 and RC3 pins switches on solid-state relay pair U4-U5 and U6-U7 respectively. The current limiting resistor RUp and RUd can be found in a similar way. During discharging mode, RC2 and RC3 become high to solid-state relay pair on U4-U5 and U6-U7 respectively. The total current taken from RC2 is about 5mA x 2 = 10mA as well as RC3. RUp can be calculated by:

$$RU_p = \frac{V_{Pin7} - V_{Diode}}{I_{TotalU4\&U5}} = \frac{4.5v - 0.9V}{10mA} = 360\Omega \approx 330\Omega = RU_d$$

The complete block diagram of the practical circuit is shown in Figure 3.9.

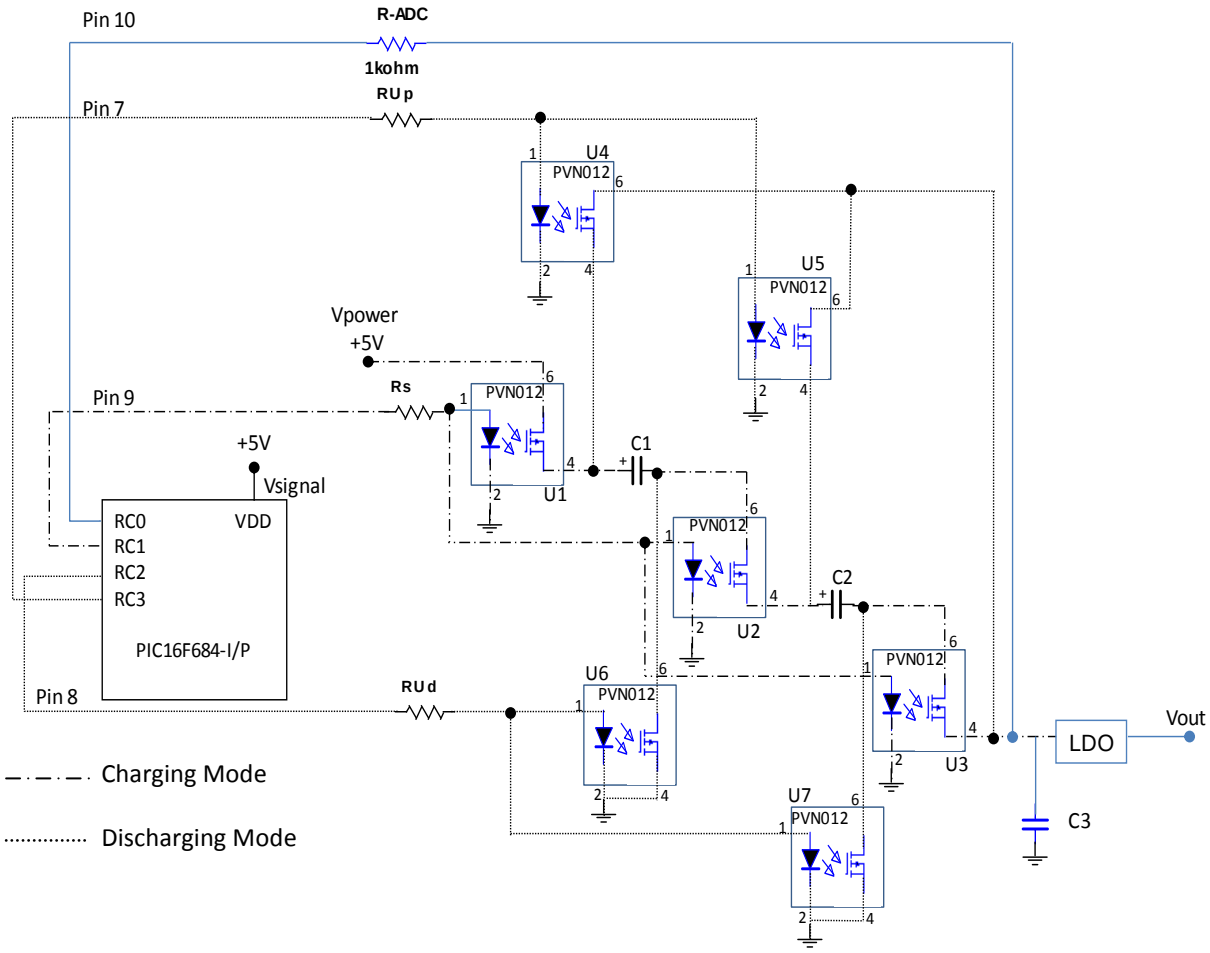


Figure 3. 9: Complete practical circuit

The circuit above have two power supplies noted as Vs = 5V (to charge up the supercapacitors during charging mode) and Vsignal = 5V (to power up the PIC controller). The output high voltage of PIC controller is about 4.5V During charging mode, RC1 of the PIC controller becomes high to solid-state relay on U1, U2 and U3. RC2 and RC3 become high to solid-state relay pair U4-U5 and U6-U7 respectively during discharging mode. Pin 10 will be connected to Analog-Digital-Converter (ADC) to compare the actual input voltage of the LDO with the set voltage inside the PIC controller. The value of R-ADC is 1kΩ. The function of Rs, RUp and RUd is to limit the current through the SSR. The red and green lines represent the circuit during charging and discharging modes respectively.

The programming of the PIC controller (MicroChip PIC16F684-I/P) is based on the flow chart in Figure 3.10 below:

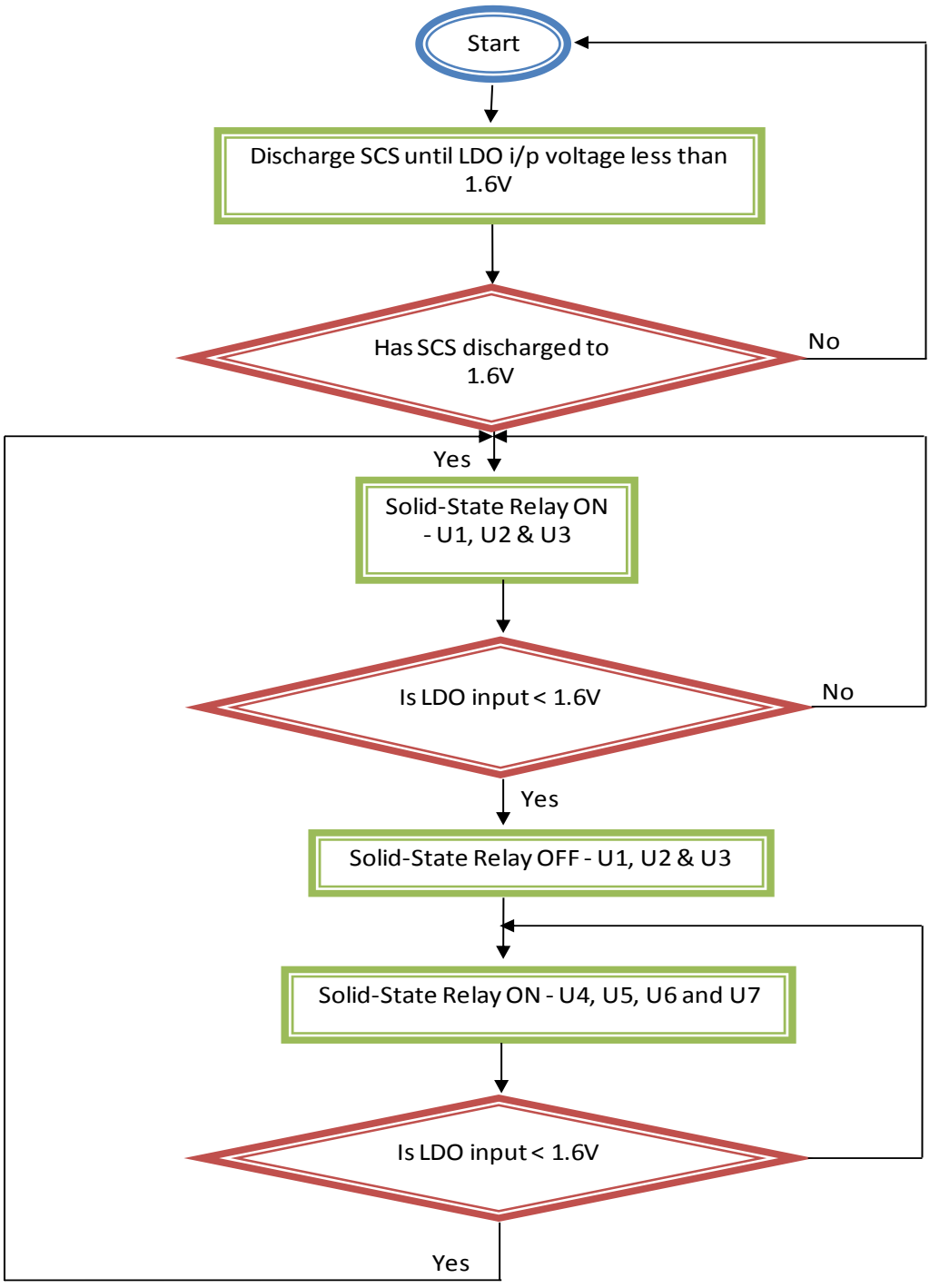


Figure 3. 10: Flow chart of C programming of the PIC controller

The PIC controller will start with discharging the supercapacitors until it reaches 1.6V. After that, the PIC controller will activate Pin 9 (SSR on U1,U2 and U3) and charge the supercapacitors until Pin 10 (ADC) detects the input voltage of LDO below 1.6V. Then, the PIC controller will turn off pin 9 and turn on pin 7 and pin 8 (SSR on U4, U5, U6 and U7). At the same time, the supercapacitors will be in parallel configuration and start the discharge until the minimum voltage at the input voltage of LDO is less than 1.6V. The PIC controller will turn off pin 7 and pin 8 and turn on pin 9 back. The same process is repeated continuously.

The actual circuit is as in Appendix 2.

Chapter 4 – Experimental Results

From the datasheet of the LDO (LP38842, National Semiconductor), the load regulation when the load current varies between 10mA to 1.5A is 0.4% /A minimum to 1.1% /A maximum. Meanwhile for the line regulation is 0.01% /V when the input voltage varies between 2.5V to 5.5V.

The output voltage of the circuit is as shown in Figure 4.1 below.

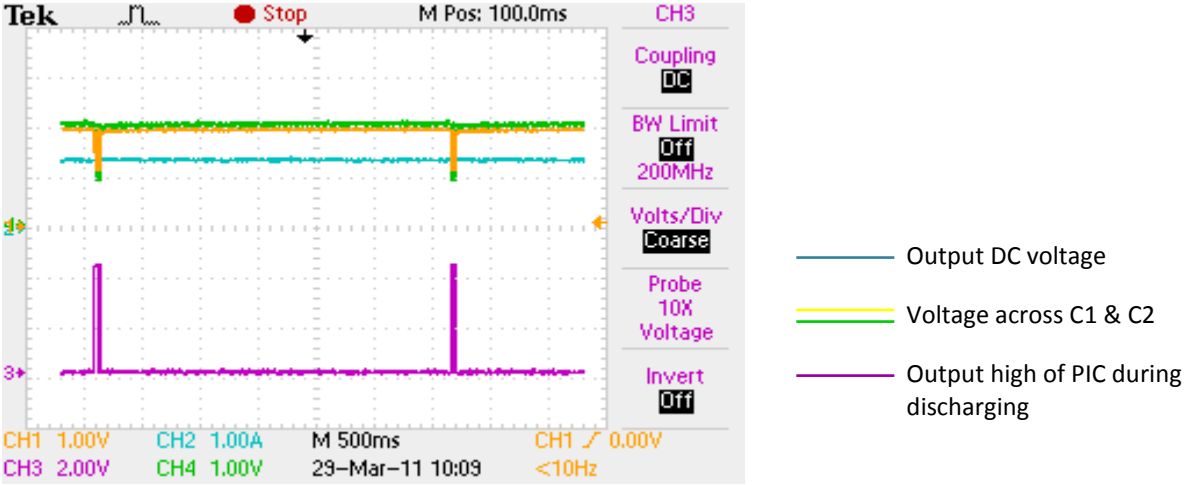


Figure 4. 1: Output DC voltage of prototype circuit

The output DC voltage of the prototype circuit is 1.4V at 10mA load current. The frequency of the system is about 1.825Hz.

4.1 Load And Line Regulation

The measurement is taken for the $Io_{(dc)}$ and $Vo_{(dc)}$ for load regulation with Vin= 5V as shown in Table 4.1.

Table 4. 1: Measurement for load regulation

Io(DC) (mA)	Vout(DC) (V)
20	1.45
40	1.43
60	1.42
80	1.41
100	1.4
120	1.39
140	1.38
160	1.37
180	1.36
200	1.35

A load regulation graph is plotted for the above reading as in Figure 4.2 below:

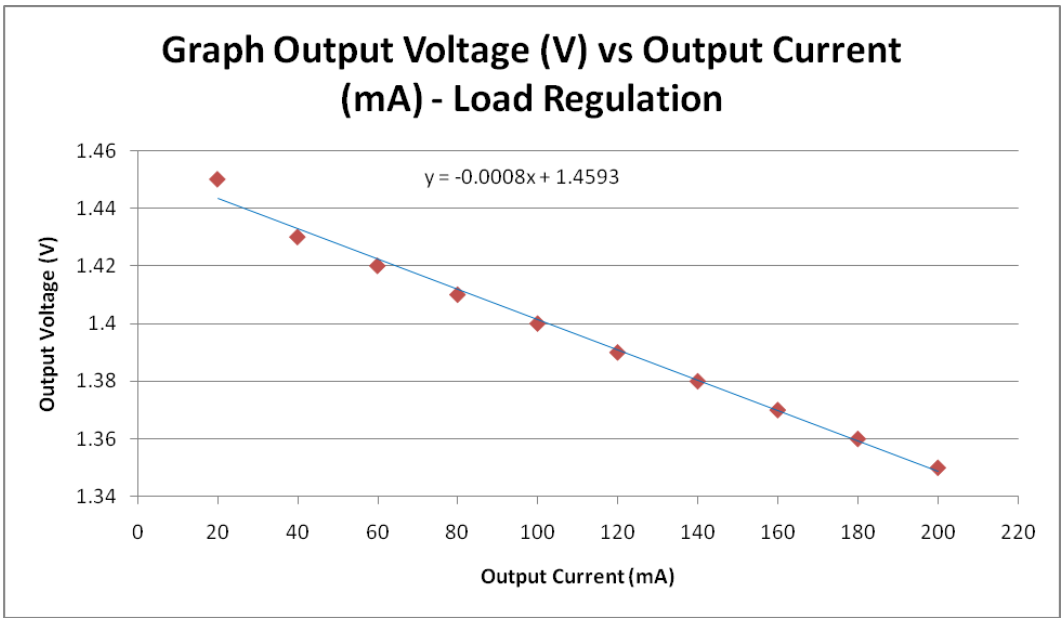


Figure 4. 2: Load regulation graph

For line regulation, the measurement for $V_{in(dc)}$ and $V_{o(dc)}$ was taken with various constant load current as shown in Table 4.2 below.

Table 4. 2: Measurement for line regulation

Vin(dc) (V)	Vout(DC) (V) at I_{LOAD}= 50mA	Vout(DC) (V) at I_{LOAD} = 100mA	Vout(DC) (V) at I_{LOAD}= 150mA	Vout(DC) (V) at I_{LOAD}= 200mA
3.50	1.43	1.38	1.38	1.38
4.00	1.42	1.38	1.39	1.39
4.50	1.41	1.42	1.41	1.38
5.00	1.42	1.42	1.39	1.39
5.50	1.43	1.40	1.38	1.38
6.00	1.44	1.42	1.38	1.38
6.50	1.44	1.40	1.38	1.36
7.00	1.44	1.40	1.39	1.37

A line regulation graph is plotted for the above reading as in Figure 4.3 below:

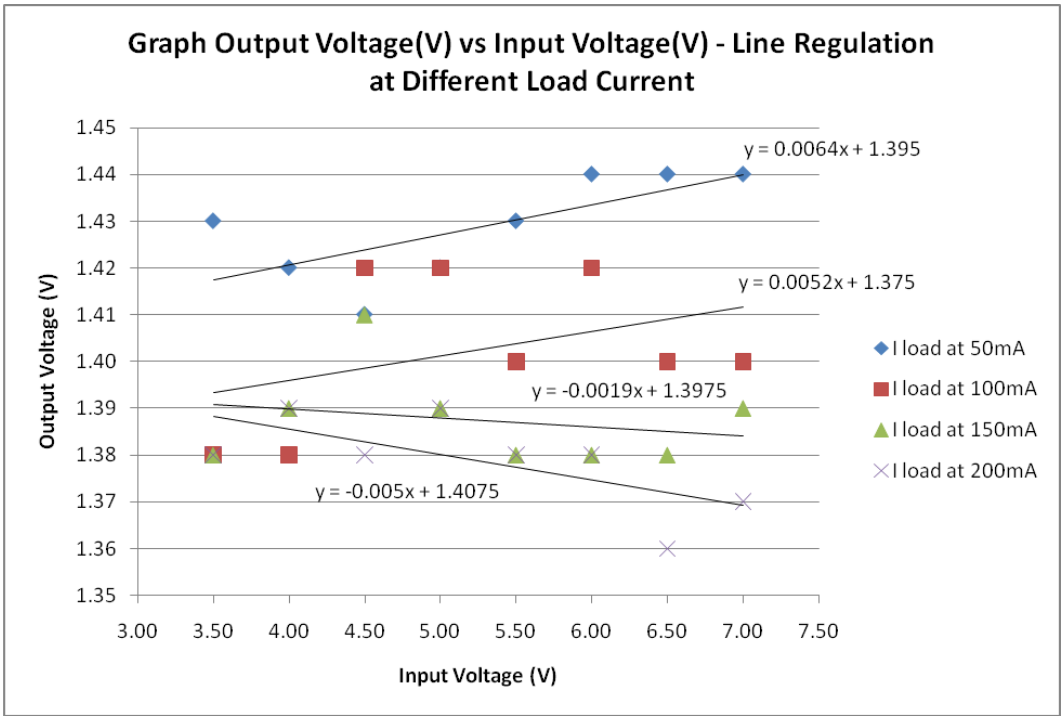


Figure 4. 3: Line regulation graph at different load current

4.2 Efficiency

For the efficiency, the readings are taken at a different output current with a constant input voltage as in Table 4.3:

Table 4. 3: Measurement of efficiency with a constant input voltage

Vin(V)	Iin(A)	Pin(W)	Iout(A)	Vout(V)	Pout(W)	Efficiency(%)
5.00	0.038	0.190	0.03	1.45	0.044	22.89
5.00	0.059	0.295	0.05	1.44	0.072	24.41
5.00	0.100	0.500	0.12	1.40	0.168	33.60
5.00	0.130	0.650	0.15	1.41	0.212	32.54
5.00	0.148	0.740	0.17	1.40	0.238	32.16
5.00	0.171	0.855	0.20	1.40	0.280	32.75

From Table 4.3, the below graph is plotted for Efficiency Vs Output Current.

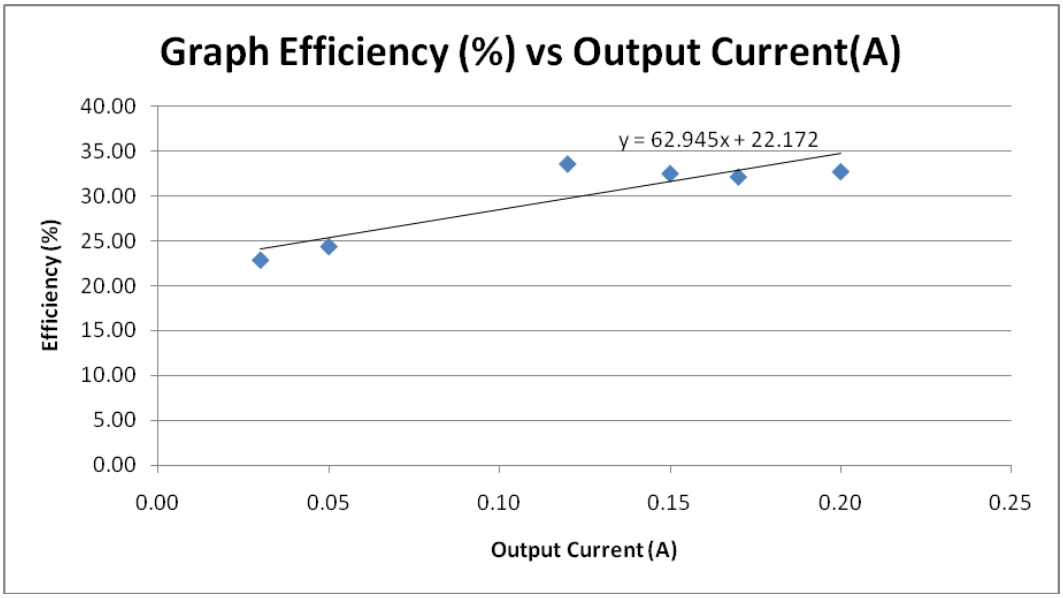


Figure 4. 4: Graph efficiency Vs output current of the circuit

The same reading as Table 4.3 above is taken but at the different input voltage with a constant output current . It is shown in Table 4.4 below:

Table 4. 4: Measurement of efficiency with a different input voltage at same load current.

Vin(V)	Iin(A)	Pin(W)	Iout(A)	Vout(V)	Pout(W)	Efficiency(%)
3.48	0.097	0.338	0.104	1.42	0.148	43.75
3.96	0.085	0.337	0.104	1.42	0.148	43.87
4.48	0.085	0.381	0.104	1.40	0.146	38.24
5.04	0.070	0.353	0.104	1.40	0.146	41.27
5.52	0.093	0.513	0.104	1.40	0.146	28.36
6.00	0.101	0.606	0.104	1.42	0.148	24.37
6.50	0.106	0.689	0.104	1.41	0.147	21.28

A table has been tabulated for the linear regulator as in Table 4.5 below:

Table 4. 5: Efficiency of linear regulator

Vin(V)	Vout(V)	Efficiency
3.50	1.50	42.86
4.00	1.50	37.50
4.50	1.50	33.33
5.00	1.50	30.00
5.50	1.50	27.27
6.00	1.50	25.00
6.50	1.50	23.08

A graph as in Figure 4.5 is plotted to compare the efficiency of the linear regulator with the supercapacitor at the different input voltage.

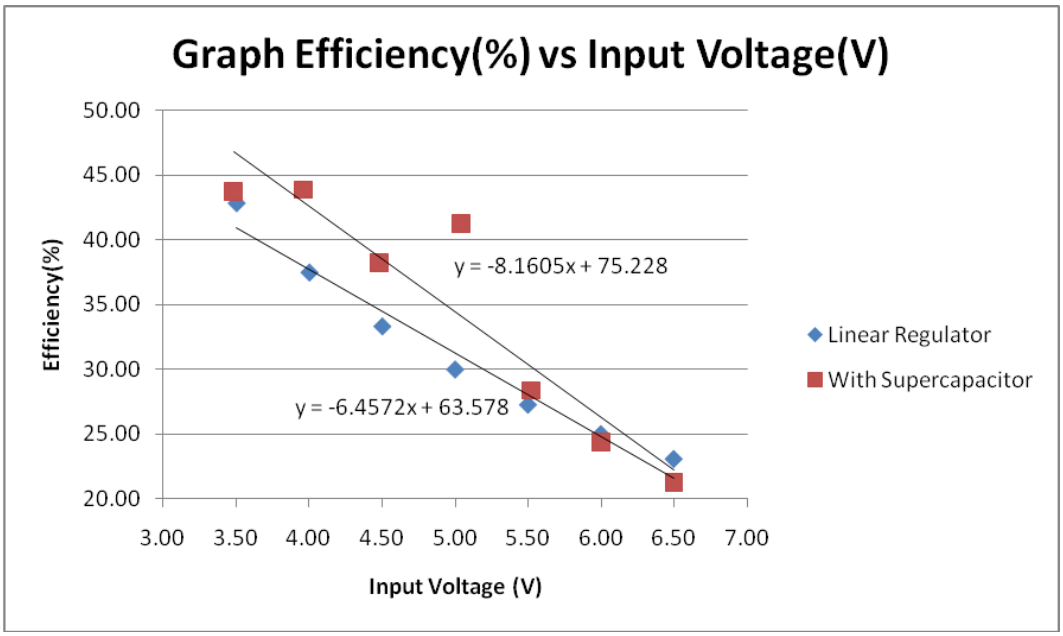


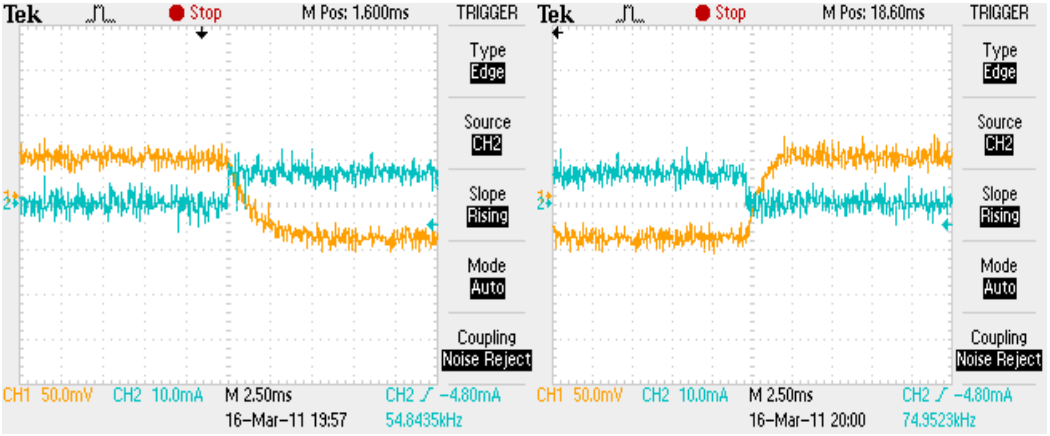
Figure 4. 5: Efficiency comparison between linear regulator and supercapacitor circuit

4.3 Transient Response

TEXIO-PXL151A is electronic equipment that acts as electronic load where load current can be changed to any value as long it is not exceeding the limit range of the TEXIO. The TEXIO have four different setting that is 30V/150A, 4V/150A, 30V/37.5A, and 4V/37.5A. For this testing, the TEXIO is set to 4V/37.5A. Load current slew rate is also available for 150A range and 37.5A range. For 150A range, the slew rate can be change between 1A/µs to 100A/µs meanwhile for 37.5A range, the slew rate can be change between 0.25A/µs to 25A/µs.

The testing has been carried out using TEXIO Electronic Load - PXL151A The switching function of the TEXIO uses to set values in PRESET A (in this experiment, we varied the value by using CC SET = 0.1A) and PRESET B (in this experiment, kept it constant at 0) to execute operation alternately and repeatedly. This switching function is set to two preset times (tA=100ms and tB=50ms). The slew

rate of the TEXIO is set to 0.75A/ µs. The frequency is 30Hz and the duty cycle is 50%. The waveforms are as below:



(a) (b)

Figure 4. 6: The transient waveform (a) rise and (b) fall

Table 4. 6: Measurement of the waveform

Preset A (Present B = 0)	Voltage Dip at the Rise Slew Rate	Voltage Dip at the Fall Slew Rate
0.1A	20mV/ms	40mV/ms

Chapter 5 – Discussion

As per load and line regulation that were obtained from this experiment, the results are not at the required output voltage of the LDO. Its understood that LDO can provide a constant output voltage of 1.5V even when there is variation of the input voltage until it drops as low as 1.6V. In load regulation graph, we can see that at 20mA load current, the output of the LDO is just 1.43V instead of 1.5V. This means that the input voltage of this circuit that provides by the supercapacitors is below than 1.6V.

Let's consider the circuit below when the charging and discharging process takes place in the circuit as in Figure 5.1 and Figure 5.2 respectively:

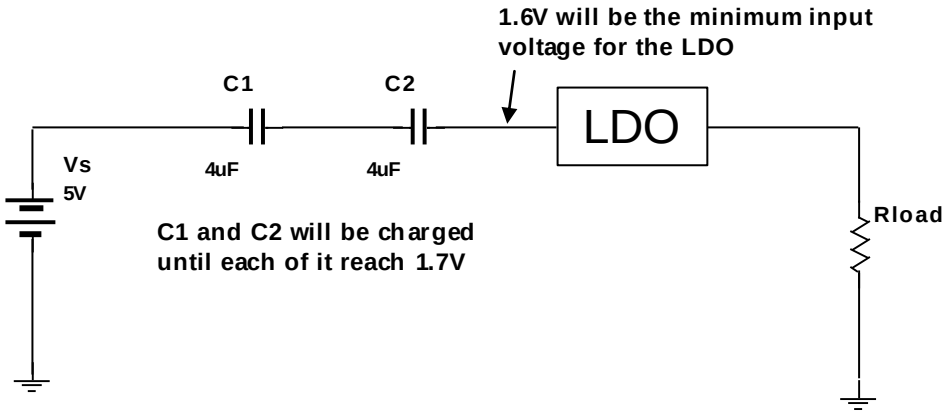


Figure 5. 1: Ideal circuit when the SCs in series and charging mode

During charging mode of the circuit, the supercapacitor will be charged until 1.7V; for each supercapacitor and the minimum input for the LDO is 1.6V.

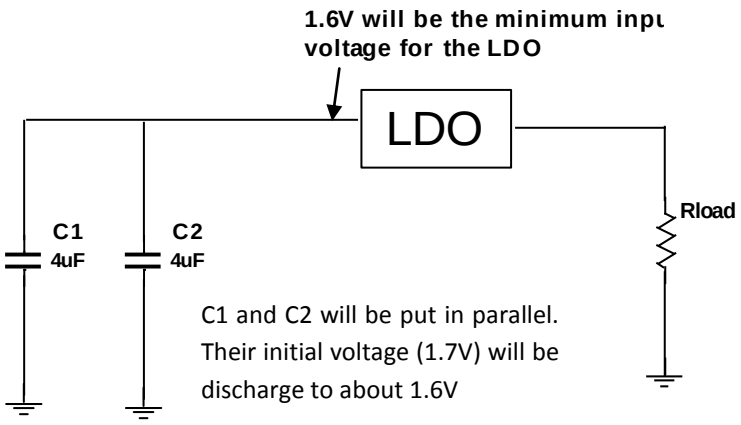


Figure 5. 2: Ideal circuit when the SCs in parallel and discharging mode

During discharging mode, the supercapacitors that had been charged up until 1.7V are put in parallel. During this time, the supercapacitor will only discharge 0.1V since the minimum voltage required of the LDO to operate is 1.6V.

All the above condition, are applied if the circuit is ideal and without any losses. During discharging, the energy delivered by the supercapacitors is very small and can be calculated as below:

$$E = \frac{1}{2}CV^2 = \frac{1}{2}(2)(0.1^2) = 0.01J$$

Where C = total of capacitance in series

$$= \frac{C1C2}{C1+C2} = \frac{(4Fx4F)}{(4F+4F)} = 2F$$

This means that during charging and discharging, the supercapacitors are just charging and discharging a small amount of energy that is later on delivered to the load. At no load, the developed circuit is capable of providing 1.5V output voltage. That's why the output voltage of this experiment is below that what it is supposed to be. During discharging, there is the possibility of the energy that is

suppose to been delivered to the load at about 0.01J might have been shared by the supercapacitors in parallel. This is due to the parallel effect of the supercapacitors and these supercapacitors will try to balance up the discharge voltage.

Now let's consider the circuit below as in Figure 5.3.

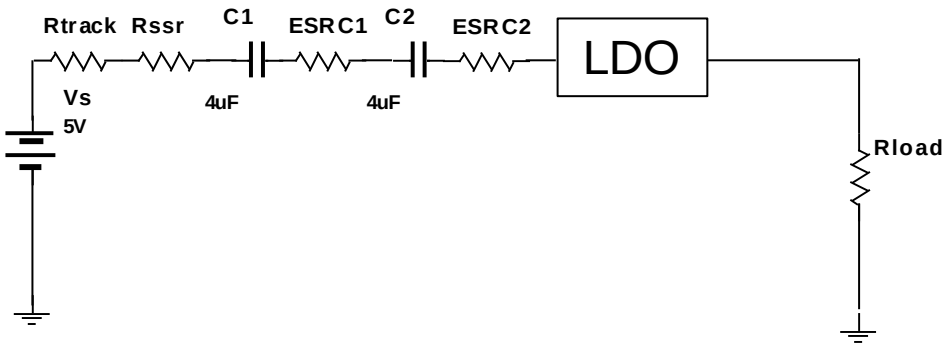


Figure 5. 3: Practical circuit when the SCs in series and charging mode

In practice there are losses due to the PCB track, solid-state relay (SSR) and ESR of the supercapacitors. For this circuit, three SSR are 'ON' during the charging mode and 'C Connection' is used for the SSR. As per datasheet of PVN012 the R_{on} of the switch for C-Connection is 40mΩ and the ESR for the supercapacitor is 400mΩ.

Let's consider during charging mode, lets assume 20mA current is drawn from load.

Therefore, the loss for switch is , $V_{SSR} = I_L R_{on(SSR)} = 20x10^{-3} \mathrm{X} 400x10^{-3}$

= 0.8mV (1 switch)

= 2.4mV (3 switches)

Loss for ESR, $V_{ESR} = I_L ESR_{supercap} = 20x10^{-3} \mathrm{X} 400x10^{-3}$

= 8.0mV (1 supercapacitor)

= 16.0mV (2 supercapacitors)

And we assume the PCB track loss is about 1mV. The total loss will be around 17mV at 20mA load current. This will increase as the load current is increased. This shows that during charging mode, each supercapacitor is actually charged to a voltage less than 1.7V. And in actual circuit, the supercapactors are not equally charged to 1.7V. This is due to the different in the actual ESR of the supercapacitor even though both capacitors are the same capacitance and voltage rating. Furthermore, when these supercapacitors are put in parallel combination during discharging mode, the input is lower than it expected. This mode is shown in the Figure 50 below.

In practice, the circuit during the discharging mode can be considered as below in Figure 5.4.

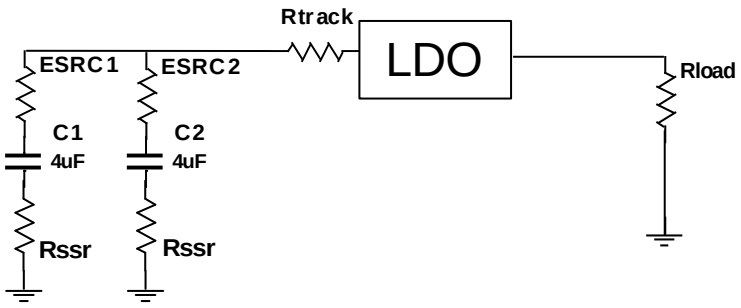


Figure 5. 4: Practical circuit when the SCs in parallel and discharging mode

For discharging mode, four solid-state relay's (SSR) are used to connect two supercapacitors in parallel. Two SSR are using 'A connection' with R_{on} = 100mΩ and the other two SSR are using 'C-connection' with R_{on} = 40mΩ.But for each one of supercapacitor, two SSR are been connected, one with A Connection and the other one with C Connection. In the Figure 5.4 above, the R_{SSR} represenst the R_{on} of the SSR with A and C Connection. These both connections are shown in Figure 5.5 below.

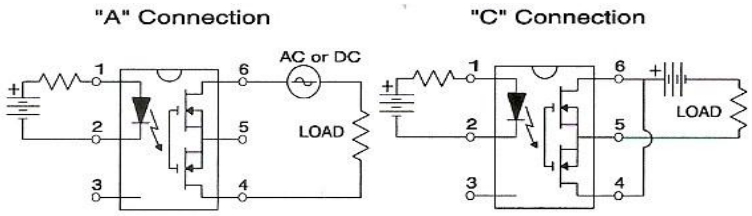


Figure 5. 5: Connection of solid-state relay (a) A connection (b) C connection

The reasons for having two SSR with A connection (labelled as U4 and U5 in the complete circuit) are because of the possibility of the current to flow from C1 to C2 or vice versa. This is due to the parallel effect of the supercapacitors. The A connection allowed either side to be positive or negative terminal. To avoid this to happen, C connection is used beside its low R_{on} compare with A connection.

Let's consider during discharging mode, the circuit draws 20mA to the load.

The total resistance of the circuit is [(R_{SSR}+ESR) of C1 // (R_{SSR}+ESR) of C2] + R_{track}

R_{SSR}+ESR of C1 = [(40mΩ+100mΩ) + 400mΩ] = 540mΩ

So, the total resistance = 540mΩ//540mΩ

= 270mΩ

The loss when the circuit draw 20mA load current = 270mΩ x 20mA

= 5.4mV

Again, the loss of the voltage of the circuit during discharging mode will increase as the load increases.

The other factor that contributes to the incapability of the circuit to provide the required input voltage of the LDO is because the LED drive current of the solid-state relay is insufficient to drive the power MOSFET inside solid-state relay into the saturation region. The diode forward voltage is 0.9V at 5mA but in the practical, there is a voltage drop inside the PIC controller. PIC controller itself

also has the dc source and its internal resistance that make other losses inside the controller as shown in the Figure 51.

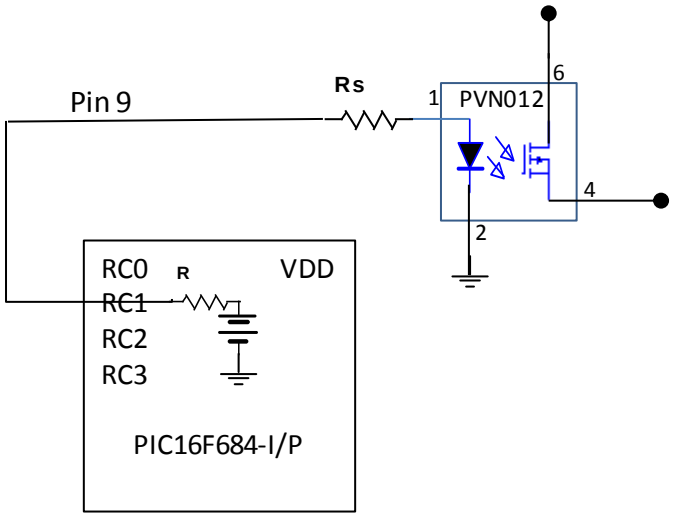


Figure 5. 6: Effect of internal resistance of PIC controller

For above application, in the design approach we assume the current that go through the circuit is given by $I = \frac{V_{PIC} - V_{diode}}{R_S}$, but in practical, there is also an internal resistor of the PIC controller and the current should be given by $I = \frac{V_{PIC} - V_{diode}}{R_S - R_{PIC}}$. This means that the actual drive current is smaller than the expected and it is insufficient to drive the power MOSFET to operate at saturation region.

Due to the effect of power MOSFET inside solid-state relay towards the prototype performance, it is recommended to use alternative components. RF MOSFETs and IGBTs are the suitable solution to overcome this problem. Their configuration as high-side switch and low on resistance are the main factor to be considered during further development of this prototype. With high side switch, the power switch prevent current flow from OUT to IN and IN to OUT when disabled as available from Texas Instrument – TPS 2024. The range of on resistance in this prototype that ranging from 40mΩ to 100mΩ can be reduce

with device such as TPC8025 – TPC8027 from Toshiba Semiconductor that ranging from only 2.1mΩ to 7.5mΩ.

As for the efficiency of the circuit, the results have shown that the efficiency of the circuit is increased when the load current is increased. However, the efficiency is much lower than 30% (Efficiency of linear regulator = $\frac{V_o}{V_{in}} = \frac{1.5}{5} x100\% = 30\%$). The efficiency is less than 30% when the load current is less than 100mA. The efficiency is starting to increase as the load current is increased from 100mA to 200mA. But as expected, since the circuit does not reflect the actual behaviour of LDO, the efficiency is just a little higher than 30%.

When tested to compare the efficiency between the linear regulator with supercapacitors based systems, it is shown that the supercapacitors circuit has more efficiency when compared with the linear regulator.

In term of transient respond, this circuit doesn't give a good transient response at very low frequency (about 30Hz).

Chapter 6 – Conclusion and Future Development

This thesis describes the approach to develop a LDO based linear regulator with a supercapacitor energy recovery technique. The results obtained from this experiment for the load and line regulation don't show the expected behaviour of the LDO as per LDO datasheet (LP38842 – National Semiconductor) The comparison of the load and line regulation between the LDO and the developed circuit are only possible when the circuit is capable of providing a reasonable output voltage with the changes in load current and input voltage.

Even the calculation of theoretical values obtain from Nihal Kularatna et al[6] shows the supercapacitors parameter are less than the basic value. It is shown as in Table 6.1 below.

Table 6. 1: Comparison between basic and the theoretical value

Parameter	Basic Value	Theoretical Value
$V_{C(\max)}$	1.7V	1.608V
$V_{in(\max),dis}$	1.7V	1.56V
$V_{in(\max),char}$	1.7V	1.52V

This prototype circuit did not work at high load current due to the effect of ESR of the supercapacitors, on resistance of the solid-state relay and the track resistance. The thin profile supercapacitors might be the solution to the high ESR of the supercapacitors used in this prototype. But the available thin profile supercapcitors in the market doesn't have high capacitance. The maximum capacitance of these thin profile supercapacitors is 2.4F.

It can be concluded that the efficiency of the LDO based linear regulator can improved by using the supercapacitor energy recovery technique even though

the load and line regulation obtained from the experiment do not reflect the actual capability of the LDO LP38842. However, the efficiency is not as high as 3 times from linear regulator as discussed in Chapter 3 for the end-to-end efficiency improvement factor. Further research is recommended.

There are several development which can be done in the future. These are listed below:

a) All the switches are system on chip (SoC) with very minimal internal resistance. At University of Waikato, a team is expected to develop a project to realise the technique as a system on chip (SoC) solution.

b) The supercapacitor technology is still developing at a fast pace. Supercapacitors with a value over 50F which has the same profile used in this circuit will be not uncommon in the future. This higher supercapacitor will increase the circuit performance. At the same time, the Equivalent Series Resistance (ESR) of the supercapacitor must be minimal as possible.

c) Power MOSFET that used in this prototype can be substitutes with RF MOSFET or IGBT. There are several devices that might be suitable for this application but due to the time constraint, the device can't be implemented in this prototype. The devices that might be suitable are as below :

    i. BF1118 – Silicon RF MOSFET from NXP Semiconductor that has a low on resistance about 23.3mΩ

    ii. TPCA8025-TPCA802r series from Toshiba Semiconductor that has a $R_{DS(on)}$ ranging from 2.1mΩ to 7.5mΩ

d) Try to find a suitable technique to balance the charging and discharging voltage of the supercapacitor when connected in series or in parallel.

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Appendix A – High Current Voltage Regulator

US Patent No: US 7,907,430 B2

US007907430B2

(12) **United States Patent**
Kularatna et al.

(10) **Patent No.: US 7,907,430 B2**
(45) **Date of Patent: Mar. 15, 2011**

(54) **HIGH CURRENT VOLTAGE REGULATOR**

(75) Inventors: **Nihal Kularatna**, Auckland (NZ); **Lewis Jayathu Fernando**, Kalutara (LK)

(73) Assignee: **WaikotoLink Limited**, Hamilton (NZ)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 174 days.

(21) Appl. No.: **12/338,723**

(22) Filed: **Dec. 18, 2008**

(65) **Prior Publication Data**

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(51) **Int. Cl.**
H02M 3/18 (2006.01)
G05F 1/00 (2006.01)
H02J 7/00 (2006.01)

(52) **U.S. Cl.** **363/59**; 323/266; 320/167

(58) **Field of Classification Search** 363/59; 323/266; 327/536; 320/167, 142
See application file for complete search history.

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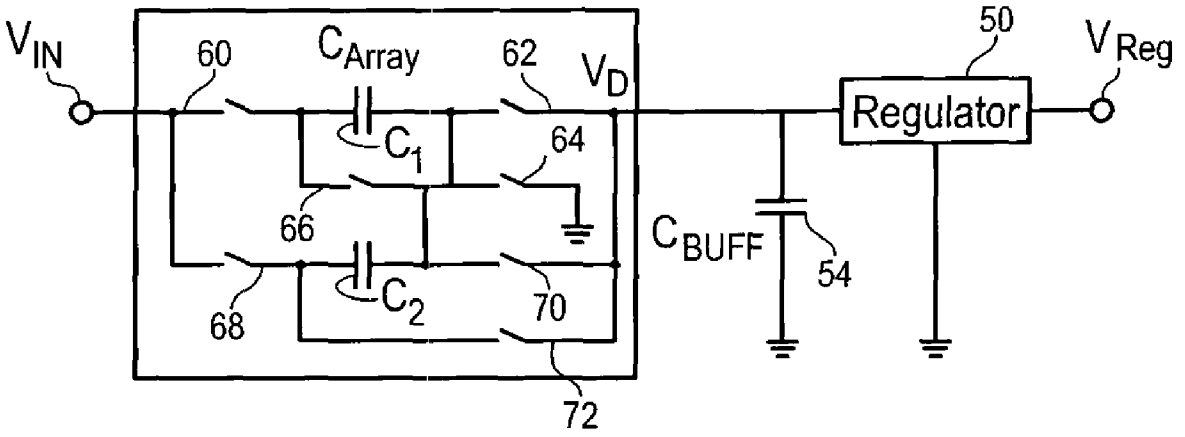
Primary Examiner — Shawn Riley
(74) *Attorney, Agent, or Firm* — Morrison & Foerster LLP

(57) **ABSTRACT**

A linear voltage regulator which includes on its input side an array of switched super capacitors coupled between the power source and the load. This apparatus is capable of delivering currents typically from milliamperes to greater than several amperes at very low switching frequencies. In addition by using capacitors rather than resistors or transistor devices to drop voltage on the input side, power consumption is reduced. The array of capacitors is switched by simple analog circuitry or a switching logic with or without a processor subsystem and the capacitors themselves are of the super capacitor type, thus providing very high capacitance, and are effectively series connected during certain phases of operation with the input terminal of the conventional linear voltage regulator portion of the apparatus. Energy stored in the super capacitors during the various phases of operation is reused.

15 Claims, 6 Drawing Sheets



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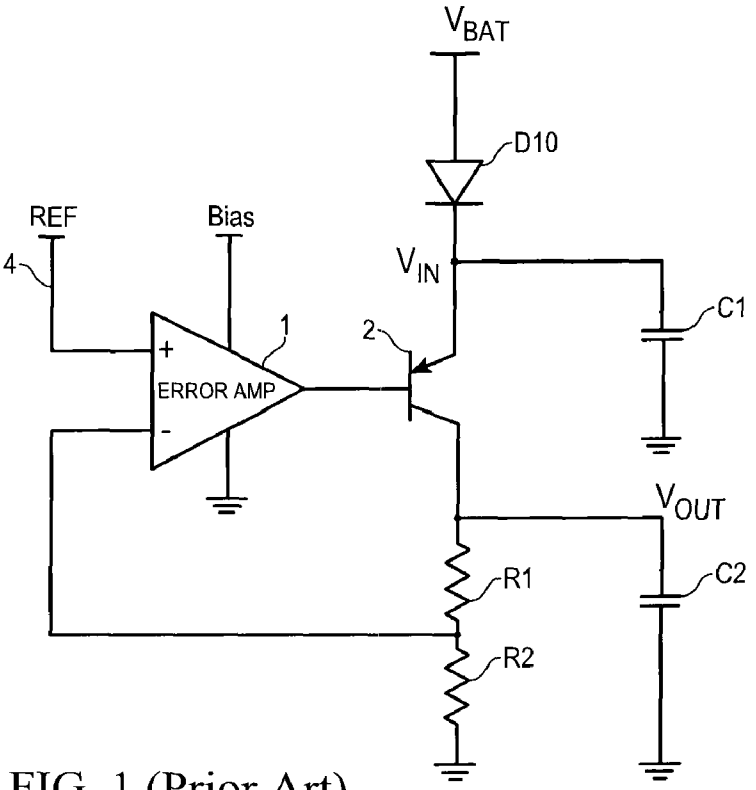


FIG. 1 (Prior Art)

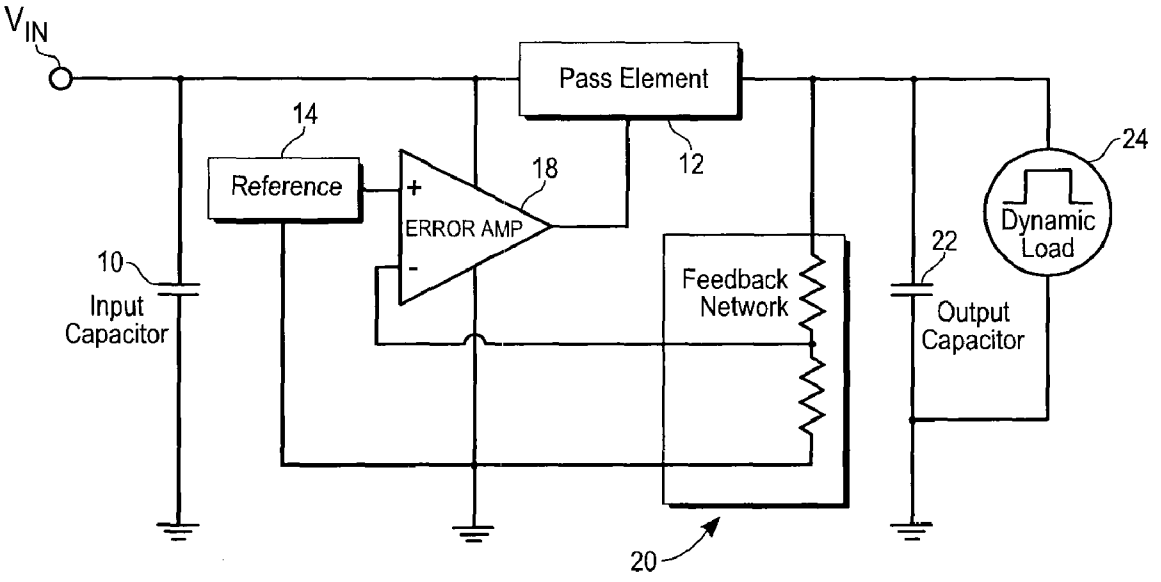


FIG. 2A

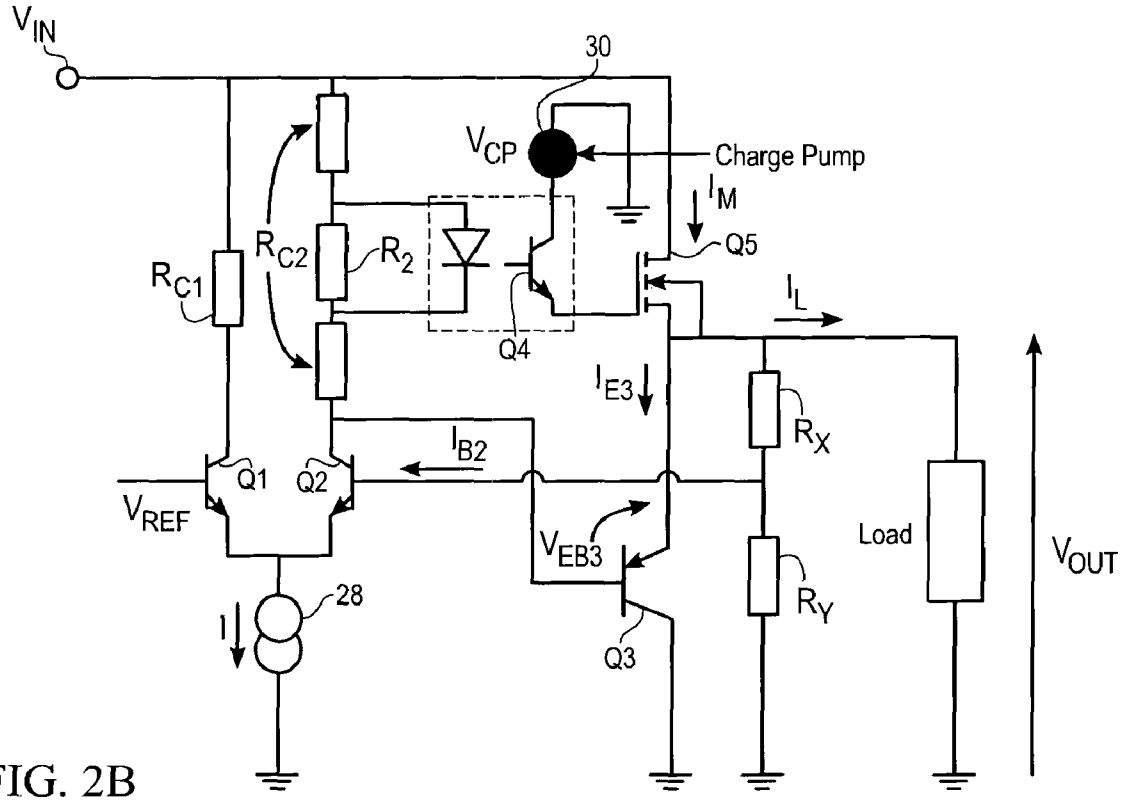

V_{IN}
30
V_{CP}
Charge Pump
I_M
Q5
R_{C2}
R_2
R_{C1}
Q4
I_L
I_{E3}
R_X
I_{B2}
Q1
Q2
V_{REF}
V_{EB3}
Load
V_{OUT}
28
I
Q3
R_Y

FIG. 2B

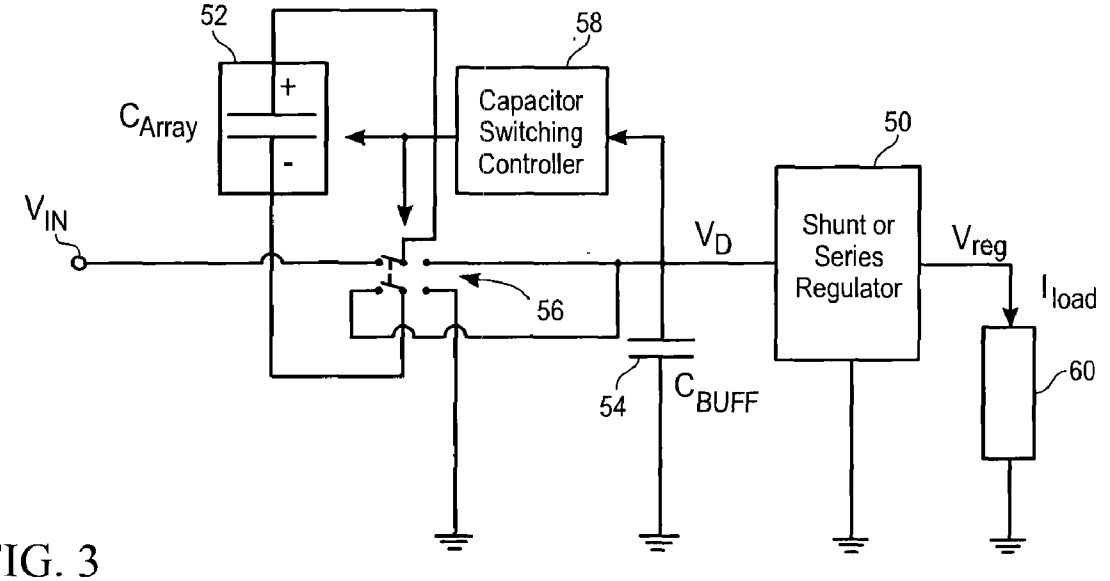

52
58
+
C_{Array}
-
Capacitor
Switching
Controller
50
V_{IN}
V_D
Shunt or
Series
Regulator
V_{reg}
I_{load}
56
60
54
C_{BUFF}

FIG. 3

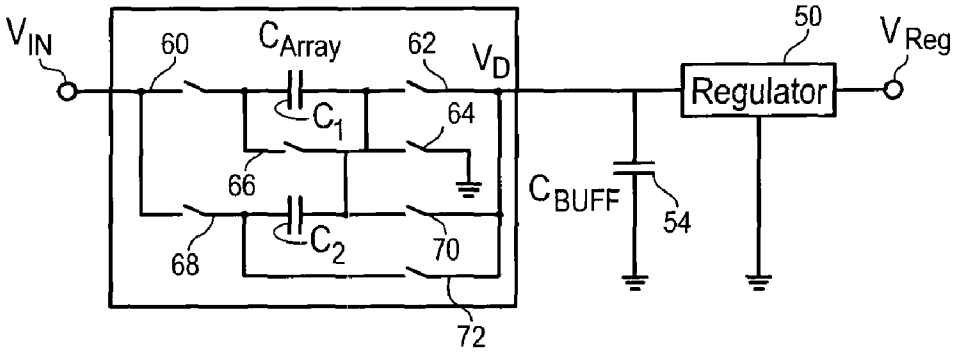


FIG. 4A

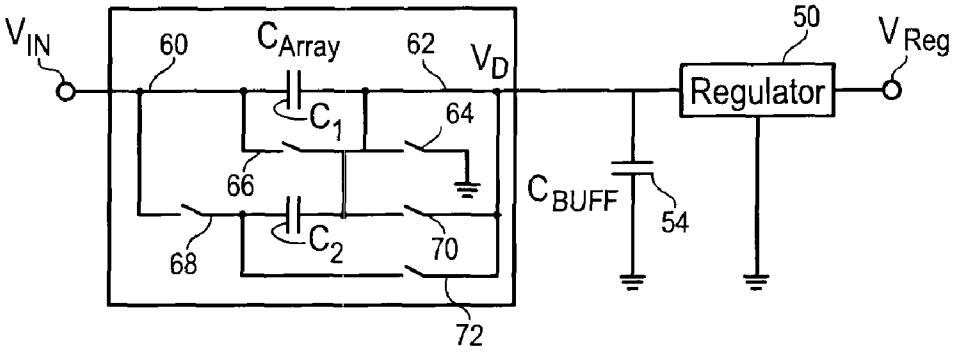


FIG. 4B

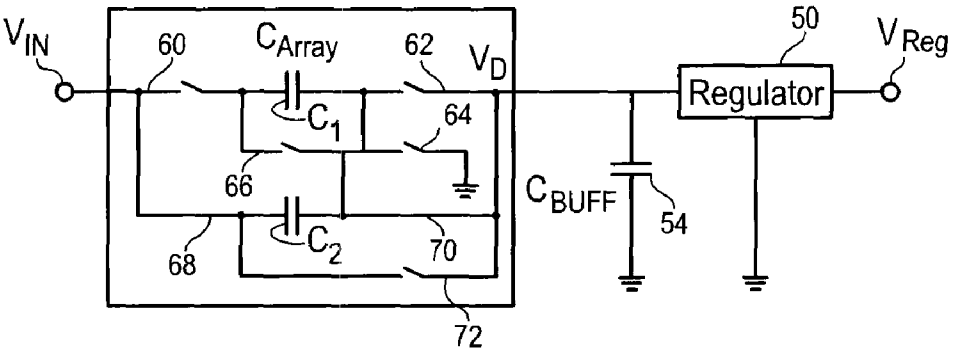


FIG. 4C

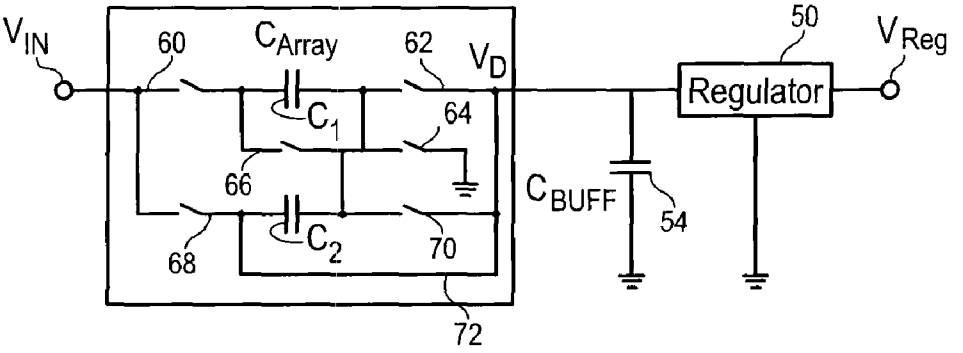


FIG. 4D

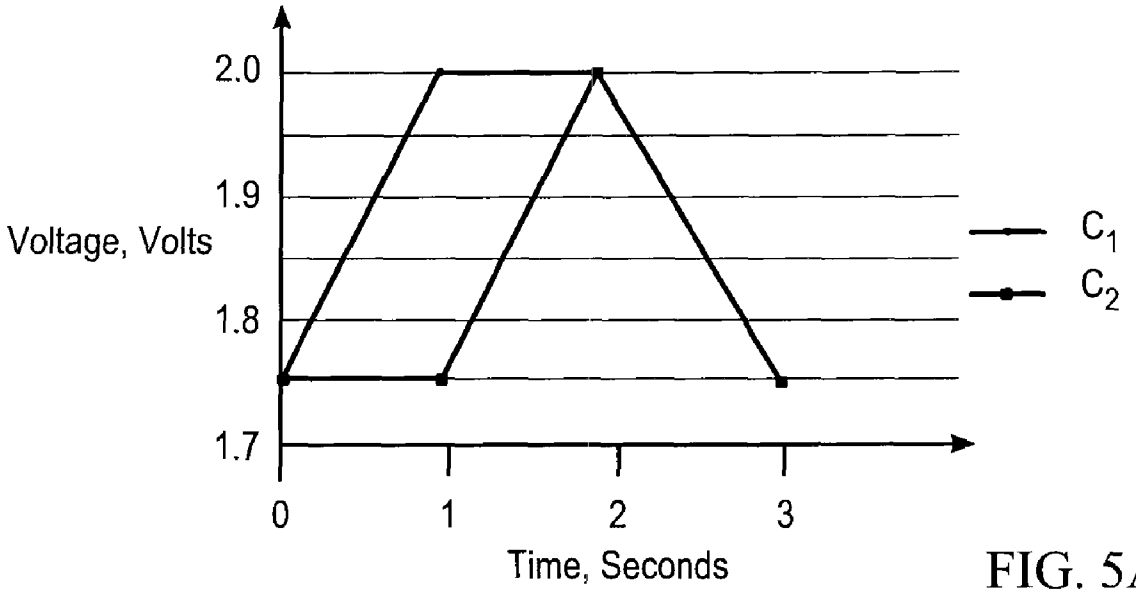

2.0
1.9
1.8
1.7
Voltage, Volts
0
1
2
3
Time, Seconds
C1
C2

FIG. 5A

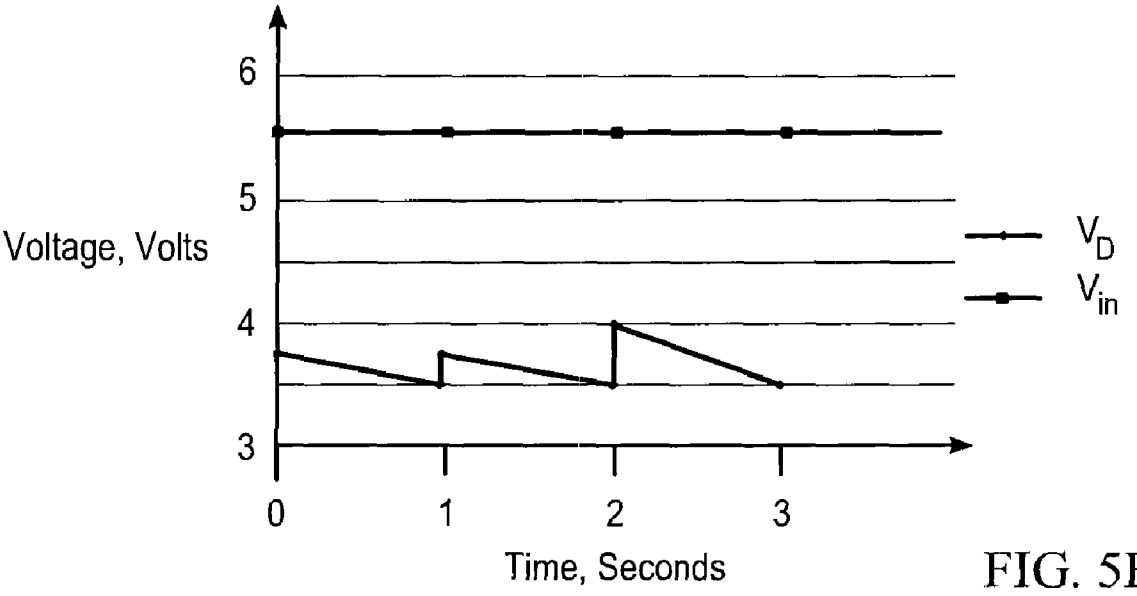

6
5
4
3
Voltage, Volts
0
1
2
3
Time, Seconds
VD
Vin

FIG. 5B

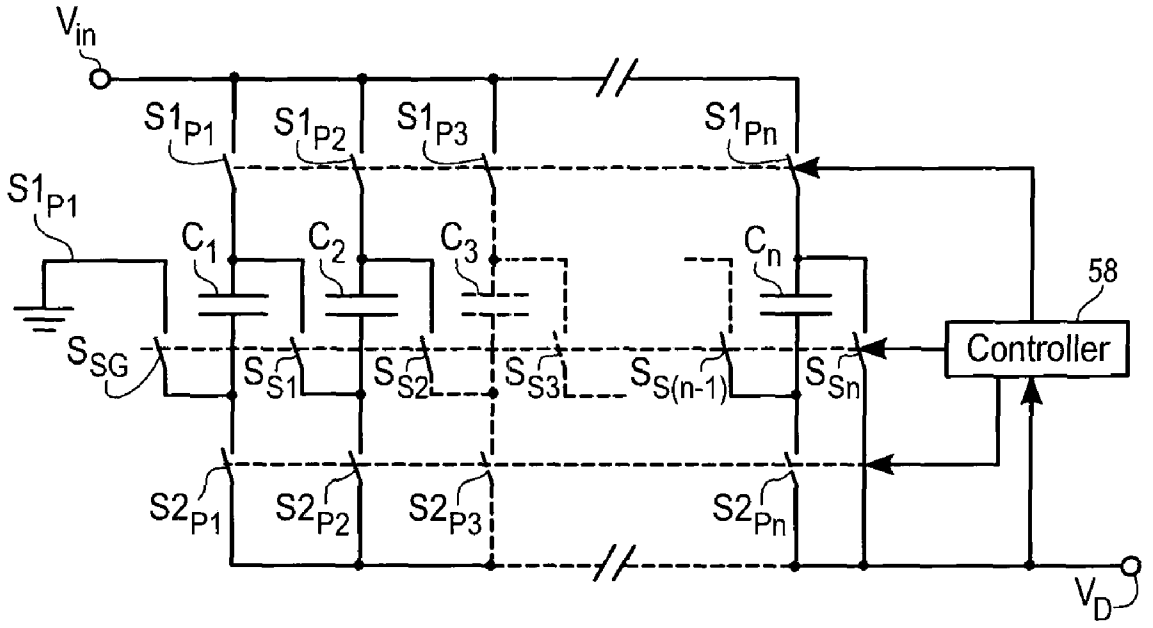

V_{in}
$S1_{P1}$
$S1_{P2}$
$S1_{P3}$
$S1_{Pn}$
$S1_{P1}$
C_1
C_2
C_3
C_n
58
S_{SG}
S_{S1}
S_{S2}
S_{S3}
$S_{S(n-1)}$
S_{Sn}
Controller
$S2_{P1}$
$S2_{P2}$
$S2_{P3}$
$S2_{Pn}$
V_D

FIG. 6A

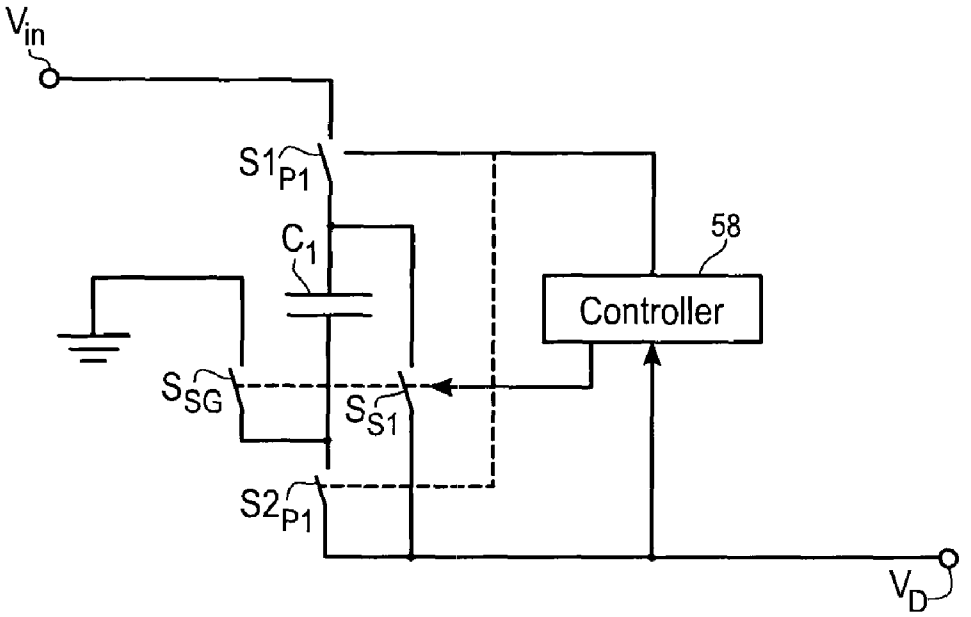

V_{in}
$S1_{P1}$
C_1
58
Controller
S_{SG}
S_{S1}
$S2_{P1}$
V_D

FIG. 6B

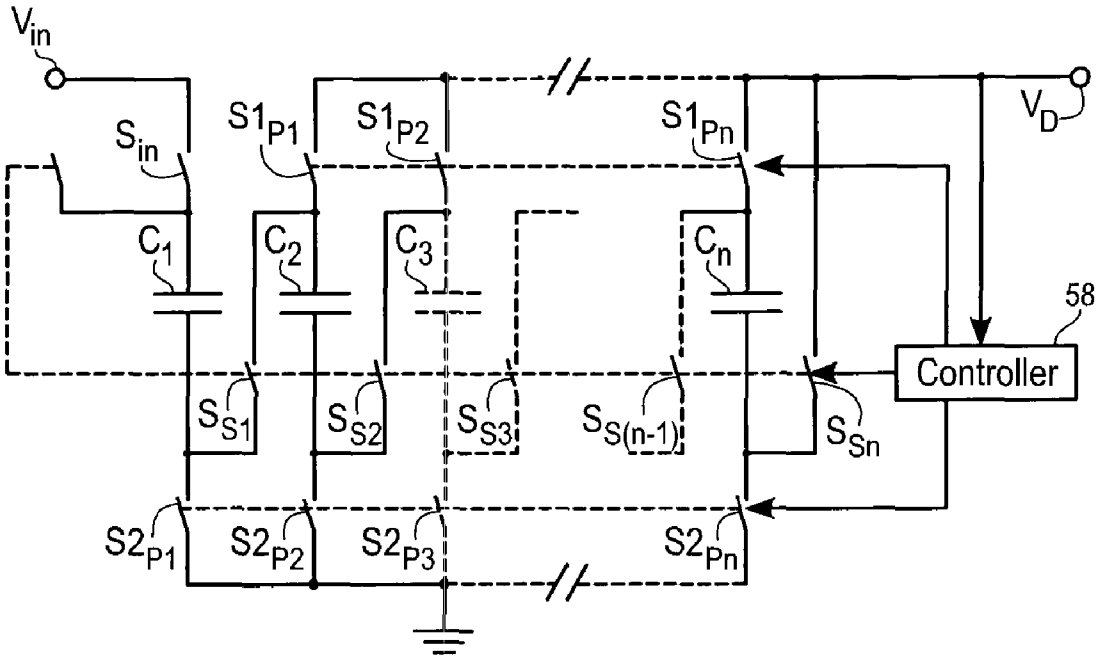

V_{in}
S_{in}
$S1_{P1}$
$S1_{P2}$
$S1_{Pn}$
V_D
C_1
C_2
C_3
C_n
58
Controller
S_{S1}
S_{S2}
S_{S3}
$S_{S(n-1)}$
S_{Sn}
$S2_{P1}$
$S2_{P2}$
$S2_{P3}$
$S2_{Pn}$

FIG. 6C

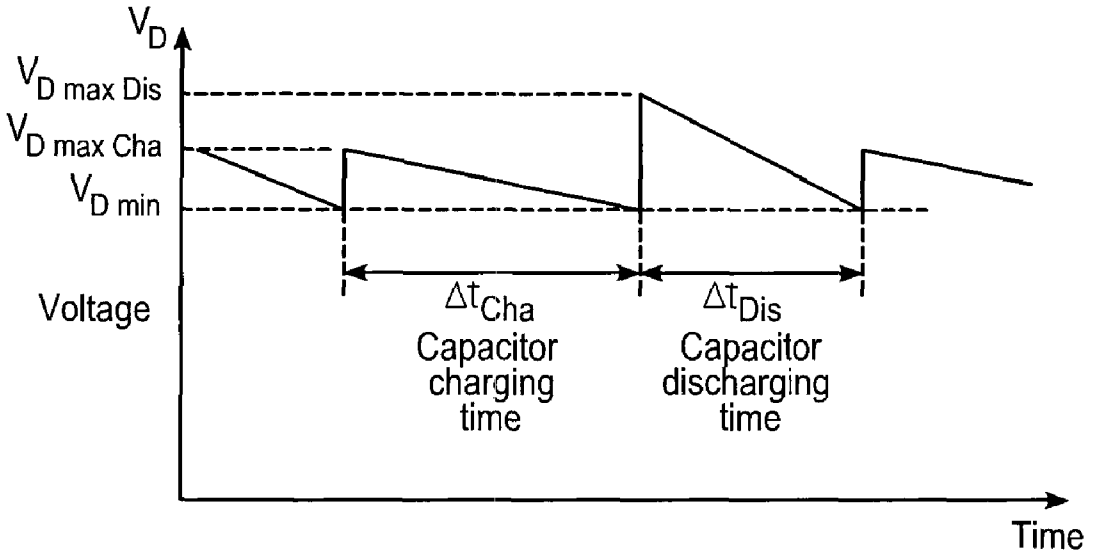

V_D
$V_{D\ max\ Dis}$
$V_{D\ max\ Cha}$
$V_{D\ min}$
Voltage
Δt_{Cha}
Capacitor charging time
Δt_{Dis}
Capacitor discharging time
Time

FIG. 7

HIGH CURRENT VOLTAGE REGULATOR

FIELD OF THE INVENTION

This disclosure relates to voltage regulators (power supplies) used for supplying electric current.

BACKGROUND

Voltage regulators are well-known in the electrical engineering field. They are also referred to as "power supplies" and are electronic or electrical circuits which output electric current at a particular DC (direct current) voltage level. They are widely used in electrical and electronic devices. Typically the actual electricity source is mains current or a battery and these voltage regulators convert and condition the battery output or mains current to a particular voltage level.

All electronic circuits, analog or digital, require such a well-regulated and stabilized DC power supply. An ideal DC power supply provides a constant output voltage irrespective of the value of the load current and the nature of the load while the output is free of noise, ripple and transient dips or surges. In modern electronic systems, DC power requirements vary widely. In small portable electronic devices, DC power supplies carry multiple "rail" voltages and values may vary from ±15 V to sub 1 V levels. Common values of voltage rails (supply) are 48V, 24V, 12V, 9V, 6V, 5 V, 3.3 V, and 1.8 to 3 V. Typical current output capability varies from tens of milliamperes to several amperes.

For larger non-portable devices with processor subsystems, a DC power supply typically has an output voltage from +5 volts to less than 3.3 volts with current requirements of several to 150 amperes. Efficiency of a power supply, particularly in high current systems, is of primary concern to avoid power wastage. A requirement for a portable device of course is also to achieve compactness of the power supply along with efficiency so as to minimize battery drain. Typical DC power supplies are linear, switch mode, and switched capacitor type, although these all have various deficiencies.

FIG. **1** shows a prior art "low drop out" (LDO) linear voltage regulator of FIG. **1** of LoCascio U.S. Pat. No. 4,779,037, incorporated herein by reference in its entirety. This is a low drop out voltage regulator with a switched redundant input. "Low drop out" refers to having a low dropout voltage. Such low dropout voltage regulators are of the type generally referred to as linear voltage regulators. The FIG. **1** device includes error amplifier **1** to compare an input reference voltage applied at terminal **4** to a signal proportional to the output voltage. Error amplifier **1** controls transistor **2** through which output current flows by adjusting transistor **2** so the output voltage at terminal V_{out} equals a fixed multiple of the reference voltage. The source or input voltage, which is typically unregulated, is supplied here from a battery connected at terminal VBAT via a diode D_{10} to the emitter of transistor **2**.

In FIG. **1**, a redundant source voltage V_{in} is also supplied, although this is not always the case with such devices. In this case, the redundant voltage is supplied from capacitor C_1. Capacitor C_2 is provided for filtering at the output terminal V_{out}. Also in this case coupled at the collector of transistor **2** are two series connected resistors R_1 and R_2. Such a voltage regulator is characterized by its "drop out" voltage, which is the lowest source voltage which allows the regulator output voltage to remain substantially constant at some proportion of the reference voltage.

Voltage regulators have several performance parameters. One is noise created by circuit elements in the regulator circuit. High noise levels are undesirable since they may be

RF (radio frequency) signals which interfere with operation of other portions of an electronic device of which the voltage regulator is a part. Most switch mode regulators generate noise at a frequency of 100 kHz to 3 MHz, which is undesirable. Another parameter is the output current capability since it is important for certain applications that the voltage regulator output relatively high levels of current. Typically however, high levels of current require switching regulators rather than low noise linear regulators of the type shown in FIG. **1**. It is a drawback that typically linear regulators are not capable of high amperage (current) output due to excessive heating effects in the series or the shunt transistor elements in the regulator.

Efficiency is also important and refers to the proportion of input power dissipated in the voltage regulator. The approximate efficiency of a typical linear voltage regulator (of the type shown in FIG. **1**) is proportional to V_{out}/V_D, where in FIG. **1** V_D is the supply voltage of the battery VBAT. Often a minimum amount of voltage drop is needed between the supply voltage and output voltage to achieve regulation, hence there is a limit to the highest efficiency possible in a given design. However, use of a series resistor or allowing a larger voltage drop across the transistor to drop the voltage is inefficient since these are inherently power dissipation devices and inefficient. The present inventors have identified that it would be useful to be able to drop part of the difference between the supplied voltage and the regulated output in a non-resistive fashion to improve efficiency. Clearly the lower this effective input voltage to the voltage regulator, the higher its efficiency.

SUMMARY

In accordance with the invention, a linear voltage regulator circuit has its power input terminal series connected to one or more super capacitors. The super capacitors are coupled thereto by an array of switches. The super capacitor array functions as an input voltage dropper in lieu of a resistor or transistor with a large voltage drop as described above. A capacitor in series takes up part of the voltage drop which directly contributes to heat dissipation and it allows the circuit to reuse the energy stored in the capacitor. Once a capacitor is fully charged, it blocks DC current, so series capacitors have not been a practical means of reducing power dissipation of a linear regulator. However, very large capacity capacitors (so-called "super capacitors") are now commercially available which take a longer time to charge and hence allow for a low switching frequency of the capacitors. This has the advantage of charging the super capacitors for a relatively longer time without blocking the DC current path and indirectly reducing high frequency noise generation, due to the low frequency switching of capacitors.

Since even a super capacitor alone and in series when subject to DC voltage charges up eventually and stops conducting, the capacitor alone is not suitable. However by using a switched capacitor array, the capacitors are cyclically charged and discharged to provide a suitable voltage drop with minimal loss. This provides a voltage regulator of the linear type that has high efficiency, low noise generation and outputs high current if needed. In embodiments of the present voltage regulator, the capacitor changeover frequency, which relates to the switching frequency, is only in the range of typically fractional Hz to 300 Hz, about 1/1000 of that of switched mode regulators and which advantageously is not RF. The present regulator in various embodiments delivers currents in excess of 1 ampere, up to 10 amperes or more. Typically such high current draw requirements in the past

required switching voltage regulators, which are inherently noisy, rather than a low noise linear voltage regulator as used here. Furthermore efficiency of the present regulator is about 60-85% and especially high under no-load conditions.

Super capacitors are well-known devices also referred to as electric double-layer capacitors or ultracapacitors. The term "super capacitor" here is intended to include these. Such devices are electrochemical capacitors having an unusually high energy storage density compared to ordinary, for instance, electrolytic capacitors. They store charges thousands of times greater than a physically similar sized electrolytic capacitor. For instance, a typical D-cell sized electrolytic capacitor has a capacitance of only hundreds of microfarads, while the same size super capacitor has a capacitance range of 0.1 farads to several farads, or even up to a few hundreds of farads which is an improvement of about 10,000 times. Commercial double-layer capacitors are available having capacities as high as 5,000 farads.

Unlike traditional capacitors, electric double-layer or super capacitors do not have a conventional dielectric, but instead include a structure that contains an electrical double layer. Hence, the effective thickness of the dielectric is exceedingly thin, which combined with a very large surface area, is responsible for the high capacitances. Each of the two layers by itself is quite conductive, but at the interface where the layers are effectively in contact, no significant current can flow between the layers. However the double layer can typically only withstand a relatively low voltage, so such super capacitors typically have relatively low voltage ratings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows schematically a prior art linear voltage regulator of the low drop out type.

FIGS. **2**A and **2**B show variations of the FIG. **1** device, also in the prior art.

FIG. **3** shows in a combined schematic and block diagram a linear voltage regulator in accordance with the present invention.

FIGS. **4**A-**4**D show operation of the FIG. **3** circuit.

FIGS. **5**A and **5**B show graphically operation of the FIG. **3** circuit.

FIGS. **6**A, **6**B and **6**C show variations of the FIG. **3** regulator.

FIG. **7** shows graphically capacitor switching in accordance with FIG. **6**B.

DETAILED DESCRIPTION

FIGS. **2**A and **2**B show schematically in the prior art variations of the FIG. **1** LDO linear voltage regulator. The FIG. **2**A type is referred to as a series type and is typically found in commercial-type integrated circuit voltage regulators, while FIG. **2**B shows a shunt or parallel type voltage regulator. The FIG. **2**A circuit includes input capacitor **10** coupled to a pass element **12**. The reference voltage terminal **14** and the feedback network **20** are coupled to the error amplifier **18**. On the output side, there is a second (output) capacitor **22** and dynamic load **24** (not shown in FIG. **1**). The FIG. **2**B device includes an error amplifier based on transistors Q**1** and Q**2** and the current source **28**. Resistors RC**1** and RC**2** are part of this error amplifier. A charge pump **30** is connected to a third transistor Q**4** which may be inside an opto-isolator in this shunt regulator configuration. Power transistors Q**3** and Q**5** are connected between the unregulated input, regulated output terminal and ground, with the resistors R_X and R_Y as shown functioning as the feedback network to have closed loop regulation.

FIG. **3** shows schematically in accordance with the invention a low dropout type linear voltage regulator. The main portion of this is the conventional shunt or series LDO linear voltage regulator **50**, which corresponds for instance to the prior art devices of FIGS. **1**, **2**A or **2**B. In this case capacitance C_{Array} **52** is a super capacitor array with associated switches **56** arranged according to the level of the unregulated input voltage applied at terminal Vin as explained below. Capacitor C_{BUFF} **54** may be a super capacitor or any other suitable capacitor which is used to power the LDO for capacitor charging and discharging change-over points. Operation of switches **56** is controlled by conventional capacitor switching controller **58** which is, e.g., logic circuitry, mixed signal circuitry or a suitable microcontroller. The regulated output voltage is at terminal V_{reg}, corresponding to V_{out} in FIG. **1**. The load is shown generally at **60**. The capacitors in the array C_{Array} are switchably connected by switches **56** to the V_D input terminal of regulator **50** so as to take up the larger part of the voltage drop between terminals V_{in} and V_D so that efficiency is improved.

While charging such a series connected super capacitor array, it takes up most of the dropout voltage energy, related to $(V_{in}\text{-}V_D)*I_{load}$, which is stored in the capacitors of the array C_{Array} and the voltage drop is taken over by the capacitors in the array C_{Array}. This is in contrast to a conventional linear regulator where this drop is across a resistive element, such as a transistor or resistor and is responsible for the bulk of the efficiency loss. Thereby efficiency of the present regulator is high and comparable to that of a switching regulator. Using an array of super capacitors C_{Array} and switches **56** to charge up to approximately the voltage level of V_{in}-V_D, the FIG. **3** circuit can operate with ideally no loss, except for whatever internal resistance is present in the super capacitor array C_{Array} and/or the switches **56**, and, any transient related energy losses.

During periods of charging and discharging, the voltage variation across the capacitor array, C_{Array}, is

$$\Delta V_C = \frac{I_L \Delta t}{C},$$

where I_L is the load current and Δt is the charge or discharge time. If the value C is high, which is of course the case with the super capacitors in C_{Array}, then ΔV_C is small during the time of charging and discharging while passing a current through the capacitors to keep the regulator and load working. That is, there are no dropouts. The goal is to keep the effective ΔV_C within the value of V_{Dmax}-V_{Dmin}, where these refer respectively to the maximum and minimum voltages at terminal V_D during the charging or discharging modes.

In this case the super capacitors in the array C_{Array} are switched by switches **56** at relatively low frequencies to minimize noise. The goal is to switch array C_{Array} to obtain the best effective ΔV_C over a full switching cycle, as explained below.

FIGS. **4**A-**4**D illustrates an exemplary capacitor switching cycle for the FIG. **3** apparatus. FIG. **4**A shows key elements of the FIG. **3** circuit with like elements similarly labeled, except that here instead of showing C_{Array} **52** and the switches **56** generally, a more detailed network is shown with two super capacitors C_1 and C_2 and associated switches **60**, **62**, **64**, **66**, **68**, **70** and **72**. In one embodiment these switches are each a

transistor or a solid state relay with sufficient capacity to carry the expected currents at the required voltages. Such transistors are generally referred to as "power transistors" and may be integrated or discrete devices. Possible switch devices are bipolar power transistors, power mosfets, insulated gate bipolar transistors, thyristors, or solid state relays. Any type of semiconductor switch with adequate capacity or even a mechanical relay is usable. In FIG. **4**D, load **60** is not shown, merely for simplicity. FIG. **4**A shows the circuit itself, but not in any operating mode, and is only for purposes of circuit illustration.

FIGS. **4**B-**4**D show the three consecutive operating phases, labeled Phase 1, Phase 2 and Phase 3, through which the circuit cycles on a continuous basis. It is to be understood that each switch in FIG. **4** is conventionally controlled by the capacitor switching controller **58** of FIG. **3**, also omitted here for simplicity. Such control of switches is routine in the power supply field and so no further detail is provided.

In Phase 1 in FIG. **4**B, assume the input voltage V_{in} is 5.5 V, the capacitor array has no internal resistance and the resistance across each switch in its ON state is zero. In Phase 1, capacitor C_1, which is connected by switch **60** to terminal V_{in}, charges from 1.75 V to 2 V. Capacitor C_2 remains at its previous state (since it is disconnected by switches **68** and **70**) at 1.75 V. The voltage at terminal V_D, which is connected by switch **62** to capacitor C_1, increases to 5.5−1.75 volts=3.75 V, then decreases linearly to 5.5−2 V=3.5 V.

In FIG. **4**C which is Phase 2, capacitor C_1 is disconnected at all three of its terminals and capacitor C_2 as shown is series connected between terminals V_{in} and V_D. At this point capacitor C_1 remains at 2 V since it is disconnected, while capacitor C_2 charges from 1.75 V to 2 V. Then V_D increases to 5.5−1.75 V=3.75 V, then decreases linearly to 5.5−2 V=3.5 V. Typically the voltage is cycling only between 3.75 and 3.5 volts in these two phases. In the last Phase 3 shown in FIG. **4**D, both capacitors C_1 and C_2 are disconnected from input terminal V_{in}, but are connected to discharge via switch **72** to terminal V_D. Capacitor C_1 discharges from 2 to 1.75 V and similarly capacitor C_2 discharges from 2 to 1.75 V. Hence the voltage at V_D increases to 4 V and then decreases linearly to 3.5 V. The total voltage swing here is only 3.5-4 V, which is a relatively modest, thereby providing relatively linear voltage. As pointed out above, the typical switching frequency is a fraction of a Hz to 300 Hz, so each phase is approximately a few seconds to 3 milliseconds in duration.

FIGS. **5**A and **5**B show this operation graphically. In FIG. **5**A, the horizontal scale is time (in seconds) and the vertical scale is voltage (in volts). There are two plots, for capacitors C_1 and C_2.

FIG. **5**B shows operation of the regulator at terminals V_D and V_{in} where again the horizontal scale is seconds and the vertical scale volts. The supply voltage at terminal V_{in} is constant, while the voltage at terminal V_D fluctuates within the relatively narrow range of 3.5-4 V.

FIGS. **6**A, **6**B and **6**C show schematically variations of the capacitor array and switches portion of the FIG. **3** circuit, all being embodiments in accordance with this disclosure. For the FIG. **6**A embodiment, the capacitor array $C_1, C_2, \ldots, C_n$ and switches are arranged for an input voltage V_{in} which is expected to be less than twice the capacitor array output voltage at terminal V_D. The switches here are designated $S\mathbf{1}_{p1}, \ldots, S\mathbf{1}_{pn}$ (first row); $S_{s1}, \ldots, S_{sn}$ (second row) and $S\mathbf{2}_{p1}, \ldots, S\mathbf{2}_{pn}$ (third row), and switch S_{SG}. The number of capacitors used here, illustrated as being "n" in number, is a design choice dependent on the value of $V_D/(V_{in}-V_D)$ as explained in more detail below. Hence all the capacitors here are connected in parallel relative to the input terminal V_{in} when charging. All the parallel connected capacitors charge at once, not one by one as in the FIG. **4** embodiment. However for discharge purposes, the switches are set so all the capacitors are coupled in series to terminal V_D.

FIG. **6**B shows a simpler embodiment with only a single capacitor C_1 in the switched capacitor array which is used when the supply voltage at V_{in} is approximately twice the value of the voltage at V_D. The four switches here are designated $S\mathbf{1}_{p1}$, $S\mathbf{2}_{p1}$, S_{s1} and S_{SG}.

FIG. **6**C shows in another embodiment an arrangement of capacitors and switches for the case where the supply voltage at V_{in} is greater than twice that at V_D. Here capacitors C_1, $C_2, \ldots, C_n$ are in series when connected to terminal V_{in}. The switches here are arranged somewhat similar, but not the same, as in FIG. **6**A, again being arranged in three rows (banks). All the capacitors are connected in parallel to discharge to terminal V_D. The number of capacitors n here again depends on the ratio of the voltage at terminal V_{in} to V_D.

In the FIG. **6**C embodiment for high voltage drop$\{(V_{in}-V_D)>V_D\}$ recovery, all the capacitors in the array are connected in series and then that series connected capacitor array is connected between the power source and the input terminal, and then the capacitors are connected in parallel and discharged to the input terminal. For low voltage drop$\{(V_{in}-V_D)<V_D\}$ recovery, all the capacitors in the array are connected in parallel and then that parallel connected capacitor array is connected between the power source and the input terminal, and then the capacitors are connected in series and discharged to the input terminal.

Table 1 indicates relationships for calculating the capacitor values, numbers, and other important technical parameters for design purposes:

TABLE 1

Parameter	$V_{in} < {}_2V_{Dmin}$	$V_{in} > 2V_{Dmin}$
n	$n \geq \frac{V_{Dmin} + \Delta V_D + I(3R_{ON} + r_S)}{V_{in} - V_{Dmin} - I(R_{ON} + r_S)}$	$n \leq \frac{V_{in} - V_{Dmin} - I(3R_{ON} + r_S)}{V_{Dmin}\lvert\Delta V_D \rvert I(R_{ON}\lvert r_S)}$
V_{Cmax}	$V_{in} - V_{Dmin} - \frac{I}{n}(2R_{ON})$	$\frac{I}{n}\{V_{in} - V_{Dmin} - I(n+1)R_{ON}\}$
$V_{Dmax,\,Dis}$	$n(V_{in} - V_{Dmin}) - I((n+3)R_{ON} + (n+1)r_S)$	$\frac{1}{n}[(V_{in} - V_{Dmin}) - I\{(n+3)R_{ON} + (n+1)r_S\}]$
$V_{Dmax,\,Cha}$	$\frac{1}{n}[nV_{in} - V_{Dmin} - I\{(n+3)R_{ON} + (n+1)r_S\}]$	$[V_{in} - nV_{Dmin} - I\{(n+3)R_{ON} + (n+1)r_S\}]$

TABLE 1-continued

Parameter	$V_{in} < 2V_{Dmin}$	$V_{in} > 2V_{Dmin}$
Δt_{Dis}	$\frac{C}{n}\left[\frac{nV_{in} - (n+1)V_{Dmin}}{I} - \{(n+3)R_{ON} + (n+1)r_S\}\right]$	$C\left[\frac{V_{in} - (n+1)V_{Dmin}}{I} - \{(n+3)R_{ON} + (n+1)r_S\}\right]$
Δt_{Cha}	$C\left[\frac{nV_{in} - (n+1)V_{Dmin}}{I} - \{(n+3)R_{ON} + (n+1)r_S\}\right]$	$\frac{C}{n}\left[\frac{V_{in} - (n+1)V_{Dmin}}{I} - \{(n+3)R_{ON} + (n+1)r_S\}\right]$
η_r	$1 + \frac{1}{n}$	$1 + n$

In Table 1:
V_{in} Input voltage to the circuit
ΔV_D Expected minimum voltage fluctuation of V_D
R_{ON} On resistance of the switch
r_S Internal resistance of the capacitors
n Number of capacitors.
V_{Cmax} Maximum voltage across each capacitor
$V_{Dmax,\ Dis}$ Maximum voltage at V_D when discharging
$V_{Dmax,\ Cha}$ Maximum voltage at V_D when charging
Δt_{Dis} Time taken to discharge the capacitors to minimum V_D (V_{Dmin}) from $V_{Dmax,\ Cha}$
Δt_{Cha} Time taken to charge the capacitors from its discharged voltage until V_D reached to V_{Dmin}. When the discharged capacitors start charging V_D goes to $V_{Dmax,\ Cha}$ and gradually decrease till V_{Dmin}
η_r Supercapacitor based efficiency improvement factor, which is the overall efficiency increasing factor of the present technique.

$$\eta_r = \frac{\text{Input power when directly connect the regulator to } V_{in}}{\text{Input power when connect the regulator to } V_{in} \text{ through this technique}}$$

Table 1 thereby shows (for the two indicated voltage regimes) equations to select the number of capacitors (n) in the capacitor array, the voltage rating of each capacitor (V_h Cmax) the parameters for finding the switching frequency (Δt_{Dis}, Δt_{Cha}), the voltage variation limits of the regulator input ($V_{Dmax.Dis}$, $V_{Dmax.Cha}$) and the relative efficiency increase (η_r) due to the present method. The two columns of Table 1 $V_{in}<2V_{Dmin}$ and $V_{in}>2V_{Dmin}$ show the relationship for the switching schemes of FIGS. **6**A and **6**C respectively.

These equations are derived based on these assumptions: the power consumed by the controller circuit is negligible compared with the output power; all the capacitors are identical and have equivalent series resistance of r_s; all the switches are identical and have ON resistance R_{ON}.

FIG. **7** shows (similarly to FIG. **5**B) graphically a waveform of the voltage V_D (for the embodiment of FIG. **6**B) when a capacitor in the present apparatus is charging and discharging. When the output draws current through the capacitor, the voltage across the capacitor increases from its initial voltage until V_D reaches V_{Dmin}. So voltage V_D starts decreasing from $V_{Dmax\ Cha}$ to V_{Dmin}. When voltage V_D reaches voltage V_{Dmin} the capacitor starts powering the regulator. At this instance the voltage V_D goes to value $V_{Dmax\ dis}$ and with the discharging of the capacitor, V_D gradually decreases up to voltage V_{Dmin}.

It has been determined that with the exemplary FIG. **6**B apparatus overall efficiency is about 80%. In the prior art, efficiency is approximately 5⁄12, less than 42%.

A parallel combination (or a diode connection) of the present voltage regulator can be used for very high current operations, or redundancy of a power supply. Thereby, for very high current applications, multiple instances of the present apparatus are coupled in parallel. This arrangement may include single or multiple banks of super capacitors and controllers, for high current or high voltage output requirements.

This disclosure is illustrative and not limiting; further modifications and improvements will be apparent to those skilled in the art in light of this disclosure and are intended to fall within the scope of the appended claims.

The invention claimed is:

1. A voltage regulation apparatus comprising:

a power supply terminal adapted to be coupled to a power source;

a linear voltage regulator circuit having an input terminal;

a switched capacitor element functioning as a voltage dropper and serially coupled between the power supply terminal and the input terminal of the linear voltage regulator, the switched capacitor element including at least one super capacitor having a capacitance of at least 0.1 farad and at least one transistor or solid state relay; and

an output terminal coupled to an output terminal of the linear voltage regulator.

2. The apparatus of claim **1**, wherein the switched capacitor element includes at least two super capacitors each series coupled to at least one switch, the two super capacitors being capable of being serial or parallel coupled by the at least one transistor or solid state relay relative to one another and to the input terminal of the linear voltage regulator.

3. The apparatus of claim **1**, further comprising control logic coupled to operate the switched capacitor element.

4. The apparatus of claim **1**, wherein the linear voltage regulator circuit is of the series or shunt type.

5. The apparatus of claim **1**, wherein the linear voltage regulator circuit is of the low drop out type.

6. The apparatus of claim **1**, wherein in operation the apparatus provides a current of at least one ampere at the output terminal.

7. The apparatus of claim **3**, wherein the control logic operates the apparatus in at least three phases, including:

a first phase where only a first super capacitor in the switched capacitor element is connected;

a second phase where only a second super capacitor in the switched capacitor element is connected; and

a third phase where neither of the first and second super capacitors are connected to the power supply terminal but both are connected to the input terminal of the linear voltage regulator.

8. A method of providing a regulated voltage from a power source using a capacitance coupled to an input terminal of a linear voltage regulator, comprising the acts of:

series coupling a first super capacitor functioning as a voltage dropper and having a capacitance of at least 0.1 farad in the capacitance between the power source and the input terminal;

disconnecting the first super capacitor and series coupling by a transistor or solid state relay a second super capacitor between the power source and the input terminal of the linear voltage regulator; and

disconnecting the second super capacitor from the power source and discharging both super capacitors to the input terminal.

9. The method of claim 8, further comprising the acts of:

series coupling the super capacitors between the power source and the input terminal; and

disconnecting the super capacitors from the power source, connecting the super capacitors in series and discharging the super capacitors from the input terminal.

10. The method of claim 8, further comprising the acts of:

series coupling the super capacitors between the power source and the input terminal; and

disconnecting the super capacitors from the power source, connecting the super capacitors in parallel and discharging the super capacitors to the input terminal.

11. The method of claim 8, wherein the connecting and disconnecting are performed by switches coupled to a control element.

12. The method of claim 8, wherein the linear voltage regulator is of the series or shunt type.

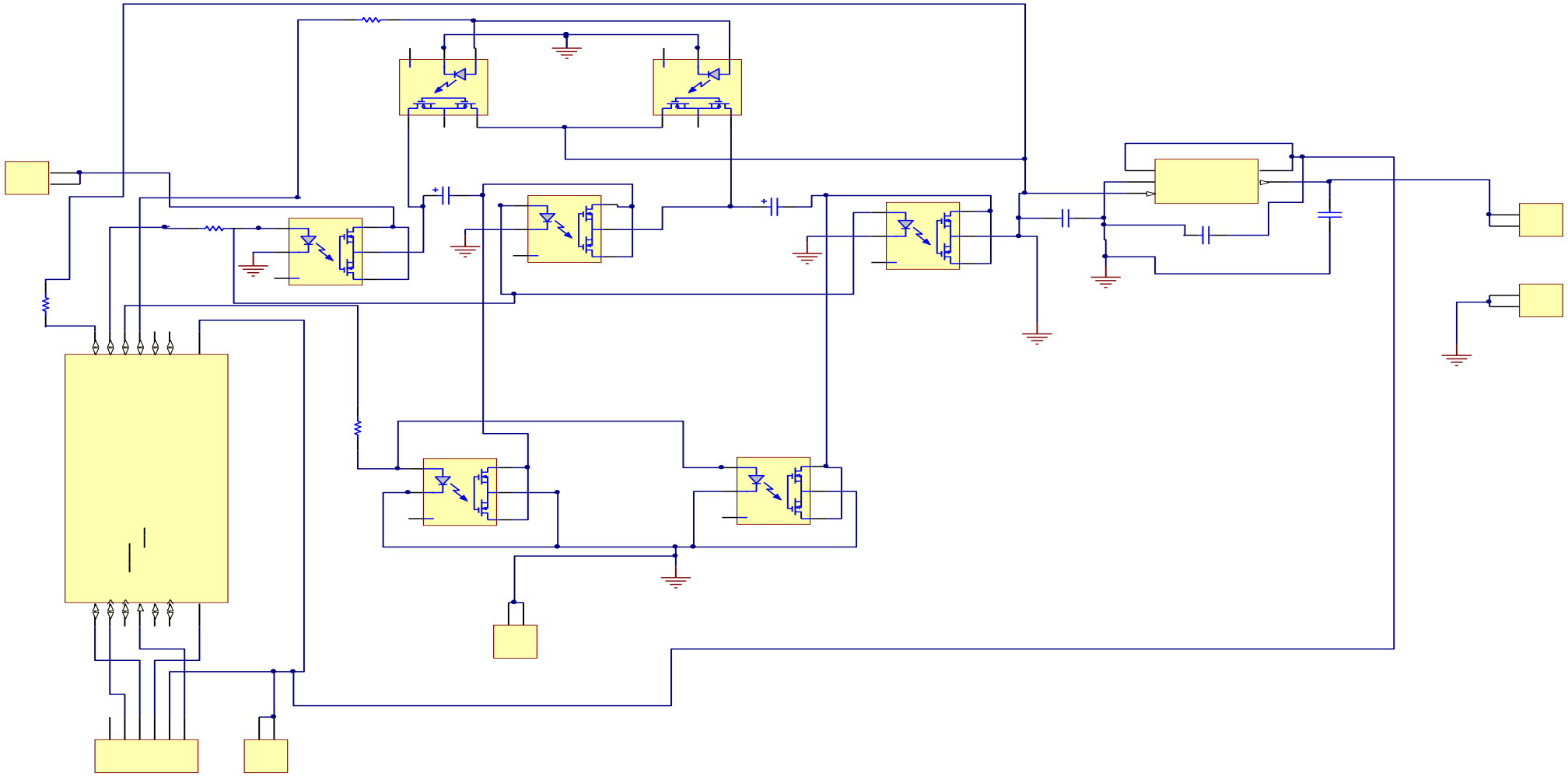
13. The method of claim 8, wherein the linear voltage regulator is of the low drop out type.

14. The method of claim 8, further comprising outputting a current of at least one ampere from the linear voltage regulator.

15. The method of claim 8, wherein a switching rate of the method is less than about 300 Hz.

* * * * *

Appendix B – Prototype Circuit



Appendix C – C Programming of MicroChip PIC16F684-I/P

```
/*
Filename :          SaifulLDO.c
Author   :          Saiful
Date     :          12.02.2011
Description:        C code for 5V to 1.5 V regulator



*/
#include <pic.h>
#include <stdlib.h>



__CONFIG(INTIO & WDTDIS & MCLRDIS & UNPROTECT & PWRTEN & BOREN);


//Defining Macros
#define U4_U5_U6_U7_ON()        {PORTC|=0b00001100;}//RC2 and RC3 on
without affecting state of RC1
#define U4_U5_U6_U7_OFF()       {PORTC&=0B00000010;}    //RC1 and RC2
off without affecting the state of RC1


#define U1_U2_U3_ON()           {PORTC|=0B00000010;}//RC1 on
without affecting the state of RC2 & RC3
#define U1_U2_U3_OFF()          {PORTC&=0B00001100;}    //RC1
off without affecting the state of RC2 & RC3



#define ON  1                                   //Define ON as
digital 1
#define OFF 0                                   //Define OFF as
digital 0
```

```
#define CLEAR 0
        //Define CLEAR as digital 0

#define TIMER1 TMR1ON                                   //Set this bit
start the timer and vice versa.



//Variables


char temp_adc_results;                                  //Used in read_adc
function

char temp;                                                      //Used
to store ADC value generate by the switches


        //temperorly

char unsigned tick;                                             //Variable to
count TIMER1 overflows

char unsigned fault;                                    //Variable that shows
which fault has been occured.



short signed int error_position;            //Variable to hold position error


short unsigned int save_timer1;                 //Used to save the TIMER1
value


short unsigned int current_level;               //Current Level of the elevator


short unsigned int count;                               //Variable to count
number of holes

short unsigned int set_level;                   //Used to hold the set_level
from button press

short signed int drive;                                 //Drive to motor value
from 0 -630
```

```
short unsigned int i;

unsigned char temp;



void delay(void){

int j;

for(j=0;j<450;j++);

}


//Defining funtions


//Function which returns the adc value when called.Remember to set the proper
channel before calling

//this function.

unsigned char read_adc(void)

{

GODONE = 1;                                                    //Set the
GODONE bit

while(GODONE);                                                 //Wait here
until GODONE is reset

temp_adc_results = 0;                                  //Reset temp_adc_results

temp_adc_results = ADRESH;                             //Copy 8 bit ADRESH to
temp_adc_resutls.

return temp_adc_results;                               //Return 8 bit ADC value

}//read_adc



void main()

{
```

```
//Setup PORT A
        TRISA = 0B00111111;                                    //All pins are
input



//Setup PORT C
        TRISC = 0B11110001;                                    //Make RC3 an
OUTPUT pin7 for S1,S2 and S3.

        //Make RC2 an OUTPUT pin8 for Ud1 and Ud2 switches.

        //Make RC1 an OUTPUT pin9 for UP1 and UP2 switches.

        //Make RC0 an INPUT  pin10 for detecting voltage at input of LDO.


//Setup AN4 or RC0 or pin 10 as the only analog pin
        ANSEL  = 0B00010000;                                   //Bit 7=0 AN7

        //Bit 6=0 AN6

        //Bit 5=0 AN5

        //Bit 4=1 AN4 analog enable for RC0 pin to measure

        //Bit 3=0 AN3

        //Bit 2=0 AN2

        //Bit 1=0 AN1,

        //Bit 0=0 AN0,


//Set the main clock at 8 MHz
        IRCF0=1;IRCF1=1;IRCF2=1;
```

```
        CMCON0  = 0X07;                                 //Turn
off voltage Reference Peripheral
        VRCON  = CLEAR;                                 //Turn
off voltage reference Peripheral



//Setup ADC module.

        ADCON0 = 0B00010001;                            //Bit 7=0 Left
justification

        //Bit 6=0 Reference is set to VDD

        //Bit 5=0 Unimplemented

        //Bit 4,3,2=100 AN4 is selected which is RA0

        //Bit 1=0 GODONE=0 Analog conversion has not started as yet

        //Bit 0=1 ADC in enable

        ADCON1 = 0B01010000;                            //Bit 6,5,4 = 101
(Fosc/16)



        //PORTC = 0;



        U4_U5_U6_U7_ON();
        delay();
        delay();
        delay();
```

```
temp = read_adc();

while(temp>40){
temp = read_adc();
}

while(1==1){
        U4_U5_U6_U7_OFF();
        U1_U2_U3_ON()
        delay();
        delay();
        temp = read_adc();
        while(temp>70){
        temp = read_adc();
        }
        U1_U2_U3_OFF();

        U4_U5_U6_U7_ON()
        delay();
        delay();
        delay();
        delay();
        delay();
        delay();
        temp = read_adc();

        while(temp>70){
        temp = read_adc();
        }
```

Appendix D – Photograph of Circuit and test Bench

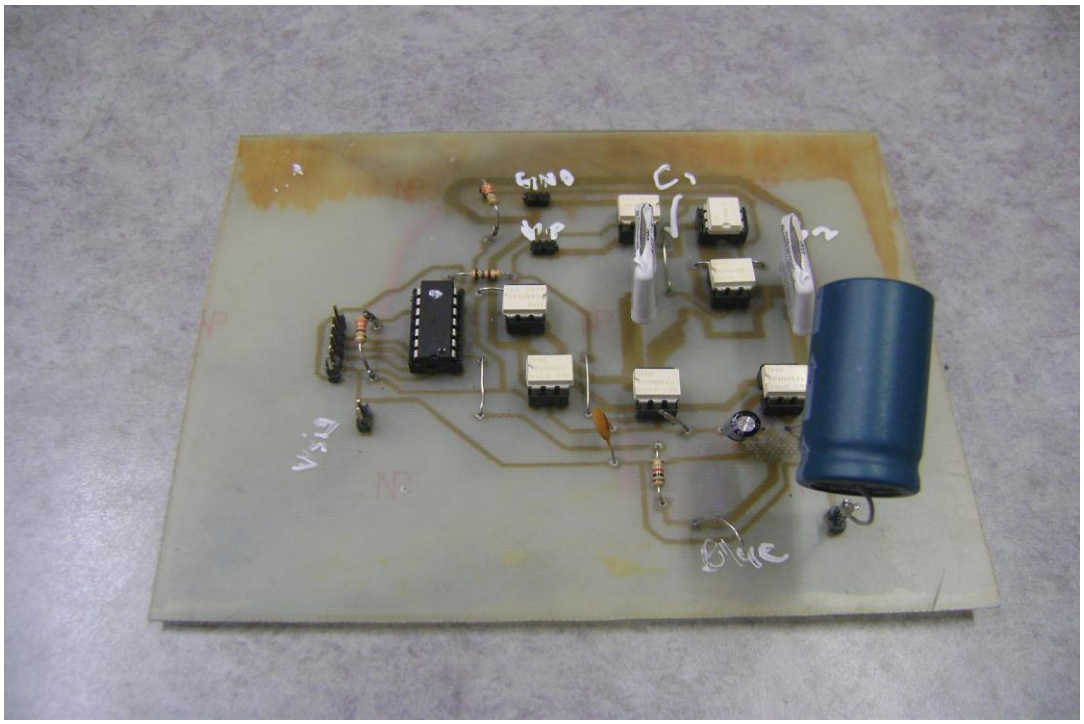


Figure D. 1: Photograph of the prototype circuit

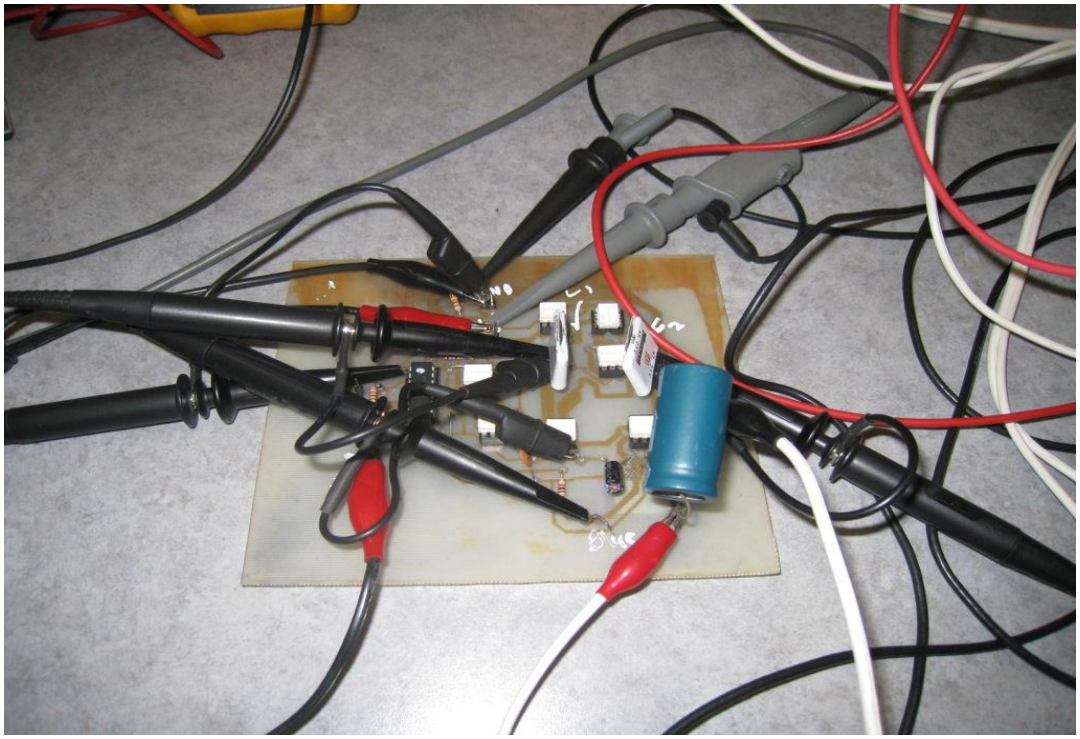


Figure D. 2: Photograph of the circuit during testing

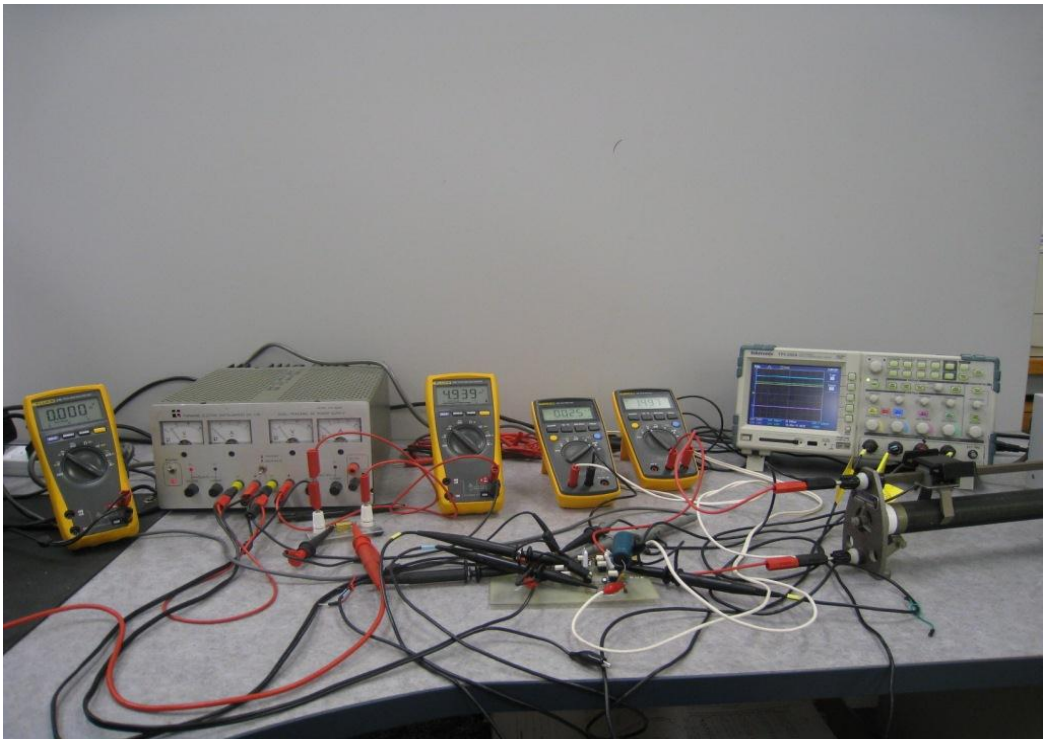


Figure D. 3: Photograph of test bench

Figure D. 4: TEXIO - PXL151A Electronic Load

Appendix 5 – Datasheets

LDO (LP38842 – National Semiconductor)

Solid-state relay (PVN012 – International Rectifier)

Supercapacitor (4F 2.5V – Maxwell Technologies)

September 2006

National Semiconductor

LP38842
1.5A Ultra Low Dropout Linear Regulators
Stable with Ceramic Output Capacitors

General Description

The LP38842 is a high current, fast response regulator which can maintain output voltage regulation with minimum input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: Vbias provides voltage to drive the gate of the N-MOS power transistor, while Vin is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low Vin voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of these devices makes them suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The parts are available in TO-220 and TO-263 packages.

Dropout Voltage: 115 mV (typ) @ 1.5A load current.

Quiescent Current: 30 mA (typ) at full load.

Shutdown Current: 30 nA (typ) when $\overline{S/D}$ pin is low.

Precision Output Voltage: 1.5% room temperature accuracy.

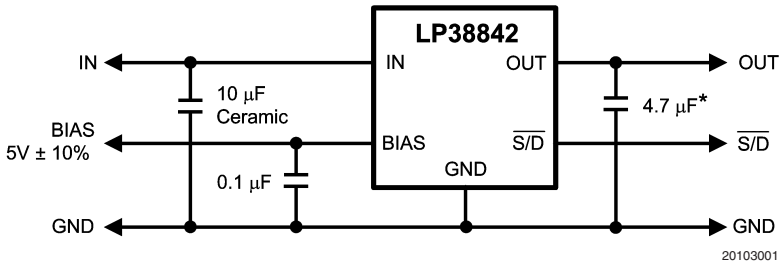
Features

- Ideal for conversion from 1.8V or 1.5V inputs
- Designed for use with low ESR ceramic capacitors
- 0.8V, 1.2V and 1.5V standard voltages available
- Ultra low dropout voltage (115mV @ 1.5A typ)
- 1.5% initial output accuracy
- Load regulation of 0.1%/A (typical)
- 30nA quiescent current in shutdown (typical)
- Low ground pin current at all loads
- Over temperature/over current protection
- Available in 5 lead TO220 and TO263 packages
- –40˚C to +125˚C junction temperature range

Applications

- ASIC Power Supplies In:
  - Desktops, Notebooks, and Graphics Cards, Servers
  - Gaming Set Top Boxes, Printers and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulator

Typical Application Circuit



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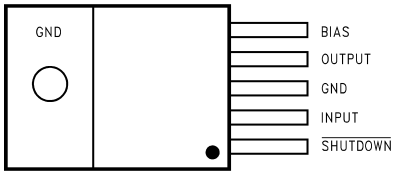
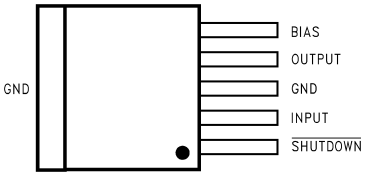
* Minimum value required if Tantalum capacitor is used (see Application Hints).

Connection Diagrams



TO-220, Top View



TO-263, Top View

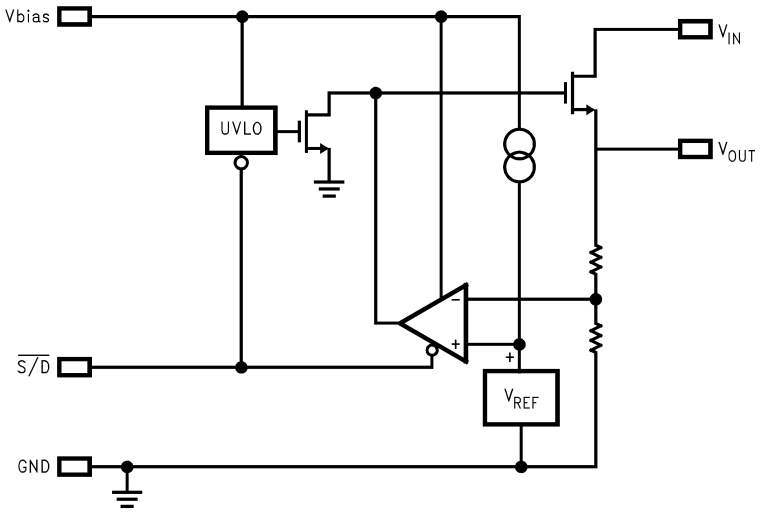
Pin Descriptions

Pin Name	Description
BIAS	The bias pin is used to provide the low current bias voltage to the chip which operates the internal circuitry and provides drive voltage for the N-FET.
OUTPUT	The regulated output voltage is connected to this pin.
GND	This is both the power and analog ground for the IC. Note that both pin three and the tab of the TO-220 and TO-263 packages are at ground potential. Pin three and the tab should be tied together using the PC board copper trace material and connected to circuit ground.
INPUT	The high current input voltage which is regulated down to the nominal output voltage must be connected to this pin. Because the bias voltage to operate the chip is provided seperately, the input voltage can be as low as a few hundered millivolts above the output voltage.
SHUTDOWN	This provides a low power shutdown function which turns the regulated output OFF. Tie to V_{BIAS} if this function is not used.

Ordering Information

Order Number	Package Type	Package Drawing	Supplied As
LP38842S-0.8	TO263-5	TS5B	Rail
LP38842SX-0.8	TO263-5	TS5B	Tape and Reel
LP38842T-0.8	TO220-5	T05A	Rail
LP38842T-0.8 LB03	TO220-5	T05D	Rail
LP38842S-1.2	TO263-5	TS5B	Rail
LP38842SX-1.2	TO263-5	TS5B	Tape and Reel
LP38842T-1.2	TO220-5	T05A	Rail
LP38842T-1.2 LB03	TO220-5	T05D	Rail
LP38842S-1.5	TO263-5	TS5B	Rail
LP38842SX-1.5	TO263-5	TS5B	Tape and Reel
LP38842T-1.5	TO220-5	T05A	Rail
LP38842T-1.5 LB03	TO220-5	T05D	Rail

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65˚C to +150˚C
Lead Temp. (Soldering, 5 seconds)	260˚C
ESD Rating	
Human Body Model (Note 3)	2 kV
Machine Model (Note 9)	200V
Power Dissipation (Note 2)	Internally Limited
V_{IN} Supply Voltage (Survival)	−0.3V to +6V
V_{BIAS} Supply Voltage (Survival)	−0.3V to +7V
Shutdown Input Voltage (Survival)	−0.3V to +7V
I_{OUT} (Survival)	Internally Limited
Output Voltage (Survival)	−0.3V to +6V
Junction Temperature	−40˚C to +150˚C

Operating Ratings

V_{IN} Supply Voltage	$(V_{OUT} + V_{DO})$ to 5.5V
Shutdown Input Voltage	0 to +5.5V
I_{OUT}	1.5A
Operating Junction Temperature Range	−40˚C to +125˚C
V_{BIAS} Supply Voltage	4.5V to 5.5V
V_{OUT}	0.8V to 1.5V

Electrical Characteristics

Limits in standard typeface are for T_J = 25˚C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, V_{BIAS} = 4.5V, I_L = 10 mA, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, C_{BIAS} = 1 µF CER, $V_{\overline{S/D}} = V_{BIAS}$. Min/Max limits are guaranteed through testing, statistical correlation, or design.

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V_O	Output Voltage Tolerance	10 mA < I_L < 1.5A $V_O(NOM) + 1V \le V_{IN} \le 5.5V$ $4.5V \le V_{BIAS} \le 5.5V$	0.788 **0.776**	0.8	0.812 **0.824**	V
			1.182 **1.164**	1.2	1.218 **1.236**	
			1.478 **1.455**	1.5	1.523 **1.545**	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation (Note 6)	$V_O(NOM) + 1V \le V_{IN} \le 5.5V$		0.01		%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation (Note 7)	10 mA < I_L < 1.5A		0.1	0.4 **1.1**	%/A
V_{DO}	Dropout Voltage (Note 8)	I_L = 1.5A		115	175 **315**	mV
$I_Q(V_{IN})$	Quiescent Current Drawn from V_{IN} Supply	10 mA < I_L < 1.5A		30	35 **40**	mA
		$V_{\overline{S/D}} \le 0.3V$		0.06	1 **30**	µA
$I_Q(V_{BIAS})$	Quiescent Current Drawn from V_{BIAS} Supply	10 mA < I_L < 1.5A		2	4 **6**	mA
		$V_{\overline{S/D}} \le 0.3V$		0.03	1 **30**	µA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V		4		A
Shutdown Input						
V_{SDT}	Output Turn-off Threshold	Output = ON		0.7	**1.3**	V
		Output = OFF	**0.3**	0.7		
Td (OFF)	Turn-OFF Delay	R_{LOAD} X C_{OUT} << Td (OFF)		20		µs
Td (ON)	Turn-ON Delay	R_{LOAD} X C_{OUT} << Td (ON)		15		
$I_{\overline{S/D}}$	$\overline{S/D}$ Input Current	$V_{\overline{S/D}}$ =1.3V		1		µA
		$V_{\overline{S/D}} \le 0.3V$		−1		
θ_{J-A}	Junction to Ambient Thermal Resistance	TO-220, No Heatsink		65		˚C/W
		TO-263, 1 sq.in Copper		35		

Electrical Characteristics Limits in standard typeface are for T_J = 25˚C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, V_{BIAS} = 4.5V, I_L = 10 mA, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, C_{BIAS} = 1 µF CER, $V_{\overline{S/D}} = V_{BIAS}$. Min/Max limits are guaranteed through testing, statistical correlation, or design. (Continued)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
AC Parameters						
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	$V_{IN} = V_{OUT}$ +1V, f = 120 Hz		80		dB
		$V_{IN} = V_{OUT}$ + 1V, f = 1 kHz		65		
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	$V_{BIAS} = V_{OUT}$ + 3V, f = 120 Hz		58		
		$V_{BIAS} = V_{OUT}$ + 3V, f = 1 kHz		58		
e_n	Output Noise Density	f = 120 Hz		1		µV/root–Hz
	Output Noise Voltage V_{OUT} = 1.5V	BW = 10 Hz – 100 kHz		150		µV (rms)
		BW = 300 Hz – 300 kHz		90		

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink thermal values. θ_{J-A} for TO-220 devices is 65˚C/W if no heatsink is used. If the TO-220 device is attached to a heatsink, a θ_{J-S} value of 4˚C/W can be assumed. θ_{J-A} for TO-263 devices is approximately 35˚C/W if soldered down to a copper plane which is at least 1 square inches in area. If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin.

Note 4: Typical numbers represent the most likely parametric norm for 25˚C operation.

Note 5: If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.

Note 6: Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.

Note 7: Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.

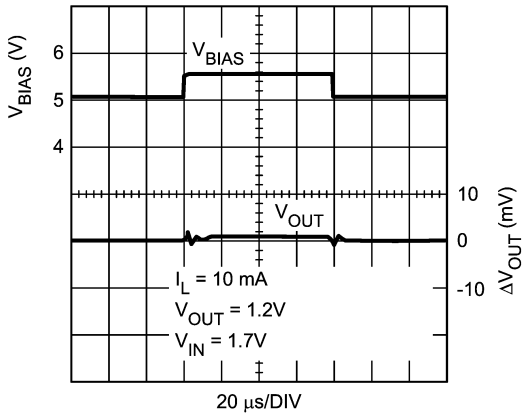
Note 8: Dropout voltage is defined as the minimum input to output differential required to maintain the output with 2% of nominal value.

Note 9: The machine model is a 220 pF capacitor discharged directly into each pin.

Typical Performance Characteristics

Unless otherwise specified: T_J = 25˚C, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, C_{BIAS} = 1 µF CER, $\overline{S/D}$ Pin is tied to V_{BIAS}, V_{OUT} = 1.2V, I_L = 10mA, V_{BIAS} = 5V, V_{IN} = V_{OUT} + 1V.

V_{BIAS} Transient Response



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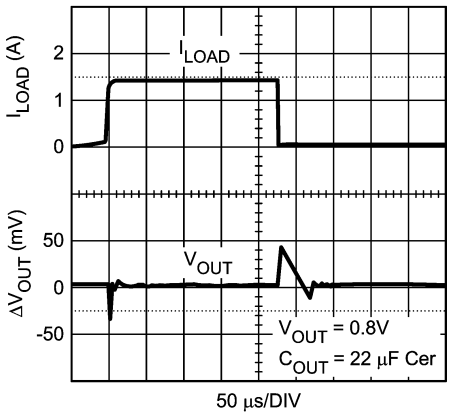
Load Transient Response



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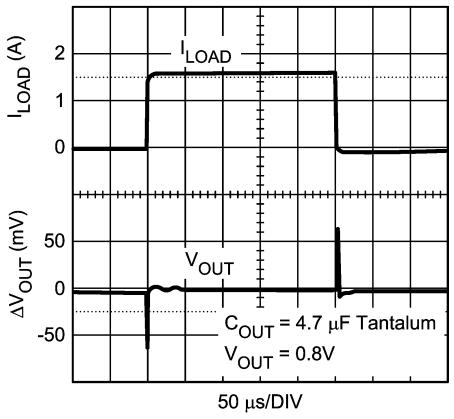
Load Transient Response



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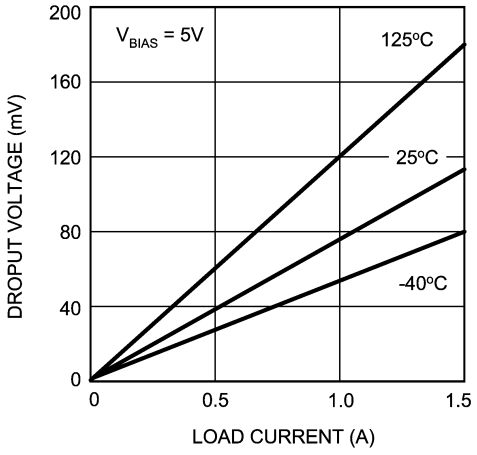
Dropout Voltage Over Temperature



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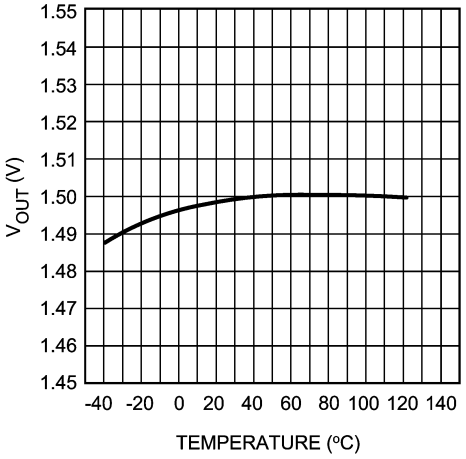
V_{OUT} vs Temperature



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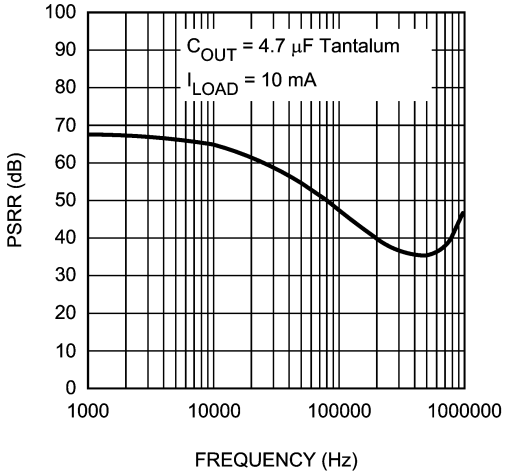
V_{BIAS} PSRR



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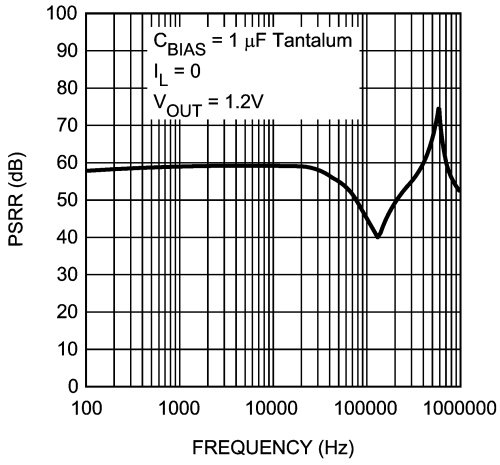
Typical Performance Characteristics

Unless otherwise specified: T_J = 25˚C, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, C_{BIAS} = 1 µF CER, $\overline{S/D}$ Pin is tied to V_{BIAS}, V_{OUT} = 1.2V, I_L = 10mA, V_{BIAS} = 5V, V_{IN} = V_{OUT} + 1V. (Continued)

V_{BIAS} PSRR



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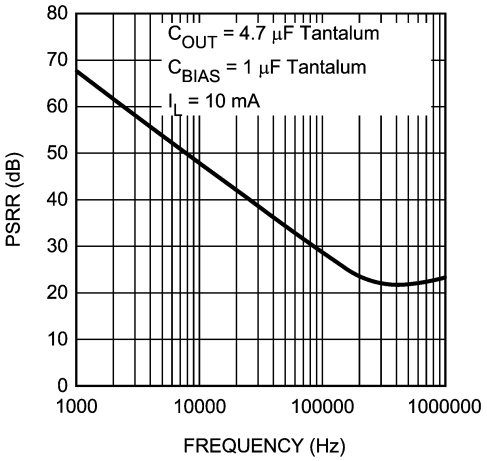
V_{IN} PSRR



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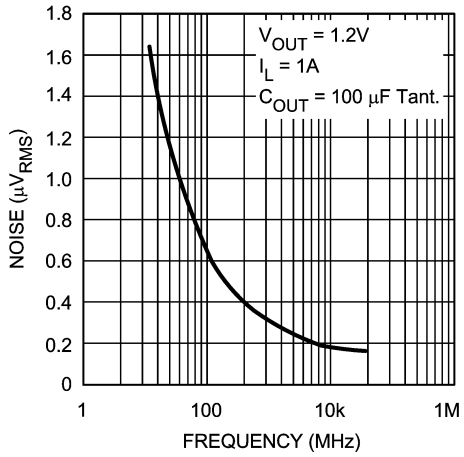
Output Noise Voltage



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Application Hints

EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the Typical Application Circuit.

OUTPUT CAPACITOR

An output capacitor is required on the LP3884X devices for loop stability. The minimum value of capacitance necessary depends on type of capacitor: if a solid Tantalum capacitor is used, the part is stable with capacitor values as low as 4.7µF. If a ceramic capacitor is used, a minimum of 22 µF of capacitance must be used (capacitance may be increased without limit). The reason a larger ceramic capacitor is required is that the output capacitor sets a pole which limits the loop bandwidth. The Tantalum capacitor has a higher ESR than the ceramic which provides more phase margin to the loop, thereby allowing the use of a smaller output capacitor because adequate phase margin can be maintained out to a higher crossover frequency. The tantalum capacitor will typically also provide faster settling time on the output after a fast changing load transient occurs, but the ceramic capacitor is superior for bypassing high frequency noise.

The output capacitor must be located less than one centimeter from the output pin and returned to a clean analog ground. Care must be taken in choosing the output capacitor to ensure that sufficient capacitance is provided over the full operating temperature range. If ceramics are selected, only X7R or X5R types may be used because Z5U and Y5F types suffer severe loss of capacitance with temperature and applied voltage and may only provide 20% of their rated capacitance in operation.

INPUT CAPACITOR

The input capacitor is also critical to loop stability because it provides a low source impedance for the regulator. The minimum required input capacitance is 10 µF ceramic (Tantalum not recommended). The value of C_{IN} may be increased without limit. As stated above, X5R or X7R must be used to ensure sufficient capacitance is provided. The input capacitor must be located less than one centimeter from the input pin and returned to a clean analog ground.

BIAS CAPACITOR

The 0.1µF capacitor on the bias line can be any good quality capacitor (ceramic is recommended).

BIAS VOLTAGE

The bias voltage is an external voltage rail required to get gate drive for the N-FET pass transistor. Bias voltage must be in the range of 4.5 - 5.5V to assure proper operation of the part.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the regulator output from turning on if the bias voltage is below approximately 4V.

SHUTDOWN OPERATION

Pulling down the shutdown ($\overline{S/D}$) pin will turn-off the regulator. Pin $\overline{S/D}$ must be actively terminated through a pull-up resistor (10 kΩ to 100 kΩ) for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to V_{BIAS} if not used.

POWER DISSIPATION/HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$P_D = (V_{IN}–V_{OUT})I_{OUT}+ (V_{IN})I_{GND}$

where I_{GND} is the operating ground current of the device.

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$T_{Rmax} = T_{Jmax}– T_{Amax}$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$\theta_{JA} = T_{Rmax} / P_D$

These parts are available in TO-220 and TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is ≥ 60 ˚C/W for TO-220 package and ≥ 60 ˚C/W for TO-263 package no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required.

HEATSINKING TO-220 PACKAGE

The thermal resistance of a TO220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for TO263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$\theta_{HA} \leq \theta_{JA} – \theta_{CH} – \theta_{JC}$.

In this equation, θ_{CH} is the thermal resistance from the case to the surface of the heat sink and θ_{JC} is the thermal resistance from the junction to the surface of the case. θ_{JC} is about 3˚C/W for a TO220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5˚C/W to 2.5˚C/W. If the exact value is unknown, 2˚C/W can be assumed.

HEATSINKING TO-263 PACKAGE

The TO-263 package uses the copper plane on the PCB as a heatsink. The tab of this package is soldered to the copper plane for heat sinking. The graph below shows a curve for the θ_{JA} of TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

Application Hints (Continued)

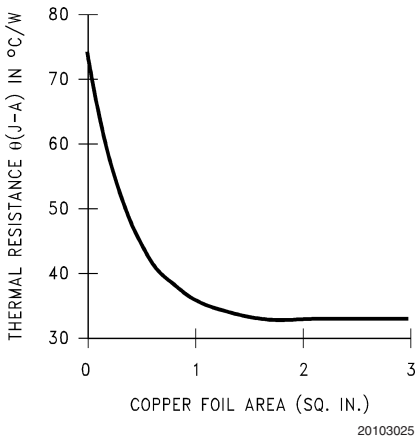


FIGURE 1. θ_{JA} vs Copper (1 Ounce) Area for TO-263 package

As shown in the graph below, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the TO-263 package mounted to a PCB is 32˚C/W.

Figure 2 shows the maximum allowable power dissipation for TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35˚C/W and the maximum junction temperature is 125˚C.

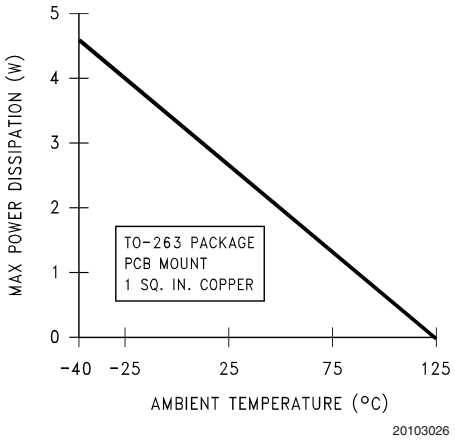
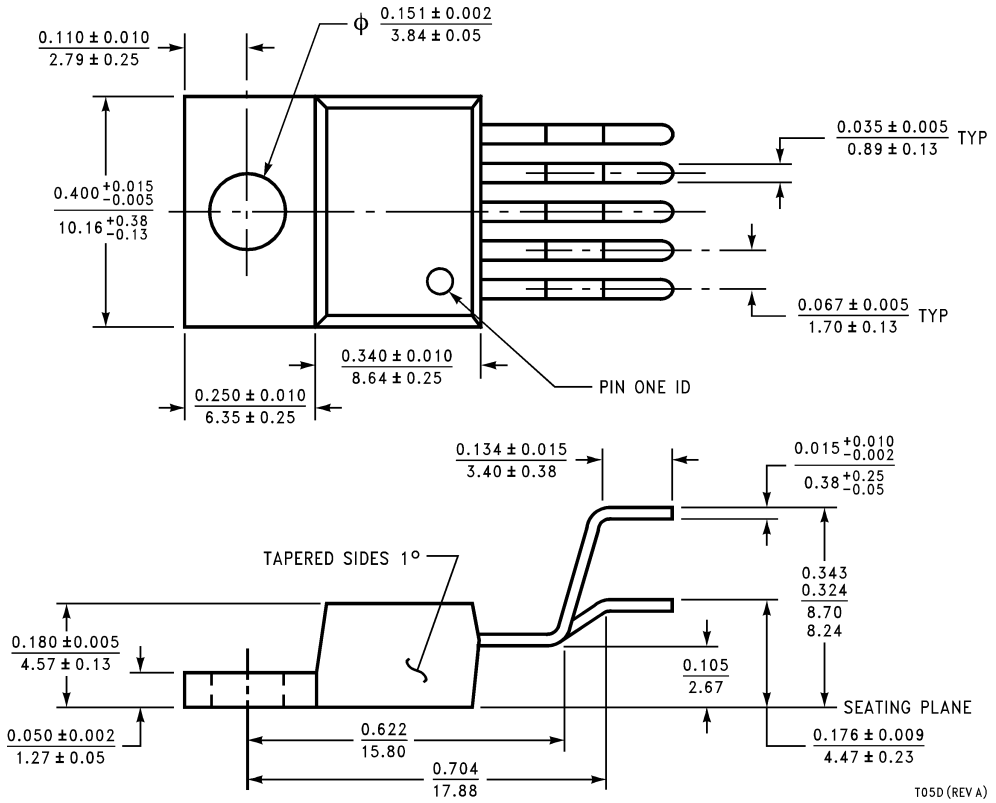
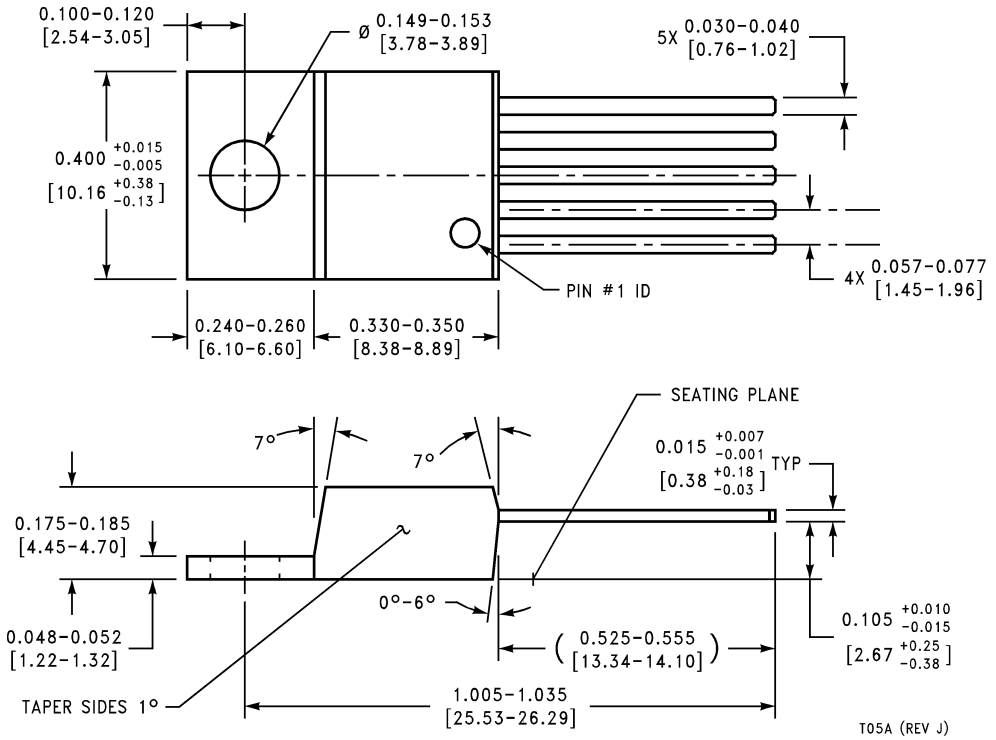


FIGURE 2. Maximum power dissipation vs ambient temperature for TO-263 package

Physical Dimensions inches (millimeters) unless otherwise noted

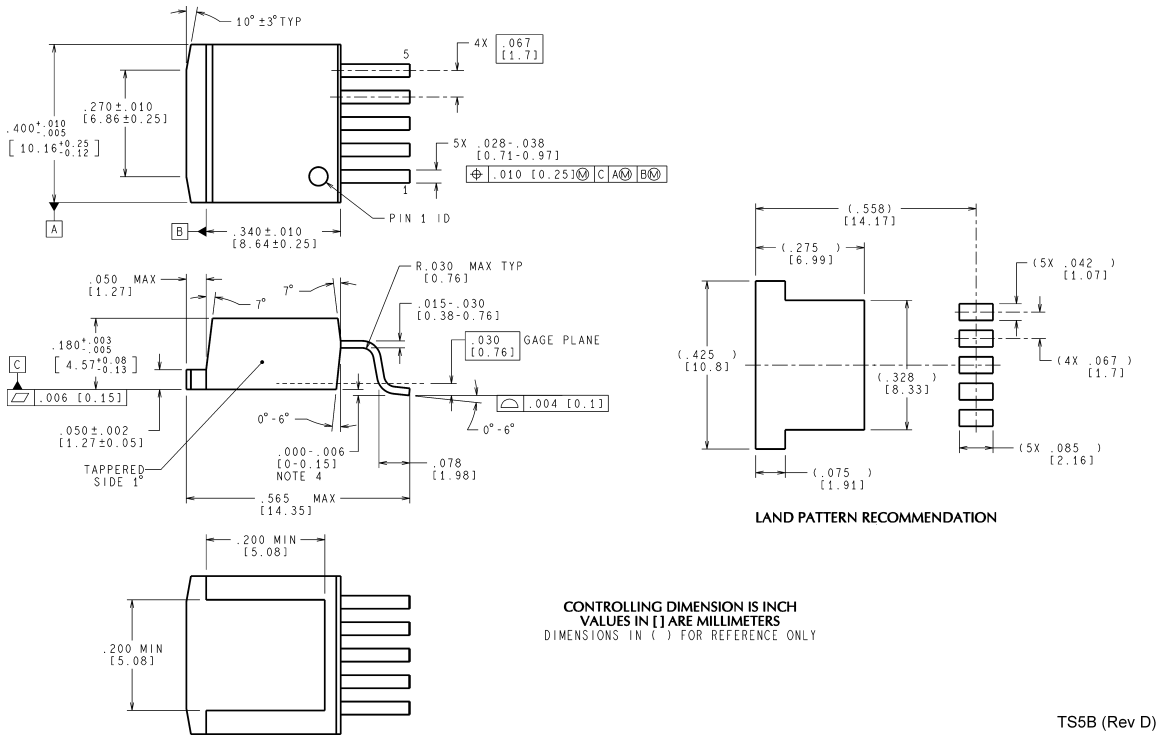


TO220 5-lead, Molded, Stagger Bend Package (TO220-5)
NS Package Number T05D



TO220 5-lead, Molded, Straight Lead Package (TO220-5)
NS Package Number T05A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



TS5B (Rev D)

TO263 5-Lead, Molded, Surface Mount Package (TO263-5)
NS Package Number TS5B

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International
IOR Rectifier

Data Sheet No. PD 10034 revK

Series PVN012PbF

Microelectronic Power IC

HEXFET® Power MOSFET Photovoltaic Relay

Single Pole, Normally Open, 0-20V, 2.5A AC/ 4.5A DC

General Description

The PVN012 Series Photovoltaic Relay at 100 milliohms features the lowest possible on-state resistance in a miniature package — lower than a comparable reed relay.

The PVN012 is a single-pole, normally open solid-state relay. It utilizes a GenerationV HEXFET output switch, driven by an integrated circuit photovoltaic generator of novel construction. The output switch is controlled by radiation from a GaAlAs light emitting diode (LED) which is optically isolated from the photovoltaic generator.

These units exceed the performance capabilities of electromechanical relays in life, sensitivity, stable on-resistance, miniaturization, magnetic insensitivity and ruggedness. They are ideally suited for switching high currents or low level signals without distortion or injection of electrical noise.

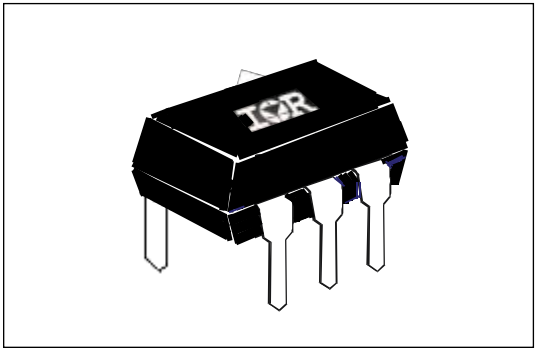
Series PVN012 Relays are packaged in a 6-lead molded DIP package with either thru-hole or surface mount (gull-wing) terminals. They are available in standard plastic shipping tubes or on tape-and-reel. Please refer to part identification information opposite.

Applications

- Portable Electronics
- Programmable Logic Controllers
- Computers and Peripheral Devices
- Audio Equipment
- Power Supplies and Power Distribution
- Instrumentation

Features

- 100mΩ On-Resistance
- GenV HEXFET output
- Bounce-free operation
- 2.5 - 4.5 Amp capacity
- Linear AC/DC operation
- 4,000 V_{RMS} I/O isolation
- Solid-State reliability
- UL recognized
- ESD Tolerance:
  - 4000V Human Body Model
  - 500V Machine Model



Part Identification

PVN012PbF	thru-hole
PVN012SPbF	surface-mount
PVN012S-TPbF	surface-mount, tape and reel

(HEXFET is the registered trademark for International Rectifier Power MOSFETs)

Electrical Specifications (-40°C ≤ T_A ≤ +85°C unless otherwise specified)

INPUT CHARACTERISTICS	Limits	Units
Minimum Control Current (see figure 1)	3.0	mA
Maximum Control Current for Off-State Resistance @ T_A = +25°C	0.4	mA
Control Current Range (Caution: current limit input LED, see figure 6)	3.0 to 25	mA
Maximum Reverse Voltage	6.0	V

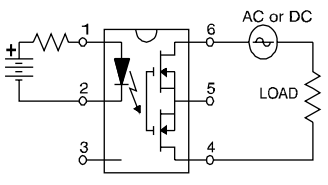
OUTPUT CHARACTERISTICS		Limits	Units
Operating Voltage Range		0 to ±20	$V_{(DC\ or\ AC\ peak)}$
Maximum Continuous Load Current @ T_A=+40°C, 5mA Control (see figure 1)			
	A Connection	2.5	A (DC or AC)
	B Connection	3.0	A (DC)
	C Connection	4.5	A (DC)
Maximum Pulsed Load Current @T_A=+25°C, (100 ms @ 10% duty cycle)			
	A Connection	6.0	A (DC or AC)
Maximum On-State Resistance @T_A=+25°C, for 1A pulsed load, 5mA Control (see figure 4)			
	A Connection	100	mΩ
	B Connection	65	
	C Connection	40	
Minimum Off-State Resistance @ T_A=+25°C, ±16V_{DC}		0.16 x 10^8	Ω
Maximum Turn-On Time @T_A=+25°C (see figure 7), for 1A, 20 V_{DC} load, 5mA Control		5.0	ms
Maximum Turn-Off Time @T_A=+25°C (see figure 7), for 1A, 20 V_{DC} load, 5mA Control		0.5	ms
Maximum Output Capacitance @ 20V_{DC} (see figure 2)		300	pF

GENERAL CHARACTERISTICS		Limits	Units
Minimum Dielectric Strength, Input-Output		4000	V_{RMS}
Minimum Insulation Resistance, Input-Output, @T_A=+25°C, 50%RH, 100V_{DC}		10^{12}	Ω
Maximum Capacitance, Input-Output		1.0	pF
Maximum Pin Soldering Temperature (10 seconds maximum)		+260	°C
Ambient Temperature Range:	Operating	-40 to +85	
	Storage	-40 to +100	

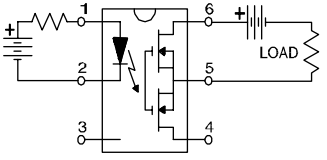
International Rectifier does not recommend the use of this product in aerospace, avionics, military or life support applications. Users of this International Rectifier product in such applications assume all risks of such use and indemnify International Rectifier against all damages resulting from such use.

Connection Diagrams

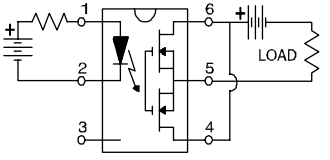
"A" Connection



"B" Connection



"C" Connection



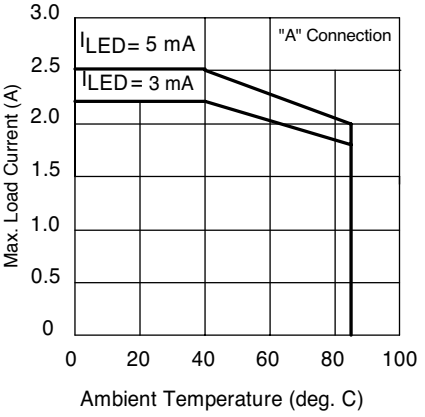


Figure 1. Current Derating Curves*

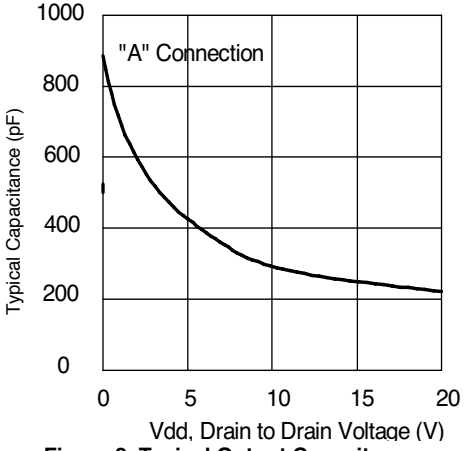


Figure 2. Typical Output Capacitance

* Derating of 'B' and 'C' connection at +85°C will be 70% of that specified at +40°C and is linear from +40°C to +85°C.

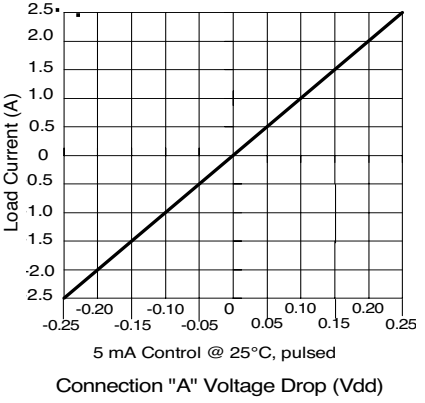


Figure 3. Linearity Characteristics

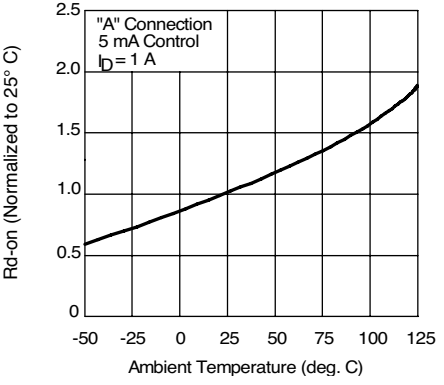


Figure 4. Typical Normalized On-Resistance

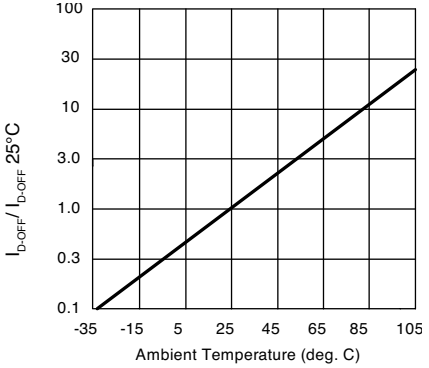


Figure 5. Typical Normalized Off-State Leakage

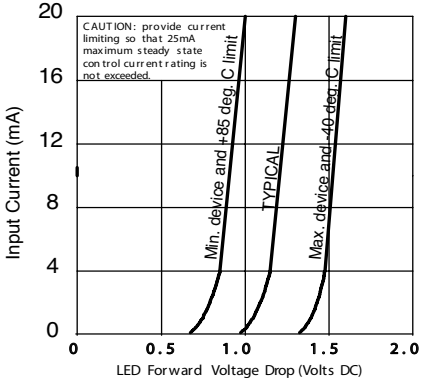


Figure 6. Input Characteristics (Current Controlled)

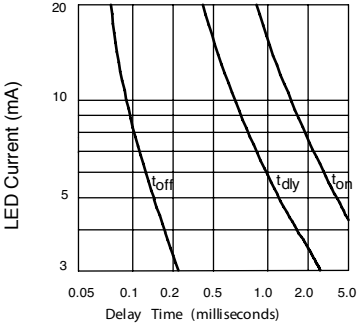


Figure 7. Typical Delay Times

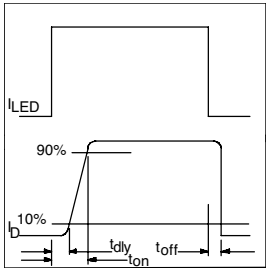
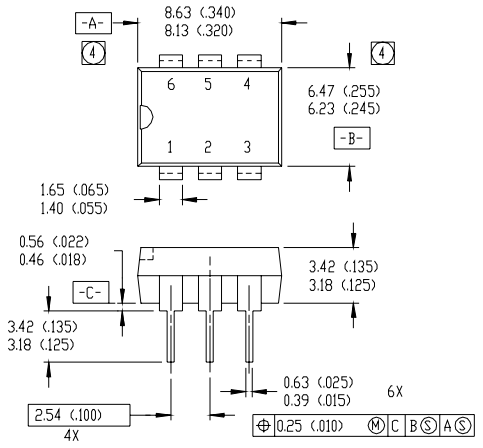
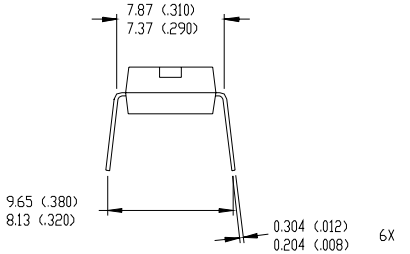


Figure 8. Delay Time Definitions

Case Outlines



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: INCH.
3 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 (.010).



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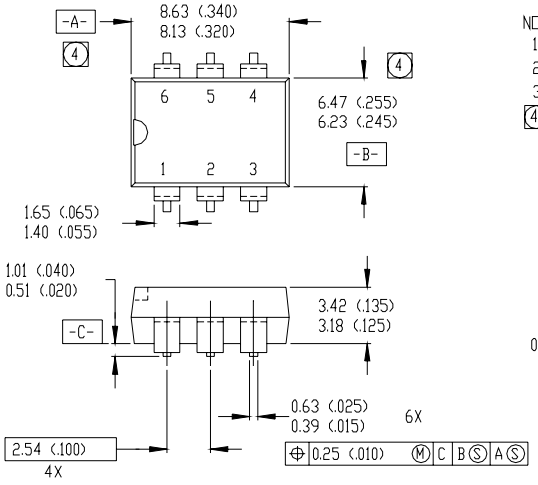

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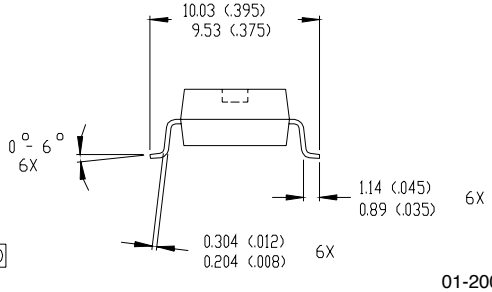


01-2009 01

Features:

- Delivers up to 100 times the energy of conventional capacitors and delivers ten times the power of ordinary batteries
- Is optimized for individual applications through its capacity to repeatedly charge and discharge
- Designed for smaller and lighter-weight products
- Offers instantaneous ride-through power
- UL recognized

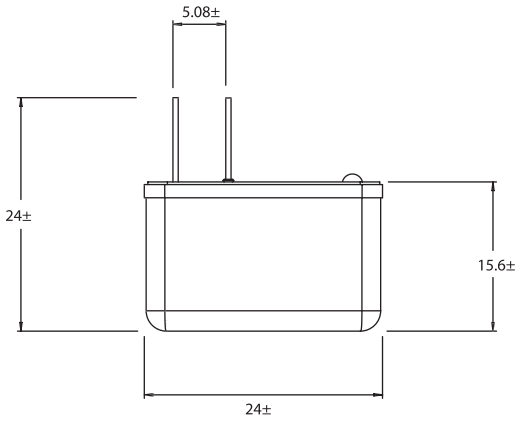
PC5

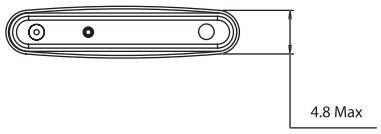
BOOSTCAP® Ultracapacitor

BOOSTCAP® Ultracapacitors provide extended power availability, allowing critical information and functions to remain available during dips, sags, and outages in the main power source. In addition, it can relieve batteries of burst power functions, thereby reducing costs and maximizing space and energy efficiency. The ultracapacitor features a cylindrical design and an electrostatic storage capability that can cycle hundreds of thousands of charges and discharges without performance degradation.

BATTERY vs. ULTRACAPACITOR vs. CAPACITOR COMPARISON

Available Performance	*Lead Acid Battery*	*Ultracapacitor*	*Conventional Capacitor*
Charge Time	1 to 5 hours	0.3 to 30 seconds	10-3 to 10-6 seconds
Discharge Time	0.3 to 3 hours	0.3 to 30 seconds	10-3 to 10-6 seconds
Energy (Wh/kg)	10 to 100	1 to 10	‹0.1
Cycle Life	1,000	›500,000	›500,000
Specific Power (W/kg)	‹1000	‹10,000	‹100,000
Charge/discharge efficiency	0.7 to 0.85	0.85 to 0.98	›0.95





NOTES:
1) DIMENSIONS ARE IN (mm)
2) TOLERANCES ARE +/- .5 UNLESS OTHERWISE SPECIFIED
3) PIN DIA .500 +/- .05 mm

Specifications

Capacitance	• 4 Farads	(DCC, 25°C)	
Capacitance Tolerance	• -10%/+30%		
Voltage			
Continuous	• 2.5 V		
Peak	• 2.7 V		
Series Resistance			
DC	• 400 mΩ	(-25%/+25%)	
1 kHz	• 123 mΩ	(-25%/+25%)	
Current (Rated) [1,2]	• 1 A		
Stored Energy	• 13 J		
Leakage Current	• 0.020 mA	(72h, 25°C)	
Weight	• 4 g		
Volume	• .0015 L		
Temperature [3]			
Operating	• -40° C to 70° C		
Storage	• -40° C to 85° C		
Life Time (25°C)	• 10 y	ΔC ›20%, ESR ‹ 200% of initial value	
Cyclability (25°C, I = 20 A)	• 500,000	ΔC ›20%, ESR ‹ 200% of initial value	

With a capacitance of 4 farads at 2.5 volts, and weighing only 4 grams in a 18 x 24 x 4.8 mm package, PowerCache's UL recognized PC5 ultracapacitor is ideal for consumer electronics, wireless transmission, medical devices, automatic meter readers, and many other applications requiring a pulse of energy that cannot be efficiently provided by a battery or power supply alone.

The PC5 works in tandem with batteries for applications that require both a constant low power discharge for continual function and a pulse power for peak loads. In these applications, the device relieves batteries of peak power functions resulting in an extension of battery life and a reduction of overall battery size and cost.

The PC5 is also an ideal source of back-up power and pulse. It can provide extended power availability, allowing critical information and functions to remain available during dips, sags, and outages in a power supply or battery change. And, like all PowerCache products, the PC5 is capable of accepting charges at the identical rate of discharge.

Physical Characteristics

Dimensions (Reference only)	• 18 x 24 x 4.8 mm	(+/- 1 mm)

NOTES

[1] Rated current: 5 sec discharge rate to ½V
[2] Device can withstand short circuit current if kept within the operating temperature
[3] Steady state case temperature

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