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A Synchronised Direct Digital Synthesiser

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Abstract

We describe a Direct Digital Synthesiser (DDS) which provides three frequency-locked synchronised outputs to generate frequencies from DC to 160 MHz. Primarily designed for use in a heterodyning range imaging system, the flexibility of the design allows its use in a number of other applications which require any number of stable, synchronised high frequency outputs. Frequency tuning of 32 bit length provides 0.1 Hz resolution when operating at the maximum clock rate of 400 MSPS, while 14 bit phase tuning provides 0.4 mrad resolution. The DDS technique provides very high relative accuracy between outputs, while the onboard oscillator's stability of ±1 ppm adds absolute accuracy to the design.

Keywords: DDS, direct digital synthesis, heterodyne, signal generator, range finder

1 Introduction

Accurate range data are an integral requirement of many developing research fields. Machine vision is one such field, requiring real-time measurements over a wide field of view with high resolution and precision. Simultaneous full-field systems have several advantages over techniques requiring laser scanning due to the latter's slow scan times (and therefore data update rate) and the requirement of using moving parts. Simultaneous acquisition can also be beneficial when operating in a dynamic scene, where measurements of multiple events in the field of view are made at the same instant in time.

Stereo vision techniques are highly dependent on both the distance of the measurement and the separation distance between cameras, and therefore provide poor accuracy for long range applications. Pulsed time of flight rangers are technically complex due to the high bandwidth and sensitivity required at the receiver, and this often limits the resolution available in full-field configurations. Other full-field ranger techniques are described in a number of papers [1,2]. The homodyne technique modulates a light source at radio frequency, illuminates the entire field of view and reflects back from any objects. A high speed shutter (often an image intensifier) is modulated at the same frequency, and is placed in front of a CCD camera. The light received at the shutter experiences a phase delay due to the distance travelled, which is then encoded into the intensity measured by the camera. Various methods are then used to remove the background intensity from the measurement. The dynamic range of current CCD camera technology is quite limited, and therefore severely restricts the performance of the system.

A heterodyne based image range finder is being developed by the authors [3]. The configuration is very similar to that used in a homodyne system, but the shutter is modulated with a frequency which is slightly different from that of the light source; refer figure 1. The result is a low frequency signal which has the range encoded as phase (rather than amplitude). The signal can easily be captured by a CCD camera operating at a standard video frame rate.

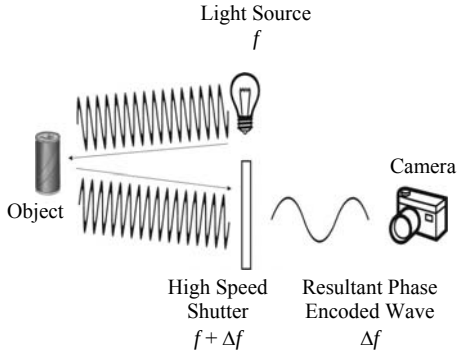

Figure 1: Heterodyning Range Imager

The heterodyne configuration is less susceptible to errors due to intensity variation (colour and texture of

the object), and because the range is encoded into a continuous variable (phase), the accuracy of the measurements are not directly constrained by the dynamic range of the camera. Although quantisation distortion can lead to phase determination errors with low amplitude signals, the resulting errors in range determination are very small compared to errors caused by low amplitudes with the homodyne approach.

2 Functional Specification

The ranger requires both the light source and shutter signals to operate at a high frequency, up to 100 MHz, and yet maintain a stable low frequency difference between the signals, preferably down to milliHertz. During initial prototyping this was provided by two frequency synchronised Agilent 8648B benchtop signal generators. With this configuration the constantly changing phase between the two signals at the start of the acquisition period is unknown, therefore only relative range measurements can be made between two objects in the same field of view. A low cost, low power alternative is desirable to allow the ranger to be developed for applications such as mobile robotic vision.

If the phase difference between the light source and shutter is known, an absolute measurement can be obtained (within the 2π unambiguous range of the modulation frequency being used). One method to achieve this is to use a phase detection circuit, either based on a digital or analogue configuration. To achieve millimetre range measurements, with a modulation frequency of 100 MHz, the phase must be measured with an accuracy of 4 mrad (calculated using equation 1). The accuracy of the reference phase measurement must therefore exceed this, preferably being known with at least 12 bit resolution (1.5 mrad).

$$\Phi = \frac{4\pi \cdot F_{\mathrm{mod}} \cdot d}{c} \qquad (1)$$

where: Φ is the measured phase

F_{mod} is the modulation frequency

d is the range

c is the speed of light.

This is a technically challenging task due to the high frequencies involved. A simple alternative solution is to generate a third output signal, operating at the low difference frequency, which is used as a reference. If all signals are initially synchronised at a known phase, the phase difference between the two high frequency signals can be obtained by measuring the phase of the low frequency signal. To overcome the 2π phase ambiguity of the distance measurements, the operating frequency needs the capability to change rapidly, making a coarse measurement at a low frequency and a precise measurement at a higher frequency.

A direct digital synthesiser (DDS) can meet these requirements. Operating from a digital clock, a DDS steps through a sine wave lookup table and passes the value to a digital to analogue converter, refer figure 2. By changing the frequency tuning word (the step size through the table), the output frequency can be precisely adjusted in very small increments from DC to the Nyquist frequency. By operating multiple synthesisers from the same digital clock source, the frequency generated has very high relative accuracy as any drift will be experienced equally at all outputs. The delay between changes in output frequency is virtually zero (unlike other methods such as an analogue phase-locked loop).

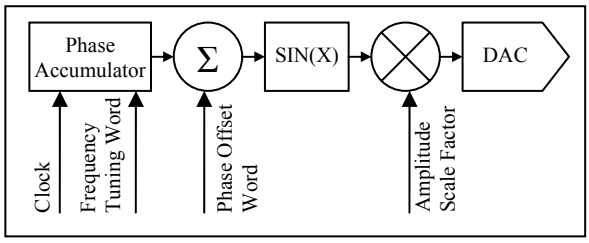

Figure 2: Direct Digital Synthesiser Core

3 Construction

A prototype board was constructed using two Analog Devices AD9852 direct digital synthesisers, controlled by an Atmel 89LS8252 micro processor. The AD9852 provides:

- An internal clock up to 300 MHz
- 48 bit frequency tuning (1 μHz resolution)
- 14 bit phase tuning (0.4 mrad resolution)
- 12 bit digital to analogue converters
- A range of operating modes, including FSK, BPSK, PSK, CHIRP and AM operation

The micro processor selected has an SPI bus interface which is used to control each AD9852. It can also operate from the same 3.3 V supply as the AD9852, simplifying the I/O interface between the devices as no voltage level shifters are required. It provides in-system programmable flash memory which allows the firmware to easily be upgraded, and PC communication through a serial interface.

The PCB design suffered from a synchronisation problem because each AD9852 independently multiplied the common 20 MHz external oscillator to the 300 MHz maximum system clock rate. This

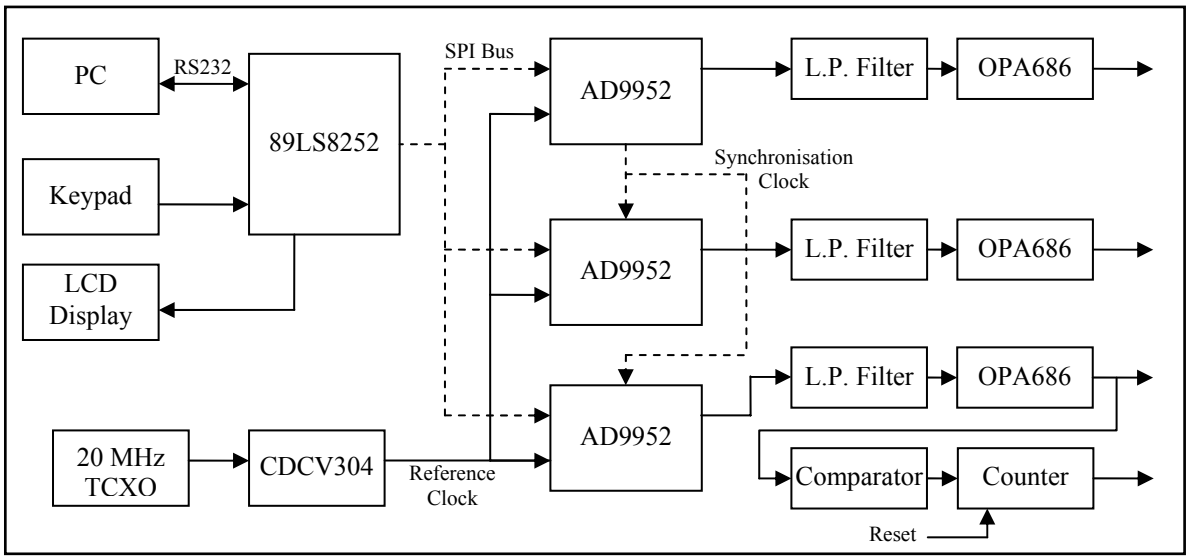

Figure 3: Block diagram of synchronised DDS PCB

method was used to reduce the design part count, as an external multiplier is not required, while also simplifying board layout and EMI constraints. However, small timing variations between devices can cause a phase error between the generated outputs. To overcome this problem when using the AD9852 DDS requires the use of high speed inputs [4], which cannot easily be achieved with standard CMOS logic. Minimising digital switching noise at the power supply was also a concern due to the relatively high current per device (about 1 ampere each when operating at the maximum clock frequency).

The newly available DDS part AD9952 addressed both of these problems; i) providing a synchronisation clock input and output to interconnect multiple devices, and ii) reducing the power consumption per device from over 3.5 W to less than 200 mW. The use of the AD9952 also:

- Increased the maximum internal clock from 300 MHz to 400 MHz
- Reduced the frequency tuning word from 48 bit to 32 bit
- Increased the output DAC from 12 bit to 14 bit
- Removed the automatic operating modes except for single tone

A PCB was built using the AD9952, following the block diagram shown in figure 3. The resultant design has an increased maximum output frequency of 200 MHz (limited by the Nyquist frequency); although in practice a 160 MHz limit is often used to provide improved spurious-free dynamic range (SFDR). The decrease of the frequency tuning word length reduced the output resolution from 1 μHz to 0.0931 Hz, calculated using equation (2), when operating at the maximum clock frequency of each device.

$$Tuning\ resolution = \frac{System\ clock\ \ frequency}{2^{tuning\ word\ length}} \qquad (2)$$

The increased resolution of the output DAC provides enhanced SFDR, however, the output amplitude is reduced from that of the AD9852. The additional amplification required may introduce noise which negates any advantage which could be gained due to the extra 2 bits from the DAC. The removal of additional operating modes (FSK, BPSK, PSK, CHIRP and AM) is of no concern to this project as they will not be used. This is primarily because the operating modes provided which are applicable to ranging techniques require linear electronics and optics, whereas the shutter (image intensifier) used in this project is a non-linear device.

Control of the DDS PCB is provided by the 89LS8252 micro processor. Standalone operation is available through a numeric keypad and LCD screen interface, or the design can be computer controlled through an RS232 port. All settings are stored in non-volatile EEPROM memory, and are recalled each time the system is powered up, making the user interface easier to use. Controlling each DDS IC through the SPI bus, the frequency, phase and amplitude can individually be specified for each output.

The system clock is generated by internally multiplying a 20 MHz reference clock within each AD9952, to a maximum rate of 400 MHz. The reference clock is provided by a TCXO [5] which provides stability of ±1 ppm over the extended temperature range of -40 to 85 °C. Fine tuning adjustment by a potentiometer allows the oscillator to

be calibrated against a reference frequency. A high speed clock buffer, Texas Instruments CDCV304, reduces loading on the oscillator to 3 pF (from 3 pF per AD9952) and also increases the slew rate to reduce the clock skew between each DDS. One AD9952 is selected to operate as a master device, which generates an output signal at one quarter of the system clock rate. This "synchronisation clock" is then used by the slave AD9952s to ensure the commands are applied at the same time to all devices – providing synchronisation of the output waveforms.

The DAC outputs from the AD9952 are low pass filtered through a 7th order elliptic filter to remove harmonics above the Nyquist frequency, and are then amplified by a high gain, wideband, voltage feedback operational amplifier (Texas Instruments OPA686) configured as a differential amplifier. This converts the differential outputs from the AD9952 into a single ended sine wave with amplitude of 2 $V_{pk\text{-}pk}$, which delivers 1 $V_{pk\text{-}pk}$ to a 50 Ω load through an impedance matched output and transmission line.

A further enhancement to the design was made by including a digital counter on the 3rd (reference) output; refer figure 3. By multiplying the generated reference signal frequency by a constant value, followed by the counter dividing by this same constant value, a digital output of the reference frequency is produced (a 4th output). The multiplied frequency output (3rd output) is then used to trigger the CCD camera. This reduces system error as the light source, shutter, and camera all utilise a common oscillator, and the reference phase is known at the beginning of each captured frame (from the digital counter output).

The PCB layout required attention to high speed design techniques, and suitable layout of the digital and analogue parts of the mixed system. Separate ground planes and voltage supply rails, along with physical separation of the analogue section, have been used to minimise digital noise on the outputs. Surface mount components have been used in the high frequency regions to reduce lead inductance. The low pass filter layout was optimised to reduce stray capacitance, and also to prevent coupling between the inductors by mounting them at 90° angles to one another. On the digital side, attention paid to the reference clock traces reduced the clock skew between parts. A high speed buffer was used to drive the update pin of the AD9952s, providing a fast slew rate to prevent input timing variation between devices.

Table 1: DDS Specifications

Parameter	Value
Bandwidth	160 MHz
Stability	±1 ppm
Frequency tuning resolution	0.0931 Hz
Phase tuning resolution	0.3835 mrad
Output waveform	Sine wave
Wideband SFDR*	39 dBc
Power consumption	3.5 W
Input voltage range	10 – 18 V DC
Size**	140 × 110 × 20 mm

* Wideband SFDR measured over the frequency span of DC to 200 MHz from generated signals between 10-110 MHz
** Does not include the keypad and LCD display

4 Software

The micro processor software accepts a target input frequency with 0.1 Hz resolution, which must be converted to a tuning word using equation (3).

$$FTW = Desired\ frequency \times 2^{32} / System\ clock\ freq \quad (3)$$

where: FTW is the 32 bit Frequency Tuning Word

To prevent rounding errors of the lower order bits, a standard 32 or 64 bit multiplication routine is not suitable for this calculation. A custom multiplication routine was written which multiplies a standard 32 bit value (the target frequency) with a predefined 40 bit constant based on the system clock frequency, producing a 72 bit result. The value is then rounded to 32 bits, producing the tuning word with maximum precision. Note that the routine was originally used with the AD9852 to produce a 48 bit tuning word from an 88 bit multiplication result, and has simply been scaled down to reduce the software processing time and RAM requirements.

5 Results

Table 1 presents specifications of the PCB design while operating at the maximum clock frequency of 400 MHz, providing 160 MHz system bandwidth. Very high absolute stability of ±1 ppm ensures that the output frequency is very consistent over a wide temperature range, and is suitable for measurement applications such as this one. As all three outputs are generated from the same clock source, any small drift from the oscillator will be common to all output signals. Therefore in a system that requires relative frequencies (rather than absolute), stability error will effectively be eliminated.

The wideband output spectrum, spanning from DC to 200 MHz, is shown in figures 4-6. The spurious-free dynamic range (SFDR) varies from 39-40 dBc in the figures shown, and is limited by a constant peak at 100 MHz.

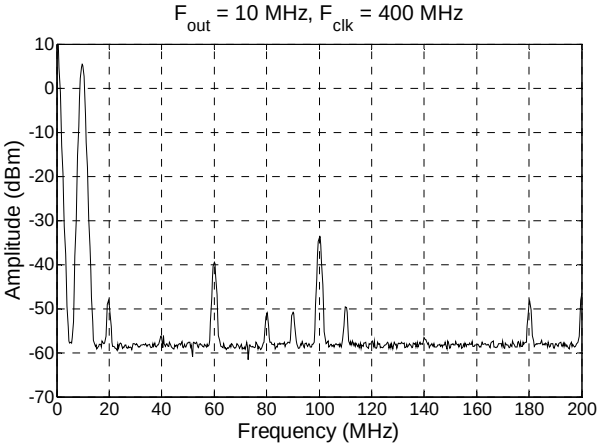

Figure 4: 10 MHz output spectrum

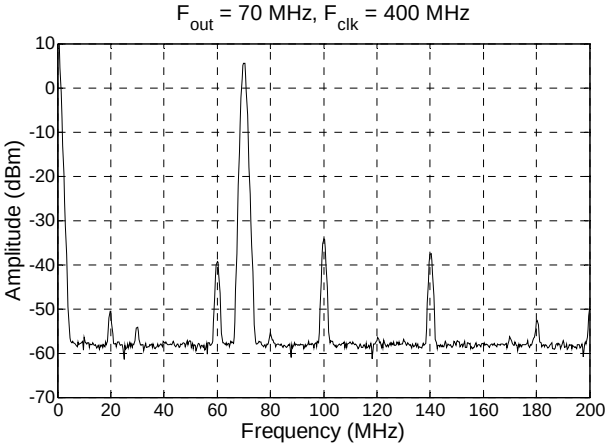

Figure 5: 70 MHz output spectrum

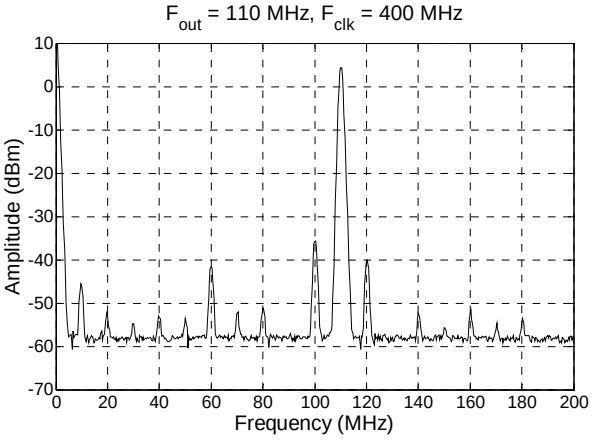

Figure 6: 110 MHz output spectrum

To identify the source of the constant frequencies (60 MHz and 100 MHz), a wideband spectrum scan was taken with the output frequency set to DC (therefore no harmonics of the output frequency can be present) and is shown in figure 7. As the synchronisation clock was previously operating at 100 MHz, which is also the 5th harmonic of the reference clock, the AD9952 internal multiplier was reduced to a value of 19. This reduces the system (internal) clock to 380 MHz, and the external synchronisation clock to 95 MHz which can be independently identified in the spectrum. The 60 and 100 MHz frequencies remain clearly visible in figure 7, and are therefore due to the 3rd and 5th harmonics of the reference clock being coupled onto the output. The 1st, 4th, and 9th harmonics (20, 80, and 180 MHz) are also visible, although have a reduced amplitude. The signals at 95 MHz and 190 MHz are being generated by the synchronisation clock's 1st and 2nd harmonics.

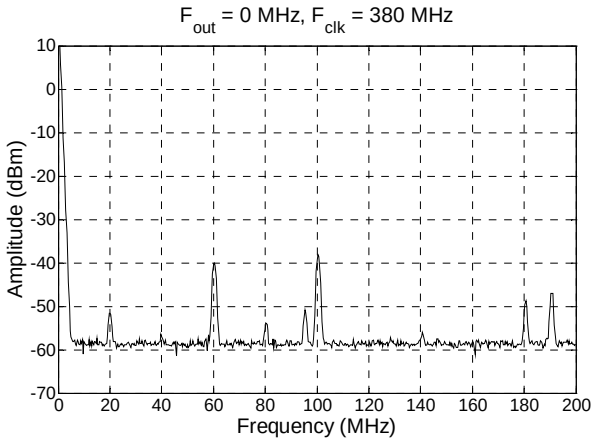

Figure 7: 0 Hz output spectrum

In figure 5, the 2nd harmonic of the generated signal seen at 140 MHz is 43 dBc. For an output of 110 MHz it increases to 24.5 dBc (this is not visible in the figures shown). It is largely due to the limited bandwidth of the high gain output amplifier, which tends to modify the sine wave towards a triangular shape at high frequencies.

A DC signal is present on all output spectra shown. This is primarily due to variations in matched component values such as the gain setting resistors of the amplifier (which have 1% tolerance). Variations in stray capacitance and/or inductance, and any differential error in the AD9952 outputs will also add a DC offset.

6 Evaluation

As the shutter (image intensifier) used in the ranger is a non-linear device, the harmonics of the signal generated by the DDS board at high frequencies will not affect the ranging system performance (the shutter is turned on and off, rather than being sinusoidally modulated). To improve performance for applications where a sinusoidal signal is required, the stray capacitance at the amplifier inputs will be reduced by cutting away the surrounding ground plane and an amplifier with higher gain bandwidth and/or a reduction in the gain level will be used. Another low pass filter could also be used after the amplification stage to remove harmonics above the 160 MHz maximum output frequency. Similarly, the DC

component does not affect the range finder project, but it could be removed with a high pass filter at the board output or reduced with tight component tolerances and layout.

The coupling from the digital reference clock (primarily harmonics at 60 MHz and 100 MHz) limits the performance of the DDS board. A single ended clock was chosen to ease routing constraints on the 2 layer PCB. By using a buffer with a differential output (such as LVDS or LVPECL), the switching noise generated on the power and ground planes, and consequently the output, will be reduced. A differential buffer will also improve performance by reducing clock skew between the AD9952s. Notably, the effect of the digital clock harmonics can be removed in the range finder application because the CCD integrates over a continuously changing input. So long as the operating frequency chosen is not a multiple of the reference clock, the (very small) error will be averaged to zero over the large number (hundreds of thousands) of light samples received at the CCD.

The versatility of the design has been recognised by other researchers looking to incorporate it into a variety of products. The PCB is capable of generating frequencies which are either dependent on one another, or completely independent. It can generate quadrature signals of the same frequency by moving one output by 90°. The wideband output can be operated from DC to 160 MHz, and changes in frequency have virtually zero settling time. Possible future improvements to further enhance the flexibility of the design include providing a USB interface in place of the existing serial RS232 connection. The use of the AD9952 comparator, or an external comparator, would provide a square wave output for clock generator applications. Other planned improvements include upgrading the manufacturing process from a 2 layer PCB to 4 layers. This will reduce noise levels by providing continuous ground and power planes, as well as superior controlled impedance routing and isolation for the high frequency traces. The PCB dimensions could be significantly reduced from their already small size (140 × 110 mm) for mobile applications; of which the design is already suited due to its ability to operate from an unregulated 12 V battery source with low power consumption of 3.5 W. 18 – 36 V DC input is also available with a simple component change. During the writing of this paper, Analog Devices released a new multi-channel DDS (AD9959) which is capable of generating four synchronised outputs with frequencies up to 200 MHz. Future work will incorporate this part, simplifying the design by removing the need for multiple DDS ICs to be used. It is worth noting that the multiple device design shown here can be applied to the AD9959 for applications which require more than four synchronised outputs.

7 Conclusions

The application of this board to the heterodyning full-field ranging system has produced a proof-of-concept system that has demonstrated 1 cm precision over a range of 1 – 5 m, with excellent linearity and repeatability. This has been achieved using an LED illumination source and an 8 bit CCD camera. Modulating the system up to 100 MHz with a 12 bit camera is currently being investigated; with the expectation that millimetre resolution will be obtained.

To the best of our knowledge, there are no commercial units comparable to this design available on the market today. Bench top signal generators can be synchronised together, but do not provide the flexibility and ease of control over the relative frequencies and phase that this design does. They are also not suitable for low power or mobile applications, and the cost is large compared with this design. The direct digital synthesiser board described here has exceeded all of the requirements for the range finding project, providing wide bandwidth, high stability, and precise tuning. Most importantly, it provides multiple outputs which are synchronised to a common source, providing exact manipulation of the relative frequencies and phase. The system is currently undergoing commercialisation evaluation by WaikatoLink, and it is hoped to market these boards in the near future.

8 References

[1] S. Christie, S. L. Hill, B. Bury, J. O. Gray, and K. M. Booth, "Design and Development of a Multi-Detecting 2-Dimensional Ranging Sensor," *Measurement Science & Technology*, vol. 6, pp. 1301-1308, 1995.

[2] T. Oggier, M. Lehmann, R. Kaufmann, M. Schweizer, M. Richter, P. Metzler, G. Lang, F. Lustenberger and N. Blanc, "An all-solid-state optical range camera for 3D real-time imaging with sub-centimeter depth resolution (SwissRanger)", *Optical Design and Engineering. Proceedings of the SPIE*, vol. 5249, pp. 534-545, 2004.

[3] Carnegie, D.A., Cree, M., and Dorrington, A. "A High-Resolution Full Field Imaging System". *Rev. Sci. Instrum.*, vol. 76, 083702, 2005.

[4] Analog Devices, "Synchronizing Multiple AD9852 DDS-Based Synthesizers" Application Note AN605, Rev. 0, 2003

[5] C-MAC Micro technology, 20.0 MHz CFPT-9006 FX 3 A, www.cmac.com/mt/