Pre-charging and DC Fault Ride-Through of Hybrid MMC Based HVDC Systems

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***Abstract*--Compared to half-bridge based MMCs, full-bridge based systems have the advantage of blocking dc fault, but at the expense of increased power semiconductors and power losses. In view of the relationships among ac/dc voltages and currents in full-bridge based MMC with the negative voltage state, this paper provides a detailed analysis on the link between capacitor voltage variation and the maximum modulation index. A hybrid MMC, consisting of mixed half-bridge and full-bridge circuits to combine their respective advantages is investigated in terms of its pre-charging process and transient dc fault ride-through capability. Simulation and experiment results demonstrate the feasibility and validity of the proposed strategy for a full-bridge based MMC and the hybrid MMC.**

***Index Terms*--Capacitor voltage ripple, DC fault, hybrid, Modular multilevel converter, power loss.**

I. Introduction

HIGH voltage direct current (HVDC) system using modular multilevel converter (MMC) has become increasingly popular due to its many advantages, such as modular design, high efficiency and scalability, and excellent output waveform with low harmonic distortion [1-11]. A single-phase structure of a MMC is shown in Fig. 1 (a) where each arm contains N sub-modules (SMs).

The basic building block in a MMC is a SM. There are mainly three different SM topologies proposed for MMC, i.e., half-bridge based sub-module (HBSM) [1-6] shown in Fig. 1 (b), full-bridge based sub-module (FBSM) [7-10] shown in Fig. 1 (c), and clamp double half-bridge based sub-module (CDSM) [11], shown in Fig. 1 (d). HBSM was first proposed in 2003 [1] and has been used in large HVDC systems. However, HBSM based MMC (HB-MMC) does not have dc fault blocking capability and thus has to rely on ac or dc circuit breakers to isolate dc faults [12-13]. This becomes problematic for both the converter as it has to withstand high fault current from the connected network since it could take considerable time for the system (especially multi-terminal system) to recover from such a dc fault [14]. Thyristors connected in parallel to the ac terminals of the SM have been employed [15-16] to bypass short-circuit current and protect the free-wheeling diodes. However, this method cannot isolate dc fault and additional devices are still required for fast fault isolation.

To address the issues of dc fault, FBSM was proposed which has the inherent advantage of dc fault blocking capability. However, the number of power devices is doubled in each SM compared to the HBSM, resulting in increased costs and power loss. To increase the utilization of the power devices, several studies have been conducted to increase the modulation index and ac voltage output by adopting the negative voltage output from the FBSM [8-10]. In [8] the concept of using negative voltage state of the FBSM to increase voltage output was proposed, but no detailed relationship between the ac and dc voltages and the limit of modulation index were considered. The relationship among the SM capacitor voltage, the ac and dc voltages was presented in [9], but the effect of the use of negative voltage state on energy variation and capacitor voltage ripple was not addressed. In [10], the focus was on eliminating the energy oscillation between the upper and lower arms using a desirable modulation index of 1.414 in the full-bridge based MMC (FB-MMC). However, for all the existing studies considering the use of the negative voltage state of the FBSM, no systematic design and detailed analysis on the relation of SM capacitor voltage variation and the maximum modulation index has been provided. Alternative clamp double half-bridge based MMC (CD-MMC) with dc fault blocking capability was proposed in [11], in which one IGBT and three diodes are added to control the fault current to flow through the capacitors in the SMs under dc faults. A hybrid MMC consisting of a combination of FBSMs and HBSMs is proposed in [17] which not only has dc fault blocking capability but also uses fewer semiconductor devices and has lower power loss compared to the FB-MMC.

For a MMC, pre-charging all SM capacitors to the pre-set value is a prerequisite for its normal operation. The conventional pre-charging process for a MMC can be divided into two stages of uncontrolled charging and controlled charging [1, 18-19]. In the uncontrolled charging stage, all capacitors are charged equally, but their voltages are insufficient for the operation of MMC. Under the controlled charging stage, various schemes have been proposed either adopting external voltage sources [1], using PWM mode to charge from the DC side [18], or using sequentially controlled charging methods to charge from AC side [19].

In this paper, strategy to optimise the configuration and control of HBSM and FBSM is proposed. In view of the relationships among ac/dc voltages and currents in FB-MMC

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with the negative voltage state, a detailed analysis on the link between SM capacitor voltage variation and the maximum modulation index is carried out. The pre-charging at start-up for the hybrid MMC which was not addressed in [17], is analyzed which reveals unequal charging between the capacitors in the FBSMs and HBSMs, and suitable charging strategies are then proposed. Although the continued operation without IGBT blocking under transient dc fault for the hybrid MMC was presented in [17], in this paper, a full operation process for the hybrid MMC under a transient dc fault is presented, including dc fault isolation without IGBT blocking, ac reactive power support during the dc fault, and dc-link voltage rebuilding process.

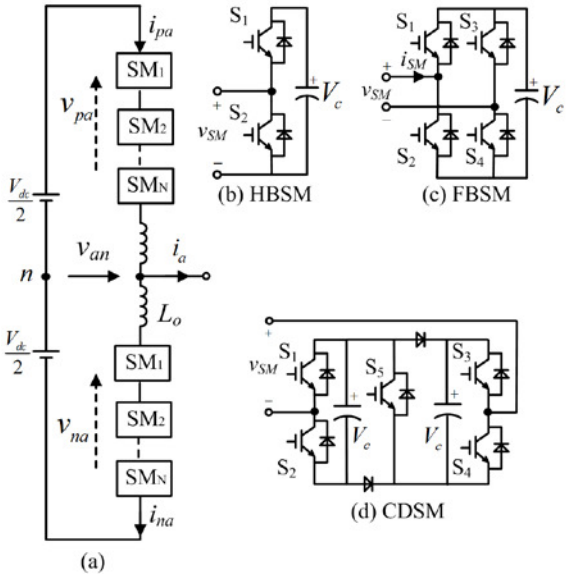


Fig. 1 Basic structure of a MMC and different sub-module arrangement

II. Basic Topology and System Control

For the MMC shown in Fig. 1 (a), V_{dc} is the dc-link voltage, L_0 is the arm inductor in each arm and C is the capacitor in each SM. v_{pa} and v_{na} are the total voltages generated by all the SMs in the upper and lower arms, respectively. i_{pa} and i_{na} are the current of the upper and lower arms, respectively. i_a is the output ac phase current.

According to Fig. 1 (a), the arm current i_{pa} and i_{na} can be expressed as [7]

$$i_{pa} = i_a/2 + i_{cca} \tag{1}$$

$$i_{na} = -i_a/2 + i_{cca} \tag{2}$$

where i_{cca} is the common mode current in phase a flowing through both the upper and lower arms. It has no effect on the output ac phase current and can be expressed as:

$$i_{cca} = \left(i_{pa} + i_{na}\right)/2 \tag{3}$$

Taking the neutral point n of the dc link as the voltage reference, the voltage and current can be expressed as

$$L_0 \frac{di_{pa}}{dt} = e_a - v_{an}, \quad L_0 \frac{di_{na}}{dt} = v_{an} - e_a \tag{4}$$

where e_a is the equivalent phase voltage in phase a and is expressed as

$$e_a = V_{dc}/2 - v_{pa} = -V_{dc}/2 + v_{na} = v_{na} - v_{pa}/2 \tag{5}$$

For the operation of a MMC, the following equation defines the dc voltage and must be satisfied under any conditions

$$v_{pa} + v_{na} = V_{dc} \tag{6}$$

Combine (5) and (6), the required arm voltage references are calculated as

$$v_{pa\_ref} = V_{dc}/2 - e_a, \quad v_{na\_ref} = V_{dc}/2 + e_a \tag{7}$$

e_a can be derived from the conventional current vector control scheme widely adopted for controlling grid connected VSCs. Appropriate PWM strategies which select the SMs to be switched in are used to produce the required arm voltage and to ensure the capacitor voltages in each SM are balanced. As this has been well documented [5, 7-8] no further details are given here.

TABLE I Switching States of FBSM

State	S_1	S_2	S_3	S_4	V_{SM}	V_C ($i_{SM} > 0$)
1	1	0	0	1	V_C	CHARGING
2	0	1	0	1	0	UNCHANGED
3	1	0	1	0	0	UNCHARGED
4	0	1	1	0	$-V_C$	DISCHARGING
BLOCK	0	0	0	0	-	-

III. Analysis of FBSM with Negative Voltage State

Table I illustrates the switching states for a FBSM shown in Fig. 1(c). Compared with the HBSM which can generate voltage states of V_c and 0, each FBSM can generate a third state of $-V_c$. Since the adopting of the negative voltage state in FBSM changes the relationship of ac/dc voltages and ac/dc side power, the arm current will also be changed, resulting in the change of capacitor voltage ripple in each SM. Thus, to keep a stable system, the limit of the number of FBSMs allowing generating the negative voltage state needs be investigated.

A. Principle of -V_c operation

The principle of the scheme is to make some of the SMs in each arm generate the voltage state of $-V_c$ so as to alter the voltage relationship between the dc and ac sides.

Considering the total number of SMs in each arm is N and the voltages across all the SM capacitors are balanced at V_c, the maximum voltage range each arm can produce is between 0 and NV_c for conventional method without using the $-V_c$ state. Therefore, the maximum value of the peak phase and dc voltages are given as

$$V_{dc} = NV_c, \quad V_{m\_\max} = \left(NV_c\right)/2 = V_{dc}/2 \tag{8}$$

If a maximum number of M SMs are allowed to operate at the $-V_c$ state in each arm ($M < N$), the maximum voltage range each arm can produce is now between $-MV_c$ and NV_c. Under such conditions, the peak phase voltage and dc voltage are given as

$$V_{dc} = \left(N - M\right)V_c, \; V_{m\_\max} = \frac{\left(N+M\right)V_c}{2} = \frac{V_{dc}}{2}\frac{\left(N+M\right)}{\left(N-M\right)} \tag{9}$$

Take $M = N/3$ as an example, i.e., one third of the SMs in each arm is allowed to produce $-V_c$, (9) can be written as

$$V_{dc} = 2NV_c/3, \quad V_{m\_\max} = 2NV_c/3 = V_{dc} \tag{10}$$

Comparing (10) and (8), if V_c remains unchanged, it can be seen that although the dc voltage is now reduced with the proposed operation, the maximum ac voltage that the MMC can produce increases from $NV_c/2$ to $2NV_c/3$ (for this reason, it is named here as Boost FB-MMC). Alternatively, if the dc voltage is to remain at the same level after introducing the $-V_c$ state, the number of SMs needs be increased by 50% but the ac output voltage increases by 100% compared to conventional control without using $-V_c$.

B. Capacitor Voltage Ripple

Since the modulation index, arm current and dc current in the Boost FB-MMC after introducing the $-V_c$ state are different to that in the conventional method, the capacitor voltages in each SM are analyzed to ensure they can remain balanced.

Neglecting converter power loss, the power balance equation between the three-phase ac and dc can be expressed as

$$P_{dc} = V_{dc}I_{dc} = 3V_mI_m\cos\varphi/2 = P_{ac} \tag{11a}$$

$$V_m = mV_{dc}/2 \tag{11b}$$

where I_m is the peak value of the output phase current, m is the equivalent modulation index, and φ is the voltage and current phase angle.

Assuming the arm current is directly controlled with no second-order harmonic circulating current, the arm voltage and current can be given respectively as

$$\begin{aligned} v_{pa} &= V_{dc}/2 - V_m\sin\omega t \\ i_{pa} &= I_{dc}/3 + I_m\sin(\omega t - \varphi)/2 \end{aligned} \tag{12}$$

Combining (11) and (12) yields the arm current as

$$i_{pa} = mI_m\cos\varphi/4 + I_m\sin(\omega t - \varphi)/2 \tag{13}$$

The instantaneous power flowing through the upper arm can be calculated as

$$p_{pa} = v_{pa}\times i_{pa} = \left(\frac{V_{dc}}{2} - V_m\sin\omega t\right)\left(\frac{I_{dc}}{3} + \frac{I_m}{2}\sin(\omega t - \varphi)\right) \tag{14}$$

Integrating (14) and substituting I_{dc} with (11), the energy variation $\Delta E(t)$ on the capacitors can be expressed as

$$\Delta E(t) = \frac{V_mI_m}{8\omega}\sin(2\omega t - \varphi) - \frac{V_{dc}I_m}{4\omega}\cos(\omega t - \varphi) + \frac{V_m^2I_m}{2\omega V_{dc}}\cos\omega t\cos\varphi \tag{15}$$

According to $\Delta E(t) = \left[CV_c^2(t) - CV_{c0}^2\right]/2$, the voltage on each SM capacitor can be calculated as

$$V_c(t) = \sqrt{2\Delta E(t)/C + V_{c0}^2} \tag{16}$$

where constant V_{c0} refers to the capacitor initial voltage.

Assuming the initial capacitor voltage is balanced at $V_{dc}/(N-M)$ as seen from (9), the SM capacitor voltage is

$$V_c(t) = \sqrt{\begin{aligned} &\frac{V_mI_m}{4\omega C}\sin(2\omega t - \varphi) - \frac{V_{dc}I_m}{2\omega C}\cos(\omega t - \varphi) \\ &+ \frac{V_m^2I_m}{\omega CV_{dc}}\cos\omega t\cos\varphi + \left(\frac{V_{dc}}{N-M}\right)^2 \end{aligned}} \tag{17}$$

For a simplified system containing 3 FBSM for each arm and rated at 6 kV dc and 9 MW, Fig. 2 compares the calculated capacitor voltage ripples using (17) and the simulation results using Matlab/Simulink. The nominal capacitor voltage in each SM is 3 kV and the dc voltage of 6 kV is defined as the unit voltage. It can be seen that the shapes of the curves are very similar. The slight differences in the maximum and minimum values are caused by the fact that the arm current used for calculation only includes the dc and fundamental components whereas the arm current in the simulation contains small 2nd order circulating current.

For different M/N ratios, the capacitor voltage ripples within a 360 degree fundamental cycle are calculated using the previous parameters and illustrated in Fig. 3. It can be observed that voltage ripples are relatively lower when M is less than N/3, which is comparable to conventional case without using negative voltage state (i.e., M=0). According to (9) and (11), the increase of M results in increased modulation index m. This in turn will make the arm current largely positive for inverter operation (and largely negative for rectifier operation), as seen in (13). For example, when M> N/3, m>2 and the arm current i_{pa} becomes purely positive (for unit power factor i.e., cosφ=1). This significantly affects the charging and discharging periods for the capacitors in the SMs and results in higher voltage ripple. Thus, in order to keep balanced capacitor voltage, M is chosen to be less than N/3.

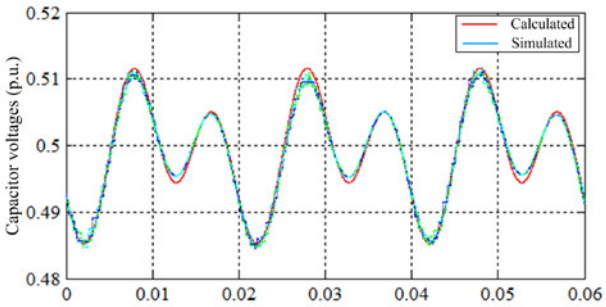


Fig. 2 Comparison of calculated and simulated capacitor ripples
(N = 3, M = 1, V_{dc}=6 kV, P=9 MW, m = 1.6, cosφ = 1, C = 1000 uF)

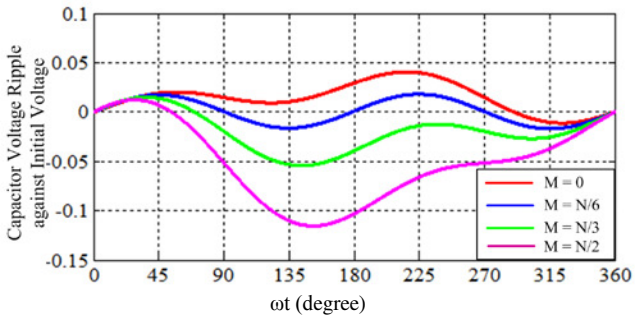


Fig. 3 Voltage ripples with different ratios of M/N

C. DC fault blocking

After all the switching devices are switched off (e.g., during a dc fault), the capacitor voltages of the FBSMs in each arm appear as serially connected voltage sources and have opposite polarity to the direction of the fault current flown from the ac side. If the total series voltage is higher than the

peak line-to-line ac voltage dc fault can be blocked. With the proposed control, the ac voltage is increased for the same dc voltage and thus it is important to check that the arm capacitor voltage is still sufficiently high to block the fault current. According to (9), (10) and (11b), in the proposed strategy the maximum modulation index is 2 and the maximum peak line-to-line ac voltage seen by the MMC during a dc fault is

$$u_{\max} = \sqrt{3} \times \frac{N+M}{2(N-M)} V_{dc} \tag{18}$$

The arm voltage formed by the voltages of the N capacitors is given as

$$u_{arm} = NV_c = \frac{N}{(N-M)} V_{dc} \tag{19}$$

Therefore, the blocking voltage formed by the two arm voltages (one upper arm and one lower arm) and the ac line-to-line voltage has the following relationship

$$u_{\max} = \frac{\sqrt{3}}{2} \frac{N+M}{(N-M)} V_{dc} < \frac{2N}{(N-M)} V_{dc} = 2u_{arm} \tag{20}$$

This proves that although the ac voltage in the proposed FBSM is increased, the converter still has sufficient capacitor voltage to block any dc faults. For case of M=N/3, the maximum ac line-to-line voltage is $\sqrt{3}V_{dc}$ compared to the blocking dc voltage of $3V_{dc}$ formed by the two arms.

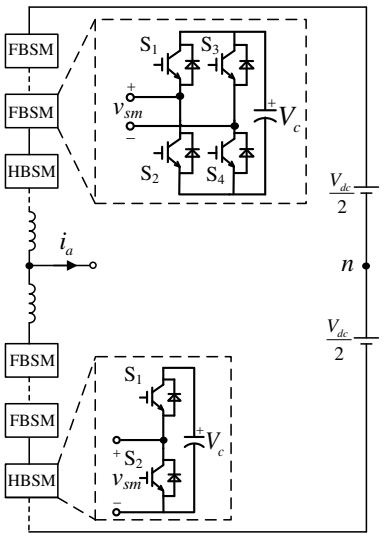


Fig.4 Schematic structure summarizing the control layer of the hybrid MMC

IV. Alternative MMC Configurations

According to the above analysis, only part of the SMs needs to produce $-V_c$. To reduce the total required power device, a hybrid MMC configuration with 2*N*/3 FBSM and *N*/3 HBSM is proposed in [17]. The schematic structure of the hybrid MMC is shown in Fig. 4. In this configuration, half of the FBSMs are allowed to produce $-V_c$ state, i.e., M= *N*/3. The basic operation of this MMC configuration including capacitor voltage balancing have been analysed in [17], so this paper will focus on the pre-charging process of the hybrid MMC and its ride-through capability under a transient dc fault both of which are vital to the operation of the converter.

A. Pre-charging process

To illustrate the pre-charging process of the hybrid MMC, Fig. 5 shows a two-phase example of a simplified MMC with each arm consisting of 2 FBSMs and 1 HBSM. In this example, $v_a > v_b$ so the initial ac charging current flows from phase *a* to phase *b*.

1) Uncontrolled charging stage

Initially, all SM capacitors voltages are assumed to be zero. To prevent large inrush current, pre-charging resistors may be inserted at the ac side. As shown in Fig. 5, the uncontrolled charging has two parallel loops in this example, one formed by the upper two arms and the other by the lower two arms. As seen, all FBSM capacitors are being charged but the charging of the HBSM capacitors is dependent on the current direction, i.e., only the HBSM capacitors in the lower phase *a* arm and upper phase *b* arm (marked as C_{a2} and C_{b1} in Fig. 5) are being charged whereas the HBSM capacitors in the upper phase *a* arm and lower phase *b* arm (marked as C_{a1} and C_{b2} in Fig. 5) are being bypassed. When the ac charging current changes direction, the charging for all the FBSM capacitors continues but the charging for the HBSM capacitors is changed, i.e., C_{a1} and C_{b2} will be charged and C_{a2} and C_{b1} bypassed. This indicates that there is unequal charging between the capacitors in the HBSMs and FBSMs. When the combined capacitor voltages within each current path become higher than the maximum value of the phase-to-phase ac voltage, the charging current gradually goes to zero and the uncontrolled charging stage ends.

2) Controlled charging stage

A grouping sequentially controlled charge method was proposed in [19] to solve the insufficient charging issue for the conventional MMC. However, to handle the unique issue of unbalanced capacitor charging, a new method is proposed as follows.

Step1: The FBSMs and HBSMs in each arm are arranged into *j* and *k* groups, respectively. Each time only one group is chosen for charging with all the IGBTs in the chosen group are all turned off. The other unselected groups are bypassed by turning on the appropriate IGBTs (v_{SM} = 0). When the sum of the series-connected capacitors voltages in the two chosen groups in the two-phase arms becomes higher than the maximum value of the phase-to-phase ac voltage of $\sqrt{3}V_{dc}$ (according to (10)), the charging current reduces to zero. Thus, to ensure the capacitors in the chosen group are charged to the pre-set value of $1.5V_{dc}/N$ (as M=N/3), the number of *j* and *k* should meet the following requirement,

$$\begin{aligned} &\frac{2N}{3j} \times \frac{1.5V_{dc}}{N} \times 2 \le \sqrt{3}V_{dc}, \qquad j \ge \frac{2\sqrt{3}}{3} \approx 1.2 \\ &\frac{N}{3k} \times \frac{1.5V_{dc}}{N} \times 1 \le \sqrt{3}V_{dc}, \qquad k \ge \frac{\sqrt{3}}{6} \approx 0.3 \end{aligned} \tag{21}$$

Equation (21) indicates that for simple and fast charging, the FBSMs in each arm can be separated into 2 groups (i.e., *j*=2) and the HBSMs are in one single group (i.e., *k*=1).

Step 2: After all capacitors in the charging group reach the pre-set value of $1.5V_{dc}/N$, SMs in this group are bypassed and the charging for the next group can start.

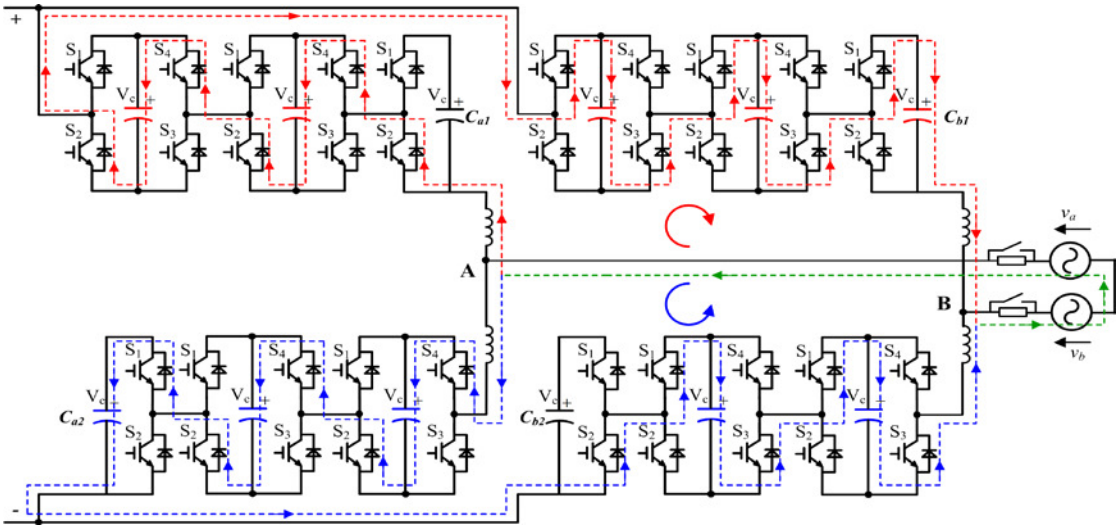


Fig. 5 Two charging current loops under the uncontrolled charging stage

Step 3: When the charging processes for all the groups complete, the controlled charging stage completes.

B. Ride-through capability under a transient dc fault

By using the negative voltage state of the FBSMs, the SMs can generate negative arm voltage. In such a way, the hybrid MMC can continue operating under the reduced dc-link voltage (even V_{dc} = 0). This means the hybrid MMC can not only block dc fault, but also continue operating to regulate its output current to the ac side, e.g., to support the healthy ac grid and to provide fast fault recovery and system restart. The control sequence can be divided into following three stages.

Stage 1: When a dc fault occurs, the dc link voltage collapses immediately. Under such a condition, the *d*-axis reference ac current for active power would reduce proportionally, (i.e. when V_{dc} = 0, I_d^* = 0), while the *q*-axis reference ac current for reactive power can remain unchanged or set to a new value to support the ac grid. For systems using over-head-line (OHL), automatically system recovery may be required as the dc fault might be temporary. For future large multi-terminal HVDC system using cables, the faulty branch maybe isolated by protection devices, e.g., dc circuit breaker and rapid system restart for the health network might be required. In this case, the control process moves to Stage 2 for the recovery operation.

Stage 2: A small dc-link reference voltage is provided and the system tries to build up the dc-link voltage. If the dc voltage can be built up successfully indicating the clearance of the dc fault, the control process moves to Stage 3. Otherwise, the dc-link reference voltage sets to zero again and the system waits for the next attempt for rebuilding the dc-link voltage.

Stage 3: The restart process can be considered under an initial condition of V_{dc} = 0 in accordance to (7). A ramp signal for the dc voltage reference can then be set and by controlling the *d*-axis and *q*-axis ac current the dc-link voltage can be built up smoothly.

V. Simulation Studies

To verify the system behaviours of the boost FB-MMC and the hybrid MMC, a point-to-point HVDC transmission system with one hybrid MMC terminal and one boost FB-MMC terminal is developed using Matlab/Simulink, and is shown in Fig. 6. The hybrid MMC adopts a configuration of 4 FBSMs and 2 HBSMs in each arm, in which two of the FBSMs are allowed to generate $-V_c$ state whereas the boost FB-MMC consists of 6 FBSMs in each arm, two of them allowed to generating $-V_c$ state. Because of the use of $-V_c$ state, the phase-to-phase ac voltage is 60 kV for a dc voltage of 60kV, being higher than the conventional MMC system for the same dc voltage. Each SM has a voltage of 15 kV, i.e., ¼ of the nominal dc voltage of 60 kV. In the simulation, the rated power is 90MW, the capacitance for all the SMs is 2200 uF, and a conventional phase-disposition PWM method with a carrier frequency is 2.5 kHz is used [2].

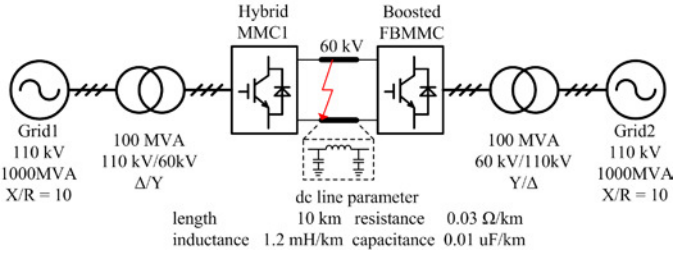


Fig. 6 Schematic diagram of the hybrid HVDC system based on the proposed MMC configurations

Figs. 7 and 8 show the simulation results illustrating the steady-state performance of the boost FB-MMC and the hybrid MMC, respectively. As shown in Figs. 8 (c) and (d), although the arm current in the boost FB-MMC is mostly negative (rectifier operation), the SM capacitors can still be charged during $-V_c$, ensuring balanced capacitor voltage. From Fig. 8, it can be observed that although the charging and discharging periods for the FBSMs and HBSMs are different in the hybrid MMC, all capacitor voltages can be balanced within each fundamental period.

Fig. 9 shows the operation of the hybrid MMC including the pre-charging process and dc fault ride-through and system recovery. In the simulation, it is assumed that the dc fault is cleared itself due to the use of OHL. However, the recovery

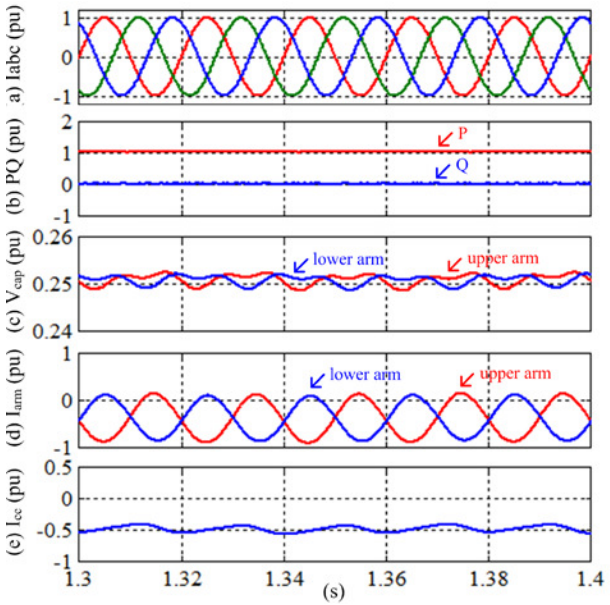


Fig. 7 Simulation results for the FB-MMC terminal, (a) ac currents; (b) converter output P and Q; (c) FBSM capacitor voltages; (d) arm currents; (e) common mode arm current.

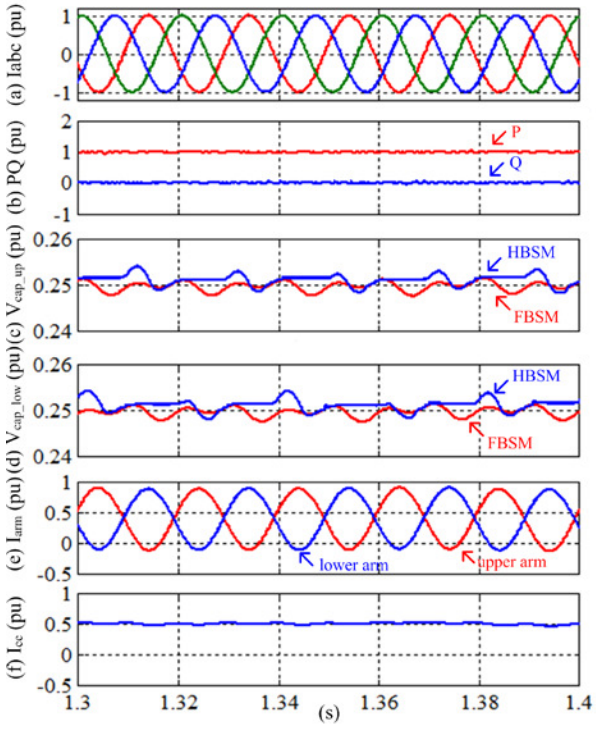


Fig. 8 Simulation results for the hybrid MMC terminal, (a) ac current; (b) converter output P and Q; (c) upper arm capacitor voltages; (d) lower arm capacitor voltages (e) arm currents; (e) common mode arm current.

process can also be used for future multi-terminal HVDC systems where the faulty branch is cleared by using other protection devices, e.g., dc circuit breaker etc. As illustrated in Figs. 9 (b) and (c), at the end of the uncontrolled charging stage (Stage I), the capacitor voltages in the FBSMs are higher than that in the HBSMs due to the unequal charging process. During stage II, the FBSMs are divided into two groups while the HBSMs are combined into one group according to (21). At 0.2s, the first FBSM group begins to be charged, and after all the capacitors in the first group reach the pre-set value, the charging process shifts to the second FBSM group, and then to the HBSM group. As shown, the presented pre-charging scheme successfully solves the unbalanced charging issue in the Hybrid MMC. After the pre-charging process, the hybrid MMC starts building the dc-link voltage (stage III). A ramp signal for the dc voltage reference (1pu / 0.1s) is provided and the dc-link voltage is built up smoothly. The hybrid MMC then resumes normal mode (Stage IV) at 1.0 s by increasing its active power transmission to 1.0 pu with 0.4 s.

At 1.8s, a temporary 250ms pole-to-pole dc fault is applied (stage V). The dc voltage quickly drops to zero, the hybrid MMC reduces the active power to zero accordingly and meanwhile, it supplies 0.3 p.u. reactive power to the ac grid. It demonstrates that the hybrid MMC can not only block the dc fault, but also continue operating to regulate the ac current. Such feature shows an excellent dc fault ride-through capability of the hybrid MMC. At 1.9s and 2.0s, two attempts for building up the dc-link voltage are carried out by setting a small dc-link reference voltage though both attempts are failed due to the existing fault. As the dc fault is cleared at 2.05s, the third attempt by the hybrid MMC at 2.1s successfully builds up a small dc-link voltage and the process then moves to the dc-link voltage building stage. At 2.2s, the dc voltage has fully recovered and the active power is then gradually increased and the system recovers to normal operation (stage VI).

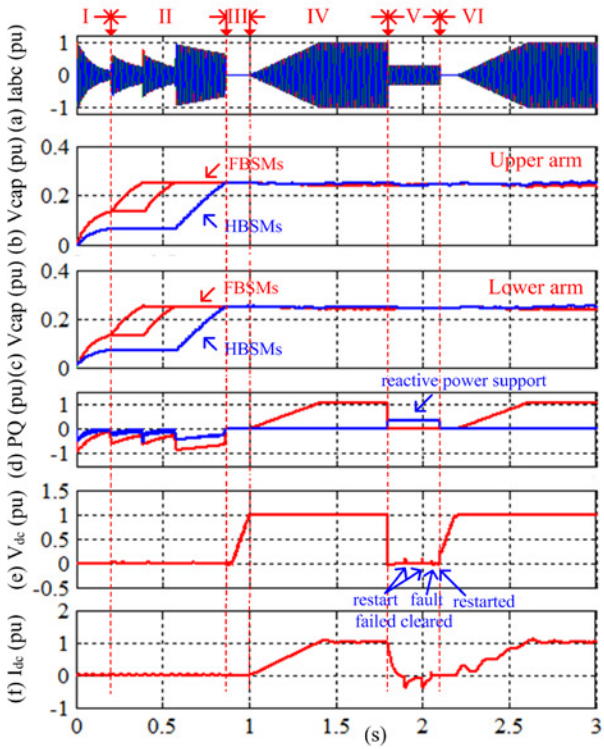


Fig. 9 Simulation results demonstrating dc fault ride-through capability of HVDC transmission systems based on the hybrid MMC, (a) ac current; (b) phase a upper arm SM capacitor voltages; (c) phase a lower arm SM capacitor voltages; (d) converter output P and Q; (e) dc-link voltage; (f) dc link current.

VI. Experimental Results

A. FB-MMC with $-V_c$ state (Boost FB-MMC)

To test the boost FB-MMC with the negative voltage state, a prototype single-phase MMC rated at 400 W was developed and its schematic diagram is shown in Fig. 10. The control system is implemented using a TMS320F2812 DSP and the main parameters are listed in Table II. Two large dc capacitors connected in series to the dc power supply are used to form the neutral point. The waveforms are captured using a Tektronix TDS 2014B oscilloscope and the voltage waveforms are taken from a signal processing board fed from Hall-effect voltage sensors

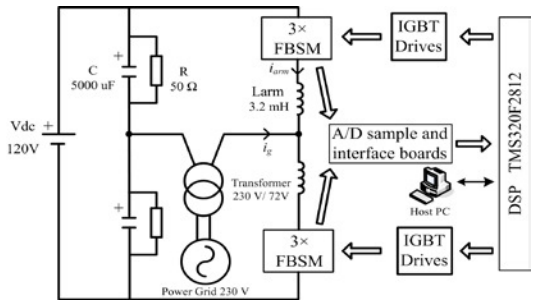


Fig. 10 Schematic diagram of the proposed FB-MMC experimental system

TABLE II Parameters of the Experimental MMC System

Item	Values
MMC rated power	400 W
DC voltage	120 V
AC voltage (phase-ground rms.)	72 V
Number of SMs per arm	3
DC voltage per SM	60 V
SM capacitor	2200 uF
Inductance per arm	3.2 mH
MMC carrier frequency	2.5 kHz

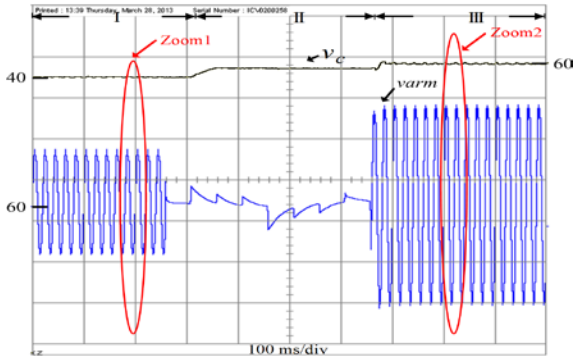
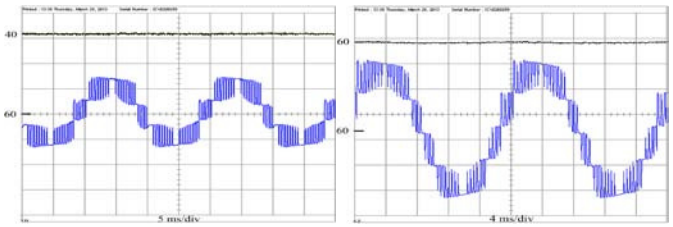


Fig. 11 Test results during the switching of the control mode with the MMC operated as an inverter; v_c: SM capacitor voltage (50V/div); v_{arm}: upper arm voltage (50V/div).



(a) Zoom 1 (b) Zoom 2

Fig. 12 Detailed SM and arm voltages.

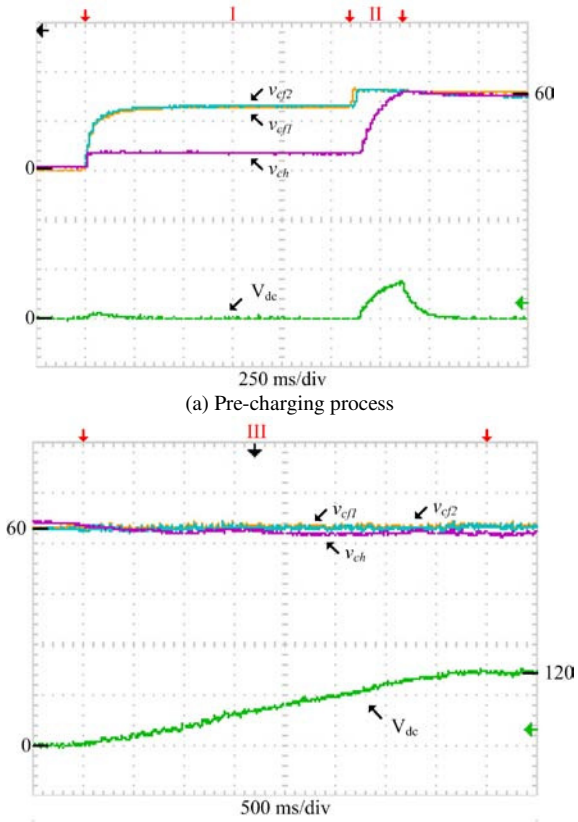
To illustrate the different operation and the impact of negative voltage state on system voltage and current, Figs. 11 and 12 show the voltage produced by the SMs in the upper arm during the transfer from traditional control strategy to the proposed control strategy in inverter mode. In stage I, the system is under traditional control strategy with each SM voltage being 40 V (for 120 V total dc voltage and three SMs per arm). The range of arm voltage is thus from 0 to 120 V, including three voltage levels shown in Fig. 12 (a). In stage II, the MMC stops and goes into a pre-charging period to increase the SM capacitor voltage to 60 V (the dc voltage remains at 120 V). In stage III, the MMC operates under the proposed control strategy with 1 out of 3 SMs in each arm permitting to produce -60 V (i.e., $-V_c$). The range of arm voltage is thus from -60 to 180 V (i.e., from $-V_c$ to $3V_c$), consisting of four voltage levels shown in Fig. 12 (b). As shown in the results, under the same dc-link voltage, the MMC based on the proposed strategy doubles the output peak-to-peak voltage from 120 V to 240 V with 50% increase of the capacitor voltage from 40 V to 60 V.

B. Hybrid MMC

To verify the pre-charging process and dc voltage building process of the hybrid MMC, the previous prototype was modified with each arm now contains two FBSMs and one HBSM. In this test, the 120V dc source is removed. As previously described, for normal three-phase hybrid MMC, the system has two parallel charging loop one formed by the upper arms and the other formed by the lower arms. For the prototype single-phase hybrid MMC shown in Fig. 10, the two resistors on the dc side also forms two parallel charging loops for the upper and lower arms, and enables the similar pre-charging process to be tested in the single-phase prototype.

Fig. 13 (a) shows the pre-charging process of the hybrid MMC. At 250ms, the uncontrolled charging stage (Stage I) begins. As can be seen from Fig. 13 (a), the capacitor voltage in the FBSM is higher than that in HBSM and the capacitor voltages are insufficient and unbalanced at the end of the uncontrolled charging stage, which is in a good agreement with the previous illustration in Section IV. Then, at the controlled charging stage (Stage II), two FBSMs are divided into two groups, and one HBSM is set into the third group, according to (21). It can be observed that the presented pre-charging scheme successfully solves the unbalanced charging issue in the Hybrid MMC. Following the pre-charging process, a dc voltage building process is presented in Fig. 13 (b). At this stage (Stage III), a ramp signal of 30 V/s is set to build up the dc voltage. It is observed that the dc voltage can track the ramp signal well and the building process is very smooth.

Fig. 14 demonstrates the ride-through capability of the hybrid MMC under during reduced dc voltage. It is observed the converter can still operate and supply reactive power to the ac grid for supporting the ac system, although the dc voltage drops from 120V to 0V. This result shows that the hybrid MMC can continue controlling the ac current under a wide dc voltage range from 0 to rated value (i.e. 120V).



(a) Pre-charging process

(b) DC voltage building process

Fig. 13 Operation of the hybrid MMC, V_{dc}: dc voltage (85V/div); v_{cf1}: capacitor voltage in FBSM1 (40V/div); v_{cf2}: capacitor voltage in FBSM2 (40V/div); v_{ch}: capacitor voltage in HBSM (40V/div)

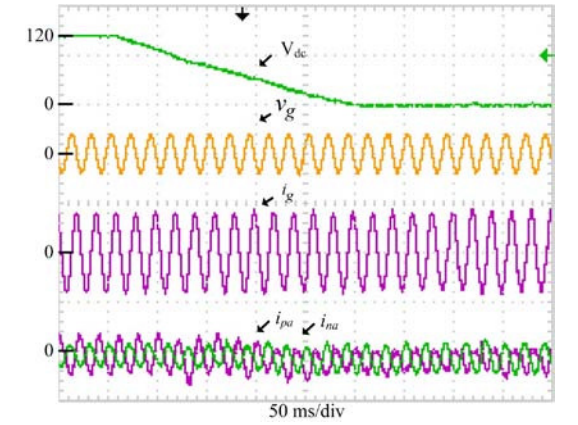


Fig. 14 Operation of the hybrid MMC under dc fault conditions, V_{dc}: dc voltage (85V/div); v_g: ac voltage (255V/div); i_g: ac current (5A/div); i_{pa}: upper arm current (5A/div); i_{na}: lower arm current (5A/div).

VII. Conclusions

This paper proposes alternative operation and SM topologies considering dc fault blocking capability, system pre-charging and restart. The principles of using the negative voltage state of full-bridge based sub-modules (FBSM) are introduced. A detailed analysis on the relationship between the capacitor voltage ripple and the maximum modulation index and required dc fault blocking voltage is presented. The pre-charging and dc fault ride-through of a hybrid configuration incorporating mixed FBSM and conventional half-bridge SM (HBSM) are carried out which show the advantages in the hybrid configurations over the conventional FBSM and HBSM systems. Both simulation and experimental results validate the feasibility and dynamics of the proposed systems.

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