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Inkjet and laser hybrid processing for the series interconnection of thin-film photovoltaics

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Keywords: Laser, Inkjet, Solar, Thin-Film, Photovoltaics, CdTe, CIGS, Interconnect

1.0 Abstract

Inkjet deposition can be a complementary technology to laser ablation to enable new processes. One such process is the One Step Interconnect (OSI) for thin-film photovoltaics, which is an improved method for series interconnection. The standard series interconnection process consists of three laser scribes between the deposition of the three key cell layers; transparent front contact, absorber layer and the metallic back contact. OSI allows the series interconnection to occur after the deposition of all layers significantly simplifying the manufacturing process. This is achieved by inkjet printing of conductive and insulative materials concurrently with depth selective laser scribes. OSI has been shown to make effective interconnects on cadmium telluride (CdTe) photovoltaics with fill factors (FF) >60%. The benefits are many and include the reduction of capital equipment costs, reduced panel wastage and potentially improved material performance. OSI is fully scalable and production ready.

2.0 Introduction

Inkjet deposition of functional materials is an enabling technology for novel processes in large area electronics. Insulators, conductors and semiconductors can already be deposited in various forms[1–3]. Combining inkjet additive manufacturing with subtractive laser processes increases the potential further. Using lasers and inkjet together allows the reduction of printed feature size, either through the subsequent laser ablation of printed tracks, selective laser sintering or laser patterning of surfaces to control wetting[4], [5] as well as embedding features within other materials.

From a machine architecture viewpoint, inkjet and laser are well aligned. Both use machine platforms with x,y motion and sophisticated control software. They have the ability to accept input in the form of digital files, removing the need for the expensive tooling of screen printing and lithographic processes and therefore allowing greater flexibility of device design. Both often utilise machine vision systems for layer to layer alignment.

The combined laser and inkjet approach is applicable to a number of large area electronic devices including capacitive touch panels, thin-film solar cells, smart windows and OLED lighting. Figure 1 shows laser isolated electrodes written into an ITO transparent conductor and a printed metallic busbar at the edge of a capacitive touch screen.

Here, the One Step Interconnect (OSI) process is introduced. It uses combined laser and inkjet processing for the series interconnection of thin-film photovoltaic (PV) modules. The process has been demonstrated on cadmium telluride (CdTe) solar cells but is applicable to all types of thin-film PV. There are many manufacturing advantages to OSI including ~25% reduction in cost of ownership, increased panel efficiency through reduction of wasted panel area and reduction of production line footprint.

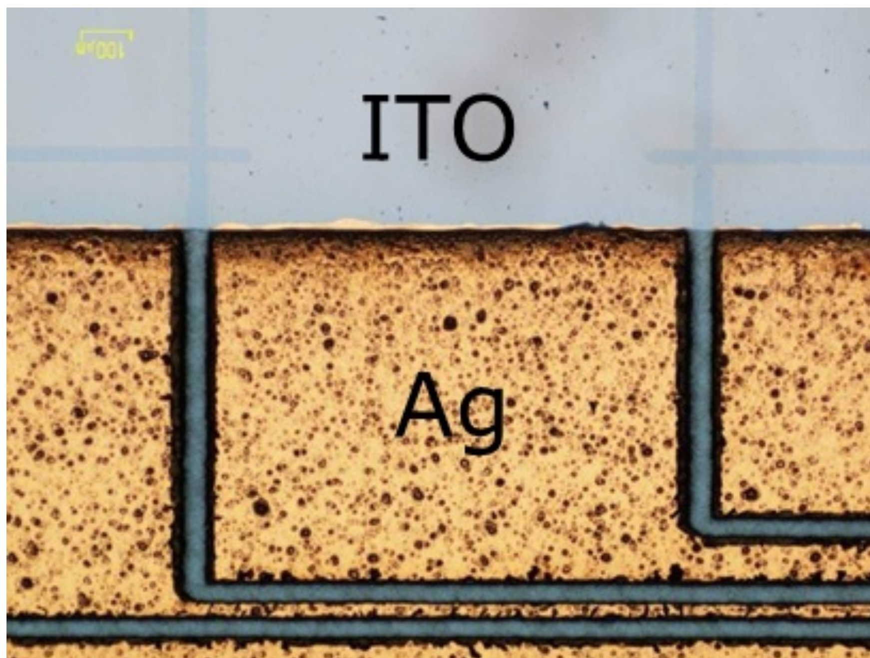


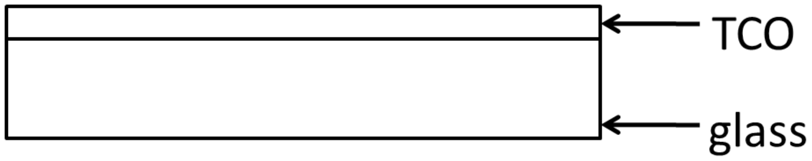
Figure 1

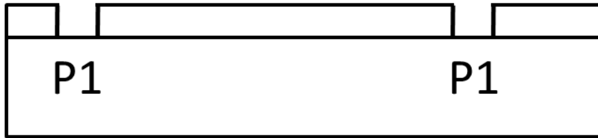
3.0 One Step Interconnect

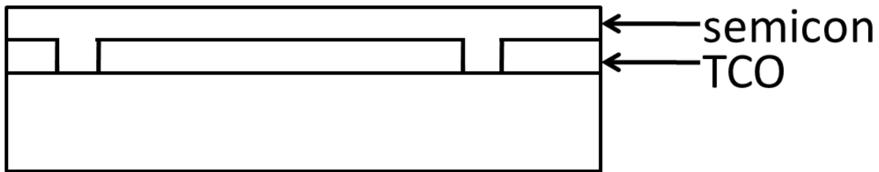
The M-Solv patented[6] OSI process has been developed to optimise the series interconnection of thin-film solar cells[7]. Complete solar modules typically have an area of around 1m^2. Without any post processing these panels would generate a high current, which scales with surface area, and a low voltage, defined by the band offset. In order to get a more useable electrical output the large panels are divided up into many smaller cells, typically around 100, connected in series. The electrical output is then a few 10's of Volts with a modest current.

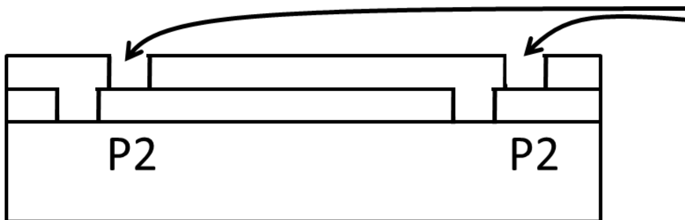
Work presented here is focused specifically on CdTe cells although OSI is applicable to all types of TF-PV. The paradigm for series interconnection is sequential laser scribing which takes place in between material deposition steps. The front contact is deposited onto a glass substrate and subsequently laser scribed into discrete lengths of cell on a pitch of 5-15mm: material dependent. Secondly, the semiconductor absorber layer is deposited and a second laser pattern written, aligned to but offset from the first. Finally the back contact is deposited and a third laser patterning step is completed, again offset. These three scribes, termed P1, P2 and P3, electrically isolate the front and back contacts and allow electrical connection by bridging the back contact of one cell and the front contact of the adjacent cell. A schematic of this process can be seen in Figure 2. Typical dimensions of the interconnect structure are;

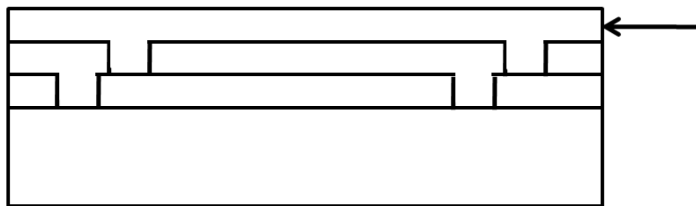
scribe width ~50μm, complete interconnect ~300μm and the thickness of the active layers ~3μm.

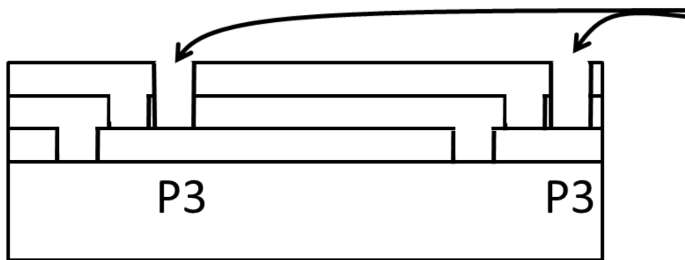

TCO
glass


P1
P1


semicon
TCO


P2
P2




P3
P3

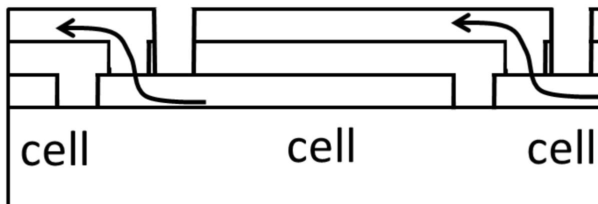

Series connection
Series connection
cell
cell
cell

Figure 2

The OSI process greatly simplifies the series interconnection by separating the material deposition and patterning steps. First all layers are deposited to form the complete cell structure, then three laser scribes are written simultaneously. Scribe A removes the entire stack to the glass resulting in electrical isolation of the front contact. Scribe B and P3 stop on the transparent conductor: one exposes the front contact for electrical connection and the other isolates the back contact. Two inkjet heads follow, the first fills in scribe A with an insulative material and the second prints a metallic bridge between the front contact of one cell and the back contact of the adjacent cell. A schematic of the OSI process can be seen in Figure 3.

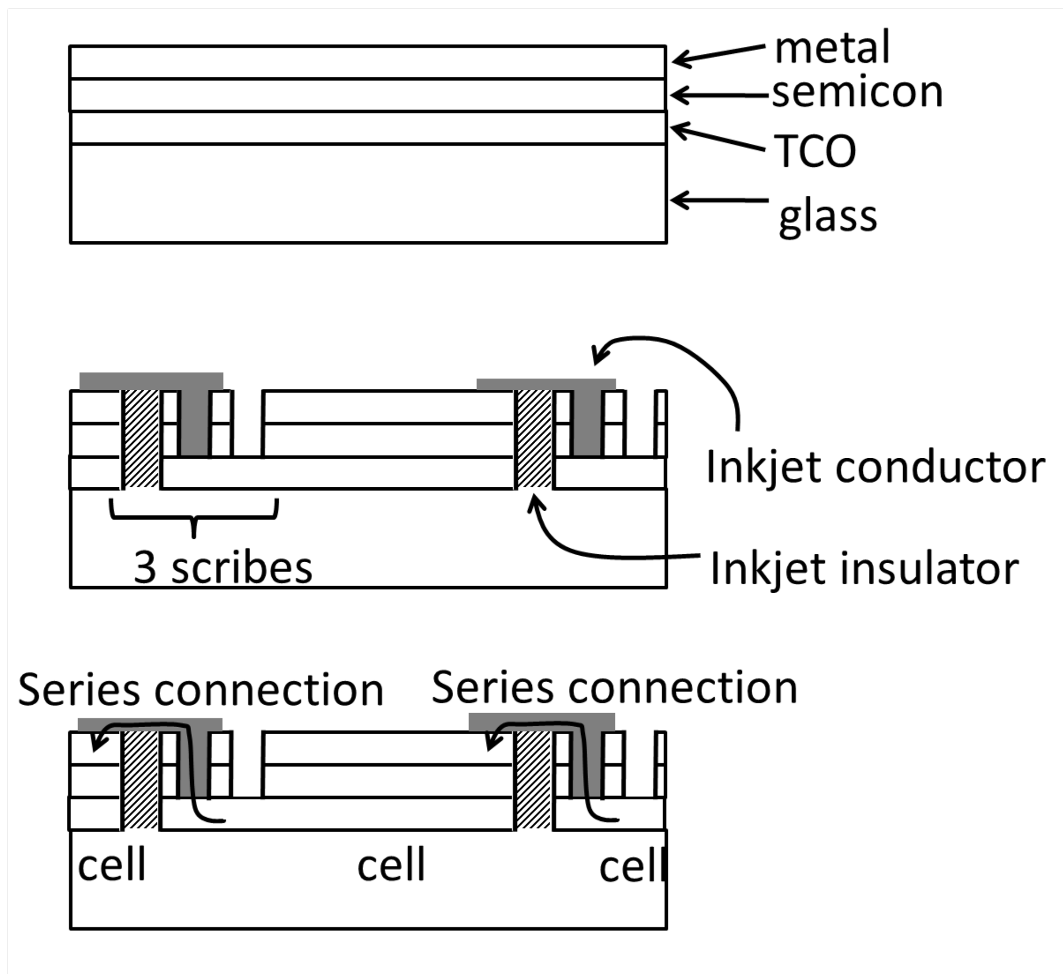


Figure 3

The OSI process has a number of benefits compared to the current paradigm. In OSI the entire interconnect is manufactured in a single pass of a single process head removing the requirement for the alignment steps that usually occur between the P1, P2 and P3 scribes. This, in return, allows a decrease of the area in-between interconnects that does not contribute to electricity generation resulting in increased panel efficiency. The material deposition can occur without breaking vacuum, allowing better control over layer interfaces. There is a large reduction in capital equipment cost and line foot print since three laser scribing platforms and a number of load locks can be removed and replaced with one OSI tool. Vacuum-air transitions can only occur at room temperature to avoid introducing stress into

the panel. Therefore the thermal profile of the panel in transit is flattened due to the removal of the atmospheric laser processes between each of the three deposition steps. In the case of CdTe the total reduction in panel temperature change has been estimated to be ~25% assuming the use of a ready coated FTO substrate, such as NSG TEC™ 10 glass and standard process temperatures. The flatter temperature profile reduces energy consumption, lessens thermally induced panel stress and removes the requirement for further capital equipment in the form of heaters and coolers.

3.1 Experimental

Cadmium telluride/cadmium sulphide (CdTe/CdS) heterojunction cells were produced by Colorado State University (CSU). The substrate used was NSG TEC™ 10 glass (10Ω/sq FTO). A thin layer of n-type CdS, <100 nm, and a thicker p-type layer (~2.5μm) of CdTe was deposited by closed space sublimation (CSS) to form the absorber layer[8]. The device then received a copper doping treatment which promotes the formation of an Ohmic contact with a metallic electrode. The cells were then sent to the Centre for Renewable Energy Systems and Technology (CREST) at Loughborough University for the deposition of a sputtered gold back contact.

A Spectra Physics Explorer-2Y 532nm diode pumped solid state (DPSS) laser was used for laser processing. The laser outputs a maximum of 2W average power in <12ns pulses of up to 200μJ energy at repetition rates from single shot to 60kHz.

Industrially capable piezo-electrically actuated drop on demand (DoD) print heads from Fujifilm Dimatix were used for the deposition of both insulative and conductive inkjet inks. These print heads are capable of dispensing small volumes (~10pl) of material with a high degree of accuracy and repeatability. The insulative ink is a commercially available graphics ink widely used for large area printing. This ink is made up of acrylate monomers which undergo free radical polymerisation when exposed to UV light. These acrylics are also good electrical insulators. A fibre optic-coupled Exfo OmniCure® 2000 UV cure lamp is positioned immediately behind the printhead dispensing the dielectric ink to enable curing.

A silver containing ink is used to form the conductive track. All metallic inkjet inks are either metal nanoparticle dispersions or organometallic complexes in solution[1]. Both types require a post deposition heat treatment to boil off solvents and to either sinter the nanoparticles or initiate reduction of the metal-salt compound. Nano-particulate inks usually have higher metal loading 20-40% by weight compared to around 12% in organometallic inks. Although the higher loading is advantageous for lower resistivities the sintering step for nanoparticle inks requires a much higher temperature than the equivalent thermal process in organometallic inks. This makes organometallic inks the preferred choice for Organic Photovoltaics (OPV) or flexible cells on polymer substrates. The ink used in this work is a commercially available, 40% loaded silver nano-particle suspension. Post-deposition the ink is sintered in a Carbolite convection oven for 15 minutes at 250°C.

Images of the OSI process were gathered with a Nikon optical microscope equipped with a DS-Fi1 colour high-definition camera. A Taylor Hobson SunStar CCI scanning white light

interferometr (SWLI) was used to assess morphology of the laser scribes and printed tracks. A Newport Oriel class A solar simulator and Keithley 2400 source meter are used to extract current/voltage (I/V) curves from the material for electrical characterisation.

3.2 Process

The laser processes are well known and understood[9]. Scribe B and P3 are identical to the conventional laser process wherein a green (532nm) laser is incident through the glass. Both the glass and TCO are highly transparent to this wavelength, therefore the majority of the laser energy is absorbed at the semiconductor interface. Local vaporisation takes place with a corresponding localised expansion. Stress builds, the semiconductor fractures and is explosively removed. This process has three main advantages, firstly it requires relatively low laser pulse energy since it does not require the vaporisation of the entire semiconductor stack, secondly the scribe is self-limiting in depth since it always breaks along the material interface and finally there is little thermal interaction with the remaining semiconductor which maintains material stoichiometry. Scribe A requires the removal of the transparent conductor along with the entire semiconductor stack. Increasing the fluence of the same 532nm laser by a factor of 4 results in a clean scribe down to the glass substrate which exhibits good electrical isolation (>5MΩ). Optical micrograph and scanning white light interferometer (SWLI) line profile of the laser process on CSU CdTe can be seen in Figure 4.

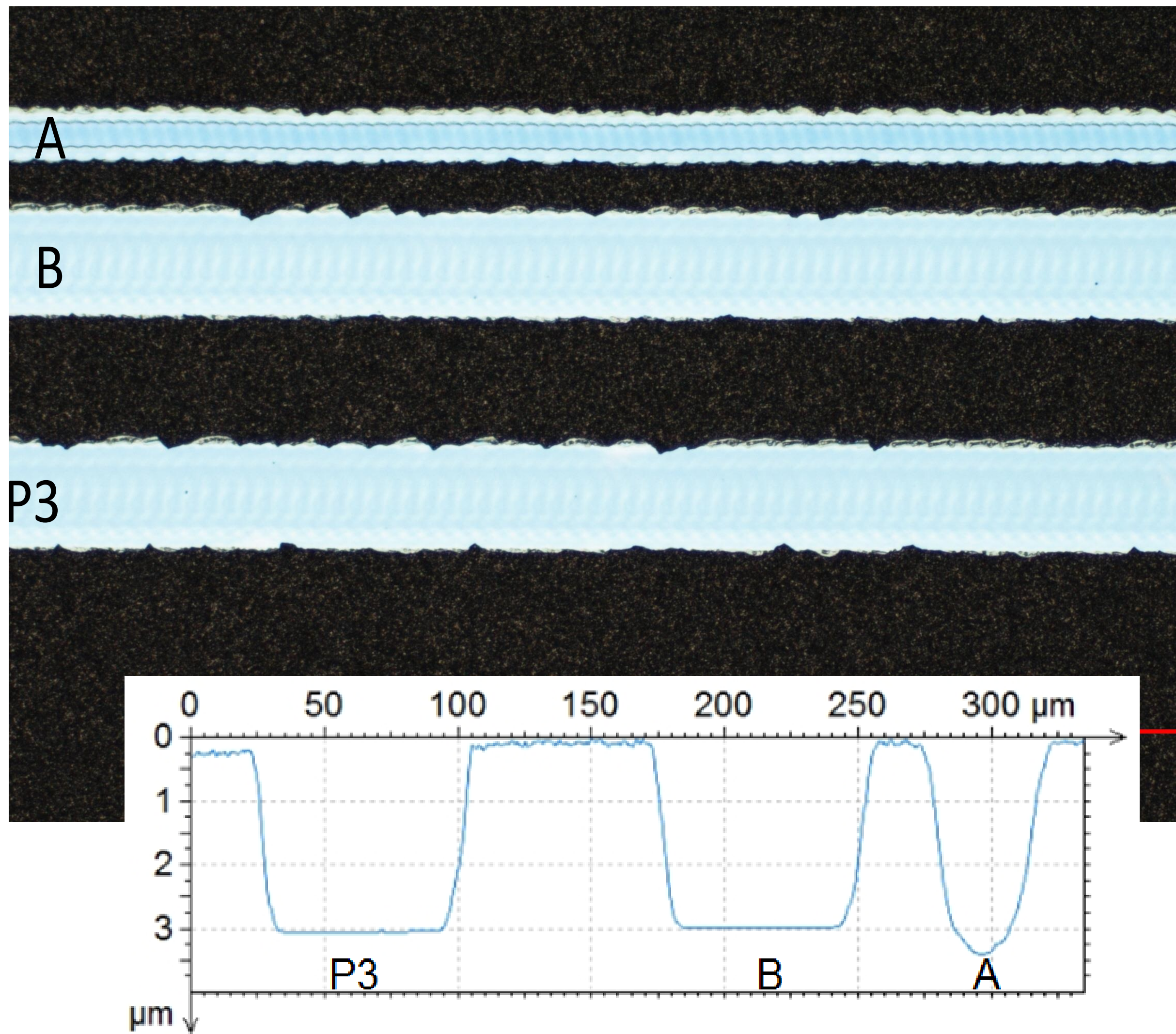
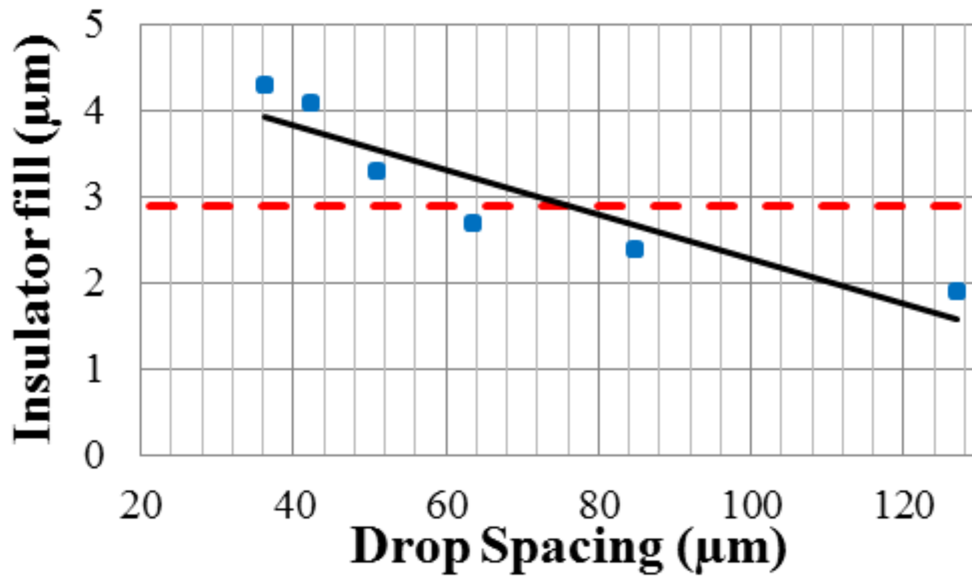


Figure 4A and 4B

The A scribe is filled with an insulative material to stop the conductive ink from shunting the cell. The level of fill and the associated morphology of the printed track are important for a robust interconnect. The fill level is measured and plotted for different inkjet drop pitches. Figure 5A shows a plot of fill depth against printed drop pitch for a typical A scribe and Figure 5B shows a SWLI plot of the filled scribe.



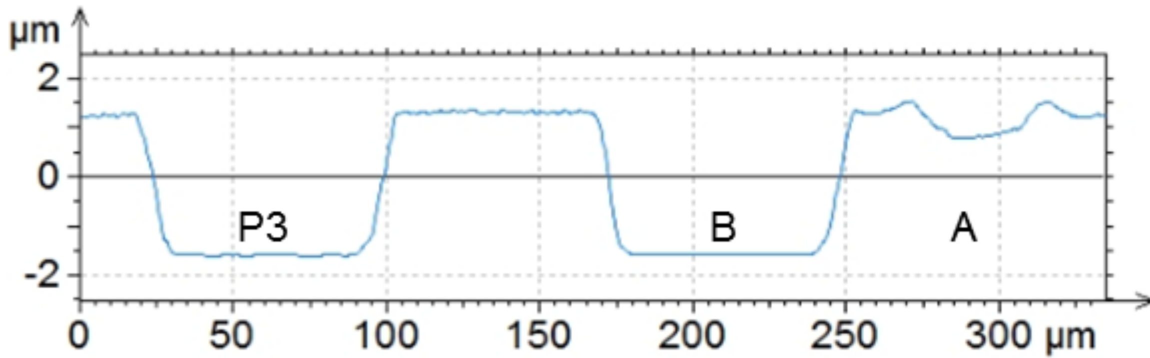


Figure 5A and 5B

After insulator deposition and UV cure, a second print head follows and deposits the conductive bridge. Figure 6A shows an optical micrograph of the CdTe cells after the deposition of a silver nanoparticle ink and post-deposition sintering for 15 minutes at 250°C. Figure 6B shows the accompanying SWLI plot.

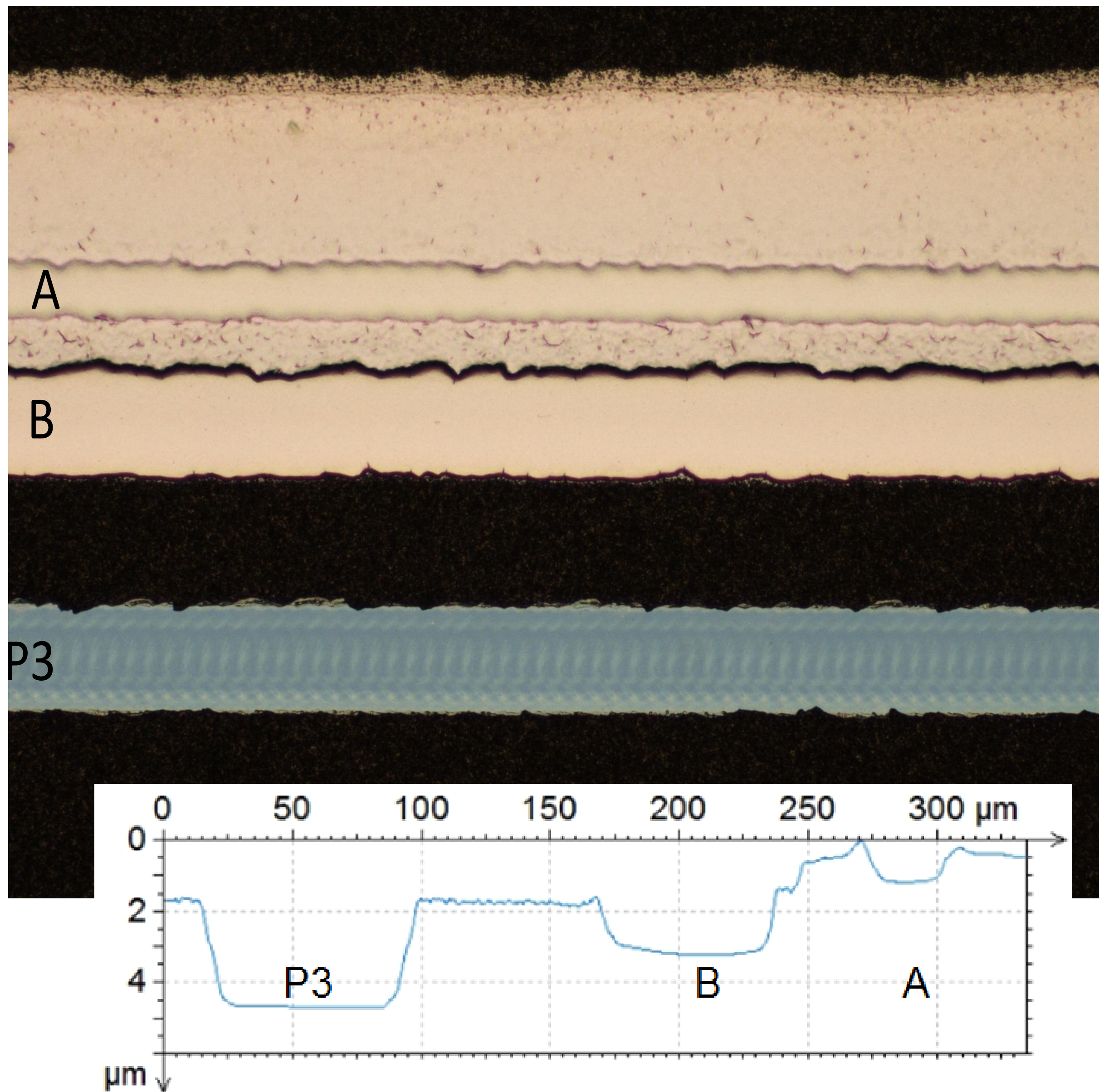
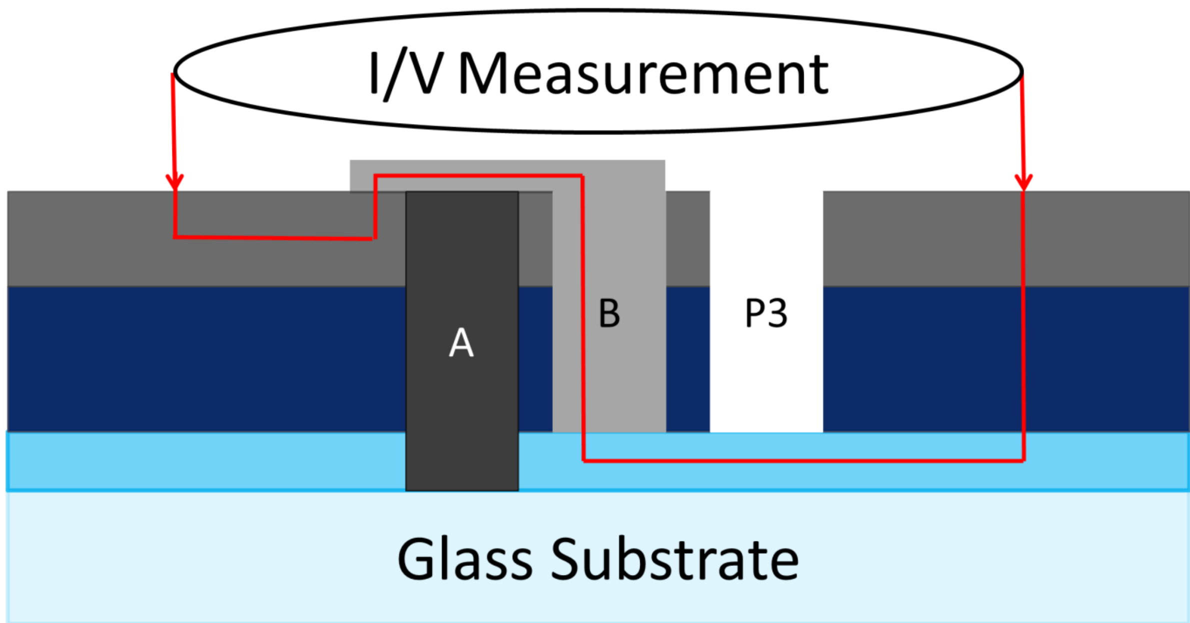


Figure 6A and 6B

4.0 Results

Eleven cells, each of cell pitch of 0.5cm and area 0.74cm^2, were manufactured on the CSU CdTe material. I/V data was collected by connecting directly to the back contact of the cell to be tested and using the back contact of the adjacent cell and the interconnect to access the front contact, see Figure 7. Each electrical measurement is a combination of both the cell and the interconnect in series. The Fill Factor (FF) is the figure of merit when assessing interconnect quality since it is sensitive to any shunts or areas of high series resistance that could be introduced. Figure 7 shows a connection schematic and equivalent circuit diagram of the OSI measurements. The solar cell is represented by the diode with R_{CSh} and R_{CSer} representing the intrinsic cell shunt and series resistances. The interconnect has the potential to introduce extra shunt and series resistances represented by R_{ISh} and R_{ISer}.



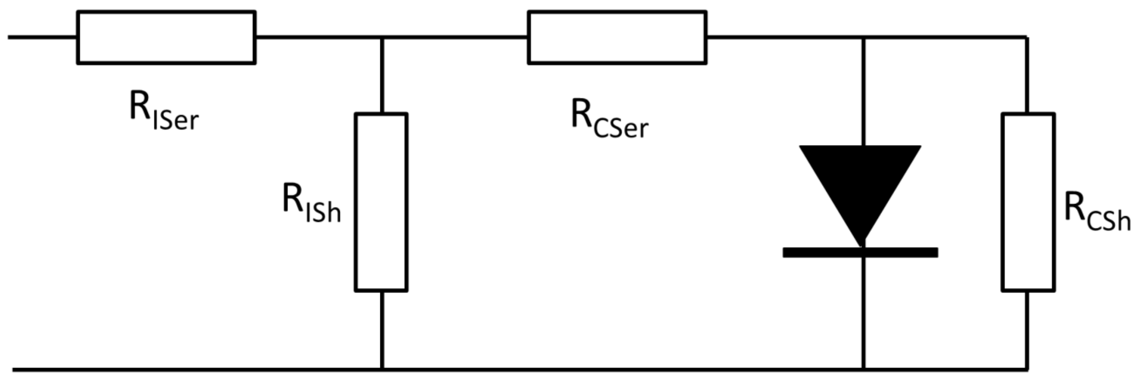


Figure 7A and B

	Best cell	Average (11 cells)	Standard deviation
Voc (V)	0.75	0.74	0.01
Jsc (mA/cm2)	21.55	21.62	0.35
FF (%)	62.64	61.07	1.65
Efficiency (%)	10.18	9.91	0.40

Table 1

A summary of the electrical performance of these eleven OSI cells can be seen in Table 1. The measured electrical characteristics are in agreement with the expectations for this particular material. A further test of interconnect performance is the interconnection of multiple cells into strings. Poor interconnects would cause degradation of fill factor as more cells are added in series. The 11 cells were made in two strings one of 5 cells and a second of 6 cells. Each string can be probed anywhere along its length from single cells to the entire string. As an example the I/V curve of one, three and six cells connected in series can be seen in Figure 7. The electrical characteristics of the six cell string are open circuit voltage (Voc) = 4.45V, short circuit current density (Jsc) = 21.7mA/cm², fill factor (FF) = 60.5% and efficiency (η) = 9.7%, again well in line with material expectations and having a FF within 1 standard deviation of the average value of the constituent single cells, FF = 61.07± 1.65%.

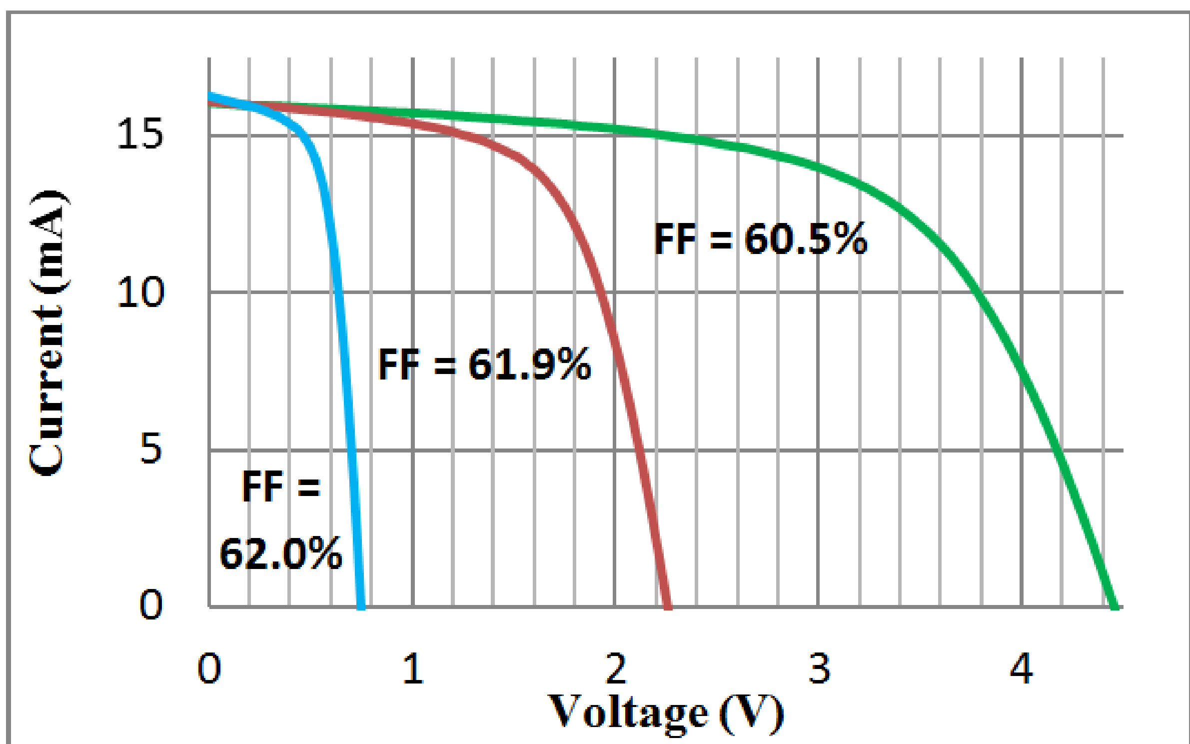


Figure 8

4.1 Cost of Ownership

An important consideration when introducing any new manufacturing technology is the cost of ownership of the required tooling. Cost of ownership for both the OSI process and the all laser P1, P2, P3 process has been modelled. The model assumes capital depreciation over a 7 year period, a modest cell power conversion efficiency of 12.7% and similar levels of beam multiplexing in both traditional laser scribers and OSI tools. Using these assumptions it is calculated that a single OSI tool is capable of producing approximately 50MW per year or approximately 580,000 panels per year with a panel handling time of ~50s including load/unload cycles. In this example the OSI process is around 25% less expensive than the

incumbent process including the extra cost of consumable: inks, printheads and UV cure equipment. In addition to this significant saving OSI allows the removal of extra equipment such as heaters/load locks, reduced process energy usage. The real benefits of OSI are even greater. Figure 9 shows a comparison of the cost of the standard and OSI processes.

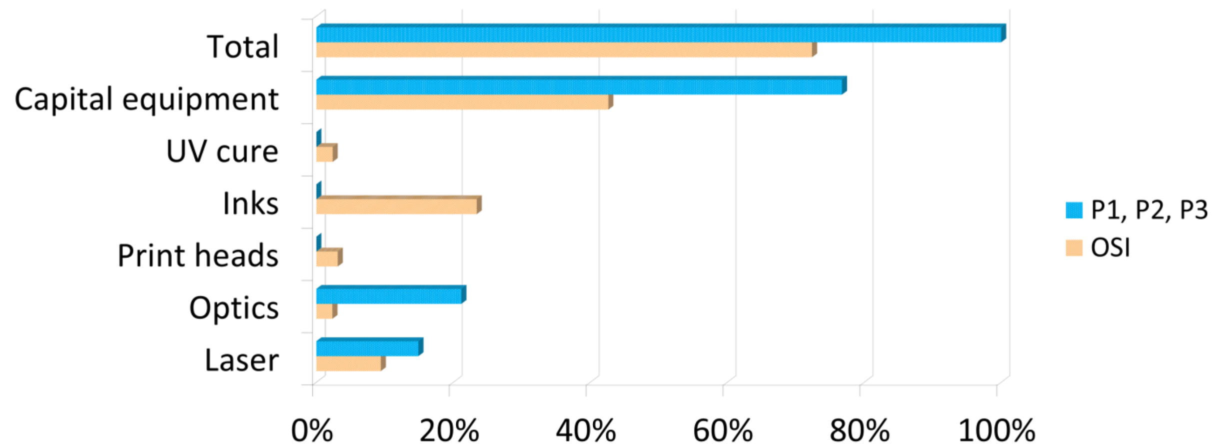


Figure 9

5.0 Conclusion

Inkjet is an enabling technology for novel processes in large area electronics. The OSI process is one such hybrid process combining both laser and inkjet. OSI has many benefits over the standard method of series interconnecting thin-film solar cells including lower capital equipment cost and footprint, improved material interface quality and less dead material per panel. OSI has been successfully demonstrated on CdTe but is applicable to all types of TF-PV including amorphous silicon (a-Si), copper indium gallium (di)selenide (CIGS), copper zinc tin sulphide (CZTS), OPV, solid state dye sensitised cells (DSC) and perovskite cells. OSI is estimated to be 25% lower cost than the P1, P2, P3 process, is fully scalable and production ready.

6.0 Acknowledgements

Our PV activities have been supported by our colleagues at Colorado State University, USA who supplied the CdTe PV cells. We gratefully acknowledge financial support for the activities described above by the UK Technology Strategy Board and the EPSRC.

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7.0 Captions

Figure 1 electrode structure laser scribed into an Indium doped Tin Oxide (ITO) transparent conductor and an inkjet printed silver busbar.

Figure 2 the current, sequential, process for the monolithic series interconnection of thin-film PV. Each scribe, P1, P2 and P3, is performed after the deposition of a device layer, font contact, absorber, back contact.

Figure 3 the OSI process for the series interconnection of thin-film PV using lasers and inkjet. A single process head completes three, depth selective laser scribes and deposits both insulating and conductive inks to form a complete interconnect in a single pass after the deposition of all layers.

Figure 4A an optical micrograph of the OSI laser process, scribes A, B and P3 on CdTe. 4B a Scanning White Light Interferometer (SWLI) plot of the same scribes.

Figure 5A a plot of insulator fill depth in the A scribe against inkjet drop pitch. The top surface of the cell is marked by the dotted line. Figure 5B an SWLI plot of the filled scribe

Figure 6A an optical micrograph of the complete OSI interconnect and Figure 6B an SWLI plot of the same interconnect.

Figure 7A a schematic of the electrical connection used to test individual cells, direct contact is made with the back contact, the front contact is accessed through the interconnect. Figure 7B an equivalent circuit diagram of the interconnect plus cell measurement. The cell is represented by the diode and the intrinsic cell shunt and series resistance, R_{CSh} and R_{CSer}. The interconnect can introduce extra shunt and series resistances represented by R_{ISh} and R_{ISer}.

Table 1 electrical performance of OSI interconnected CdTe cells.

Figure 8 the I/V measurement of an OSI interconnected single cell, 3 cell string and 6 cell string.

Figure 9 a cost comparison of the standard interconnect and the OSI process. The relative cost of OSI is ~25% lower than that of the equivalent all laser process even after taking into account the extra cost of consumables.