

SUBSTRATE-DEPENDENT HIGH-FIELD TRANSPORT AND
SELF-HEATING IN GRAPHENE TRANSISTORS

BY

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DISSERTATION

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ABSTRACT

Over the last decade graphene has attracted much interest for nanoelectronic applications due to its high and symmetrical carrier mobility, and high drift velocity compared to silicon. However, when graphene is placed on insulating substrates such as SiO₂ or flexible plastics, its inherent superior qualities get suppressed by the influence of the underlying substrate. Interfaces and substrate material properties have a significant impact on graphene based nano-scale devices due to the reduced dimensions and large surface-to-volume ratio.

Motivated by this issue, in this work we have investigated the substrate dependence of the electrical and thermal transport in graphene field-effect transistors (GFETs). We developed a simple yet practical electro-thermal model along with extensive calibration with experimental data. Special emphasis is given to the study of high-field transport and investigation of temperature-induced effects on device performance.

First, we have used this electro-thermal model to examine the scaling effect of the supporting insulator (e.g. SiO₂, BN) thickness on temperature maximum (hot spot) formation. Our findings showed average and maximum temperatures of GFETs scale differently due to competing electrostatic and heat sinking effects. Self-heating in GFETs causes current degradation (up to ~10-20%) in micron-sized devices on SiO₂/Si but is reduced if the supporting insulator thickness is scaled down. The transient behavior of such FETs has thermal time constants in the range of 50-250 ns, dominated by the thickness of the supporting insulator and that of device capping layers. Self-heating is also reduced in shorter channel devices, due to partial heat sinking at the contacts.

Next, we investigate the effect of different supporting dielectrics such as hexagonal boron nitride (h-BN), HfO₂ and SiO₂ on the velocity saturation of GFETs. We examine the effects from

different substrates as they each present a unique scenario due to their different (remote) phonons and thermal conductivities, all of which influence high-field transport in GFETs. Additionally, we studied the origins of the poor current saturation in short-channel GFETs in detail. We study and compare the temperature profiles generated in GFETs on different insulating materials for bottom oxide and substrate through full thermal finite element method (FEM). Materials with anisotropic thermal conductivity showed significant impact in heat spreading and temperature rise in the hot-spot. We apply our findings to add a guideline for the maximum “safe” power density, e.g. in GFETs on flexible substrates such as polyimide (PI), without inducing thermal deformation; the maximum is found to be $\sim 1.8 \text{ mW}/\mu\text{m}^2$ (with 200 nm BN dielectric).

Finally, we also develop a physics-based compact model based on existing literature, for GFETs with well calibration against experimental data and other finite element models. This model has been implemented into a circuit simulator like Verilog-A with a minimum number of iterations for channel potential calculation.

These results shed important physical insight into the high-field and thermal profile of graphene transistors. Moreover, the electro-thermal model and results presented in this dissertation can be extended for analysis of other 2D materials beyond graphene.

*To my mother, for the sacrifices she made to provide a better life
for us, and my father, from whom I learned to dream big.*

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Chapter 1

INTRODUCTION

Semiconductor technology over last 40 years has achieved a 1000-fold increase in integrated circuit density, with minimum feature size down to 22 nm [1]. This scaling trend of semiconductor devices has followed rules described by Gordon Moore at Intel [2], which stated that the number of transistors in advanced integrated circuits would double approximately every two years [3-5]. To extend Moore's law even beyond 14 nm, a complex combination of advanced imaging, computation, patterning and inverse lithography methods is being adopted [6]. But this aggressive device downscaling may face a roadblock due to the physical silicon crystalline structure. Hence, besides the coordinated miniaturization following Moore's law, the International Semiconductor Roadmap for Semiconductors (ITRS) also considered adding functional diversification through different geometric structures, alternative channel materials etc., a trend known as 'More than Moore'.

It is also important that as we down-scale the device dimensions, we make sure that the short-channel effects, off-state leakage current, etc., are not degrading device performance. To achieve that, the most prominent examples of novel device structures are multiple gate field-effect transistors (FinFETs) [7], ultra-thin body silicon-on-insulator (UTBSOI) [8], and gate-all-around transistors, all of which are schematically shown in Fig. 1.1; these structures take advantage of improved electrostatics in order to continue transistor scaling. However, at nanoscale dimensions, material properties such as surface roughness and dangling bonds arise even with advanced geometries [9-11]. These problems have motivated the semiconductor community to investigate

the use of atomically thin 2D channel materials, such as graphene, which present the opportunity for ideal electrostatics and the ultimate ultra-thin body FET [12, 13].

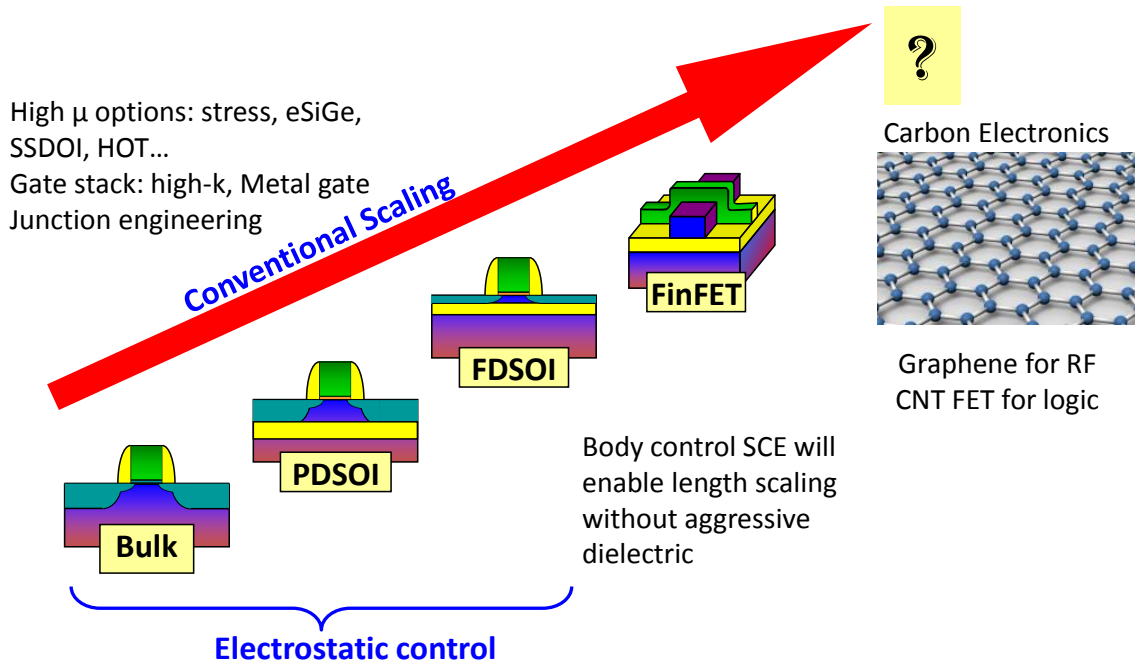


Figure 1.1: Silicon based device evolution and future trend. Figure concept adapted from [14].

1.1 Graphene

Crystal Structure

A whole new era in the semiconductor research community began with the experimental breakthrough of graphene in 2004 [15]. The researchers from the University of Manchester reported the preparation of graphene by mechanical exfoliation and observed the field effect and high carrier mobilities in their samples. Around the same time, a group from Georgia Institute of Technology also reported field effect in their graphene sample prepared from sublimation of Si from SiC surfaces [16]. Since its discovery, graphene has attracted considerable attention in the device community, due to the combination of many unique physical and electrical properties [17,

18], with the added benefit of a rather straightforward method for preparing and transferring graphene samples. Graphene is a planar sheet of sp^2 bonded carbon atoms, which is one atom

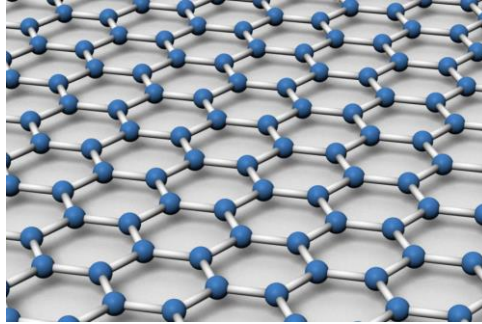


Figure 1.2: The atomic structure of graphene. Carbon atoms are arranged in a 2D honeycomb lattice (image courtesy of 3dprint.com).

thick and arranged in a honeycomb crystal lattice, as shown in Fig. 1.2. It is the fundamental building block of graphitic materials, and thus is important in determining the electronic properties of other carbon allotropes such as graphite, carbon nanotubes and fullerenes. In the hexagonal structure of graphene each carbon atom is bonded to its nearest neighbor by a strong covalent sp^2 bond. This sp^2 bond is the combined form of $2s$, $2p_x$ and $2p_y$ and this hybridization leads to the formation of the σ bonds. These chemical bonds form an angle of 120° between them and are accountable for the hexagonal lattice structure of graphene. The chemical bonding of the carbon atoms in graphene is maintained by these three orbitals, and the mechanical properties of graphene are determined by the rigidity of the bond. The remaining p_z orbital is perpendicular to the plane and creates a hybridized form of π bonds, which are responsible for the unique electronic properties of graphene. The hexagonal lattice can be viewed as two interpenetrating triangular lattices, each containing one set of equivalent carbon atom sites [19].

Band Structure

Figure 1.3(b) shows the band structure of semimetal graphene where valence and conduction bands just touch at discrete points in the Brillouin zone. The energy momentum dispersion relation becomes linear in the vicinity of those points, with the dispersion described by the rela-

tivistic energy equation, $E = |\hbar\mathbf{k}|v_F$, where $v_F \sim 10^8$ cm s⁻¹ is Fermi velocity, $\hbar = h/(2\pi)$ is the reduced Planck constant and $|\mathbf{k}| = \sqrt{k_x^2 + k_y^2}$ is the wave vector of carriers in the two-dimensional (2D) (x,y) plane of the graphene sheet. The point $|\mathbf{k}| = 0$, referred to as the “Dirac point,” is a convenient choice for the reference of energy. Each \mathbf{k} point is two-fold spin degenerate ($g_s = 2$),

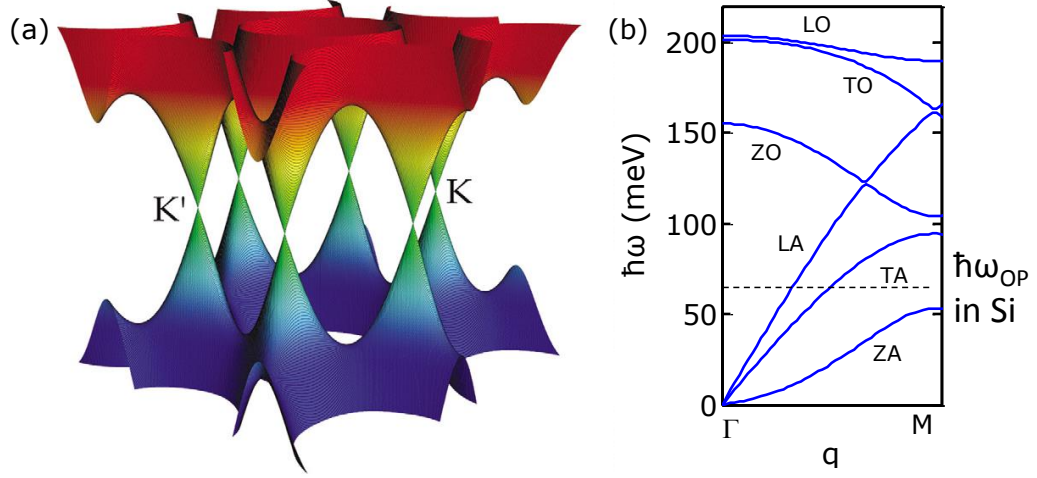


Figure 1.3: (a) Band structure of graphene. The conduction band touches the valence band at the K and K' points [20]. (b) Phonon dispersions for monolayer graphene (image courtesy Andrey Serov).

and there are two valleys in the first BZ, the K and K' valleys, $g_v = 2$ [20]. To find the 2D sheet density of such intrinsic carriers in graphene, the linear density of states (DOS) [21] is:

$$\rho_{gr}(E) = \frac{g_s g_v}{2\pi(\hbar v_F)^2} |E| \quad (1)$$

Unlike in typical semiconductors like Si, Ge, or GaAs where mobilities are asymmetric for electrons and holes, graphene shows symmetric mobilities, which originate from the symmetry of the conduction and valence bands around the Dirac point.

Graphene Properties

Large-area graphene is a semimetal with zero band gap, making it unsuitable for logic applications. However, it is possible to open a band gap in graphene by patterning a single layer

of graphene into nanoribbons. This band gap opens up due to the quantization of the width direction, which is beyond the scope of this study. Analog circuits, on the other hand, are typically based on “ON” current and the $I_{\text{ON}}/I_{\text{OFF}}$ ratio and off-state leakage are less important metrics. Undoubtedly, the one feature that has created the most excitement surrounding graphene electronics is the high carrier velocity. Also high low-field carrier mobility ($\sim 10^4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) [18] and good current density [22] can be utilized in analog applications and interconnects. At room temperature, mobility exceeding $100,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ has been observed for suspended graphene [23]. Recent work has also found drift velocity saturation at high field in graphene, at values several times higher than in silicon [24]. However, velocity saturation alone does not directly lead to current saturation, which is difficult to achieve in a zero band gap material where the channel cannot be fully pinched off. Current saturation is important for low output conductance and amplifier gain [18, 25] and in practice it has been partly achieved through some combination of velocity saturation and electrostatic charge control [26, 27]. In addition, high-field transport is also influenced by self-heating [24, 28], as revealed by recent thermal infrared imaging of graphene transistors [29, 30]. Therefore, to understand the performance of graphene devices, it is necessary and important to include both electrical and thermal effects via a self-consistent scheme in simulations.

Besides the superior electrical transport properties, graphene also shows great mechanical strength, flexibility, optical transparency and thermal conductivity. The phonon dispersion of graphene, shown in Fig. 1.3(b), gives us an idea of the thermal dispersion of graphene. Phonons for single-layer graphene have six branches corresponding to two atoms in the elementary cell: three optical modes (transverse TO, longitudinal LO and flexural ZO) and three acoustic modes (transverse TA, longitudinal LA, and flexural ZA). The TA and LA have high sound velocity,

which leads to strong contribution to thermal conductivity. For suspended graphene, flexural ZA mode has a high contribution to the thermal conductivity with its higher density of states [31]. Thermal conductivity for suspended graphene could exceed $2000 \text{ Wm}^{-1}\text{K}^{-1}$, where on supported samples it is $\sim 600 \text{ Wm}^{-1}\text{K}^{-1}$ [32]. This degradation is occurring as ZA modes are suppressed by the interaction with the substrate [32, 33]. Also due to this relatively high energy of optical ($\hbar\omega_{OP} = 200 \text{ meV}$) and intervalley acoustic phonons ($\hbar\omega_{OP} = 140 \text{ meV}$), high low-field mobility in suspended graphene can be explained [34].

Graphene's bendability can be used in flexible electronic applications, whereas the 98% transparency is ideal for transparent electronics. In Chapter 6 we analyze the GFETs on flexible electronics and the effect of temperature on them. Graphene is shown to be the strongest material ever measured [35]. Graphene is also chemically stable even when the oxygen environment up to few hundred degrees Celsius [36]. The strong sp^2 carbon lattice that lacks dangling bonds on the surface of the crystal is the reason for this stability.

In conclusion, despite the fact that there are many properties of graphene that could make it an ideal FET channel material, the absence of a band gap makes it unsuitable for conventional digital transistors because of low on/off ratios.

1.2 Review of Graphene FET Models

Right after graphene was experimentally discovered in 2004, full-quantum models like Tight-Binding (TB) [37] and Density-Functional Theory (DFT) [38] calculations were the first tools used for the investigation of its properties. However, the computational cost limits its application to extremely small volume. Most experiments on graphene conductivity properties were done on GFET) devices with gate length ranging from hundreds of nanometers up to several microns. These ranges of dimensions are called large-area graphene because the main

electronic transport mechanism is drift-diffusion rather than ballistic transport [24, 39]. This leads to semi-classical modeling to be a more appropriate tool for the analysis for GFETs [40-43]. Few semi-empirical models [44],[45] for semiconductors were adapted to graphene [41, 46]. A model combining ballistic and diffusive transport has also been reported [47]. Large-area short-channel graphene has also been simulated, although in the ballistic transport limit [48]. Although all these models are based upon the drift-diffusion transport equations, they can be categorized from semi-analytical to purely analytical approaches. The extensive experimental data enables the validation of these models. In semi-analytical approach, the channel length dimension is discretized in a vector of points; channel potential and the quantum capacitance effects are then iteratively evaluated for each point. The resultant electric-fields and current are calculated from resulting potential profile using the drift-diffusion transport equation [18, 41, 42]. Purely analytical models avoid any iterative method and are benchmarked extensively against measurements [49-51]. More discussion of closed expression compact model for graphene transistors is presented in Chapter 7, along with state-of-the-art circuit implementations. Their accuracy together with the small computational load makes those models suitable for compact modeling in circuit simulators.

In this work, we study the large-area graphene transistors and the aim is to model single-layer graphene devices, whereas few-layer graphene devices and graphene nanoribbons will be considered as out of scope.

1.3 Electro-Thermal Model

Our model calculates the charge densities, field, potential and temperature along the graphene channel in a self-consistent approach [24, 52]. Both mobility model and velocity

saturation model implemented here include dependencies on carrier density and temperature, from Ref. [24].

Charge Density Model

To obtain a reasonable mobility and output current we include the gate induced carrier (n_{cv}), thermally generated carrier (n_{th}), and residual puddle charge (n^*) densities into our carrier density calculation. The gate-induced charges are incorporated with a charge balance equation $n_{cv} = p - n = C_{ox}V_G/q$, where $C_{ox} = \epsilon_{ox}/t_{ox}$, is the capacitance of a SiO₂ layer, V_G is the back-gate voltage and q is the elementary charge. To account for the thermally generated carriers, we use $n_{th} = (\pi/6)(k_B T_0/\hbar v_F)^2$ [21] for a monolayer graphene, where k_B is the Boltzmann constant, \hbar is the Planck constant and T_0 ($= 293$ K) is the base temperature. The puddle charges originating from charged impurities in the SiO₂ create inhomogeneous charges, resulting in a potential landscape with respect to moving carriers in the graphene channel [53]. Next, we define an average Fermi level E_F such that $\eta = E_F/k_B T$, leading to the mass-action law [54]:

$$pn = n_{th}^2 \frac{\mathfrak{F}_1(\eta) \mathfrak{F}_1(-\eta)}{\mathfrak{F}_1^2(0)} \quad (2)$$

where $\mathfrak{F}_1(\eta)$ is the Fermi-Dirac integral ($\mathfrak{F}_j(\eta)$ with $j = 1$ and $\eta = E_F/k_B T$), $\mathfrak{F}_1(0) = \pi^2/12$ and n_{th}^2 as mentioned above. Combining the charge balance equation with Eq. (2), we obtain a quadratic equation (e.g. for the hole density), whose solution is:

$$p = \frac{1}{2} \left[N - \frac{C_{ox}}{q} V_G + \sqrt{\left(N - \frac{C_{ox}}{q} V_G \right)^2 + 4n_i^2 \frac{\mathfrak{F}_1(\eta) \mathfrak{F}_1(-\eta)}{\mathfrak{F}_1^2(0)}} \right] \quad (3)$$

It is not possible to obtain an explicit expression for the total carrier density by averaging Eq. (3) and the charge balance equation; the expression must be determined numerically. In order to simplify this, we note that at low charge density ($\eta \rightarrow 0$) the factor $\mathfrak{F}_j(\eta) \mathfrak{F}_j(-\eta)/\mathfrak{F}_j^2(0)$ in Eq.

(2) approaches unity. Meanwhile, at large $|V_{G0}|$ and high carrier densities the gate-induced charge dominates, i.e. $n_{cv} \gg n_{th}$ when $\eta \gg 1$. Finally, we add a correction for the spatial charge inhomogeneity discussed above, resulting in a minimum carrier density of $n_0 = [(n^*/2)^2 + n_{th}^2]^{1/2}$. Consequently, solving the above equations with the approximations given here results in an explicit expression for the concentration of electrons and holes:

$$n, p \approx \frac{1}{2} \left[\pm n_{cv} + \sqrt{n_{cv}^2 + 4n_0^2} \right] \quad (4)$$

Our finite element grid along the GFET is $x = 0$ to L ; 0 (L) being the left (right) edge of the graphene channel. We use the current continuity condition of $I_D = \text{sgn}(p_x - n_x)qW(p_x + n_x)v_{dx}$, where the subscript x refers to a position along the channel x -axis, v_d is the drift velocity and W is the width of the graphene channel. A schematic for typical back-gated graphene transistor is shown in Fig 1.4(a) assuming length: $L = 10 \mu\text{m}$, width, $W = 2 \mu\text{m}$ and on SiO_2 insulating layer thickness $t_{ox} = 90 \text{ nm}$, contacted by two metal electrodes at the ends of the graphene sheet. Figure 1.4(b) shows the calculated densities p , n and $p+n$ as a function of V_{GD} with $t_{ox}=90 \text{ nm}$, based on Eq. (9). The thermally excited carrier density is $n_{th} \approx 8 \times 10^{10} \text{ cm}^{-2}$ at room temperature and the puddle density is assumed to be $n^* = 1.5 \times 10^{11} \text{ cm}^{-2}$, resulting in the intrinsic carrier density of $n_0 \approx 2.3 \times 10^{11} \text{ cm}^{-2}$.

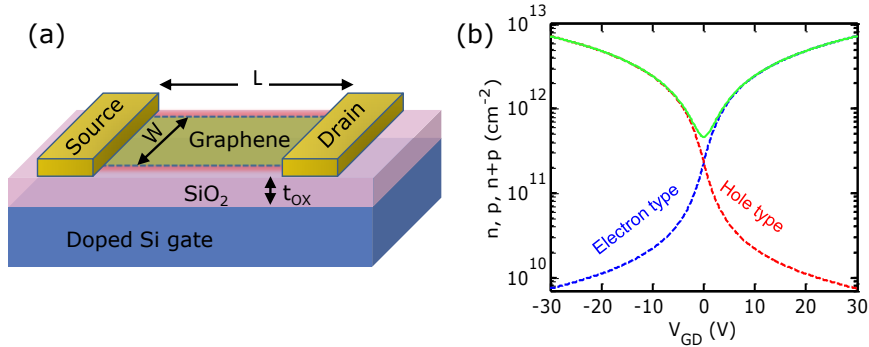


Figure 1.4: (a) Schematic of a back-gated graphene transistor, (b) carrier densities as a function of back-gate voltage.

Thermal Model

As the main objective of this thesis is to explore high-field transport of graphene, we must include a thermal model to analyze the supported-graphene device structure. We estimate the average device temperature due to self-heating via the thermal resistance network, as shown in Fig. 1.5(a),

$$\Delta T = T - T_0 = P(\mathcal{R}_B + \mathcal{R}_{ox} + \mathcal{R}_{Si}) \quad (5)$$

where $P = IV$, $\mathcal{R}_B = 1/(hA)$, $\mathcal{R}_{ox} = t_{ox}/(\kappa_{ox}A)$, and $\mathcal{R}_{Si} \approx 1/(2\kappa_{Si}A^{1/2})$ with $A = LW$ the area of the channel, bottom oxide thickness t_{ox} (300 nm and 90 nm considered for the following calculations), $h \approx 10^8 \text{ Wm}^{-2}\text{K}^{-1}$ the thermal conductance of the graphene-SiO₂ boundary [55], κ_{ox} and κ_{Si} the thermal conductivities of SiO₂ and the doped Si wafer, respectively. At 300 K for our geometry $\mathcal{R}_{th} \approx 10^4 \text{ K/W}$, or $\sim 2.8 \times 10^{-7} \text{ m}^2\text{K/W}$ per unit of device area, where \mathcal{R}_{th} is simply the total thermal resistance calculated by summing the individual thermal resistance components in series. The thermal resistance of the 300 nm SiO₂ (\mathcal{R}_{ox}) accounts for $\sim 84\%$ of the total thermal resistance, while the value would be 71% if $t_{ox} = 90 \text{ nm}$. The spreading thermal resistance into the Si wafer (\mathcal{R}_{Si}) and the thermal resistance of the graphene-SiO₂ boundary (\mathcal{R}_B) account for only $\sim 12\%$ and $\sim 4\%$, respectively (for 90 nm SiO₂ 19% and 10% respectively). So a device on a thinner oxide has more pronounced roles of \mathcal{R}_{Si} and \mathcal{R}_B . The thermal model in Eq. (5) can be used when the sample dimensions are much greater than the SiO₂ thickness ($W, L \gg t_{ox}$) but much less than the Si wafer thickness [56].

Based on above thermal model, the temperature of the graphene device is determined by solving the 1D heat equation of a graphene sheet [52]:

$$A \frac{\partial}{\partial x} \left(k \frac{\partial T_x}{\partial x} \right) + P_x - g(T_x - T_0) = 0 \quad (6)$$

This expression is self-consistently solved along with the electrical transport model, allowing us to understand the Joule-heating effect in graphene based transistors. Figure 1.5(b) shows an $I_{SD} - V_{SD}$ curve at $V_{GD} = 0$ V calculated by our electro-thermal, and at $V_{SD}=10$ V, 7 V and 3V the temperature profiles along the channel are shown.

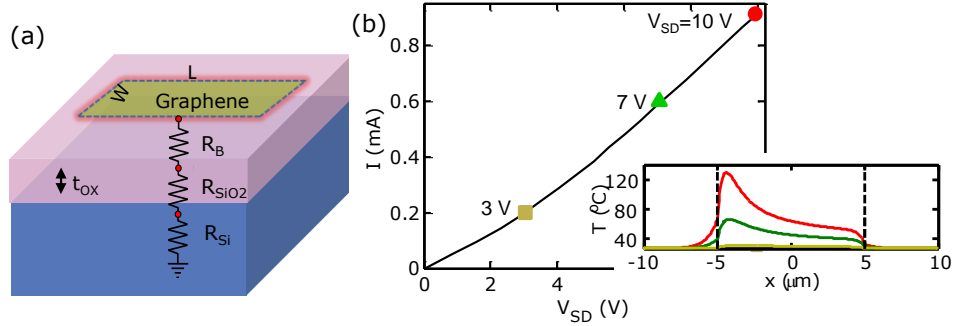


Figure 1.5: (a) Thermal series resistance network. (b) $I_{SD} - V_{SD}$ curves at $V_{GD} = 0$ V; inset shows the temperature rise along the channel at $V_{SD}=10$ V, 7 V and 3V.

Low-Field Mobility and Saturation Velocity

The drift velocity is determined by the mobility and electric field, where we use an empirical model for mobility:

$$\mu(n, T) = \frac{\mu_0}{1 + (n/n_{ref})^\alpha} \times \frac{1}{1 + (T/T_{ref} - 1)^\beta} \quad (7)$$

Here μ_0 is the low-field mobility; n_{ref} , T_{ref} , α and β are implemented as fitting parameters. As an example of typical values of these fitting parameters, $\mu_0 = 4650 \text{ cm}^2/\text{V s}$, $n_{ref} = 1.1 \times 10^{13} \text{ cm}^{-2}$, $T_{ref} = 300 \text{ K}$, $\alpha = 2.2$ and $\beta = 3$ were used to fit the data from Ref. [24].

The electric field is calculated by:

$$F = \frac{v_d}{\mu \left[1 - (v_d / v_{sat})^\gamma \right]^{\frac{1}{\gamma}}} \quad (8)$$

where $\gamma = 2$, which agrees with a previous study [27].

We model the saturation velocity (v_{sat}) based on a steady state carrier distribution in which carriers occupy states up to an energy $\hbar\omega_{OP}$ higher than carriers moving against the net current [24, 57]:

$$v_{sat}(n, \omega_{OP}, T) = \frac{2}{\pi} \frac{\omega_{OP}}{\sqrt{\pi(n+p)}} \times \sqrt{1 - \frac{\omega_{OP}^2}{4\pi(n+p)v_F^2}} \frac{1}{N_{OP} + 1}, n + p > n^* \quad (9)$$

$$v_{sat}(\omega_{OP}, T) = \frac{2}{\pi} \frac{v_F}{N_{OP} + 1}, n + p < n^* \quad (10)$$

where $n^* = (\omega_{OP}/v_F)^2/2\pi$ is the minimum carrier density to observe constant v_{sat} and $N_{OP} = 1/[\exp(\hbar\omega_{OP}/k_B T) - 1]$ is the phonon occupation. This model has been calibrated with experimental data, considering optical phonons (OP) as a fitting parameter. In Ref [24], the optimized effective phonon energy of $\hbar\omega_{OP}$ was 82 meV, which lies between SiO₂ substrate ($\hbar\omega_{OP} = 55$ meV [58]) and graphene ($\hbar\omega_{OP} = 160$ meV [59]). This model assumes v_{sat} is limited by inelastic emission of OP and approximates the high-field distribution with the two half-disks model [57]. We provide a reminder that this model is most likely an oversimplification of the electron distribution in the high-field regime for graphene transistors. It should be viewed as an empirical equation for a simple “streaming” model for v_{sat} . However, numerous devices fabricated within the research group as well as other collaborations have shown excellent fit if calibrated to experimentally extracted values.

Metal Contact Resistance

The contact resistance between the graphene and the metal is determined by the sheet resistivity of the graphene underneath metal as well as the contact resistivity. The total device resistance R includes:

$$R = \left(\frac{L}{W}\right) R_{sh} + 2R_C + R_{series} \quad (11)$$

where R_{sh} is the sheet resistance of the graphene and R_{series} is the total series resistance of metal wires contacting the device. We include contact resistance (R_C) into our model by [60]:

$$R_C = 2 \frac{\sqrt{R_{sh}\rho_c}}{W} \coth(L_c/L_T) + R_{lead} \quad (12)$$

where L_c is the length of the contact, ρ_c the contact resistivity and R_{lead} the resistance of the metal leads. Current crowding occurs at the metal contact region in the graphene over a certain length known as the transfer length $L_T = (\rho_c/R_{sh})^{1/2}$. As the graphene sheet resistance R_{sh} varies with V_{G0} , and from Eq. (12), we see that contact resistance is a function of R_{sh} , and R_C has a dependence on the gate voltage as well. Transfer length measurements have suggested that ρ_c is independent of V_{G0} [61], while measurements using a three-terminal cross-bridge-Kelvin structure have suggested that ρ_c increases near the Dirac voltage due to the lower carrier density in the graphene under the metal contact [62]. Using this contact resistance model, with an assumption that the difference in resistance between two-terminal and four-terminal measurements is described by R_C , we extensively use this to extract ρ_c as a function of V_{G0} . We also note that for the extreme cases of $L_c > 1.5L_T$ and $L_c < 0.5L_T$, Eq. (12) can be simplified to $R_C \approx 2\rho_c/L_TW + R_{lead}$ and $R_C \approx 2\rho_c/L_cW + R_{lead}$ respectively. Since the Joule heating at the contact region is due to the current crowding in the L_T range from the edge of the metal on the graphene, the potential drop along the graphene-metal contact is defined by $V_x = (I_D/W) (R_{sh}\rho_c)^{1/2} \cosh(x/L_T)/\sinh(L_c/L_T)$ [60], where x is the horizontal distance from the graphene-metal edge, and the corresponding power for the Joule heat is $I_D(-dV_x/dx)$ per unit length (W/m).

Thermoelectric Effect

To capture the Joule heating at the contacts, thermoelectric effect needs to be integrated into the transport model. We implement a model of the Seebeck coefficient consistent with the transport model described above. Starting with the semi-classical Mott relationship [63]:

$$S = -\frac{\pi^2 k_B^2 T}{3|q|} \frac{1}{G} \frac{dG}{dV_g} \frac{dV_g}{dE_F} \quad (13)$$

where G is the conductance and we assume that $G = \frac{W}{L} q(n+p)\mu$. By solving $\frac{dG}{dV_g}$ and $\frac{dV_g}{dE}$,

then substituting in Eq. (13), we get:

$$S = -\frac{2\pi^{3/2} k_B^2 T}{3q\hbar v_F} \frac{(n-p)\sqrt{|n-p|}}{(n+p)^2} \quad (14)$$

The model is calibrated with existing experimental data of Ref. [64] for the Seebeck coefficient near room temperature in Fig. 1.6. In order to avoid the mismatch in the model and the data, we should use $T=0.7T_B$, as shown in Fig. 1.6. The mismatching in the case of $T = T_B$ could be because we neglected the change of the mobility, μ in a hole and electron doped region [65].

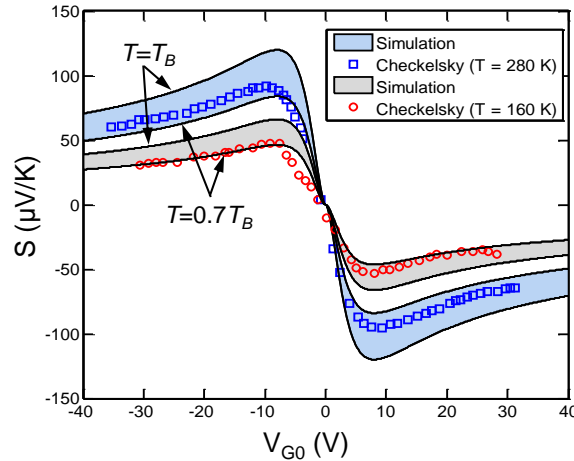


Figure 1.6: Seebeck coefficient as a function of back-gate voltage; comparing existing experimental data of Ref. [64] near room temperature. (Figure courtesy Feifei Lian.)

The weak localization effect due to the disorder or impurities [66] is also not added here, which results in repeatable conductance fluctuations as a function of V_{GD} . However, as the weak localization effect is only observable at a sufficiently low temperature region, our model can be acceptable for the higher temperature region before showing the weak localization effect. The simplified Eq. (13) without any parameter can be directly used to estimate the power generation due to the Peltier effect by using $P_{TE} = \pm WS_x T_x V_x / \rho_C$ per unit length (W/m), which can be either positive or negative dependence on the direction of current (+ for current into contact, - for current out).

Chapter 2

SCALING OF HIGHLY LOCALIZED HEATING IN GRAPHENE TRANSISTORS

The temperature maximum (hot spot) forms at the position of minimum charge density and maximum electric field along the GFET channel [29]. In ambipolar transport the CNP corresponds to the minimum charge density and the thermal hot spot marks the location of the CNP. Combining hot spot imaging with current measurements and simulations provides valuable information for understanding transport physics in GFETs. However, until now, the hot spot observed in GFETs has been quite broad ($>15\ \mu\text{m}$), making it challenging to fine-tune transport models or to understand the physical reason behind this broadening, e.g. imaging limitations, electrostatics, or simple heat diffusion. In addition, more precise spatial heating information is desirable to understand the long-term reliability of graphene electronics.

In this work we definitively elucidate the high-field hot spot formation in ambipolar GFETs, and find that the primary physics behind it are electrostatic in nature. Through infrared (IR) thermal imaging of functioning GFETs we show that more spatially confined (sharper) hot spots are formed in devices on thinner ($\sim 100\ \text{nm}$) SiO_2 layers vs. previous work [67-69] on 300 nm oxides. The device fabrication and infrared (IR) thermal imaging were done by Dr. Myung-Ho Bae and described in the Methods section in Ref [29]. The measured device current and temperature profiles are in excellent agreement with our simulations which include electrostatic, thermal, and velocity saturation effects. Once this model is calibrated, we then investigate the hot

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spot scaling with the SiO₂ substrate thickness over a wide range of practical values. Interestingly, we find that during ambipolar operation the *average* channel temperature scales with oxide thickness as expected, but the *peak* temperature is minimized at an oxide thickness of ~90 nm, due to competing electrostatic and thermal effects. The results provide novel insight into high-field transport and dissipation in graphene devices, and suggest that sharply peaked temperatures can have an impact on long-term device reliability [70, 71] and must be carefully considered in future device designs.

2.1 Ambipolar Transport in Graphene Transistors

Figure 2.1(a) displays measured graphene resistance (symbols) vs. back-gate voltage ($V_G \approx V_{GD} \approx V_{GS}$) at small $V_{SD} = 20$ mV. The peak resistance is at $V_{GD} = V_0 = 5.2$ V, also known as the Dirac voltage. V_0 corresponds to the Fermi level in the graphene sheet crossing the average Dirac point of the X-shaped electronic band structure [72] and to zero net charge density in the graphene channel ($n - p = 0$). Nevertheless, we note that zero *net* charge density does not imply a lack of free carriers, as there are equal numbers of electron and hole ‘puddles’ contributing to the non-zero conductivity at the Dirac point ($n = p \neq 0$). This puddle density is owed to charged impurities [73] in the SiO₂ and to thermally excited carriers [54] which form a non-homogeneous charge and potential landscape [24, 72] across the graphene device at the Dirac voltage. At higher (lower) gate voltages with respect to V_0 , the majority carriers become electrons (holes) respectively [24] and the charge inhomogeneity is smoothed out.

Based on an analytic electrostatic model explained in Chapter 1, we rigorously take into account the above phenomena [24], we fit the resistance data as shown by the dashed curve in Fig. 2.1a with a low-field mobility $\mu_0 = 3700$ cm²V⁻¹s⁻¹ and a puddle density $n_{pd} = 3.5 \times 10^{11}$ cm⁻². This fitting also considers the varying contact resistance as a function of gate voltage [70, 74,

75], including the role of the finite transfer length, L_T , the distance over which $1/e$ of the current

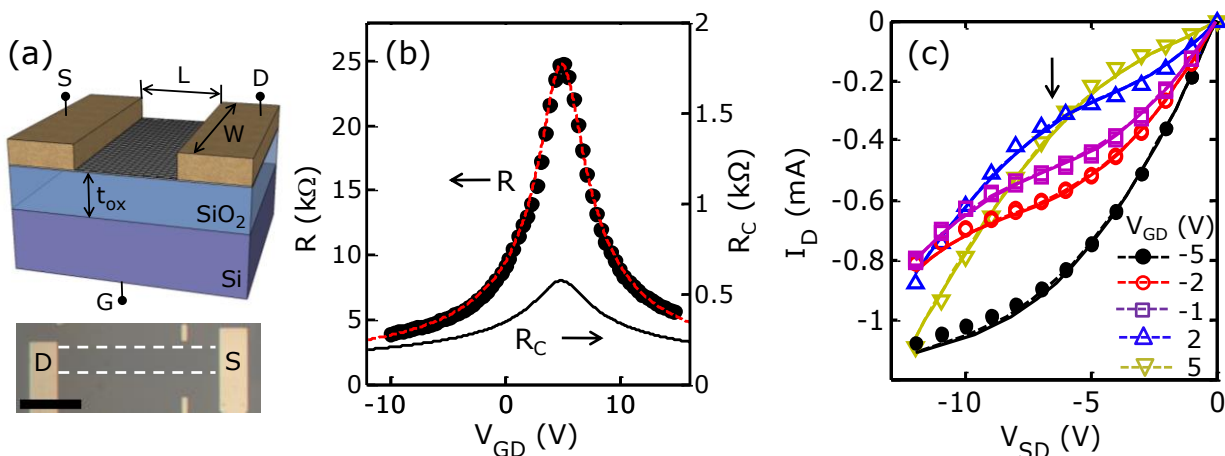


Figure 2.1: (a) Resistance (R) vs. back-gate voltage (V_{GD}) curves of a GFET on 100 nm thick SiO₂ layer, where scattered points and a dashed curve are experimental data and fit results, respectively. Inset: optical photography of the GFET on 100 nm thick SiO₂ layer, where D and S indicate drain and source, respectively. Dashed lines indicate the edges of the channel of GFET. Scale bar is 10 μm . (b) Drain current (I_D) vs. source-drain voltage (V_{SD}) with various back-gate voltage values, where scattered points and dashed curves indicate experimental and calculation results, respectively.

transfers between the graphene and the overlapping metal electrode. For simplicity, in this study we assume a constant mobility that is equal for electrons and holes, although there are indications that the mobility decreases at higher charge densities, as noted by our previous work [24]. However, this does not alter our conclusions and the excellent agreement between experiment and simulation below, since all ‘hot spot’ phenomena take place at relatively low charge density.

Figure 2.1b displays current vs. drain-source voltage (I_D - V_{SD}) measurements up to relatively high field (symbols) and our simulations (lines) at various back-gate voltages V_{GD} . We note that the transport is diffusive both at high-field and at low-field in our devices. At high-field, velocity saturation [24] occurs at fields $F > 1$ V/ μm , which corresponds to scattering rates [76] $1/\tau \sim 50$ ps⁻¹ and a mean free path $\ell_{HF} \sim v_F/\tau \sim 20$ nm. Taking $v_{sat} \sim 3 \times 10^7$ cm/s at $F \sim 3$

V/ μm (Refs.[24, 76]), the high-field mobility is of the order $v_{sat}/F \sim 1000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. As the low-field mobility is only about a factor of four higher in our samples, the low-field mean free path is of the order $\ell_{LF} \sim 80 \text{ nm}$, in accordance with previous estimates made by Ref. [67]. Thus, both the low-field and high-field mean free path of electrons and holes in our samples are significantly smaller than the device dimensions (several microns) and diffusive transport is predominant in these samples.

At high V_{SD} and under diffusive transport conditions, the electrostatic potential varies significantly along the channel [67]. The electrostatic potential at the drain is set by V_{GD} (Figure 2.1b), while that at the source is:

$$V_{GS} = V_{GD} + V_{DS} = V_{GD} - V_{SD} \quad (15)$$

For instance, with V_{SD} decreasing from zero, at $V_{GD} = 2 \text{ V}$ and $V_{SD} \approx -7.2 \text{ V}$, V_{GS} is near $V_0 = 5.2 \text{ V}$ and the Dirac point (CNP) is in the channel exactly at the edge of the source. This is seen as a change in curvature of the ambipolar ‘‘S’’-shaped I_D - V_{SD} plot, marked by an arrow on the blue triangle data set in Figure 2.1b. The channel resistance now decreases as the source-drain voltage drops below $V_{SD} < -7.2 \text{ V}$ because the electron density at the source increases. The other, primarily unipolar, operating regimes have been described in detail in Ref. [67].

2.2 Thermal Characterization in Ambipolar Conduction

We now consider the power dissipation through the Joule self-heating effect [77] along the graphene channel, and focus specifically on the ambipolar conduction mode described above. As the chemical potential changes drastically, neither the electric field nor the carrier density are uniform along the channel under high field conditions. But, because carrier movement along the GFET is unidirectional (from source to drain) the current density J must be continuous, where

$$J = \frac{I_D}{W} = q(n + p)v_d \quad (16)$$

is proportional to the local carrier density ($n + p$) and the drift velocity (v_d) at every point along the channel. Thus, regions of high carrier density have low drift velocity, and vice versa. The highest field ($F \sim v_d/\mu$) and highest localized power dissipation ($p \sim J \cdot F$) will be at the region corresponding to the minimum carrier density [67], which is where one expects the hot spot to be localized. In particular, in the ambipolar conduction state the minimum carrier density spot matches the CNP which is now located within the GFET channel.

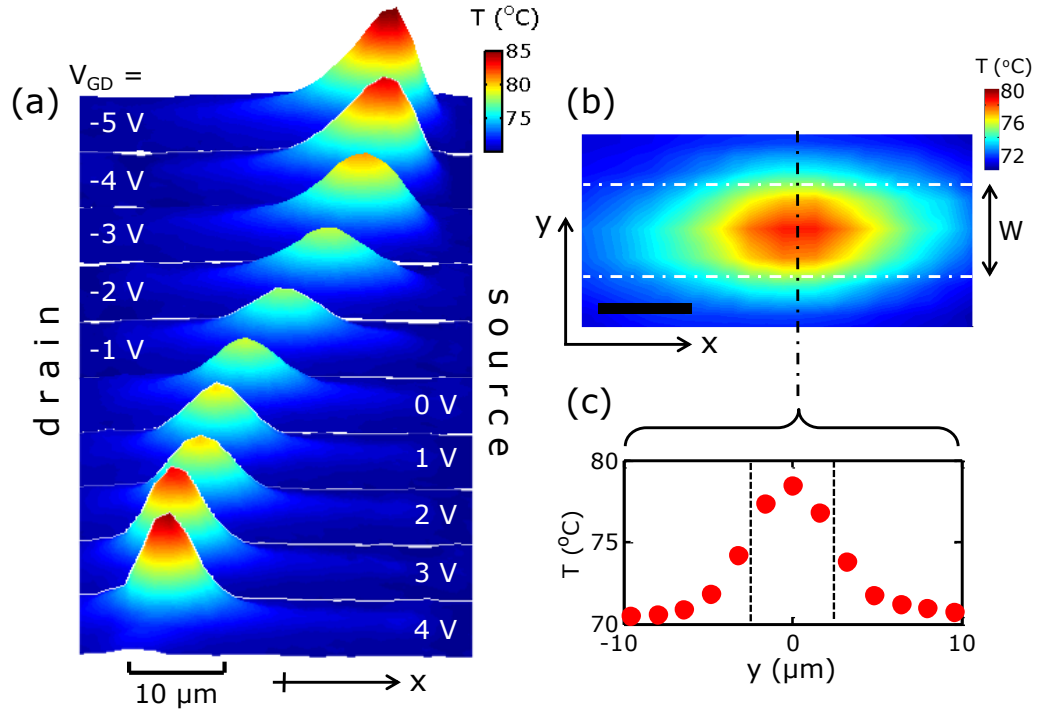


Figure 2.2: (a) Three-dimensional mapping of temperature profile along the GFET channel on 100 nm thick SiO_2 with various back-gate voltage (V_{GD}) values. The images were taken at $V_{SD} = -12$ V. (b) Top view of the hot spot at $V_{GD} = -2$ V, showing symmetric temperature distribution in the transverse (y -direction) as expected. Scale bar is 5 μm . (c) Temperature profile along the cross-section in (b); dashed lines mark the width (W) of the device.

To examine this point, we measured the temperature along the graphene channel with fixed $V_{SD} = -12$ V and at various gate-drain voltages V_{GD} , as shown in Figure 2.2. At $V_{GD} = -5$ V

($\ll V_0$) the drain is heavily hole-doped but $V_{GS} = +7$ V so the region near the source is lightly electron-doped (keeping in mind that $V_0 = 5.2$ V for this device). Thus, the CNP is located very close to the source and so is the hot spot, as can be seen in the upper panel of Figure 2.2. As we increase V_{GD} as marked in the figure, V_{GS} continues to increase according to Eq. (15), reaching $V_{GS} = +16$ V ($\gg V_0$) in the bottom panel of Figure 2.2. At this point, the source is heavily electron-doped and the drain is lightly hole-doped, very close to the CNP ($V_{GD} = 4$ V $< V_0 = 5.2$ V). Thus, during the entire imaging sequence shown in Figure 2.2 the GFET is operating in the ambipolar transport regime, but changing the gate voltage gradually alters the relative electron and hole concentrations, moving the hot spot (location of CNP) from near the source to near the drain. This experimental trace of the CNP also provides an excellent tool for checking the validity of electronic *and* thermal transport models under such inhomogeneous carrier density along the channel.

To complement the thermal imaging along the GFET (x -direction), Figure 2.2(b) and (c) show a top view of the hot spot at $V_{GD} = -2$ V and a thermal cross-section of the GFET along the dashed line (y -direction) as indicated. We note that the width of the GFET here is only slightly larger than the IR resolution (see Methods), and thus the cross-section view should be used only for qualitative inspection. By comparison, higher resolution scanning Joule expansion microscopy (SJEM) [78] has revealed a uniform transverse temperature profile with slightly cooler edges from heat sinking and higher carrier density due to fringing heat and electric field effects.

2.3 Velocity Saturation Models Comparison

Our graphene device simulation approach was previously described, in Ref. [67, 70, 79] and also in Chapter 1. To obtain the current as a function of voltage, our electro-thermal model

has been solved iteratively and self-consistently, until changes in charge density converge to less than 1% and the temperature converges to within less than 0.01 K between iterations. Figure 2.1b shows that the simulation results (lines) are in excellent agreement with the experimentally measured I_D - V_{SD} data. All data were stable and reproducible during measurements, partly enabled by protection offered by the top PMMA layer and partly from limiting the maximum voltages applied.

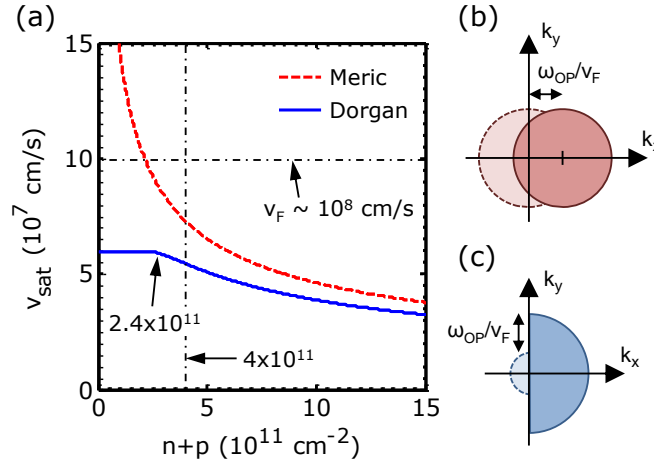


Figure 2.3: (a) High-field saturation velocity models vs. carrier density. At low density, here $<2.4 \times 10^{11} \text{ cm}^{-2}$, the Dorgan [24] model reaches a constant value ($\sim 2v_F/\pi \approx 6.3 \times 10^7 \text{ cm/s}$, slightly lower here at $\sim 70 \text{ }^\circ\text{C}$, whereas the Meric *et al.* [41] model can diverge. However, due to temperature effects and puddle charge, the carrier density in our device is always $>4 \times 10^{11} \text{ cm}^{-2}$ during operation, as marked by an arrow. Thus, in the device simulated here either model can be applied, as in Figures 2.1 and 2.4. (b, c) Schematic assumptions of carrier distribution at high field used to derive the closed-form v_{sat} expressions in the (b) Meric *et al.* [41] and (c) Dorgan *et al.* [24] models.

To better understand high-field transport, we considered two recent models for the drift velocity saturation (v_{sat}), as shown in Figure 2.3. In one case, Meric *et al.* [41] have suggested

$$v_{sat} = \frac{\omega_{OP}}{\sqrt{\pi(n+p)}} \quad (17)$$

where $\hbar\omega_{OP}$ is the dominant optical phonon (OP) energy for carrier energy relaxation.

This is an approximation based on a shifted Dirac circle in the limit of $T = 0 \text{ K}$ (Figure 2.3b and

supplement of Ref. [41]), and is generally applicable at “large” carrier density ($n + p \gg n_0$). On the other hand, following initial work by Barreiro and co-workers, [80] Dorgan *et al.* [24] have proposed the velocity saturation model in Eq. (17). These models are based on a steady-state population in which carriers contributing to current flow occupy states up to an energy $\hbar\omega_{OP}$ higher than carriers moving against the net current [80] (Figure 2.3c). Note that both models suggest v_{sat} decreases approximately as the inverse square root of the carrier density, and in both models $\hbar\omega_{OP}$ is treated as a fitting parameter. However, v_{sat} in the Meric’s model is derived in the limit $T = 0$ K and can approach infinity as the carrier density tends to zero. The Dorgan model includes a semi-empirical temperature dependence [24] and approaches a constant at low carrier density, $v_{max} \sim (2/\pi)v_F \sim 6.3 \times 10^7$ cm/s (closer to $\sim 6 \times 10^7$ cm/s at 70 °C when the temperature dependence is taken into account, as in Eq. (17) and Figure 2.3a).

Consistent with the previous studies [24, 79, 81, 82] we choose $\hbar\omega_{OP} = 59$ meV ($\gamma = 1.3$ in Eq. (8)) and 81 meV ($\gamma = 1.5$) for the Meric’s and Dorgan’s models, respectively. These fitting parameters were chosen so as to yield virtually indistinguishable characteristics in Figure 2.1b. We plot v_{sat} from the two models as a function of total carrier density ($n + p$) in Figure 2.3a, showing the expected behavior as described above. With our present parameters, the Dorgan model reaches a constant below charge densities $n + p < n^* = 2.4 \times 10^{11}$ cm⁻². However, we note that the minimum charge density achieved during all simulations in this work was $\sim 4 \times 10^{11}$ cm⁻² due to puddle charge and thermally excited carriers. In addition, the maximum longitudinal fields were ~ 0.9 V/ μ m (see Figure 2.4), and thus full velocity saturation was never reached (see, e.g. Figure 3 of Ref. [24]). This explains that relatively good agreement can be attained between both model and our data in Figure 2.1b, within the present conditions. (Future work on shorter devices

at higher electric fields will be needed to elucidate the role of saturation velocity at low carrier density.)

2.4 Electro-Thermal Simulation and Comparison with Data

With the parameters discussed above, Figure 2.4 shows carrier densities and temperature profiles at the last drain bias point ($V_{SD} = -12$ V) for three representative gate voltages, $V_{GD} = -2$, -1 , and 2 V. Once again, excellent agreement is found between simulation results obtained with the two different v_{sat} models (solid curves) and the experimental temperature profiles (symbols). The position of the CNP for each V_{GD} can be visualized by comparing Figs. 2.4(a-c) with Figs. 2.4(d-f) as the crossing point of electron and hole carrier density profiles and that of the hot spot. We also plot the corresponding electric field profiles in Figs. 2.4(g-i), where the position of the maximum field matches that of the hot spot. The CNP clearly moves from source to drain when the gate voltage changes, as visualized in Figure 2.2 and previously explained in qualitative terms. We note that the profile of the hot spot with 100 nm underlying oxide thickness (Figs. 2.2 and 2.4 here) is much better defined and ‘sharper’ than what was previously observed on 300 nm oxide [67, 68].

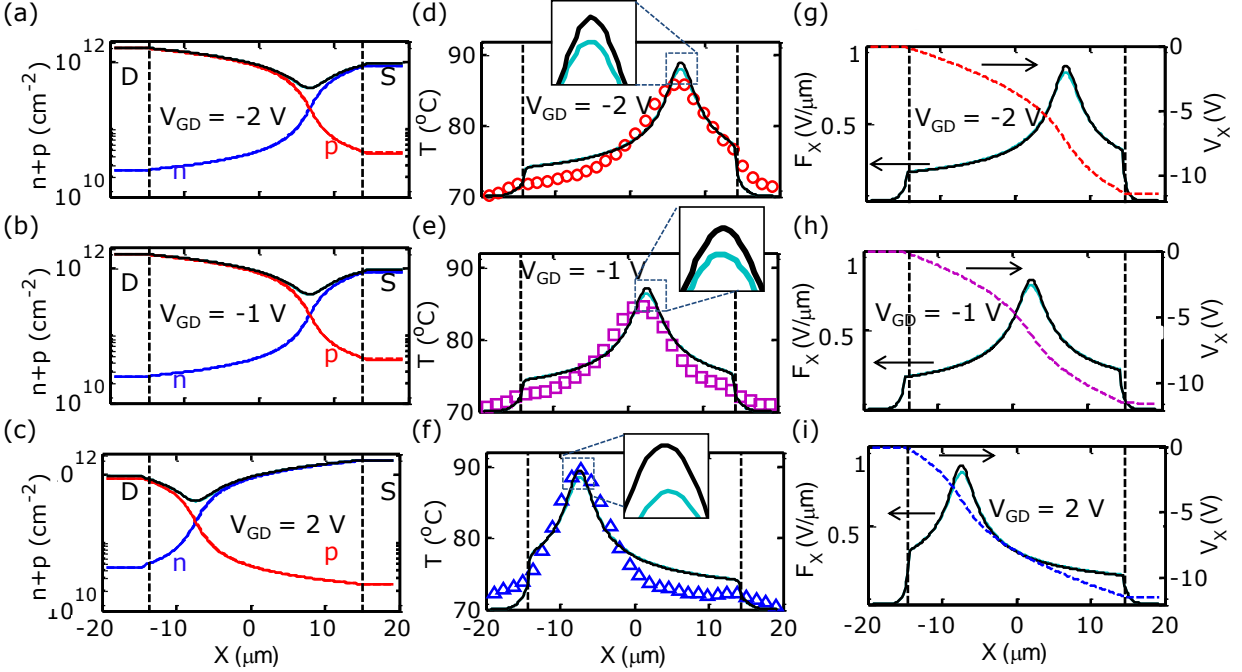


Figure 2.4: (a)-(c) Carrier densities along the GFET channel on 100 nm thick SiO_2 at given V_{GD} with $V_{SD} = -12$ V. (d)-(f) Temperature profiles and (g)-(i) Electric field and potential profile along the channel along the GFET at given V_{GD} corresponding to (a)-(c), respectively. Black and Teal curves are calculation results with saturation velocity model for Dorgan *et al.* [24] and Meric *et al.* [41] respectively for 100 nm thick SiO_2 layers, with the same power. Here, scattered points in (d)-(f) are experimental data. For (g)-(i) the corresponding axis are showed by the arrows.

Comparing the simulations obtained with the two v_{sat} models, we note that the carrier density profiles are nearly identical in Figs. 2.4(a-c). However, the lower v_{sat} (at a given carrier density) of the Dorgan model [24] yields slightly higher electric fields and higher hot spot temperatures, as shown in Figs. 2.4(d-i) (also see the insets). The temperature difference here is up to ~ 1 $^{\circ}\text{C}$ between the two models, or $\sim 5\%$ of the total temperature change, although the applied power is the same between the separate simulations. We note that since velocity saturation is never fully reached in the present simulation (and measurement) conditions, the differences in computed temperature and electric field are more subtle than the apparent difference between the two models in Figure 2.3 would imply. Nevertheless, the disparities are

more apparent if we inspect how “close” to saturation the transport becomes, i.e. the ratio $|v/v_{sat}|$ at each point along the channel, as plotted in Figs. 2.4(g-i). In this case, the Dorgan model (upper black curves) yields transport closer to the saturation condition, given that its v_{sat} is typically lower. Following Eq. (8), this also implies higher local electric fields, thus higher local power dissipation and temperature.

The simulation results in Figure 2.4 suggest that while the IR microscopy used here provides significant insight into high-field transport in graphene, it is not quite sufficient to distinguish with certainty the drift velocity saturation behavior. Nevertheless, we believe the principle of the approach is sound. In other words, thermal measurements of high-field transport in GFETs at conditions of higher fields ($>1 \text{ V}/\mu\text{m}$) and lower carrier densities ($<5.5 \times 10^{11} \text{ cm}^{-2}$) through a tool such as Raman spectroscopy [81, 83] should resolve with more accuracy the drift saturation behavior, providing significantly more insight than electrical measurements alone.

2.5 Scaling of Heating with Oxide Thickness

Having established good agreement between our experimental data, numerical simulations, and qualitative understanding, we now seek to extend our knowledge of ambipolar transport in graphene and test the physical mechanisms defining the hot spot. Thus, we simulate device behavior and temperature profiles with various underlying SiO_2 thickness (t_{ox}) during ambipolar transport as shown in Figure 2.5. Here, all calculations are performed with total power $P = 9.25 \text{ mW}$, corresponding to the experimentally applied bias conditions at $V_{GD} = -1 \text{ V}$ with $t_{ox} = 100 \text{ nm}$ (Figure 2.4(e)). This is an important consideration for an appropriate comparison, since thinner (thicker) oxides are expected to lead to lower (higher) average channel temperature. Moreover, to compare the hot spot between the various cases, we aligned the positions of the

CNP for all t_{ox} values by changing V_{GD} and I_D while keeping the total power constant, as shown in Figure 2.5(a).

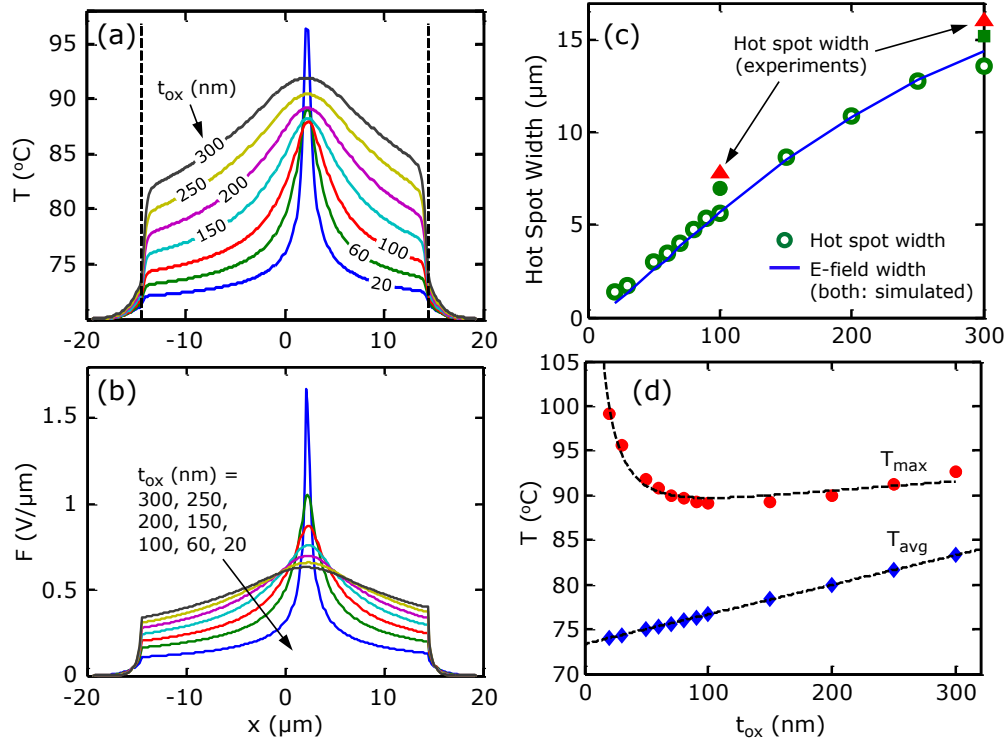


Figure 2.5: Calculated temperature profile along the graphene channel for various SiO₂ thickness. All data are obtained at the same power (9.25 mW), which is selected from the experimental power at $V_{GD}=-1$ V for $t_{ox}=100$ nm. (b) Calculated (circles) and fitted (dashed curve) width of hot spot as a function of t_{ox} . Triangle and square: width of hot spot experimentally obtained from $t_{ox}=100$ and 300 nm, respectively. (d) $T(t_{ox})=at_{ox}^{-1} + bt_{ox}^c$, where a,b and c are 389.3, 66.26 and 0.05285, respectively.

We also plot the electric field (F) profiles in Figure 2.5(b). Then, based on Figure 2.5a, we plot the relationship between hot spot width and t_{ox} in Figure 2.5(c) (circles), showing a linear scaling between the two. Here, the size of the hot spot is defined as the full width at half the temperature between the peak and the ‘shoulder’ near the contacts. We also plot the width of the electric field profile width (solid curve) vs. t_{ox} , showing essentially the same scaling as the hot spot. The experimentally measured widths of the hot spots are shown in Figure 2.5(c) as triangles for $t_{ox} = 100$ nm from Figure 2.4(e), and for $t_{ox} = 300$ nm from Ref. [67], respectively. While the

scaling is similar to that predicted by our simulations, the slight discrepancy is most likely due to finite resolution of the IR microscope. By comparison, averaging the simulation results with a ~ 2 μm -wide broadening function yields the solid circle in Figure 2.5(c), which is closer to the experimental data for $t_{ox} = 100$ nm. For the $t_{ox} = 300$ nm case, the solid square is from a simulation in Ref. [67], also showing improved agreement when the particular parameters of this device are used.

As the oxide thickness is scaled down from $t_{ox} = 300$ nm to 20 nm, we find that both the *average* channel temperature (Figure 2.5(d)) and the width of the hot spot decrease (Figure 2.5(c)), i.e. the hot spot becomes ‘sharper’. The former occurs because the thermal resistance of the SiO_2 is lowered, and the latter is due to increasing capacitive coupling between the back-gate and the charge carriers in the channel. We note that the average channel temperature in Figure 2.5(d) does not reach the base temperature (here, $T_0 = 70$ °C) even in the limit of vanishing t_{ox} due to the remaining thermal resistance of the silicon substrate. To understand this, the average thermal resistance of the device can be estimated as [24] $R_{th} \approx t_{ox}/(k_{ox}LW) + 1/[2k_{Si}(LW)^{1/2}]$, where the first term is the lumped thermal resistance of the SiO_2 layer, and the second term is the spreading thermal resistance [77] of the silicon substrate ($k_{Si} \approx 100 \text{ Wm}^{-1}\text{K}^{-1}$ for the highly doped Si wafer).

Interestingly, Figure 2.5(d) indicates that the *peak* temperature of the hot spot (T_{max}) begins to *increase* when t_{ox} is scaled below ~ 90 nm, despite a lower average temperature in the channel. This trend occurs because the Joule heating effect induced by the high electric field at the CNP overcomes the cooling effect of the lowered oxide thickness at $t_{ox} \approx 90$ nm. To gain more insight into this observation, we return to the temperature and electric field profiles along the graphene channel in Figs. 2.5(a) and 2.5(b). We note that the temperature qualitatively

follows the electric field profile, and the source of the hot spot is clearly electrostatic in nature. In addition, this finding suggests that one should consider the formation of highly localized hot spots in future devices which would have thinner underlying oxide layers. While a thinner t_{ox} does lead to a lower average temperature, the *peak* temperature is actually increased due to electrostatic effects. This effect is expected to be the same in top-gated as in bottom-gated graphene devices, because the electrostatic effects are controlled by the gate, whereas heat flow is limited by the underlying oxide. The local temperature increase and highly localized electric field at the hot spot could lead to long-term oxide reliability issues [71] which must be accounted for.

2.6 Conclusion

In summary, we have examined the physical mechanisms behind high-field hot spot formation in graphene transistors on SiO₂ and found them to be electrostatic in nature. Using self-consistent electro-thermal simulations and infrared thermal imaging, we established that the maximum temperature of a graphene device in high-field operation is sensitive to the peak electric field and carrier saturation velocity. We have also confirmed that the average temperature of a functioning GFET scales proportionally to the thickness of the supporting SiO₂, as expected. However, the maximum temperature of the GFET can be minimized for a given insulator thickness (here ~90 nm for SiO₂) due to competing electrostatic and heat sinking effects. These results suggest a route for the optimization of graphene substrates for proper heat dissipation, and highlight existing trade-offs for practical device reliability.

Chapter 3

ROLE OF JOULE HEATING IN CURRENT SATURATION

Recent work has also found drift velocity saturation at high field in graphene, at values several times higher than in silicon [24]. However, velocity saturation alone does not directly lead to current saturation, which is difficult to achieve in a zero band gap material where the channel cannot be fully pinched off. Current saturation is important for low output conductance and amplifier gain [18, 25] and in practice it has been partly achieved through a combination of velocity saturation and electrostatic charge control [26, 27]. High-field transport is also influenced by self-heating [24, 28], as revealed by recent infrared imaging [30, 52, 84] and temperature-dependent Raman spectroscopy of graphene transistors [85-87].

In this work we examine the effect of self-heating on current saturation in graphene-on-insulator (GOI) transistors through electro-thermal device simulations. We consider the role of the buried oxide thickness (t_{box}) under the graphene, and of the device length (L) in the sub-micron regime. We also observe that practical graphene transistors could be operated in a transient (e.g. pulsed) mode, and calculate their thermal time constants, i.e. the time scales over which the device temperature ramps up or cools down after electrical switching.

3.1 Effect of Joule Heating

The schematic of a typical GOI transistor is shown in Fig. 3.1(a). Our simulations are based on the drift-diffusion approach, calculating carrier densities, electric field, drift velocity,

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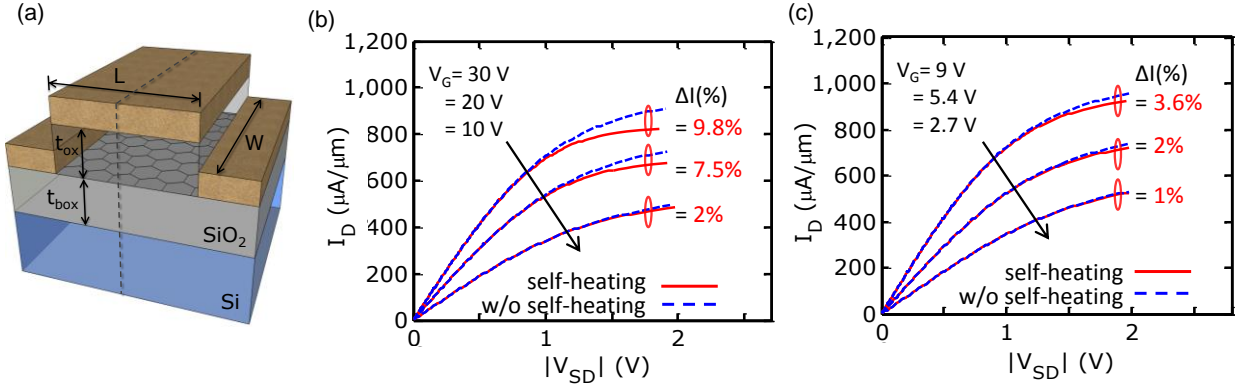


Figure 3.1: (a) Schematics of simulated graphene device on SiO₂/Si substrate (image courtesy of F. Lian). Current saturation with self-heating (solid) compared to isothermal simulations (dashed) at three vertical E-fields ($= V_{GS}/t_{ox}$) for (b) $t_{box} = 300$ nm and (c) $t_{box} = 90$ nm.

potential, and temperature along the channel and contacts self-consistently. The simulator was extensively tuned against experimental data [52, 84], including contact effects [70]. The metal-graphene contact resistance per unit area used here is $\rho_C = 111 \Omega \cdot \mu\text{m}^2$ which is near the low end of the range for typical Pd- or Au-graphene contacts [70]. The Dirac voltage of simulated devices is $V_0 = 0$ V and the background temperature is $T_0 = 293$ K. Other parameters are as in Ref. [24], including compact models of mobility and velocity saturation-dependent on carrier density and temperature. Since carrier mean free paths in typical GOI transistors are in the 20-80 nm range [52, 84], the model is most reliable for devices greater than $\sim 0.1 \mu\text{m}$.

We first investigate self-heating and current saturation in a device with channel length and width $L = W = 1 \mu\text{m}$. Fig. 3.1(b-c) shows the computed current vs. source-drain voltage (I_D - V_{SD}) of this GOI device on $t_{box} = 300$ nm and 90 nm SiO₂ with vertical electric fields of 0.3, 0.6, and 1.0 MV/cm, respectively. The dashed lines represent the current without self-heating ($T = T_0$), while the solid lines show some current degradation when Joule heating is self-consistently taken into account. Thus, the simulations suggest that self-heating is at least partially responsible for the current saturation observed in recent experiments on devices of comparable size and bias [26, 27]. Figs. 3.2(a-b) and (c-d) show the total carrier density and electric field (E-field) at the

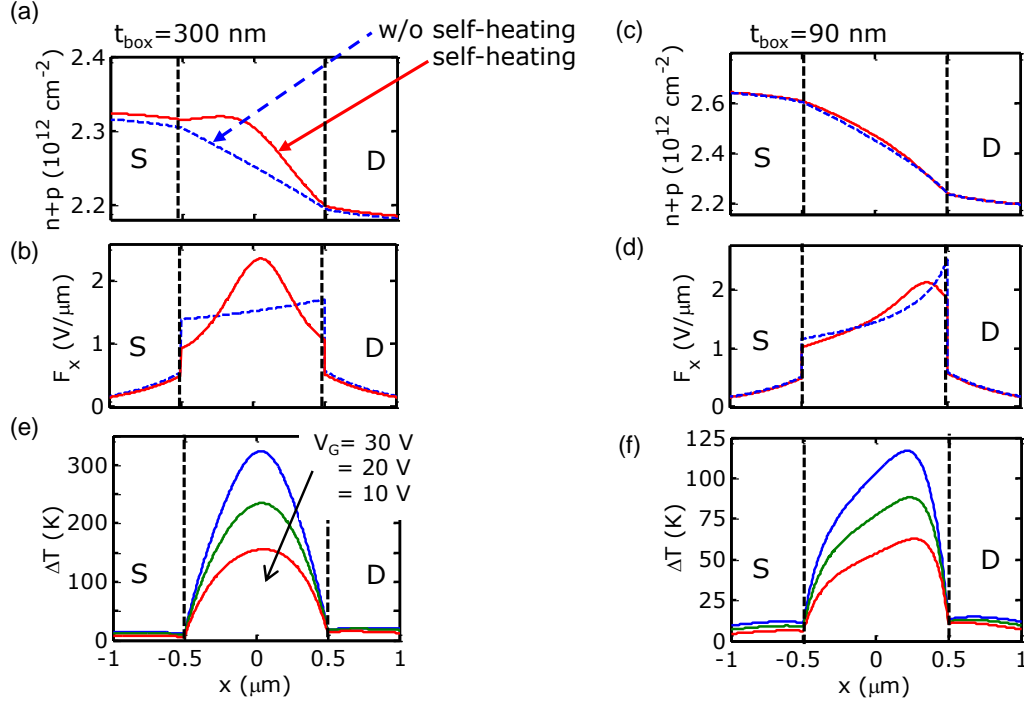


Figure 3.2: Carrier density and E-field along the channel at vertical field 1 MV/cm, respectively, with and without self-heating, for $t_{\text{box}} = 300$ nm (a-b) and (c-d) $t_{\text{box}} = 90$ nm. Temperature profiles along the channel at $V_{SD} = 2$ V in including self-heating; for $t_{\text{box}} = 300$ nm (e) and (f) $t_{\text{box}} = 90$ nm.. The device considered here has $L = W = 1 \mu\text{m}$.

highest voltage and current biasing point from Fig. 3.1(b) and (c), respectively, both with and without self-heating. Interestingly, because graphene is a gapless material, we find that significant self-heating during operation can alter the majority carrier concentration through thermal generation [24]. In turn, this affects the E-field distribution along the channel as shown in Fig. 3.2(b) and (d). Thus, self-heating at high field can influence not only the current saturation of the device, but also the internal carrier distributions and E-fields. Figure 3.2(e-f) displays the temperature profiles corresponding to the maximum bias points for the three cases in Fig. 3.2(b). The temperature distribution qualitatively follows the E-field profile as recently noted by experiments [84].

We now study the peak temperature rise (ΔT) and the percentage of saturation current degradation ($\Delta I/I_{\text{sat}}$) as we reduce t_{box} from 300 nm to 50 nm. For all t_{box} , the peak ΔT and I_{sat} are

taken at the same $V_{SD} = 2$ V for vertical fields of 0.5, 1, and 2 MV/cm. Fig. 3.3(a) shows that the peak ΔT of devices with channel length $L = 1$ μm scales proportionally with t_{box} , as expected. However, we note that even in the limit of $t_{\text{box}} \rightarrow 0$ (graphene device directly on substrate, similar to graphene on SiC), the temperature rise is non-zero due to the thermal resistance of the graphene-substrate interface and that of heat spreading into the substrate itself [24, 84]. Fig. 3.3(b) shows $\Delta I/I_{\text{sat}}$ due to self-heating as a function of t_{box} . As a simple guideline, a $\sim 5\%$ degradation in I_{sat} corresponds to $\Delta T \sim 170$ K above room temperature. For current density near ~ 1 mA/ μm , as for the top curve in Fig. 3.1(b) on $t_{\text{box}} = 300$ nm, the current degradation due to Joule heating can be $>10\%$, and for higher current densities the self-heating effect is proportionally larger. This can be partly compensated by reducing t_{box} and L , as described here and below. These results should provide a useful design space for future GOI devices in order to reduce the self-heating effect. In addition, elevated temperatures not only decrease device performance, but also have profound effects on long-term device and dielectric reliability [88].

We next explore the effect of Joule heating while scaling the channel length from 1 to 0.25 μm . Fig. 3.3(c) shows current-voltage curves computed with and without self-heating, indicating the self-heating effect is less in shorter channel devices. Fig. 3.3(d) also plots $\Delta I/I_{\text{sat}}$ due to self-heating vs. t_{box} for the same channel lengths, at the same drain output conductance $g_d = \partial I/\partial V_{SD}$. Less current degradation at shorter channel lengths is explained by an enhanced role of heat dissipation “laterally” to the contacts in addition to “vertically” through the oxide. This was also recently observed in experimental work on sub-0.5 μm graphene nanoribbons (GNRs) [89] which noted that heat dissipation into the contacts begins to play a role when device dimensions become $\leq \sim 3$ times the thermal healing length. The thermal healing length is a measure of the lateral heat diffusion along the graphene, $L_H \approx 0.2$ μm in graphene on SiO_2 and

approximately half in GNRs which have lower thermal conductivity [52, 89]. Increased heat loss to the contacts is also seen as a sub-linear rise of current degradation in Fig. 3.3(d) for the shorter devices. Our present model numerically accounts for heat spreading into the substrate and the contacts [84], however this can also be approximated well analytically as in Ref. [89].

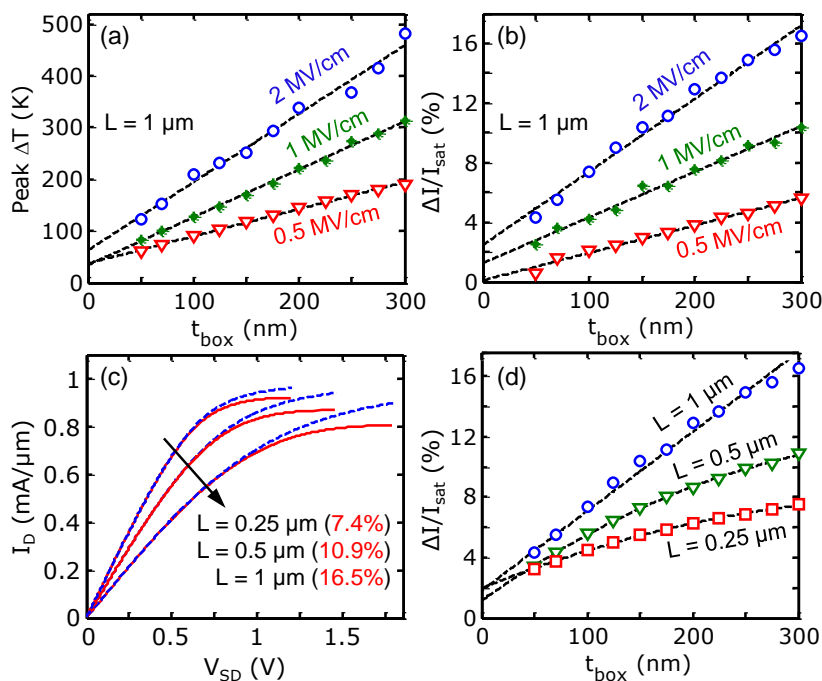


Figure 3.3: (a) Calculated peak ΔT and (b) self-heating effect on saturation current as a function of t_{box} for three vertical fields, at channel length $L = 1 \mu\text{m}$. Dashed lines are linear fits. (c) Current-voltage simulations with self-heating (solid) and without (dashed) for devices of $L = 0.25, 0.5, 1 \mu\text{m}$, on $t_{\text{box}} = 300 \text{ nm}$ and vertical field 2 MV/cm . (d) Self-heating effect on saturation current as a function of t_{box} for the same three channel lengths and vertical field. Dashed lines show lower degradation and sub-linear dependence on t_{box} for sub- $0.5 \mu\text{m}$ channel lengths due to heat sinking effect of contacts.

3.2 Thermal Transient

While the section above focused on effects of self-heating on DC characteristics, this section explores the transient device behavior. We perform finite element (FE) simulations as shown in Figs. 3.4(a-b), the device being symmetric along the cross-section marked by a dashed line in Fig. 3.1(a) and only one half needs to be simulated. Isothermal boundary conditions ($T =$

T_0) are applied 10 μm away from the device at the bottom and right edges of the Si substrate, and other boundaries are adiabatic. We used temperature-dependent values for the thermal conductivity and heat capacity of the oxide [90], although the effect was relatively small, $<5\%$.

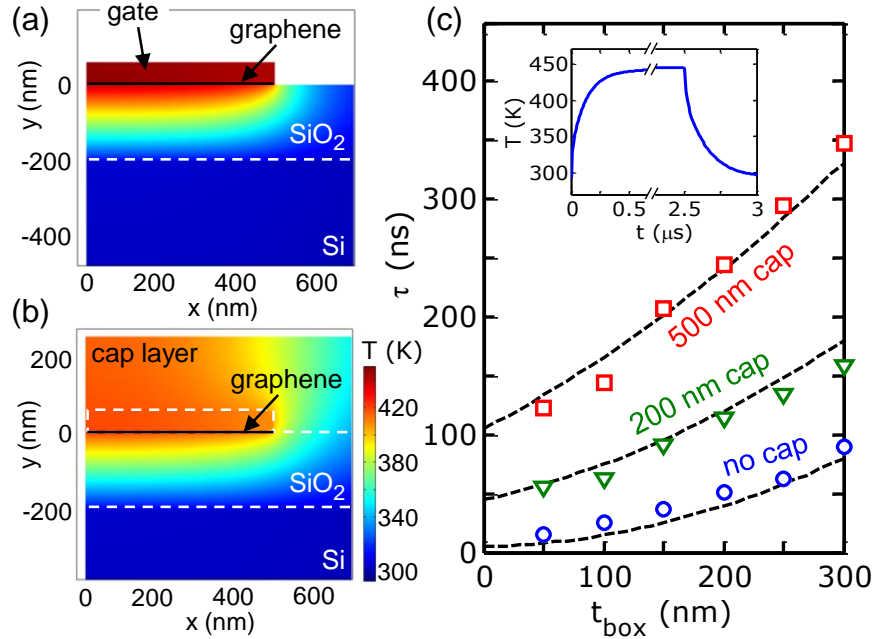


Figure 3.4: Cross-section of graphene device temperature from Fig. 3.1 with (a) no capping layer and (b) 200 nm SiO₂ cap layer, obtained 2.5 μs after a 0.5 mW input pulse. (c) Calculated thermal time constants of graphene devices as a function of t_{box} without a capping layer (\circ), 200 nm cap layer (∇), and 500 nm cap layer (\square). Dashed lines are fits with Eq. (18). The inset shows the temperature transient for $t_{\text{cap}} = 200$ nm and $t_{\text{box}} = 250$ nm. The power is turned on at $t = 0$ s and off at $t = 2.5$ μs .

An input power of 0.5 mW is initially applied to the graphene channel then turned off after 2.5 μs . Figs. 3.4(a-b) correspond to temperature distributions at the end of the heating pulse in a device without and with a capping layer (assuming SiO₂), respectively. These can be roughly understood as a typical device in a laboratory setup vs. one that is integrated in a package. The temperature transient of the graphene channel mid-point is shown in the inset of Fig. 3.4(c) for a capping layer $t_{\text{cap}} = 200$ nm and $t_{\text{box}} = 250$ nm. The thermal time constant τ is obtained by fitting the temperature decay as $T(t) = T_0 + T_1 e^{-t/\tau} + T_2 (1 + t/\tau_0)^{-b}$, where $T_0 = 293$ K is the base temperature, $T_0 + T_1 + T_2$ is the steady-state peak temperature, and the third term is used to fit the

long tail of the temperature decay due to the (small) residual heating transient of the Si substrate, where b is in the range of 0.5-2.5 and τ_0 is from tens to hundreds nanosecond. In “no cap” case, T_2 is smaller than 30% of T_1 , but it becomes comparable to T_1 in “with cap” cases.

The symbols in Fig. 3.4(c) summarize the calculated thermal time constant of the graphene device as the t_{box} is scaled, for devices with a capping layer of 200 nm, 500 nm, and without (“no cap”). We can understand the scaling of the thermal time constant through a simple analytic model which treats each region as a lumped thermal resistor as well as a lumped thermal capacitance. This allows us to estimate the related equivalent thermal time constant τ by summing the contributions from all the regions to give the total thermal resistance (R_{th}) and thermal capacitance (C_{th}):

$$\tau = R_{th} C_{th} \approx f_1 \frac{C_V}{k_{ox}} t_{box}^2 + \left[f_2 \frac{C_V}{k_{ox}} t_{cap} + \frac{C_{Vm}}{k_m} t_m \right] (t_{box} + t_{eq}) \quad (18)$$

where $C_V = 1.76 \text{ MJ K}^{-1} \text{ m}^{-3}$ and $C_{Vm} = 2.88 \text{ MJ K}^{-1} \text{ m}^{-3}$ are the heat capacities of the oxide and metal gate, respectively [91]. t_m and k_m (40 W m⁻¹ K⁻¹ for Pd) are the thickness and thermal conductivity of the top metal gate, respectively. The geometrical pre-factors $f_1 \sim 0.6$ and $f_2 \sim 0.8$ represent the fraction of the total temperature drop in the bottom oxide and top capping layer, respectively. The last term $t_{eq} \sim 200 \text{ nm}$ accounts for the thermal equivalent of transient cooling in the silicon substrate (the limit $t_{box} \rightarrow 0$), consistent with previous studies on bulk CMOS devices [92].

The model of Eq. (18) is plotted with dashed lines in Fig. 3.4(c), in good agreement with our FE simulations (symbols). We note that our FE results are realistic within 10-20% accuracy, depending on the simulated domain size and choice of 3D vs. 2D simulations (the main trade-off being CPU time); however, the main physical trends persist. These results suggest that thermal

time constants follow an approximately quadratic dependence on t_{box} , which contributes to both the thermal resistance and thermal capacitance of the device. The capping layer and metal gate contribute to the term in Eq. (18) that is linear in t_{box} , but do not aid in “cooling” the device otherwise. Thus, a thicker gate or capping layer only adds “thermal ballast” and can increase the thermal time constant. Interestingly, due to its thinness, the graphene layer itself does not influence the thermal transient of the device, which is dominated by heating of the surrounding materials. This is a unique aspect of graphene devices vs. that of silicon-on-insulator (SOI) technology, where the thin Si “body” retains a non-negligible heat capacity and thermal resistance [93, 94]

3.3 Conclusion

To conclude, we have found that Joule heating during operation is partially responsible for current saturation and degradation observed in graphene device experiments. Self-heating is reduced with thinner dielectrics, and for sub-0.5 μm channel lengths the contacts begin to play a greater role in heat sinking. The thermal time constants of graphene devices are of the order ~ 100 ns, but strongly dependent on the materials surrounding the channel. Thermal transients are much slower than electrical transients ($\sim 1-10$ ps), consistent with previous work on SOI technology [93, 94]. This implies that graphene devices are slow to heat up or cool down after electrical switching and, for instance, pulsed operation on time scales shorter than the thermal time constant can benefit from reduced self-heating compared to DC operating modes.

Chapter 4

EFFECT OF CHANNEL LENGTH SCALING ON CURRENT SATURATION IN GRAPHENE TRANSISTORS

High intrinsic cutoff frequencies ($f_T > 300$ GHz) have recently been achieved in graphene devices by scaling down channel the length to 40 nm [95]. However, another important figure of merit for practical electronic applications is intrinsic voltage gain ($A_v = g_m/g_d > 1$), where g_m is transconductance and g_d is output conductance. Although long-channel ($> 2 \mu\text{m}$) graphene field-effect transistors (GFETs) have demonstrated some quasi-saturation behavior, this is harder to achieve in sub-micron devices [96]. This lack of saturation degrades output conductance (g_d), which ultimately results in small A_v . The origins of this experimentally observed low gain need to be better understood in order for graphene FETs to eventually compete with other similar technologies such as high-electron-mobility transistors (HEMT) or silicon n-channel metal-oxide-semiconductor field-effect transistors (MOSFETs). In our work, we find that weak current saturation in sub-micron graphene devices is one of the main limiting factors to their implementation in analog and RF electronics.

4.1 State-of-the-Art Performance of Graphene FTEs

Figure 4.1 displays a survey of the graphene field-effect transistor (GFET) literature [95-108] on g_m , g_d and A_v . We observe that with downscaling of channel length L , g_m improves. However, at the same time, as L is reduced below $1 \mu\text{m}$, g_d significantly degrades. In other words current saturation degrades as channel length decreases. For this overview we selected and calculated (when not explicitly reported) the best g_m and corresponding g_d values reported in the

literature. The intrinsic voltage gain ($A_v = g_m/g_d$), is one of the parameters that determines performance of analog FETs. At lower L , both g_m and g_d increase, resulting in small A_v , as shown in Fig. 4.1(c). Only few studies achieve a modest $A_v > 1$. Some of the “best” gains [red squares in Figs. 4.1(a-c)] have been achieved in devices with a localized back-gated configuration, which avoids processing issues with the deposition of dielectrics onto graphene. Nonetheless, this device configuration is not practical for large-scale device integration. The spread in the g_m , g_d and A_v data can be understood by noting that different studies used graphene of different qualities, as well as FETs with different contact resistances and gate capacitances (equivalent oxide thickness or EOT).

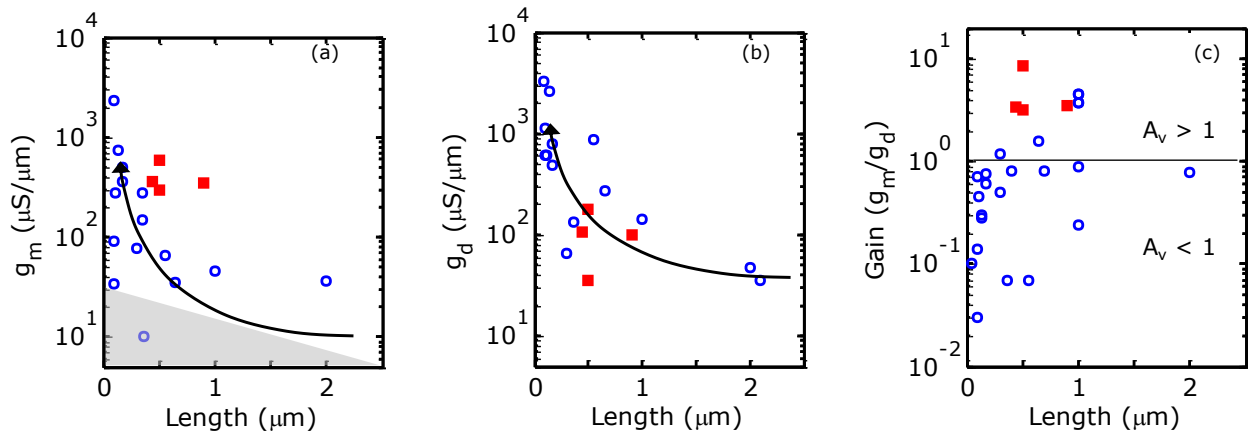


Figure 4.1: Survey of transconductance (g_m) and output conductance (g_d) reported for graphene FETs in the literature^{1, 3-15}. (a) Typical g_m , (b) g_d , and (c) intrinsic gain as a function of channel length L . The intrinsic gain exceeds unity ($A_v > 1$) only for a small set of published devices, primarily due to poor current saturation (large g_d). Arrows represent approximate scaling trends. Shaded area in (a) corresponds to g_m of Si based MOSFET for EOT = 16 Å. Data show both top-gated (blue circle) and back-gated (red square) devices. Some values are estimated from published I_D - V_D curves and may not be at the same exact bias points.

Most of the top-gated devices showed $g_m > 100 \mu\text{S}/\mu\text{m}$ at $L > 350 \text{ nm}$, while for localized back-gated devices had $g_m > 300 \mu\text{S}/\mu\text{m}$ even at $L > 500 \text{ nm}$. The shortest channel lengths measured ($L \sim 0.1 \mu\text{m}$) display effectively *no* current saturation, with high output conductance g_d

$> 1000 \mu\text{S}/\mu\text{m}$ [96, 99, 100]. Similar studies on g_m of Si MOSFETs also show strong dependence on length scaling [109-111]. The highest g_m achieved by silicon on insulator (SOI) is $\sim 1300 \mu\text{S}/\mu\text{m}$ for a 45 nm long device [112]. On the other hand, even for GFETs with channel length twice as long (90 nm), g_m almost twice as large can be achieved [99]. This higher g_m value, even for longer channel lengths, is indicative that the higher mobility (μ) of graphene has a dominant and important role in g_m and gain. Furthermore, in order to compare g_m corresponding to graphene technology vs. Si based MOSFETs, we include a shaded region in Fig. 4.1(a) for calculated g_m values as a function of channel length (EOT = 16 Å, $\mu = 400 \text{ cm}^2/\text{V}\cdot\text{s}$, width (W) = 1 μm and drain voltage (V_{SD}) = 50 mV).

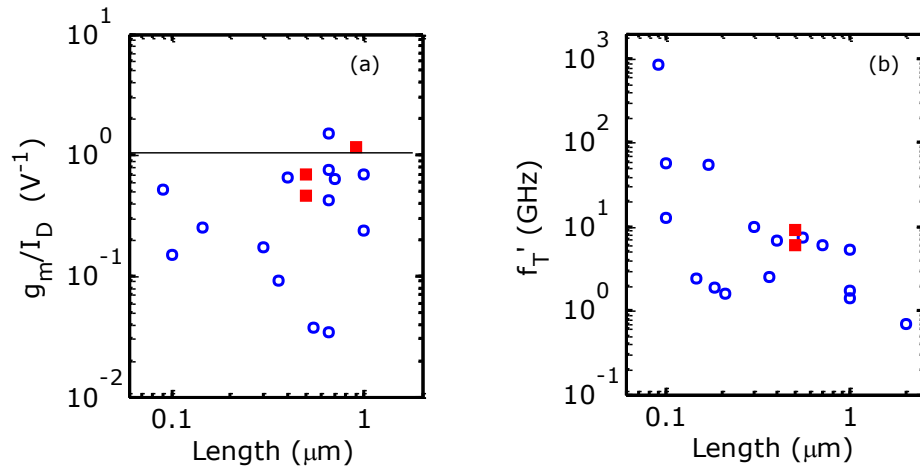


Figure 4.2: Review for graphene FETs in the literature:³⁻¹⁵(a) normalized transconductance over drain current as a function of channel length L . Almost all values of g_m/I_D for GFETs lies below unity (b) transit frequency as a function of L . There is a three order of magnitude increase in f_T by down scaling L from 2 μm to 90 nm.

One of the fundamental design tools for analog circuit design is g_m normalized over drain current I_D (g_m/I_D) [113], which indicates how much current is needed to achieve a desired g_m and points at the power efficiency of the device. From our review, almost all g_m/I_D values for GFETs lie below unity, as shown in Fig. 4.2(a), which does not indicate a promising power efficient scenario to achieve high g_m from GFETs. For this review, most of the g_m values are calculated at

close to saturation I_D , which results in a lower value for g_m/I_D . In silicon-based CMOS technology, we see g_m/I_D approaches unity in strong inverted channel [114]. At weak inversion region, high values of g_m/I_D ($> 20 \text{ V}^{-1}$) are reached [114-116], which is not observed in GFETs. We also note that g_m/I_D does not increase with shorter L for GFETs, as seen for Si MOSFETs [114]. However, g_m is a function of I_D and it is important to perform a controlled study where g_m is calculated at the same bias conditions, the same device structure and fabrication conditions. Interestingly, the lowest and highest points in Fig. 4.2(a) are calculated from the supplement of the same Ref. [95] at $L = 650 \text{ nm}$. Both cases have epitaxial graphene, which is usually inherently n-type. In the first case, Al_2O_3 gate dielectric adds additional n-type doping and shifts the charge neutrality point (V_{CNP}) far away (beyond -10 V) from zero gate voltage (V_G). On the other hand, a dielectric stack of Si_3N_4 compensates the original n-type doping and shows $\sim 6x$ higher peak g_m ($50x$ higher g_m/I_D) than the previous case. So graphene growth technique, selection of dielectric material, etc., play a crucial role in device performance. Another figure of merit is the transit frequency $f_T = g_m/2\pi C_{\text{gg}}$, which quantifies how much total gate capacitance (C_{gg}) is required to achieve the desired g_m . In Fig. 4.2(b) calculated f_T from our review is shown as a function of L . When C_{gg} was not directly reported in the reviewed papers, we calculate it from oxide thickness t_{ox} and established value of the dielectric constant. As we are using an approximated value for C_{gg} , we are denoting this frequency as f_T' . By scaling down L from $2 \mu\text{m}$ to 90 nm , we increase f_T' by an order of three.

4.2 Length Scaling Effect on Current Saturation

In order to understand the conditions which lead to the presence or lack of current saturation in the GFET experiments, we use our simulation platform [29, 52] which self-consistently solves the coupled electron and hole transport, Poisson equation, contact resistance,

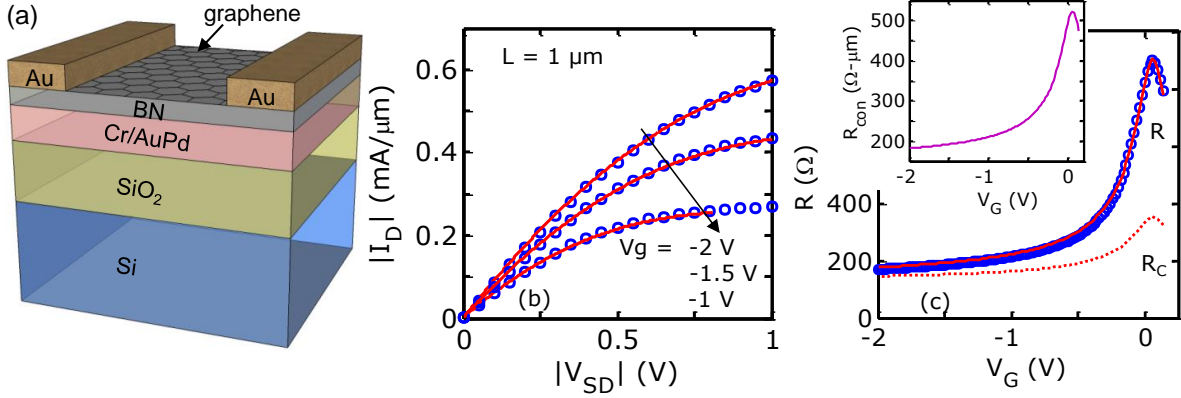


Figure 4.3: Schematic of simulated GFET device with top-gate or back-gate configuration. (b) Calibrating model at low-field (red lines) against graphene-on-BN experimental data (blue symbols) with high mobility ($\mu \sim 13,000 \text{ cm}^2/\text{V}\cdot\text{s}$) and good long-channel current saturation ($L = 1 \mu\text{m}$). Inset shows fitted bias-dependent contact resistance per unit width ($R_C \cdot W$), corresponding to graphene-metal contact resistivity $\rho_C = 150 \Omega \cdot \mu\text{m}^2$. (c) Calibrating model I_D - V_D (red lines) at high-field against measured data (blue) from the same study [41].

high-field velocity saturation (v_{sat}), and self-heating (SH) effects. We first calibrate this model to the experiments for graphene on hexagonal boron nitride (h-BN) [102], one of the few studies where current saturation was observed for sub-micron GFETs. Figure 4.3(a) shows the device structure considered where buried bottom electrode is used to gate the channel. Experimental data (blue circles) show excellent agreement with simulations (red lines) at both low-field and high-field transport in Figs. 4.3(b-c), with a calibrated mobility of $13500 \text{ cm}^2/\text{V}\cdot\text{s}$ and a puddle charge density is in order of 10^{10} cm^{-2} . The bias-dependent R_C in Fig. 4.3(c) accounts for electrostatics, current crowding and carrier density under the contact [70]. The inset shows the fitted bias-dependent contact resistance per unit width ($R_C \cdot W$). Thus the contact resistivity per unit area ($\rho_C = 150 \Omega \cdot \mu\text{m}^2$, unless stated otherwise) is the “correct” metric for the graphene-metal contact, a quantity which is independent of bias [70].

First we analyze the effect of L scaling on device performance utilizing our calibrated model. Output characteristics are shown in Fig. 4.4(a) for different channel lengths ranging from

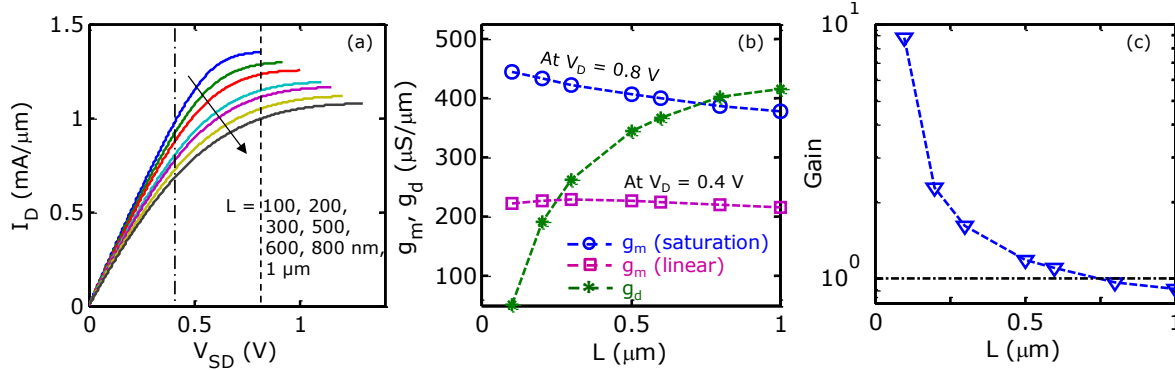


Figure 4.4: Simulated characteristics of graphene-on-BN device (see Fig. 4.3) here with contact resistivity of $\rho_C = 150 \Omega \cdot \mu\text{m}^2$. (a) Calculated I_D - V_D with channel L scaling. (b) Calculated g_m and g_d at $V_{SD} = 0.8 \text{ V}$. (c) Calculated gain, indicating that shorter devices *should* present advantages (e.g. saturation at low voltage). We note that this device had equivalent oxide thickness (EOT) $\sim 8 \text{ nm}$,¹⁰ thus the gain can in practice be further raised with a thinner EOT.

100 nm to 1 μm . The phonon mean free path in oxide-encased graphene is $\sim 16 \text{ nm}$ at room temperature, which is well below 100 nm. This allows us the use of our heat diffusion model in this length regime [117]. For all length cases, we kept a consistent vertical electric field of 2.3 MV/cm across the 8.5 nm thick h-BN dielectric, which is the buried back gate oxide. Shorter channel devices exhibit current saturation at lower V_{SD} . In Fig. 4.4(a) we find that for 100 nm long device, current saturation occurs at the lowest knee voltage of $V_{SD} = 0.8 \text{ V}$ [dashed line Fig. 4.4(a)]. In this case, we perform *lateral scaling* by varying the channel length, while keeping all the other parameters constant. Note that the lateral electric field varies for different channel lengths. We calculate g_m and g_d at the same $V_{SD} = 0.8 \text{ V}$ [Fig. 4.4(b)] and compare results. Both g_m (increases) and g_d (decreases) improve as we downscale L . Both trends contribute to achieve higher A_v values at smaller L . Devices with longer L saturate at higher V_{SD} as expected, hence g_d at a particular V_{SD} seems reduced. In Fig. 4.4(c), gain exceeds unity ($A_v > 1$) only when $L < 600 \text{ nm}$, which is due to the low value of g_d , as devices with shorter L saturate at lower V_{SD} (where we are calculating g_m and g_d , that is $V_{SD} = 0.8 \text{ V}$ for Fig. 4.4(a)). We also notice that g_m does not have a strong length dependence; it only varies by about 16% for $L = 100 \text{ nm}$ to 1 μm . We also

calculated g_m in the linear region at $V_{SD}=0.4$ V, as shown with a dashed-dot line in Fig. 4.4(b) with magenta squares, and found that the L dependence is as weak as observed for the saturation regime.

Next, we look at the case of a “perfect” contact ($\rho_C = 0 \Omega \cdot \mu\text{m}^2$) and show the output characteristics in Fig. 4.5(a) for several values of L . Figure 4.5(b) shows calculated g_m at both linear and saturation region. The g_m dependence as a function of L becomes stronger in the linear region, and we find a 60% decrease in g_m as we increase L from 100 nm to 1 μm . In Ref. [118] g_m suggested to be inversely proportional to L for GFET operation. However, we find that for high-field transport where velocity saturation plays a role, this inverse dependence on L no longer holds and the dependence becomes weaker. Only at the extreme case of zero contact resistance and at linear region of operation, we do see a two-fold change in g_m as we increase L from 100 nm to 1 μm .

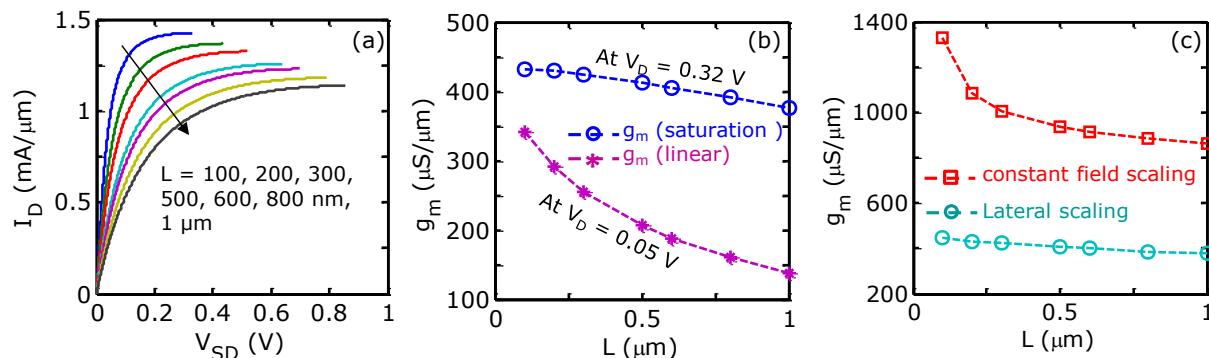


Figure 4.5: (a-b) For ideal contact ($\rho_C = 0 \Omega \cdot \mu\text{m}^2$) device, corresponding (a) I_D - V_{SD} , and (b) calculated g_m as a function of L , at linear region $V_{SD} = 0.05$ V (magenta star) and at lowest knee voltage of $V_{SD} = 0.32$ V (blue open circle), which corresponds to the current saturation in the device with $\rho_C = 0 \Omega \cdot \mu\text{m}^2$. (c) With contact resistivity of $\rho_C = 150 \Omega \cdot \mu\text{m}^2$ gm for constant field scaling (red) and only length scaling (teal).

There are some key differences between our work and Ref. [118], e.g., instead of using lumped contact resistance, we used bias-dependent R_C which has been extracted from the experimental data. Additionally, v_{sat} in our model is calibrated against the saturation region.

From this calibration we extract a phonon energy of $\hbar\omega_{\text{OP}} = 104$ meV. This value agrees well with lower SO phonon values used in the calculation of high-field operation of graphene on BN [28]. We also perform *constant field scaling*, where we scale the V_G , oxide thickness t_{ox} and L with same scaling parameter. Applied vertical field of 2.5 MV/cm is maintained consistently across the local buried gate dielectric. Similar trends are found for g_m but with a higher range of values for constant field scaling, as shown in Fig. 4.5(c). Note that in Fig. 4.5(c), R_C is included for both constant field and lateral scaling.

4.3 Contact Resistance Scaling

Up to this point, we have described electrical characteristics with contact resistivity values close to the lower end of the state-of-the-art devices [$\rho_C = 150 \Omega\cdot\mu\text{m}^2$, except for Figs. 4.5(a-b)] [119]. Now we study the effect of introducing higher contact resistances up to $500 \Omega\cdot\mu\text{m}^2$. Figures 4.6(a-b) show the I_D - V_{SD} characteristics for two devices with $L = 200$ nm and $1 \mu\text{m}$, respectively, where the change of contact resistance affects the linear regime and the onset of the saturation. We evaluate g_m , g_d and A_v for these devices at the bias point corresponding to the current saturation in the device with $\rho_C = 0 \Omega\cdot\mu\text{m}^2$. These voltages are 0.45 V and 0.65 V for $L = 200$ nm and $1 \mu\text{m}$, respectively. Figures 4.6(c-e) show g_m , g_d and A_v as a function of contact resistance. As expected, improvement in g_m is observed when we reduce ρ_C from $500 \Omega\cdot\mu\text{m}^2$ to an “ideal contact” ($\rho_C = 0 \Omega\cdot\mu\text{m}^2$). However, as ρ_C increases, the 200 nm device goes from the saturation into the linear regime, which is accompanied by an increase of g_d . Beyond this point, further increase of ρ_C leads to a decreased I_D - V_{SD} slope, which results in a decrease of g_d , as shown in Fig. 4.6(d). Both the increase of g_d and decrease of g_m contribute to a strong gain degradation when ρ_C increases, as shown in Fig. 4.6(e). The effect of ρ_C on g_d is quite significant and is worse at short L . The fact that g_d gets much worse for shorter length devices is reflected

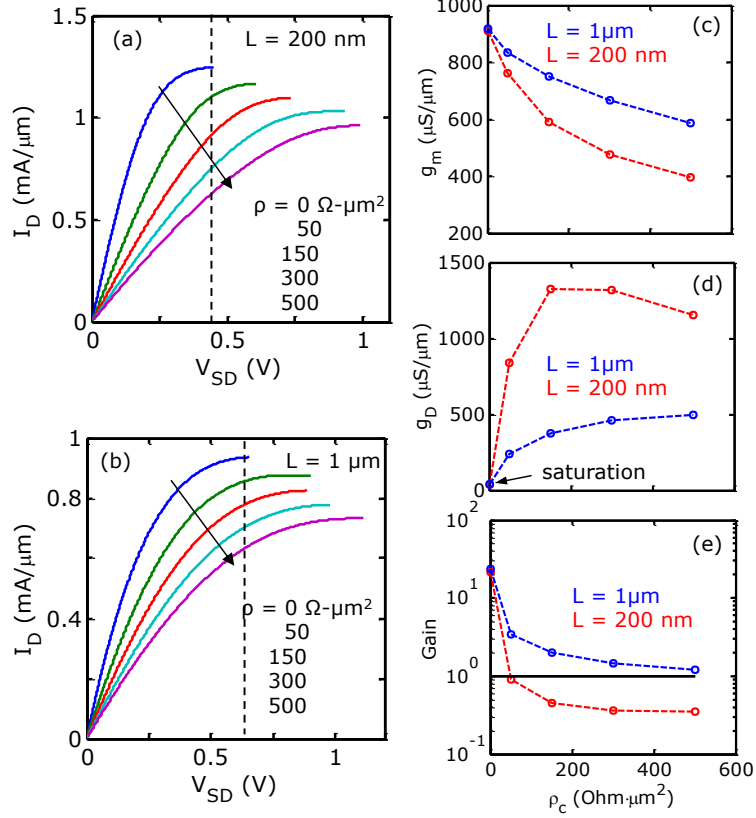


Figure 4.6: Computed I_D - V_{SD} characteristics for channel lengths (a) $L = 200$ nm and (b) $L = 1$ μm , with contact resistivity $\rho_C = 0, 50, 150, 300, 500$ $\Omega\cdot\mu\text{m}^2$. The left-most curve represents the ideal scenario with zero contact resistance ($\rho_C = 0$), reaching saturation at ~ 0.3 and 0.6 V, respectively. (c-e) Computed g_m , g_D and intrinsic gain at constant voltage $V_{SD} = 0.5$ V for $L = 200$ nm, and $V_{SD} = 0.9$ V for $L = 1$ μm device. g_D is worse for an intermediate ρ_C value (see text). In all cases, gain is highest with $\rho_C = 0$.

in the A_v vs. ρ_C plot in Fig. 4.6(e), which shows higher gain for longer L devices. However, using longer devices results in larger operating voltages, which is also far from ideal.

4.4 Self-Heating Effect on Output Conductance

Finally, in Fig. 4.7 we examine the role of self-heating (SH) at high bias on I_D saturation, output conductance and gain. Here we examine devices of channel lengths ranging between 200 nm and 1 μm on SiO_2 substrates. We chose SiO_2 instead of h-BN, since temperature-dependent data is available for this case [29, 52]. From these simulations, we observe better I_D saturation

when SH is taken into account [120]. The role of SH on g_d is shown in Fig. 4.7(b), where thicker buried oxide (t_{box}) leads to better I_D saturation (lower g_d). Interestingly, the SH effect is stronger for the longer channel devices ($L = 1 \mu\text{m}$), since short-channel devices ($L = 200 \text{ nm}$) sink more heat into its contacts during operation [120].

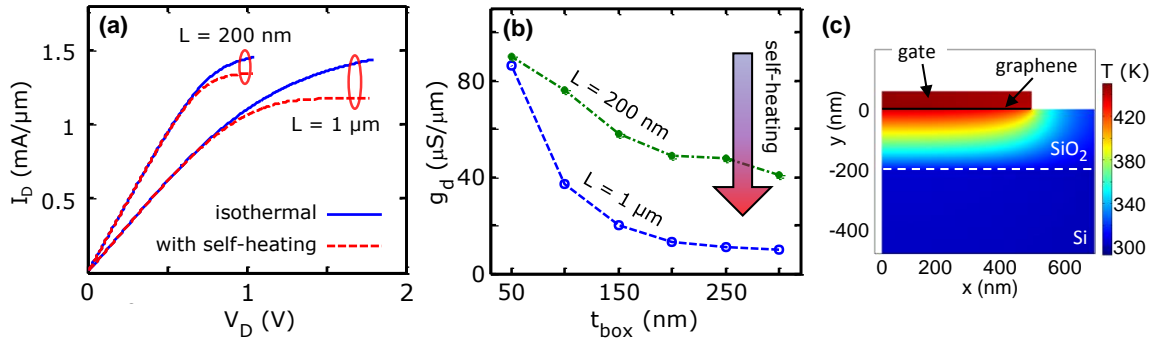


Figure 4.7: Effect of self-heating (SH) on current saturation for GFETs on SiO_2 , using model fit against temperature-dependent data^{24, 25} (we note that cross-plane thermal conductivity of BN is comparable to that of SiO_2 or SiN .) (a) Computed I_D - V_{SD} with SH (dashed red) and without (solid blue) for $L = 200 \text{ nm}$ and $1 \mu\text{m}$ on $t_{\text{box}} = 300 \text{ nm}$ (see Fig. 4.2a). (b) SH effect on output conductance g_d as a function of buried oxide thickness. SH effect is weaker for the shorter device ($L = 200 \text{ nm}$), which sinks more heat into its source and drain contacts. (c) Cross-section of GFET showing temperature rise due to SH during operation. (Here, for all cases $V_G = 4 \text{ V}$ and $\rho_C = 200 \Omega \cdot \mu\text{m}^2$ was used.)

4.5 Conclusion

In conclusion, we presented a comprehensive study of I_D saturation and gain in GFETs. We find that better I_D saturation and gain can be obtained in short- L devices only if the contact resistivity ρ_C is significantly reduced below present state-of-the-art values (few hundred $\Omega \cdot \mu\text{m}^2$). From our survey we find that besides contact resistance, issues like dielectric depositions (top gated or only back gated), optimized gate control over graphene channel (i.e. gate overlap/underlap) etc., also play a role in determining device performance. Interestingly, self-heating can also be used to improve I_D saturation in longer- L devices; however this may not be a very robust approach due to potential oxide reliability issues. In practice, with very few

exceptions [98], short-channel GFETs [96-102] have not yet observed good saturation and gain due to ρ_C and self-heating which limits the maximum voltages applied during measurement. This study serves to identify such obstacles and guide future work towards much improved GFETs.

Chapter 5

SUBSTRATE-DEPENDENT VELOCITY SATURATION

The performance of graphene field-effect transistors (GFETs) strongly depends on the interfaces between the graphene layer and the supporting and top gate dielectrics. In this study, we combine our simulation approach [120] with new and existing experimental data to provide the first detailed analysis and comparison of the high-field properties of graphene on hexagonal boron nitride (h-BN) [102, 121], on HfO₂ (examined here for the first time) and on SiO₂ [24]. These substrates each present unique scenarios because they have different (remote) phonons and different thermal conductivities (k), all of which influence high-field transport in GFETs.

5.1 Electro-Thermal Simulations and Data Calibrations

We use an existing simulation platform [120] which self-consistently couples electron and hole transport, the Poisson equation, contact resistance, velocity saturation (v_{sat}), and self-heating (SH) effects. Experimental and simulated devices have the schematic shown in Fig. 5.1(a), where graphene is sitting on 8.5 nm of h-BN (effective oxide thickness, EOT is 10 nm) serving as the substrate as well as dielectric material. The structure consists of a Cr/AuPd (1 nm/20 nm) localized buried gate and 285 nm thick SiO₂ substrate. This buried gate with BN dielectric structure is one of the few studies available in literature where current saturation was observed for sub-micron GFETs [102, 121]. First, we analyze the low field transport of two GFETs on BN with device length (L) of 1 μm (grey circle) and 3 μm (magenta circle) as shown in Fig. 5.1(b). The bias-dependent contact resistances R_c , which accounts for current crowding and carrier density under the contact [78] are shown in inset of Fig. 5.1(b). The extracted contact resistivities per unit area (ρ_C) for $L = 1$ and 3 μm are 150 and 260 $\Omega \cdot \mu\text{m}^2$, respectively. Figures

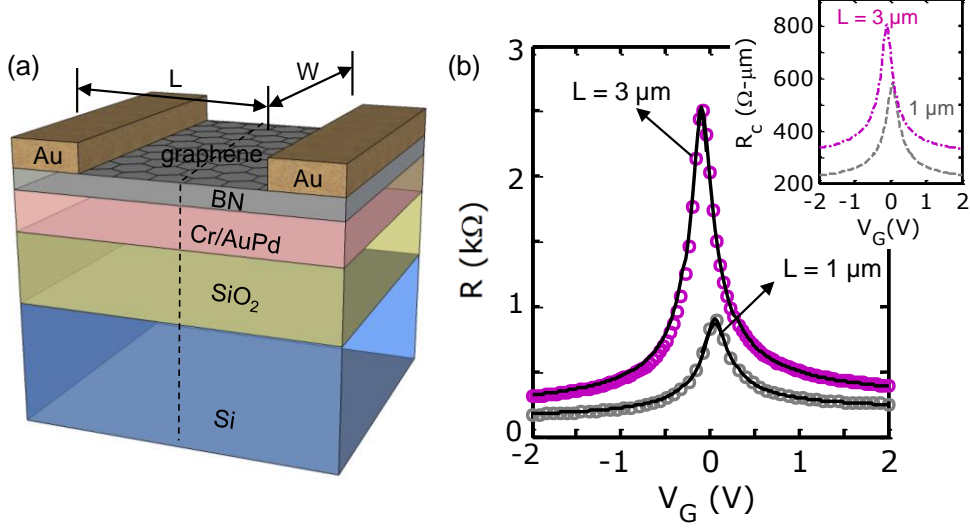


Figure 5.1: (a) Schematic of simulated GFET device with localized buried back-gate configuration. (b) Calibrating model at low-field (black lines) against graphene-on-BN experimental data for $L = 3 \mu\text{m}$ (magenta symbols) and $L = 1 \mu\text{m}$ (grey symbols) [102]. Extracted mobility is $12000 \text{ cm}^2/\text{V}\cdot\text{s}$ for $L = 3 \mu\text{m}$ and $13500 \text{ cm}^2/\text{V}\cdot\text{s}$ for $L = 1 \mu\text{m}$ device. (c) Extracted bias-dependent contact resistance (Ω) from R - V_g fitting in (b). Corresponding to graphene-metal contact resistivity $\rho_c = 260$ and $150 \Omega\cdot\mu\text{m}^2$ for $L = 3$ and $1 \mu\text{m}$ respectively.

5.2(a-b) show that upon model calibration, simulations (lines) reach excellent agreement with experimental data (symbols) at high-field transport. The values of extracted hole mobility are $\mu = 13,500 \text{ cm}^2/\text{V}\cdot\text{s}$ and $12,000 \text{ cm}^2/\text{V}\cdot\text{s}$, for $L = 1 \mu\text{m}$ and $3 \mu\text{m}$ devices, respectively, and the impurity density at the graphene and BN interface is on the order of 10^{10} cm^{-2} . The measured dielectric constant is found to be in the range of 3 to 3.5 and we use 3.5 for our calculation. High-field simulations include an analytic v_{sat} expression (similar as in in Ref. [24]) with temperature dependence (due to SH), carrier density dependence, and dominant optical phonon energy ($\hbar\omega_{\text{OP}}$). We fit our model to the high-field transport using a generic form of v_{sat} ,

$$v_{\text{sat}} = \frac{\omega_{\text{OP}}}{\pi\sqrt{n+n_{\text{ref}}}} \frac{1}{N_{\text{OP}}+1} \quad (19)$$

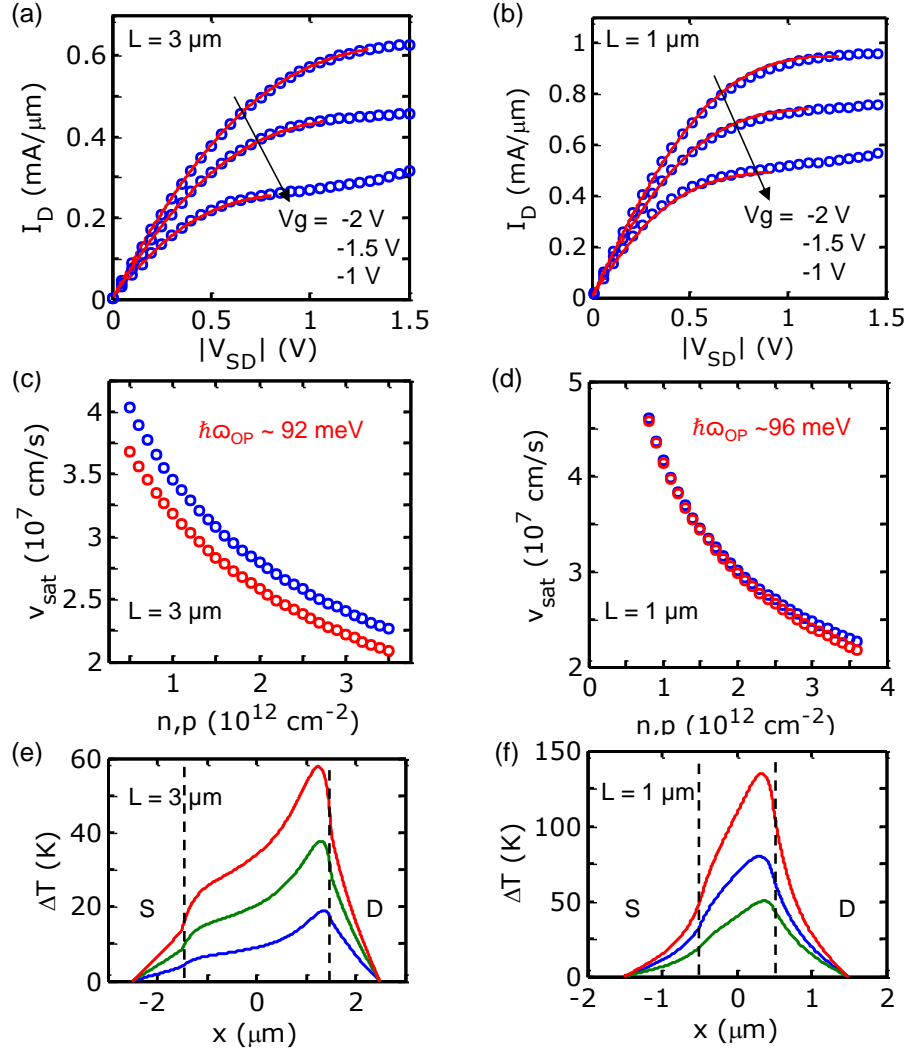


Figure 5.2: Calibrating model for I_D - V_D (red lines) at high-field against graphene-on-BN experimental data (blue) from the same study as Fig. 5.1 [102] for (a) $L = 3 \mu\text{m}$ and (b) $L = 1 \mu\text{m}$. Extracted model for saturation velocity as function of carrier density of the channel. Both temperature-dependent (red) and constant temperature (blue) extraction were fitted with phonon energy of 92 and 96 meV for (c) $L = 3 \mu\text{m}$ and (d) $L = 1 \mu\text{m}$ respectively. (e,f) Temperature profile along the channel for $L = 3, 1 \mu\text{m}$ device.

where n is the carrier density, $N_{OP} = 1/[\exp(\hbar\omega_{OP}/k_B T) - 1]$ is the phonon occupation and $n_{\text{ref}} \sim 1 \times 10^{11} \text{ cm}^{-2}$ is a fitting parameter. This expression has an inverse dependence on the square root of carrier density which is used in the literature to analyze the experimental data [41, 102, 122]. Figure 5.2(c-d) show v_{sat} as a function of carrier density in the channel, corresponding to the highest V_{SD} of the simulated I_D of Fig. 5.2(a-b). Optical phonon energies are fitted with $\hbar\omega_{OP} =$

92 and 96 meV for $L = 3$ and $1 \mu\text{m}$, respectively, which is very similar to the numerically calculated surface polar phonon (SPP) energy for BN, ~ 102 meV [28]. According to infrared data [123], ab-initio [124] and other [125] calculation, this phonon energy corresponds to ZO mode in phonon dispersion for h-BN. The red and blue open circles correspond to v_{sat} with and without self-heating effect added into simulation, respectively. Both temperature-dependent and independent fittings were possible just by tweaking the phonon energy by $\sim 4\%$. Temperature profile along the channel is shown in Figs. 5.2(e-f) for $L = 3$ and $1 \mu\text{m}$. Higher drain current in $1 \mu\text{m}$ long device than the $3 \mu\text{m}$ one corresponds to the higher temperature rise (ΔT) in Fig. 5.2(f).

Due to the close proximity to a polar substrate with a graphene layer, and small vertical dimension, SPP scattering in graphene can be the dominating scattering mechanism. Our extracted phonon energies from v_{sat} are similar to the SPP energies, suggesting that this inelastic nature of SPP is playing the prominent role to achieve the current saturation. Some uncertainty in the extraction of contact resistivity ρ_C affects the extraction of $\hbar\omega_{OP}$ from I_D - V_{SD} characteristics, which is explored in Fig. 5.3(a) for an extended range of carrier density. The variation in v_{sat} for

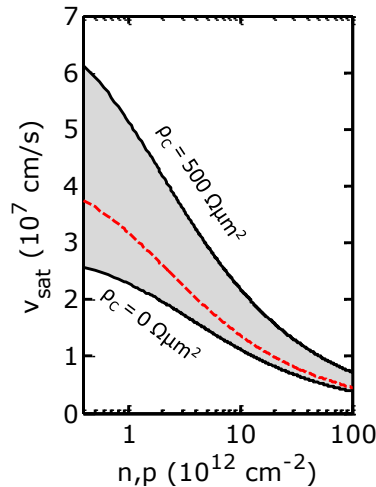


Figure 5.3: Saturation velocity for a broader range on carrier density of $L = 3 \mu\text{m}$ long device with BN as insulating layer error bar added for a range of contact resistivity from 500 to $0 \Omega\mu\text{m}^2$. The red dashed line represents the extracted $\rho_C = 260 \Omega\mu\text{m}^2$.

$\rho_C = 0$ to $500 \Omega \cdot \mu\text{m}^2$ is shown by the shaded grey region in Fig. 5.3. For example, at a carrier density of $5 \times 10^{12} \text{ cm}^{-2}$, the variation was found to be $\sim 50\%$.

Next, we perform FEM simulations implemented by the COMSOL software to investigate the high-field, high-temperature regime, as shown in Fig. 5.4. Simulated structure in Fig. 5.4(a) is similar to the schematic in Fig. 5.1(a) along the dashed line. The static heat conduction equation is solved along the cross-section marked by the dashed line in Fig. 5.1(a) as shown in Fig. 5.4(a). Due to the symmetry, only one-half of the cross-section needs to be simulated.

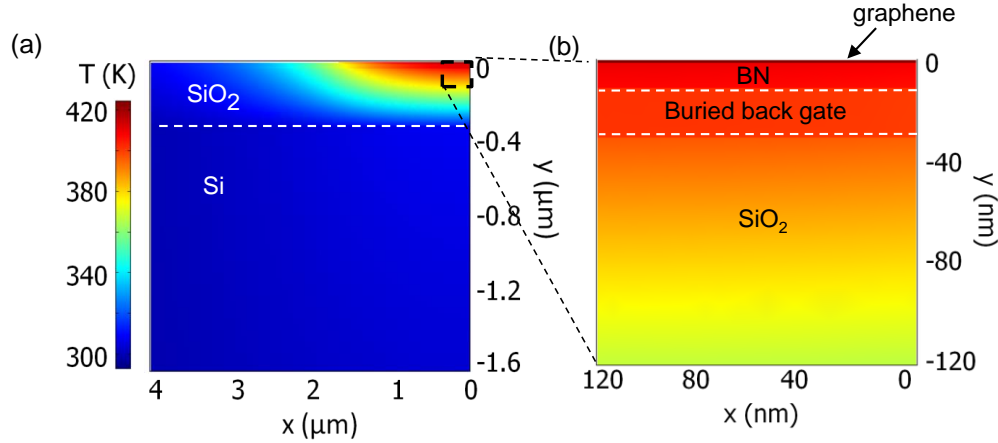


Figure 5.4: Cross-sectional steady-state temperature profiles obtained from FEM simulations with an input power of 0.5 mW in a $1 \times 0.5 \mu\text{m}^2$ graphene sheet. Here device structure is (a) similar to buried back gated device shown in Fig. 5.1a. Here graphene device with 10 nm BN as insulator layer, 20 nm of buried Au gate in on 300 nm SiO₂. (b) Zoomed in version of the dashed square shown in (a).

An isothermal boundary condition ($T = T_0 = 20 \text{ }^\circ\text{C}$) is applied at the bottom and the right edge of the Si substrate, while all other boundaries of the device are assumed to be adiabatic. An input power of 2 mW is applied to the half graphene channel. A zoomed version of the dashed square in Fig. 5.4(a) is shown in Fig. 5.4(b), where the temperature distribution between different layers is visible.

Boron nitride can take different crystalline forms such as wurtzite, zinc blende and hexagonal. As for our dielectric, we had hexagonal form of BN, which shows strong anisotropy in thermal conductivity (k_{BN}). We account for the highly anisotropic $k_{\text{BN},i} = 400 \text{ Wm}^{-1}\text{K}^{-1}$ (in plane) [126] and $k_{\text{BN},c} = 3 \text{ Wm}^{-1}\text{K}^{-1}$ (out of plane) [127] in our simulation. A recent study has reported different numbers for these values [128], which might be misleading to capture the self-heating effect in the device. Due to the higher lateral k_{BN} , a clear heat spreading along the channel is evident in Fig. 5.4(a).

Next, we examine the data for a GFET on 12 nm thick HfO_2 (EOT = 3.6 nm), both for low and high fields. The geometry is the same as shown in Fig. 5.1(a). Black solid line in Fig. 5.5(a) shows a good agreement with the experimental data (symbols). Inset shows the bias-dependent contact resistance R_c with the extracted contact resistivity per unit area (ρ_c) of $200 \text{ }\Omega\cdot\mu\text{m}^2$. The extracted mobility is $\sim 600 \text{ cm}^2/\text{V}\cdot\text{s}$, which is significantly lower than that of on BN. From the high-field data, saturation is found to be rather weak (Fig. 5.5(b)). To fit the high-field data, we used a carrier-dependent mobility with an expression of $\mu = \mu_0/(1+n/n_{\text{ref}})$ and fitted it to a value of $n_{\text{ref}} = 3.3 \times 10^{13} \text{ cm}^{-2}$. Constant mobility fitting is also possible by changing the v_{sat} with 10% lower values of the phonon energies for both with and without temperature added into calculation, but the fit is much better for the case of carrier-dependent mobility.

As for v_{sat} , we use the same expression as Eq. (19) for fitting and the extracted phonon energy is found to be $\hbar\omega_{\text{OP}} \sim 34 \text{ meV}$. Interestingly, this number falls in between the theoretically calculated phonon energies for HfO_2 . From different theoretical studies, SPP energy for HfO_2 has been reported [28, 58, 129] to have values of $\sim 21.6 \text{ meV}$ from low frequency Raman spectra and $\sim 54.2 \text{ meV}$ for high frequency Raman spectra. So our analysis indicates that both of the components contribute in scattering for graphene on HfO_2 . Velocity saturation calculated at the

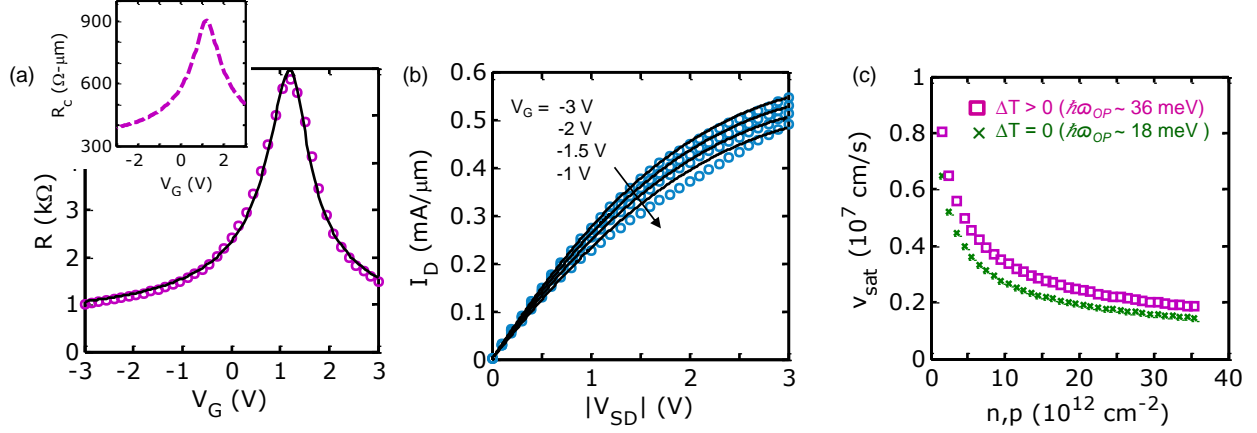


Figure 5.5: Low-field calibration (black line) against experimental data (magenta symbols) for graphene on 12 nm thick HfO₂ with $L/W = 3/3.4 \mu\text{m}$. Extracted mobility is $\sim 600 \text{ cm}^2/\text{V}\cdot\text{s}$ for both electron and hole transport. Carrier-dependent mobility is used for best fitting. Corresponding to graphene-metal contact resistivity is $\rho_C \sim 200 \Omega\cdot\mu\text{m}^2$. Inset: The gate bias-dependent contact resistance ($\Omega\cdot\mu\text{m}$) is shown with magenta dashed line. (b) High-field calibration (black line) against experimental data (blue symbol) at gate bias = -3, -2, -1.5 and -1 V. (c) Extracted saturation velocity as function of carrier density. Temperature-dependent (magenta square) and independent (green triangle) extraction for $\hbar\omega_{\text{OP}} = 36, 32 \text{ meV}$ respectively.

highest drain voltage ($V_{\text{SD}} = 3 \text{ V}$) of Fig. 5.5(b), is shown as a function of carrier density in Fig. 5.5(c). The magenta squares and green crosses correspond to v_{sat} with and without self-heating effect added into the simulation and fitted with phonon energies of 36 meV and 18 meV, respectively. Unlike BN, temperature-dependent vs. independent fitting requires quite different value of phonon energies for HfO₂. Comparing with the data for GFET on BN, data for HfO₂ is at higher field of $1 \text{ V}/\mu\text{m}$, which corresponds to higher power of $1.6 \text{ mW}/\mu\text{m}$, hence higher temperature. As a comparison, at $V_g = -2 \text{ V}$ for device $L = 3 \mu\text{m}$ on BN, peak power is $0.9 \text{ mW}/\mu\text{m}$. Thus temperature effect is more prominent in this case for phonon energy extraction.

At room temperature, thermal conductivity of thick ($> 500 \text{ nm}$) microcrystalline HfO₂ films with 3ω measurements is $1.2 \text{ Wm}^{-1}\text{K}^{-1}$ [130]. As in our structure HfO₂ is 12 nm, we use a reduced thermal conductivity of 0.9 [131]. While graphene shows high velocity saturation when

on BN, this is not the case on HfO₂. With the presence of these low energy SPP phonons in HfO₂, much stronger remote phonon scattering limits the v_{sat} to a $\sim 5\times$ lower value.

5.2 Velocity Saturation Comparison

Finally, in Figs. 5.6(a-b) we compare the velocity-field extracted here on BN and HfO₂ with existing data on SiO₂, [24] at two carrier densities of 10^{12} and 10^{13} cm⁻². Among three cases, graphene on BN shows an immediate rapid rise in the velocity due to the high mobility. We find that v - F model for graphene on BN and SiO₂ are quite close while the drift velocity for graphene on HfO₂ is much lower. A strong ionic polarization in HfO₂ also gives rise to a very strong scattering process for the carrier in graphene. With much lower SPP energy, HfO₂ is subjected to much stronger remote phonon scattering, which results in low velocity and is consistent with other theoretical study [132]. The dependence of v_{sat} on carrier density n is shown in Fig. 5.6(c), where scattered points are directly extracted from the experimental data as described above, and dashed lines are the analytic v_{sat} model from Eq. (19) and Ref. [24], with the calibrated parameters. From our simulations graphene on BN is subjected to a higher SPP energy of 94meV than on SiO₂, which has a value of 81meV. However, we find that, instead of having higher values at all carrier densities, the v_{sat} model of BN dielectric shows either similar or even lower values. This result can be explained by the fact that, as the interface between graphene and BN is much smoother than SiO₂ [133], the reduced inter atomic distance is causing graphene electrons to be more strongly influenced by the SPP. That is why ultimately v - F is very similar for BN and SiO₂ dielectrics. Interestingly, we find that v_{sat} on BN and on SiO₂ are similar at high carrier density, where screening of SPPs by charge carriers should be more important. The v_{sat} for graphene on HfO₂ remains $\sim 5\times$ lower for all carrier densities.

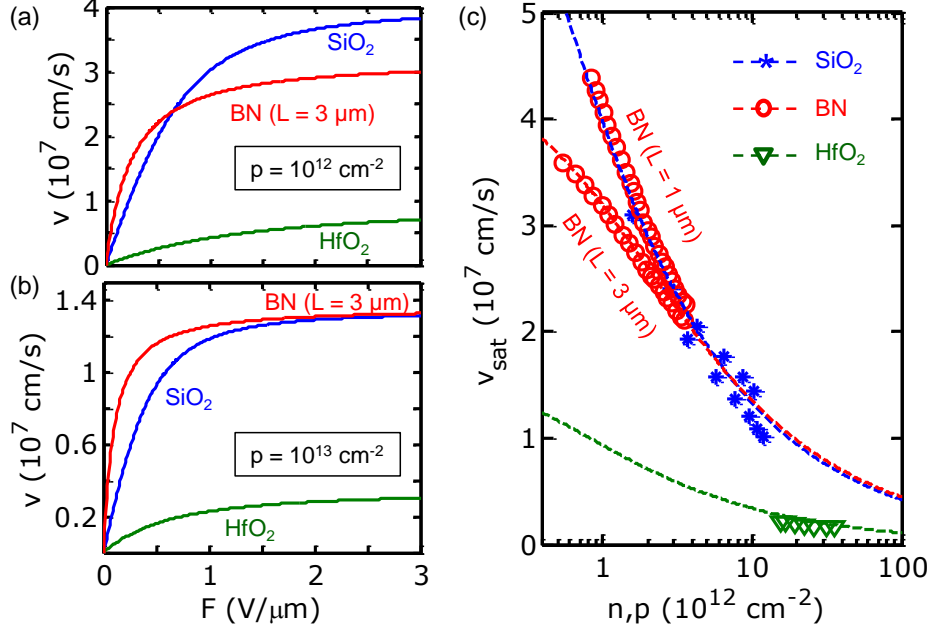


Figure 5.6: Comparison of field-velocity model for graphene on SiO₂ (blue), BN (red) and HfO₂ (green) at carrier density of (a) $1 \times 10^{12} \text{ cm}^{-2}$ and (b) $1 \times 10^{13} \text{ cm}^{-2}$. (d) Comparing saturation velocity of on SiO₂ (blue, star) [24], BN (red, circle) and HfO₂ (green, triangle) for a larger range of carrier density. Dashed lines represent simulation results and symbols are the extraction from high-field data.

5.3 Conclusion

To summarize, we investigated high-field transport in graphene on BN, HfO₂ and SiO₂ dielectrics through extensive calibration with both low and high-field experimental data, including the role of (anisotropic) self-heating. It is found that for graphene on BN, extracted $\hbar\omega_{OP}$ (~ 94 meV) and v_{sat} are similar to those of graphene on SiO₂. However, on HfO₂, $\hbar\omega_{OP}$ has a significantly lower value of 34 meV and v_{sat} is also $\sim 5x$ lower than graphene on BN/SiO₂. These results are important for the optimization and physical analysis of graphene devices in contact with various dielectrics, operating at realistic fields and temperatures.

Chapter 6

GRAPHENE TRANSISTOR ON FLEXIBLE SUBSTRATE

Recently, GFET on flexible substrates attracted considerable attention, with materials like polyimide (PI) [134-136], polyethylene naphthalate (PEN) [137, 138] being used as substrates. It is desirable for flexible electronics to achieve excellent mechanical robustness, flexibility and electronic functionality, as well as an ability to perform under high bias condition. The flexible substrates having inherently inferior thermal conductivity are often subjected to thermal breakdown at high-field operation. We extend our study to analyze data for GFET on flexible substrate at high-field operation. Finally, we conduct a comprehensive study on the effect of different combinations of bottom dielectric and substrate on temperature profile of a GFET device.

6.1 Electro-Thermal Simulations for Graphene on Flexible Substrate

While the preceding sections of this paper focused on velocity saturation and corresponding phonon energies for GFETs on BN and HfO₂, GFET on flexible plastic substrates are explored next. We analyze the data from Lee *et al.*, which is one of the very few experimental studies where saturation is achieved on a flexible substrate [134]. Flexible plastic substrate material like polyimide (PI) has glass transition temperature (T_{gt}) ranging from 250 to 320 °C [139, 140] and low thermal conductivity $k_{PI} \sim 0.5$ W/m·K [141, 142]. These properties cause high temperature rise in the device, which plays a crucial role by eventually resulting in physical deformation. This is a well-experienced phenomenon associated with flexible substrate that restricts us to do high-field measurement for graphene devices [143], as well as other general devices [143, 144].

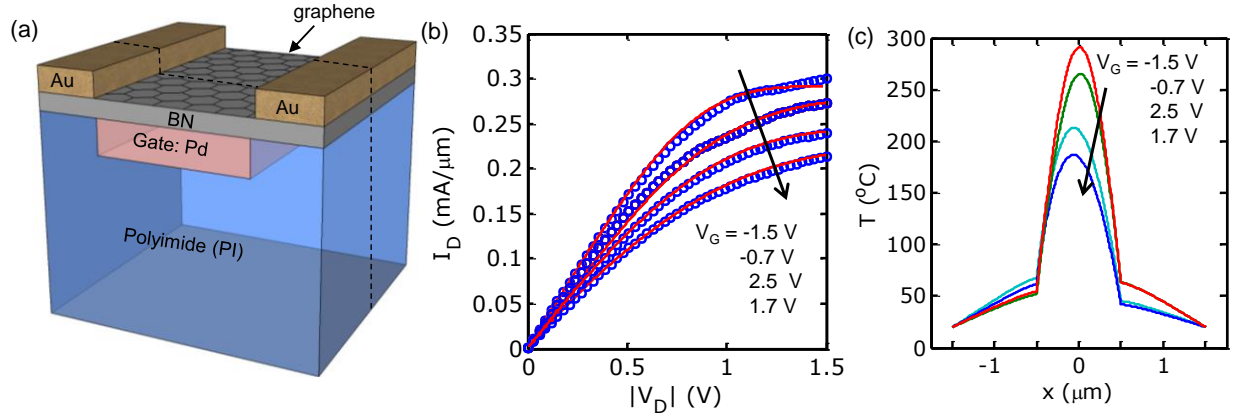


Figure 6.1 Schematic of simulated GFET device with BN bottom dielectric and Pd localized buried back gate. (b) Calibrating model for I_D - V_{SD} (red lines) at high-field with experimental data (blue open circle) [145] for $L = 1 \mu\text{m}$ device at different gate voltages. (c) Simulated temperature profile along the channel corresponding to V_G as in (b).

Figure 6.1(a) shows the schematic of the simulated device. Here graphene is on 19 nm thick BN working as a gate dielectric. The substrate is 20 μm thick flexible PI and the device is gated by 50 nm thick Pd localized buried back gate. The source and drain contacts are 50 nm thick Au. Details of the fabrication process can be found in Ref. [134]. Using our simulation platform described above, we analyze the data for both low and high-field transport. We use a carrier and temperature-dependent mobility model of equation (5) from Ref. [24], where $\mu_0 = 1700 \text{ cm}^2/\text{V} \cdot \text{s}$, $n_{\text{ref}} = 5 \times 10^{12} \text{ cm}^{-2}$, $\alpha = 2$, $T_{\text{ref}} = 220 \text{ K}$ and $\beta = 2.2$. In Fig. 6.1(b), the I_D - V_{SD} data is shown with blue open circle symbol and simulation results are shown with red lines at different gate biases (V_G). The extracted $\hbar\omega_{\text{op}}$ is 90 meV for high-field I_D - V_{SD} simulation, which is similar to our extracted number in previous section. However the impurity density at graphene and BN interface is in order of 10^{11} cm^{-2} , which is 10x higher than our previous extraction. This might be occurring due to wet transfer, lack of annealing etc. The temperature rise along the channel is shown in Fig. 6.1(c), which corresponds to V_G values, as shown in Fig. 6.1(b).

Next, in Fig. 6.2, a 3D thermal simulation by COMSOL is performed for the device structure as shown in Fig. 6.2(a). Due to symmetry half of the device is simulated, along the dashed line of Fig. 6.1(a). Isothermal boundary conditions (base temperature $T_0 = 20\text{ }^\circ\text{C}$) are applied at the back and bottom surfaces of the substrate, while the other boundaries are adiabatic. An input power of 4.5 mW is applied to graphene and peak temperature (T_{peak}) is $283\text{ }^\circ\text{C}$. This is the maximum power applied to the experimental device, which corresponds to the $V_G = -1.5\text{ V}$. At this V_G , ΔT calculated by our drift-diffusion model is $290\text{ }^\circ\text{C}$ (red curve in Fig. 6.1(c)). So our drift-diffusion calculation and COMSOL model agree very well. Anisotropic thermal conductivity is used for BN as mentioned in the previous section. This temperature rise is within the safe range ($\Delta T < T_{\text{gtt}}$) and we do not observe any thermal deformation for this device. In

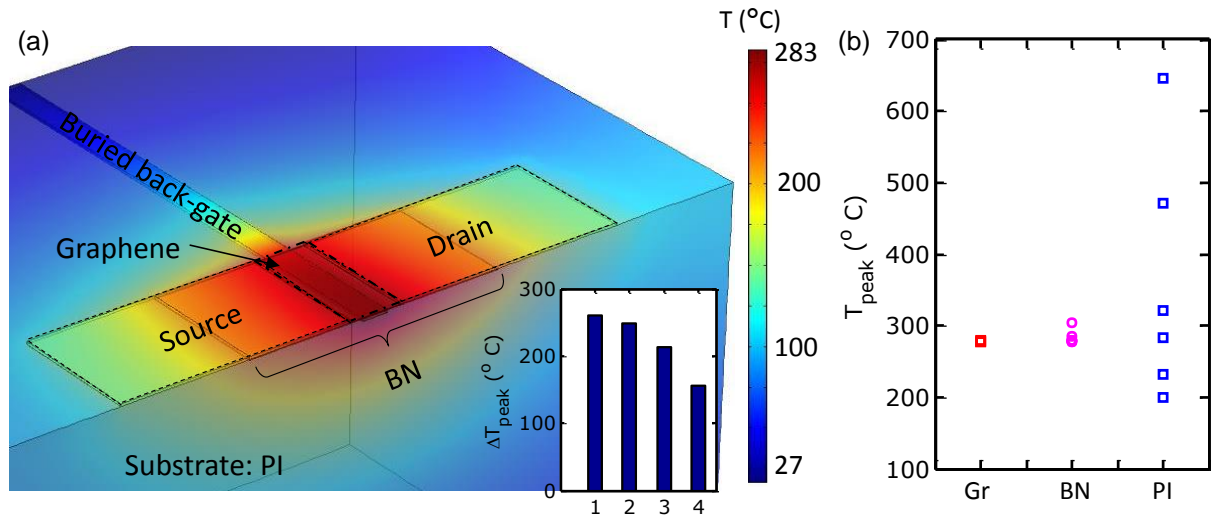


Figure 6.2: (a) FEM simulation of the device as shown in Fig. 6.1(a). An input power of 4.5 mW is applied to graphene as shown with an arrow. Inset: Peak temperature from FEM simulation for different combination of components as shown in (a). X-axis numbers corresponds to: 1: Gr+BN, 2: Gr+BN+BG, 3: Gr+BN+BG+SD (Pd) and 4: Gr+BN+BG+SD (Au). Here Gr: graphene, BN: BN layer, BG: back-gate, SD: source-drain. Right-most two bars are for the same structure; one with Pd electrodes another with Au. All of the structures are on PI substrate. (b) Peak temperature sensitivity on variation of thermal conductivity of graphene, BN and PI layer.

addition, we notice that heat is spreading along the palladium back-gate, which has a k_{Pd} of ~ 72 W/m·K [146].

To study the thermal contribution from each component of graphene, BN layer, back-gate (BG) and source-drain (SD), we add them layer-by-layer and list the ΔT_{peak} in the inset of Fig. 6.2(a). If we apply a power of 4.5 mW in a $2 \times 10 \mu\text{m}^2$ graphene sheet sitting directly on PI substrate, the T_{peak} is 825 °C (not shown in the inset). Addition of the 20 nm BN layer with high lateral k_{BN} results in a $\sim 55\%$ reduction in the T_{peak} . Addition of the electrodes contributes in the heat spreading and further reduces the ΔT_{peak} . Replacing the electrode material Pd with a higher thermally conductive material like Au results in the lowest ΔT_{peak} (shown in 4th column).

A range of thermal conductivities has been reported for PI, BN and graphene material. Thermal conductivity of PI and graphene ranges from 0.2 to 1 W/m·K [141, 142] and 400 to 1000 W/m·K [32, 147], respectively. For BN, in plane $k_{\text{BN},i}$ ranges from 30 to 400 W/m·K [126, 148] and for out of plane $k_{\text{BN},c}$ it is from 1.5 to 3 W/m·K [127, 149]. Using our thermal model we study the sensitivity of rise of T_{peak} on thermal conductivity of different layers. We keep $k_{\text{BN},c} = 3$ W/m·K when we vary $k_{\text{BN},i}$, and $k_{\text{BN},i} = 400$ W/m·K for vice versa. Varying k for these three materials, we get T_{peak} variation as shown in Fig. 6.2(b). The change is threefold for the variation of k_{PI} , where in case of k_{BN} variation its 25%. However varying the k_{gr} does not have significant impact on T_{peak} . In order to keep the flexibility of the electronics, options are limited to add different material layers for heat sinking. So the material type or quality of the plastic substrate is found to be the dominant factor affecting T_{peak} .

6.2 Thermal Breakdown

The SEM image of a similar buried gate device structure but with Al_2O_3 dielectric material and 10-finger electrode configuration is shown in Fig. 6.3(a-b). Each device is $0.5 \mu\text{m}$

long and 10 μm wide. The thermal conductivity of amorphous Al_2O_3 , $k_{\text{Al}_2\text{O}_3}$ is $\sim 2 \text{ W/m}\cdot\text{K}$ [150], which is much lower than BN. This lower $k_{\text{Al}_2\text{O}_3}$ leads to a thermal breakdown that causes physical deformation [151, 152]. The physical condition before and after applying high-field bias is shown in Figs. 6.3(a-b), respectively. A zoomed version of the damaged device is shown in the inset. An abrupt breakdown occurs at field $>1 \text{ V}/\mu\text{m}$ and the device is damaged and wrinkled.

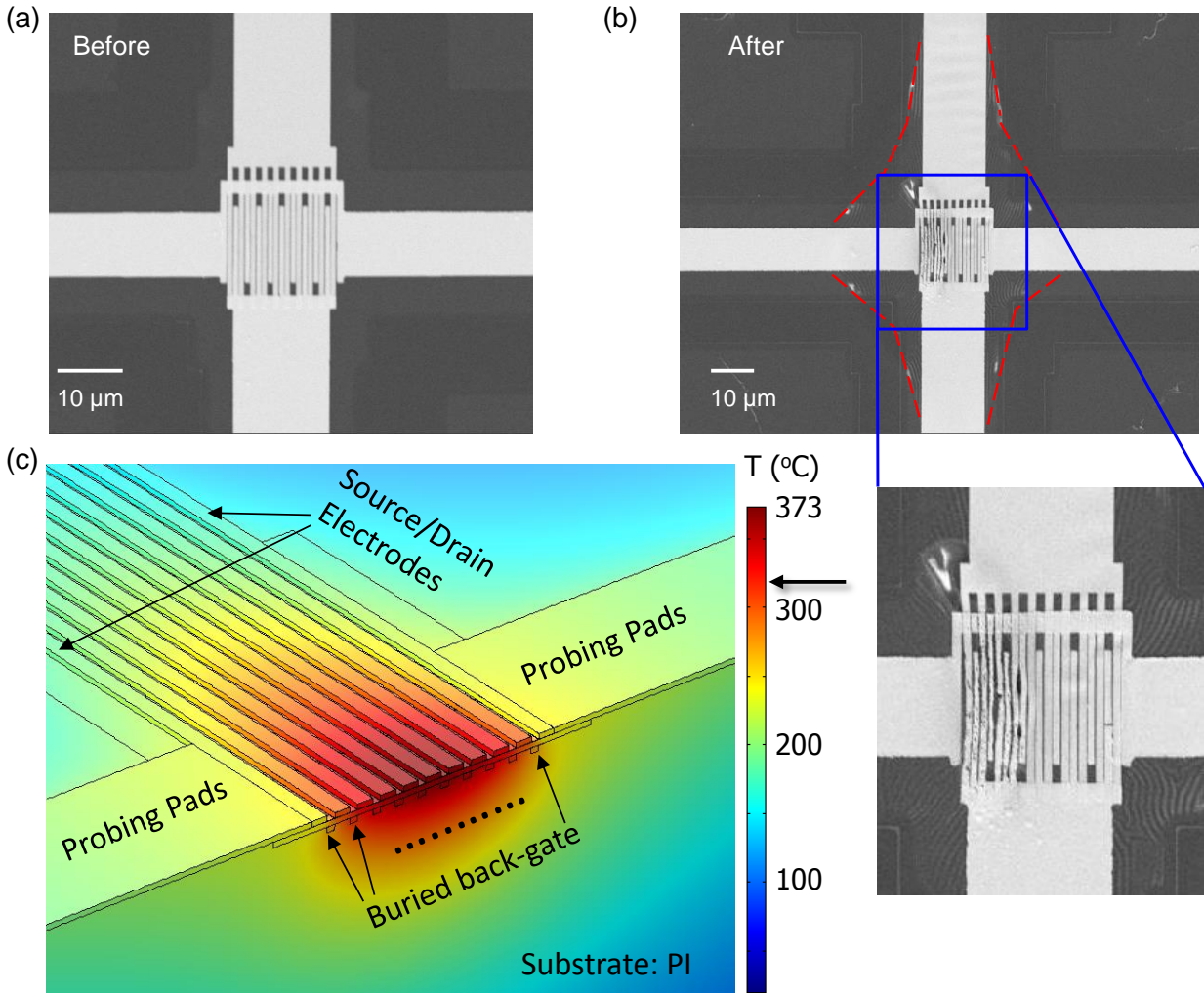


Figure 6.3: The SEM image of GFET on flexible PI substrate with 10-finger electrode configuration (a) before and (b) after thermal breakdown. The red dashed line in (b) marks the damaged area due to breakdown. Scale bar here is 10 μm . Inset: zoomed version of the damaged device. (c) Thermal simulation shows $T_{\text{peak}} > T_{\text{gtt}}$ at the maximum input power of 1.5 mW. The arrow at the temperature bar on right is pointing at the T_{gtt} .

This enforces a limitation to apply high field for GFET on flexible substrate, in turn achieve current saturation. The deformed area is shown by red dashed line in Fig. 6.3(b).

Using the COMSOL platform, we simulate this configuration, as shown in Fig. 6.3(c), to study the thermal breakdown. To reduce the computational complexity, instead of separate source and drain electrodes for each device, we simulate a merged metal finger. The maximum input power applied to this device is 1.5 mW at the thermal breakdown [151]. At this input power we found that, at the bottom of the 20 μm thick PI layer, the temperature does not drop to T_0 . In a realistic scenario the measurements were done on a metal chuck, which helps heat sink. To include that effect, we added a 20 μm thick nickel plate underneath PI. The T_{peak} at graphene rises to 373 $^{\circ}\text{C}$, which is higher than T_{gtt} and the temperature of PI below the channel region is also higher than T_{gtt} . This temperature profile agrees with the thermal breakdown as seen in the experimental device. The arrow at the temperature bar on the right is pointing at the T_{gtt} .

Next, to study and compare the effect of the substrate material on device self-heating, we calculate the temperature profile for a generic top-gated MOSFET structure as shown in Fig. 6.4(a). An input power of 1 mW/ μm^2 is applied to $1 \times 1 \mu\text{m}^2$ graphene channel. The heat conduction equation is solved for one-half of the cross-sectional area of the device due to symmetry of the device, as shown with the dashed line in Fig. 6.4(a). The thicknesses of the top oxide, bottom dielectric and substrate are 20 nm and 200 nm and 10 μm , respectively. Isothermal boundary conditions are applied at the bottom and right edges of the substrate and other boundaries are adiabatic (similar to Fig. 5.4). A thermal interface resistance (r_{int}) of $1.15 \times 10^{-8} \text{ m}^2\text{K/W}$ is implemented, which is similar to graphene-SiO₂ interface [153]. Variation of this thermal interface resistance does not have a big effect on temperature calculation. For example increasing the resistance by 10x, there is 10% rise in the T_{peak} . As for the bottom dielectric, we

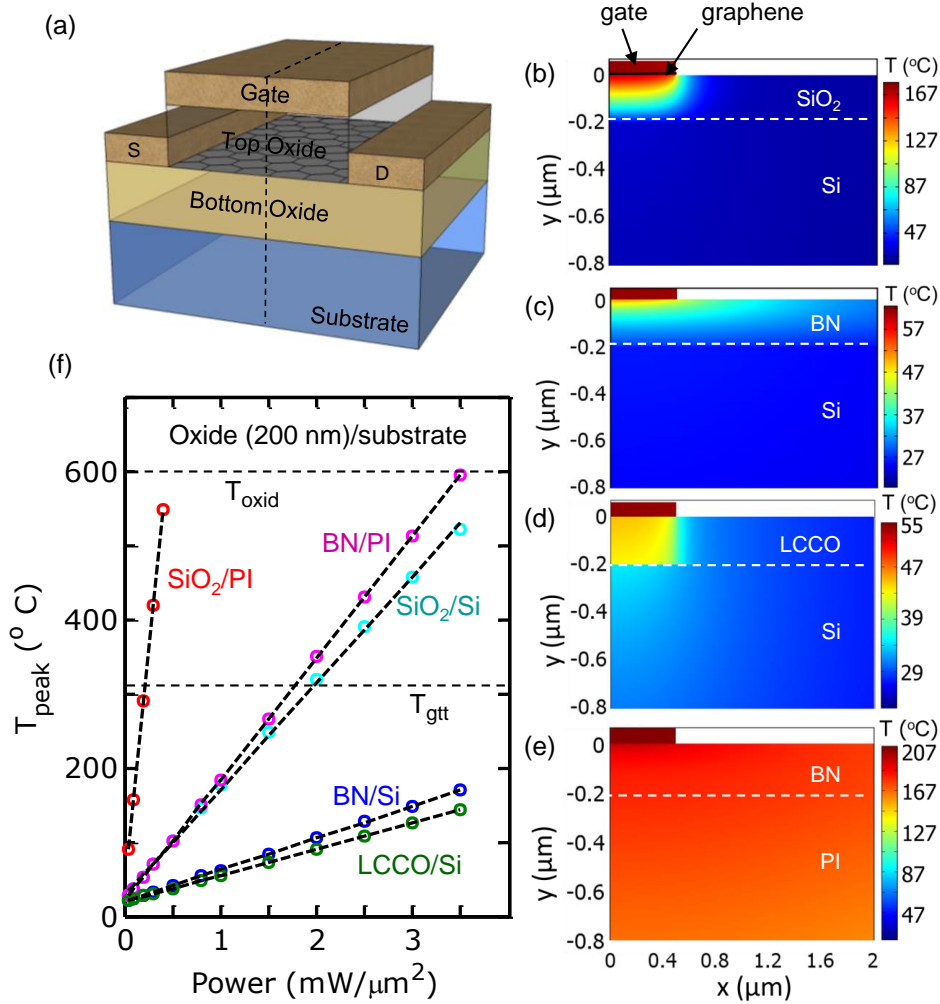


Figure 6.4: (a) Schematic of the simulated device: generic top-gated MOSFET structure. (b-e) Cross-sectional steady-state temperature profiles obtained from FEM simulations with an input power of 1 mW are applied to $1 \times 1 \mu\text{m}^2$ graphene sheet (half of the device is simulated due to symmetry). Different combinations of BOX and substrate material of SiO₂/Si, BN/Si and LCCO/Si are implemented here, respectively. (e) Calculated T_{peak} for different combinations of BOX and substrate material from (b-d) and SiO₂/Si as a function of input power in graphene channel. Vertical line is for maximum power applicable for PI substrate without inducing thermal physical deformation from Ref [145].

implement an isotropic thermally conductive material like SiO₂ and an anisotropic one like BN and LCCO (La₅Ca₉Cu₂₄O₄₁). The thermal conductivity of LCCO (k_{LCCO}) is higher (100 W/m·K) along the cross-plane and lower (2 W/m·K) in-plane [154]. A recent study showed that incorporating LCCO as bottom dielectric material reduces temperature generation at the hot spot

in an extremely thin silicon-on-insulator (ETSoI) chip [155]. We simulate different combinations of bottom dielectric and substrate: SiO₂/Si, BN/Si, LCCO/Si and BN/PI as shown in Figs. 6.4(b-e), respectively.

A few observations can be made by comparing Figs. 6.4(b-e). First, in Fig. 6.4(b-d), with Si substrate and the same input power of 1mW/μm, ΔT for BN or LCCO as the bottom dielectric is only one-fourth of ΔT for SiO₂. Second, comparing BN/Si and BN/PI substrates in Fig. 6.4(c) and (e), respectively, we find that ΔT is much higher for the latter case due to a low k_{PI} . Third, by comparing Fig. 6.4(c) and (d), we can see a clear heat spreading along the channel and cross-plane, respectively, which is due to the anisotropy of k_{BN} and k_{LCCO} . Note that the temperature scales are different in Figs. 6.4(b-e) for better visualization of temperature spreading in the bottom dielectric layer.

We compare the calculated T_{peak} for different combinations of bottom dielectric and substrate material as mentioned above in Fig. 6.4(f). We calculate T_{peak} for a range of input power of 0.05 to 3.5 mW/μm². Here the power is normalized by length and width. For all combinations, T_{peak} increases linearly. Having higher k , at least in one direction, makes BN and LCCO on Si a better choice to keep lower T_{peak} than the other materials. We also add the worst case scenario for thermal generation for SiO₂/PI. For SiO₂/PI, the temperature rise is too high and for simulation convergence we could only apply input power as high as 0.4 mW/μm². The bottom horizontal line at 310 °C indicates the T_{gt} . So for any device with PI substrate, this line guides to a maximum limit of ‘safe power’ to apply in GFET without inducing any thermal deformation. The top horizontal line at 600 °C is for the oxidation temperature (T_{oxid}) for graphene. Here with a 200 nm thick SiO₂ layer, the T_{peak} for SiO₂/Si (cyan open circles) will reach this T_{BD} at ~ 4 mW/μm².

6.3 Thermal Spreading Resistance Model

Finally, we explore a compact thermal model based on the work of Dryden [156], which takes into account the thermal spreading resistance (R_{spr}). In our structure, as shown in Fig. 6.4(a), graphene is acting as a heat source and BN and PI layers correspond to material-1 and material-2, respectively, when compared to the structure modeled in Ref. [156]. So, for our structure, the ratio $t_{BN}/a < 1$, where t_{BN} is the thickness of the BN layer and a is the radius of the heat source (in this case $\pi a^2 = LW$), which leads us to implement eqn. (21) of Ref. [156]:

$$R_{spr} \cong \frac{1}{4k_{PI}a} + \frac{1}{\pi k_{eff}a} \left(\frac{t_{eff}}{a} \right) \left[1 - \left(\frac{k_{eff}}{k_{PI}} \right)^2 \right] \quad (20)$$

Here, we use an effective thermal conductance k_{eff} and thickness t_{eff} for BN layer. Direction-dependent thermal conductivities of an orthotropic system can be transformed into an effective isotropic thermal conductivity $k_{eff} = \sqrt{k_{BN,c} \times k_{BN,i}}$ [157]. Also the thickness of the anisotropic material layer is transformed into a much larger physical thickness, defined as $t_{eff} = t_{BN} \sqrt{k_{BN,c} / k_{BN,i}} + r_{int} k_{eff}$. If $t_{BN} = 20$ nm as in Fig. 6.1(a), k_{eff} and t_{eff} are 34.6 W/m-k and 630 nm, respectively. This simple compact thermal model can be very useful in calculating the thermal spreading resistance without getting into complex FEM simulations for both isotropic and anisotropic materials. A similar model has been implemented to study the thickness-dependent modulation of thermal transport across graphene [158]. Implementing this model into our drift diffusion model results in a 12% higher T_{peak} than our 2D FEM simulation. This is expected as in the latter case we are performing 2D thermal simulation where an infinitely long width is assumed, so better heat sinking leads to lower T_{peak} .

6.4 Conclusion

To summarize, high-field transport for GFETs on flexible substrates can cause physical deformation due to thermal breakdown. However anisotropic thermal conductivity of dielectric material can improve the scenario by reducing the heat generation. With a 200 nm thick BN layer for GFETs on PI substrate we found a maximum power of $1.8 \text{ mW}/\mu\text{m}^2$ applicable before damaging the device. However this ‘safe power’ limit will depend on the thickness, thermal conductivity and material quality of the underlying dielectric layer. Since cooling options are limited if the electronics are to be kept flexible, the thermal conductivity of the plastic substrate is found to be the dominant bottleneck of the performance. These results are important for the optimization and physical analysis of graphene devices in contact with various dielectrics, operating at realistic fields and temperatures.

Chapter 7

COMPACT MODEL FOR GRAPHENE TRANSISTORS

In recent years, different building blocks for RF circuits based on graphene FETs have been developed, such as ring-oscillator [103], frequency multipliers [95, 159, 160] and amplifiers [97, 104]. To maintain the pace with the experimental development of carbon based field-effect transistors (FETs) technology, modeling of the electrical characteristics is essential, to cover aspects such as performances prediction, device design optimization, and exploration of analog/RF circuits. The goal is to predict device properties, with high accuracy in all operation regions. That raises a fundamental challenge to develop a sufficiently simple mathematical description that allows its implementation in existing circuit design environments. This demand for accurate GFET compact models which will contain unique features of graphene transport physics, has yielded a number of closed-form analytical models [46, 49, 50, 161, 162]. Our goal is to develop such an in-house compact model based on existing research and integrate it in a circuit simulator using hardware description languages (HDL) such as HSPICE or Verilog-A.

7.1 Drain Current Model

Our physics based compact model of the I - V characteristics of GFETs is based on explicit closed-form expressions for the drain current [49, 161]. The main framework is a field-effect model and drift-diffusion carrier transport, which is accurate to explain the electrical behavior of GFETs [81, 162]. This model has been benchmarked by the resulting I - V characteristics with experimental results extracted from the device in [163].

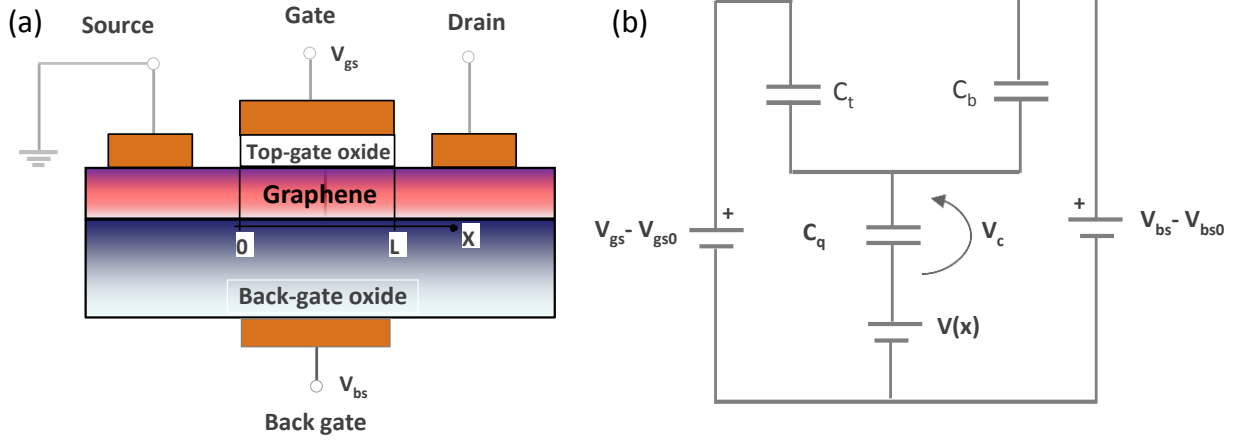


Figure 7.1: (a) Cross section of the dual-gate GFET. (b) Equivalent capacitive circuit of the dual-gate GFET.

We consider a dual-gate GFET as shown in the schematic in Figure 7.1(a). The graphene sheet under gate electrodes plays the role of active channel, where the graphene under the source and drain electrodes are assumed to be ohmic. The carrier concentration of graphene is determined by electrostatic modulation via a double-gate stack consisting of top and bottom gate dielectrics and the corresponding metal gate. The reference potential is the source, which is grounded. An equivalent capacitive circuit is shown in Figure 7.1(b). Here, C_t , C_b and C_q are the top and bottom oxide capacitances and quantum capacitance of graphene, respectively. The potential V_c represents the voltage drop across C_q , where $C_q = k/V_c l$, and $k = (2q^2/\pi)(q/(v_F)^2)$, and v_F ($= 10^6$ m/s) is the Fermi velocity. The channel potential is $V(x)$, which is zero at the source end ($x = 0$) and equal to the drain–source voltage V_{ds} at the drain end ($x = L$). The overall net mobile sheet charge density in the graphene channel, $Q_c = q(p - n) = -(1/2)C_q V_c$, is calculated using basic equivalent capacitive network and V_c can be expressed as:

$$V_c = \frac{-(C_t + C_b) + \sqrt{(C_t + C_b)^2 \pm 2k[(V_{gs} - V_{gs0} - V)C_t + (V_{bs} - V_{bs0} - V)C_b]}}{\pm k} \quad (21)$$

Here, V_{gs0} and V_{bs0} are the top and back-gate Dirac voltages, respectively. The drain current is defined as $I_{ds} = -W/Q_c(x)/v(x)$, with the theory of drift-diffusion transport. As electrons

and holes move in opposite directions under the electric field operation, they additively contribute to the drain current, so absolute value of Q_c is used. Here, $v(x)$ can be expressed as $v = \mu E / (1 + \mu E / v_{\text{sat}})$, where E is the electric field, μ is the carrier low-field mobility, and v_{sat} is the saturation velocity. The latter is concentration dependent and given by $v_{\text{sat}} = \Omega / \sqrt{\pi \rho_c}$ [41]. Next, we apply $E = -dV(x)/dx$, insert the equations for v and v_{sat} , and integrate the resulting equation over the device length. Moreover, (21) provides relation $dV/dV_c = -(1 + (kV_c \text{sgn}(V_c) / C_t + C_b))$, where sgn refers to the sign function. Based on all these equations the following explicit drain current expression can be finally obtained:

$$I_{ds} = \mu \frac{W}{L_{\text{eff}}} \left\{ q\rho_0 V_{ds} - \frac{k}{6} (V_{cd}^3 - V_{cs}^3) - \frac{k^2}{8(C_t + C_b)} (\text{sgn}(V_{cd})V_{cd}^4 - \text{sgn}(V_{cs})V_{cs}^4) \right\} \quad (22)$$

The denominator representing an effective length L_{eff} is from eqn. (5), Ref. [161], which takes into account the saturation velocity effect. Here ρ_0 accounts for the impurity carrier density. To calculate a realistic result we need to account for the voltage drop at the S/D contacts. We can also find the drain current as a function of internal V_{ds} instead of external V_{ds_ext} by solving the equation: $V_{ds} = V_{ds_ext} - I_{ds}(V_{ds})(R_s + R_d)$.

7.2 Results

Based on the model described above, we simulate the I_d - V_g curves for a top-gated device with $L = 10 \mu\text{m}$, $W = 5 \mu\text{m}$, and HfO_2 as a dielectric with thickness of 40 nm. The flatband voltage was $V_{\text{gs}0} = 0.85 \text{ V}$ according to the experiment. Low-field mobility source/drain resistance R_s , R_d values were determined as fitting parameters with the values of $7500 \text{ cm}^2/\text{V}\cdot\text{s}$ and 300Ω , respectively. The resulting I_d - V_g characteristics are shown in Fig. 7.2 (a) for $V_d = \pm 0.1, \pm 0.5, \pm 0.75, \pm 1 \text{ V}$. Figure 7.2(b) shows the effect of R_s , R_d on the transfer characteristics.

The dashed line represents the model with ideal contacts and blue and purple solid lines are for $R_s = R_d = 300 \Omega$ and 1000Ω . As expected for GFETs, the transfer characteristics demonstrate

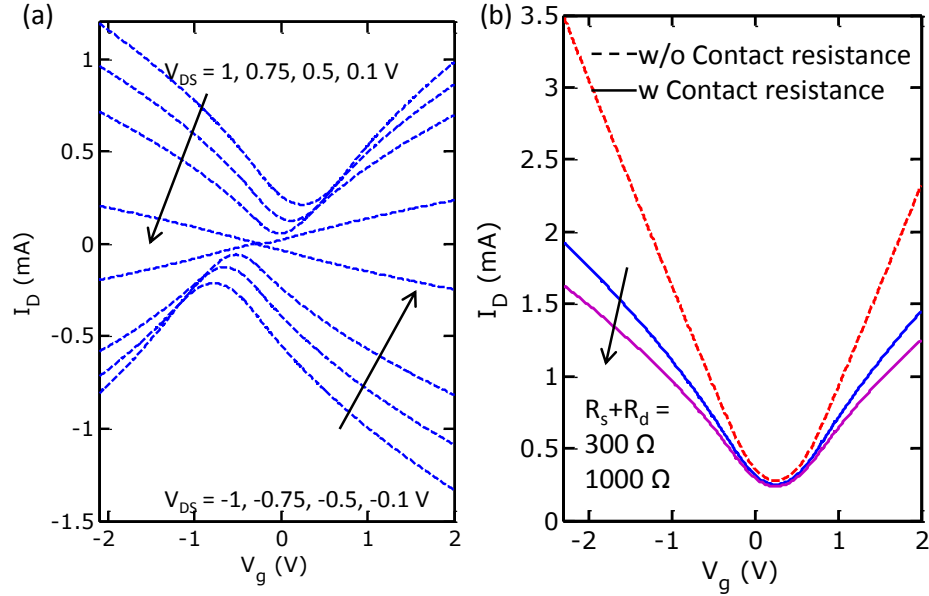


Figure 7.2: (a) Transfer characteristics obtained from the analytical model. (b) I_{ds} - V_{gs} characteristics with and without adding contact resistance.

the ambipolar behavior dominated by holes (electrons) below and above the Dirac gate voltage. Figure 7.3(a) shows the output characteristics with current saturation as well as kinks in the I_d - V_d curves, which is a characteristic of ambipolar transport of GFETs. Increasing the $R_s = R_d = 300 \Omega$ to 1000Ω in Fig. 7.3(b) decreases the slope of the linear region of the curve and also shifts the saturation to a higher voltage. As discussed in the previous chapters the optical phonon energy, $\hbar\omega_{OP}$ highly depends on the substrate material, and it is impractical to use a universal value for all GFETs. The effect of $\hbar\omega_{OP}$, on drain current saturation with high- and low-end values is shown in Fig. 7.4(a).

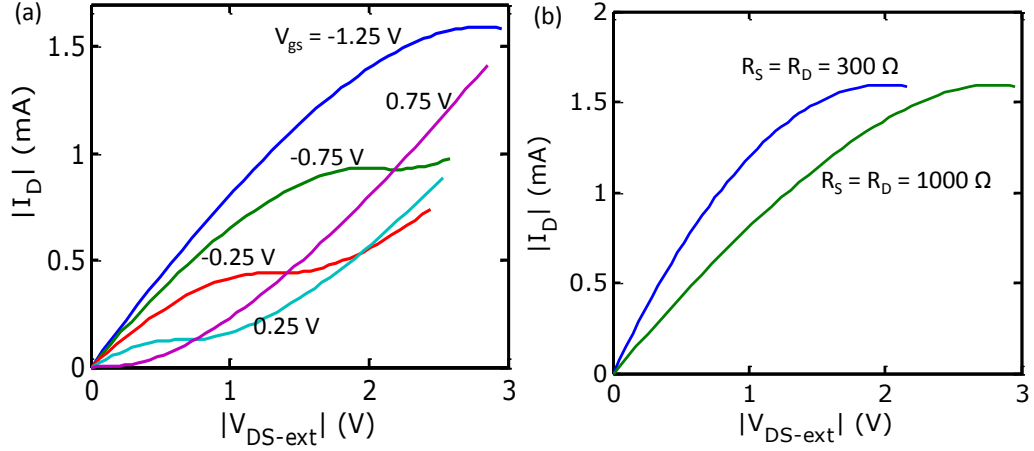


Figure 7.3: (a) output characteristics obtained from the compact model. (b) I_{ds} - V_{ds} characteristics at source and drain contact resistance 50Ω and 300Ω .

Heat generation and the associated thermal management is an issue for graphene based devices [120], the dominant factor being that device is thermally isolated from the substrate by the buried oxide layer. To account for self-heating, we estimate the average device temperature through a series thermal resistance R_{th} and the temperature rise is calculated with $\Delta T = T - T_0 = P(R_{sub} + R_{ox} + R_B)$ [24]. Here P is the power input originating from $P = I_{ds}V_{ds}$ and R_{sub} , R_{box} and R_B are the thermal resistances of the substrate, bottom oxide and interface (graphene-oxide), respectively.

We found that depending on bottom oxide thickness, t_{box} , 80%-90% of the thermal

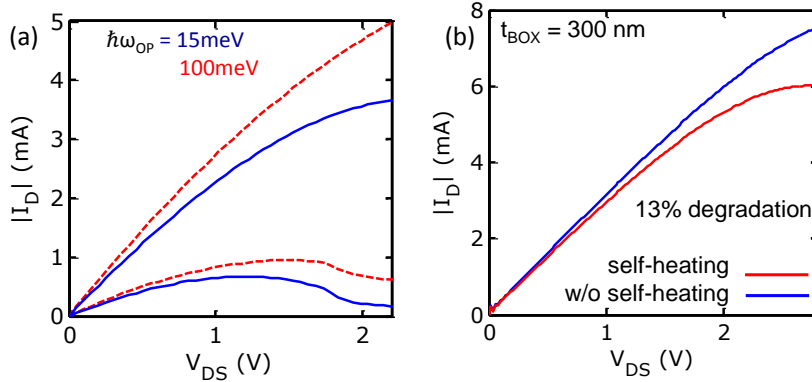


Figure 7.4: Output characteristics (a) with a $\hbar\omega_{OP} = 15 \text{ meV}$, 100 meV , and (b) with and without adding self-heating effect into the calculation.

resistance R_{th} is from R_{box} . In Fig. 7.4(b), we compare the self-heating added $I_{ds}-V_{ds}$ with an isothermal simulation for a structure with $t_{box} = 500$ nm SiO_2 and observe a $\sim 13\%$ current degradation.

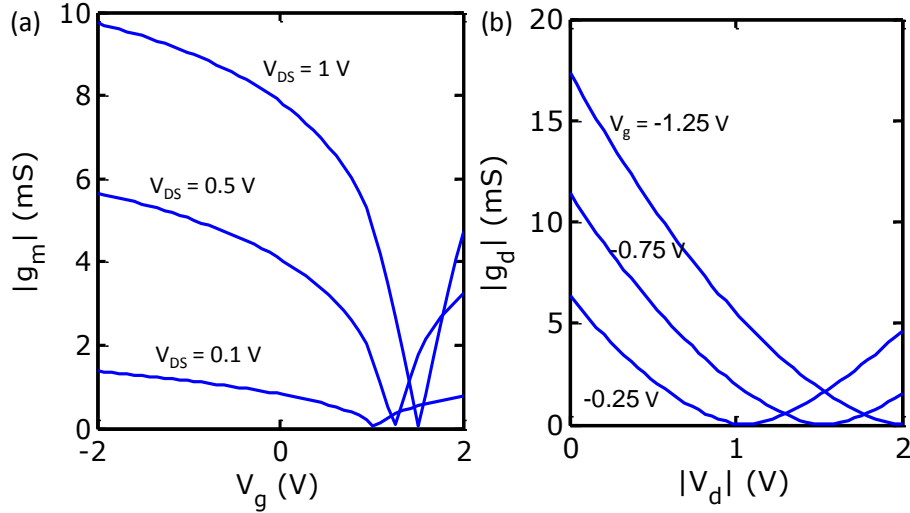


Figure 7.5: Calculated (a) transconductance and (b) output conductance at different biases.

Next, using this DC model, we calculate transconductance ($g_m = (\partial I_{ds}/\partial V_{gs})$) and output conductance ($g_d = (\partial I_{ds}/\partial V_{ds})$), as shown in Fig. 7.5(a-b), which are important figures of merit for practical RF/analog applications. The small signal quantities, g_m and g_d , are derived from the DC model using the following equations [49]:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{\mu kW}{2L_{eff}} \left(\frac{g'(V_{cd})}{1 + \text{sgn}(V_{cd}) \frac{kV_{cd}}{C_t + C_b}} - \frac{g'(V_{cs})}{1 + \text{sgn}(V_{cs}) \frac{kV_{cs}}{C_t + C_b}} \right) \quad (23)$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{\mu kW}{2L_{eff}} \frac{g'(V_{cd})}{1 + \text{sgn}(V_{cd}) \frac{kV_{cd}}{C_t + C_b}} \quad (24)$$

Here, g'_m is defined as $g'_m = -V_c^2 - \text{sgn}(V_c)kV_c^3/(C_t + C_b)$.

7.3 Integration of Compact Model into Circuit Simulator

The major challenge for circuit simulations would be to add a variability factor to different device parameters like Dirac voltage, mobility contact resistance, etc. These variability effects in graphene can result from the surrounding environment and the graphene material itself, creating a critical issue of feasibility of large-scale circuit simulations. Typically these variations can be categorized into two parts: spatial variations (e.g. contact resistance) and temporal variations (e.g. hysteresis). A compact model enables these studies across many (1000s) device samples. Besides the variation study, the compact model could also be utilized to study the behavior of circuits with more than one device.

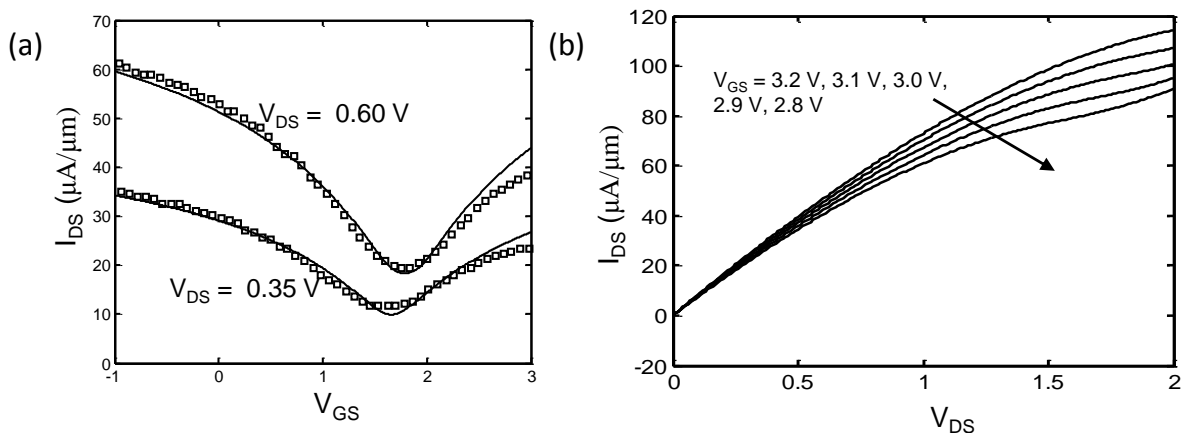


Figure 7.6: Simulated (a) transfer and (b) output characteristics curves from Verilog-A circuit simulator.

This capacity is important especially for evolving technology like graphene in order to have realistic estimation of the technology projections. As we successfully modeled the transfer and output characteristics of GFET transistors with closed-form expressions, this model is ready to integrate into a circuit simulator. From a collaboration with Stanford University, a circuit simulator has already been generated based on the above compact model and other studies [46, 164]. The model has been appended by self-heating and fringe-capacitance. In Fig. 7.6(a-b) I_{ds} -

V_{gs} and I_{ds} - V_{ds} are generated by a Verilog-A circuit model. The model is calibrated against experimental data [46], as shown with open squares in Fig. 7.6(a) and (b). Fig. 7.6(c) shows the saturation behavior in graphene using the model calibrated from the above experimental data. Good convergence is achieved and through this model we can explore simple and complex graphene based circuits. At present, we do not have variability inside the model but it can be externally plugged in as a part of the circuit test bench.

7.4 Conclusion

In conclusion, the aim of this project is to generate physics-based compact models for monolayer graphene FETs with explicit and compact drain current model. The model has been extensively calibrated with experimental data from the literature. The closed form equations are based on drift-diffusion carrier transport, including saturation velocity and self-heating effects. The physics behind all regions of operation have been captured properly. However, for useful application of this model for design of analog and RF electronics, further improvement is required like adding hot-channel effects, nonquasi-static effects, extrinsic capacitances etc. An ongoing collaboration already incorporated this model into the Verilog-A circuit model. This in-house model will play a crucial role in the development of higher-level information processing technology by facilitating simulations of the complex high-level circuits, based on the information of low-level nanoscale device models.

Chapter 8

CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

We have investigated the physical mechanisms behind electrical and thermal transport in supported monolayer graphene transistors. The self-consistent electro-thermal model described and implemented throughout this work has been benchmarked with numerous devices fabricated both within our research group and in collaboration with other groups.

We examined high-field hot spot formation and saturation current degradation, both as functions of the thickness of the supporting SiO₂ layer. Due to competing electrostatic and heat sinking effects, the average and maximum temperatures of GFETs scale differently. We also found that self-heating is reduced linearly as we scale the dielectrics, and for sub-0.5 μm channel lengths the contacts begin to play a greater role in heat sinking. We provided a guide for future pulsed operations in GFETs with a thermal transient model that can help to design with shorter time scale than the time constant. Thus devices suffer less from self-heating compared to DC operating modes. We also showed that significant reduction in the contact resistivity is required to achieve current saturation, especially in short channel devices.

Through extensive calibration, we investigated high-field transport in graphene on BN, HfO₂ and SiO₂ dielectrics. Our extraction results showed that for graphene on BN, extracted $\hbar\omega_{OP}$ (~ 94 meV) and v_{sat} are similar to those of graphene on SiO₂. However, on HfO₂, $\hbar\omega_{OP}$ has a significantly lower value of 34 meV and v_{sat} is also $\sim 5x$ lower than graphene on BN/SiO₂. We also found that the isotropic/anisotropic nature of thermal conductance of the substrate material has a significant impact on temperature rise. When placed on a flexible substrate, low conductive

material like Al_2O_3 can cause thermal damage, while the anisotropic thermal conductive dielectric material, e.g. BN, can improve the scenario by heat spreading. With a 200 nm thick BN layer for GFETs on PI substrate, we found a maximum power of $1.8 \text{ mW}/\mu\text{m}^2$ applicable before damaging the device. However this ‘safe power’ limit will depend on the thickness, thermal conductivity and material quality of the underlying dielectric layer.

Finally, we developed (based on an existing model available in literature) a sufficiently simple closed-form mathematical description (compact model) and improved that by adding our understanding of and experience with transport physics of GFETs. We have incorporated this model into a Verilog-A circuit model, which can play a crucial role in the development of higher-level complex circuit analysis, based on the information of low level nanoscale device models.

Our simulations consistently showed that substrate effects play a dominant role in limiting transport in supported-graphene devices. This trend is also expected in other reduced dimensions and large surface-to-volume ratio materials. Choosing the optimal substrates for ideal interfaces is an essential task for the future development of 2D nanoelectronics. This thesis suggests a route for the optimization of graphene substrates for proper heat dissipation, and highlights existing trade-offs for practical device reliability.

8.2 Future Work

Substantial progress has been made in both understanding the transport physics in GFETs and enhancement of its performance. However, numerous questions still remain which will determine whether graphene transistor will become a commercially sustainable technology.

As the performance of GFETs significantly depends on dielectric materials, intensive research needs to be carried out to find the optimal one. Tremendous opportunity lies in the use

of graphene in flexible electronics, where it can provide great mechanical flexibility and superior electronic properties. However, heat generation in the device needs to be considered, especially while designing for GFET on flexible substrate. To capture the practical temperature rise through thermal simulations, external elements around the active device, e.g. extended metal gates, contact pads, and metal chuck (metal plates on which the measurements are conducted) need to be added. Materials with higher dielectric constant will be required for short channel GFETs. In addition, design considerations need to be taken for high-field operations as the substrate phonon dominates the scattering process. It is also necessary to ensure unipolar device operation by controlling the channel doping.

The lack of band gap makes graphene a less desirable candidate for logic applications. However, instead of replacing fully matured technology, novel applications need to be engineered to utilize the superior unique properties of graphene. We believe that this work, which provides significant insight into transport properties, will facilitate the advancement of graphene and other 2D-based material technology.

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