GRAPHENE ETCH MASK FOR SILICON

BY

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THESIS

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ABSTRACT

In this thesis, an alternative future use for graphene will be explored. Graphene, a popular two-dimensional material of remarkable electrical properties, has been thought to be a successor to current day microelectronic materials. With the many challenges posed by the manufacture of conventional devices from graphene, other adaptations for its properties are sought in the work that follows. Chiefly, its mechanical and chemical strength as an etch mask for silicon is tested. We attempt to present the progress toward a working model of a graphene etch mask. The influence of the mask geometry, etch method, etch conditions, substrate quality and other factors will be explored to present a clear understanding of methodology and requirements for carrying out the process. Along the way, other aspects of the project such as the growth and transfer of graphene, which are not the focus but extremely crucial to the results, will be elucidated as required. Possible future directions will also be presented to provide a notion of where the idea can head.

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TABLE OF CONTENTS

1 INTRODUCTION 1

2 EXPERIMENTAL METHODS 7

3 RESULTS AND DISCUSSION 16

4 CONCLUSION AND FUTURE 30

REFERENCES 31

1 INTRODUCTION

1.1 Overview of Processing

Semiconductor processing has evolved tremendously since the conception of high-volume manufacture. Optimization of each aspect of the process has been continually ongoing with bright new cost cutting and efficient ideas periodically taking the place of their predecessors. This is largely related to the Moore's law trend, which predicts the increase in the density of manufacture as shown in figure 1. Now, billions of transistors are produced on a single die on a twelve-inch wafer in the most advanced labs; the starting point was thousands of transistors per die in the 1960s.

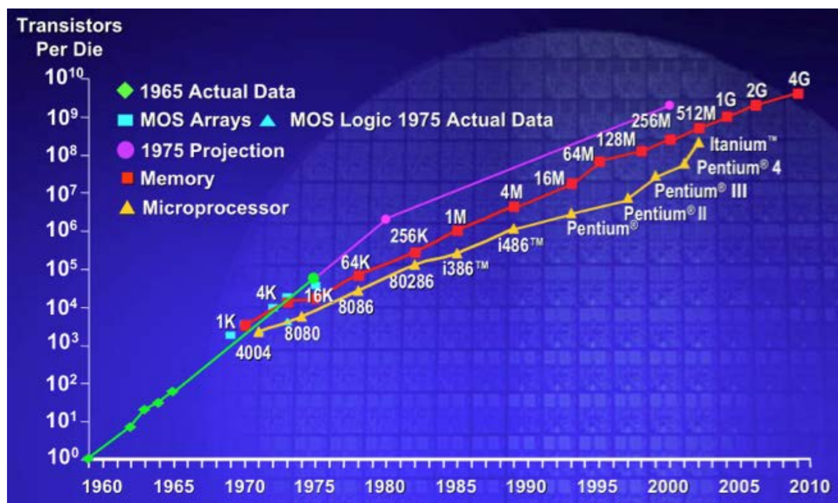


Figure 1: Moore's law in action through the years.

Each process in semiconductor manufacturing has had its own metamorphosis. For instance, metallization has many variants. Evaporation of metal in a low-pressure environment was the primary route and the method of evaporation evolved from filament heated to electron-beam assisted heating. Other techniques such as sputter deposition offer alternatives that do not use heat. The path to current silicon/silicon dioxide etching has also seen numerous changes. Liquid phase etching was the chief choice and it usually came with undercut, which is a result of unidirectional, or isotropic, etch. A desire to get rid of this undercut brought about the anisotropic Reactive Ion Etch (RIE) because it gave practically no undercut.

Advancements in anisotropic etching, such as the Bosch process and LE4 process [1], aim to give the best of both worlds in terms of chemical selectivity and physical directionality. Lithography has also tremendously improved in recent times, with advancements in laser technology to provide shorter wavelengths of light and the concurrent development of photoresist (PR) to allow more precise development. Compounds with 35 nm half-pitch [2] to allow nano-patterning and others that are compatible with excimer lasers [3] are available.

Newer practices utilize immersion lithography (companies like Cymer, Nikon are commercial examples), electron-beam (e-beam) lithography [4] and even ion beam lithography [5]. The resolution is within a few tens of nanometers or even less with these techniques.

1.2 Graphene

Graphene is a crystalline allotrope of carbon that is formed by a hexagonal network of sp_2 hybridized electron orbitals. Each carbon atom forms bonds with three other carbon atoms in a two-dimensional plane. The lattice of a graphene sheet is shown in figure 2. The fourth electron from each carbon atom's valence shell contributes to the delocalized π-electron cloud. In this structure, the graphene linkage has a tensile strength of 130 giga pascal (GPa) [6] and is stronger than structural steel and Kevlar. It also has a high Young's modulus value of 150,000 GPa, though it is also brittle and can crack like glass. While the focus and hype with graphene has mostly been with its high mobility and excellent electrical properties, it has much to offer from a mechanical point of view as well.

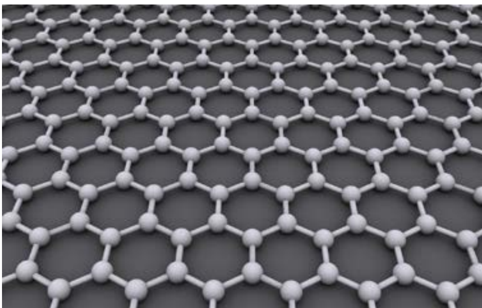


Figure 2: Hexagonal honeycomb structure of graphene. Each bubble is a carbon atom and the distance between nearest carbon atoms is 0.142 nm. Image courtesy: Wikipedia – Graphene.

1.3 Current Technology Challenges

Lithography and etching are major concerns in the semiconductor processing industry. They contribute heavily to operating and manufacturing costs. The equipment is extremely expensive, and costs have been increasing due to technology scaling and the need for smaller nodes. This makes lithography in particular a complicated process and induces many variables and avenues for error. Smaller nodes require more precision and alignment; this puts added stress on the machinery that performs other tasks since subsequent masks need to be aligned correctly. Variations generated by side-wall deposition or isotropicity of etch need to be minimal. Hence, a sturdier mask capable of adhering to the surface topology is always welcome.

Furthermore, only so much can be eked out of a particular wavelength for the development of PR before resolution (R) limits, given by equation (1), are realized.

$$R = k_1 \times \frac{\lambda}{NA} \tag{1}$$

Here, λ is the exposure wavelength, NA the numerical aperture of the lens, and k_1 a lithography process parameter.

Techniques such as immersion lithography can be utilized, though they only prolong the inevitable (new photoresist compound, laser source will be needed) rather than provide a more scalable, long-term solution. Making a laser source of smaller wavelength, such as an excimer or carbon-dioxide laser, is again an extremely challenging task and a lot of capital is used to find solutions [7]. On the contrary, if the utilized mask is capable of being willfully patterned to any scale and shape, and also strong enough to resist the etching process of the masked material, the costs go down and processing complications decrease. Bottom-up control in the nanoscale, once perfected, is much less complicated than engineering a top-down approach with a myriad of error-prone processes. While controlled upward pattern growth is the other side of the coin, the hope and attempt with this project is to show that graphene can offer silicon protection under etch conditions and retain pattern originality.

Some hard carbon masks do exist [8] but contain their own set of challenges. The technology is not matured yet and small resolutions are difficult to attain. The graphene mask will fall under the broad umbrella of carbon masks and will be used to address some of the current concerns in this area. Once perfected, this mask will give a comparatively enhanced resolution.

1.4 Why Graphene for the Etch Mask?

The next logical question would then be to ask why graphene should be used, as opposed to some other material. What we are looking for in an etch mask of this nature is patternability, conformity and etch resistance. An etch mask needs to be patternable for the obvious reasons. Substantial control over the features and shapes of a mask is needed to fabricate devices that meet the blueprint. Otherwise, device behavior can become unpredictable or erratic, or the device design would need a major overhaul to adapt the technology to available process capability. Graphene allows a good degree of patternability in this sense, since numerous bottom-up approaches of controlled nanoribbon growths have been reported [9], [10]. Shown in figure 3 is one of the instances where successful bottom-up growth was demonstrated. This is even more convenient when considering the future and the need for FinFET devices.

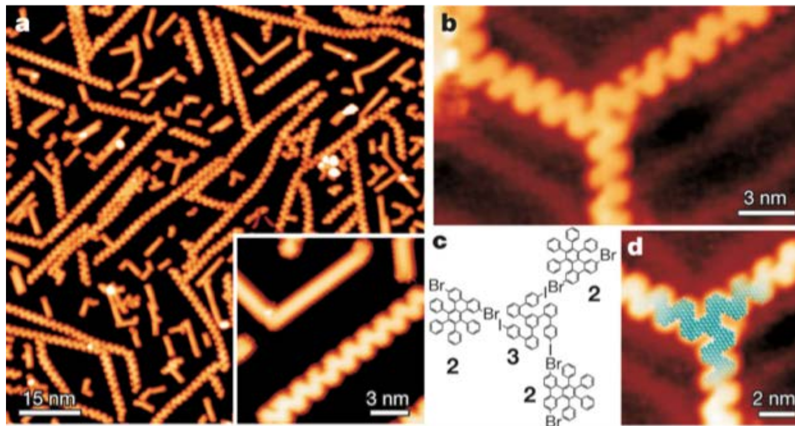


Figure 3: Atomically sharp GNRs by bottom-up synthesis [9].

Post-patterning of graphene from a monolayer, like during traditional lithography with PR, is a trickier process, though it is possible to get sub-10 nm features with ion beam

lithography [5]. The main advantage in this case is that a secondary sacrificial layer such as silicon dioxide (SiO_2) or nitride, which is usually grown or deposited on silicon, is not needed. The graphene acts as both the resist and shield for processes PR cannot withstand. In this thesis, graphene has been patterned using traditional photolithography to microscale levels for a proof of concept.

Secondly, graphene is conformal to the features that it drapes. Since it is a single atomic layer, it has the flexibility to wrap the terrain it sits on. This has been demonstrated on occasions [11]. Graphene wraps around nanoscale water features that are between it and mica and a graphical rendering of this is shown in figure 4. This is an important feature for a nanoscale mask that aims to effectively protect the substrate and maintain the integrity of the pattern.

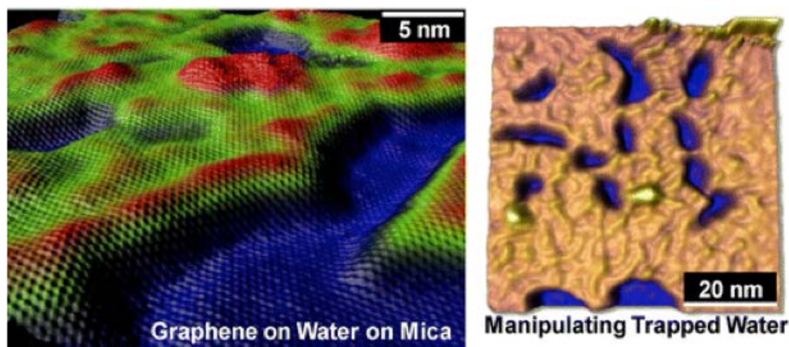


Figure 4: Graphene conformal to nanoscale water [11].

Finally, graphene is resistant to many of the processes that etch silicon. This is an important criterion for any etch mask, since it should offer protection to the areas that are not to be removed. In this sense, graphene is a suitable choice because fluorine-based processes do not chemically remove graphene. On the other hand, many silicon etch processes often involve removal using some state of fluorine (XeF_2, Freon RIE etc.).

Exposing graphene to a fluorine-rich environment serves only to fluorinate the graphene sheet, as seen by the Raman peaks in figure 5. Though this process chemically changes the graphene by confining the delocalized π-electron cloud with C-F bonds, it leaves the graphene physically unaltered. Hence, this triumvirate of useful properties can combine to

give an etch mask for silicon.

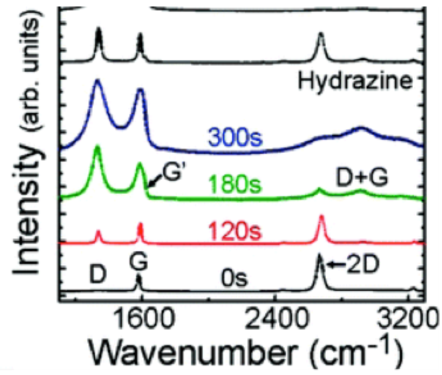


Figure 5: Fluorination of graphene - Raman shift confirms graphene's chemical alteration, but physical stability [12].

2 EXPERIMENTAL METHODS

2.1 Growth and Transfer of Graphene

The first stage of the process begins with the growth and transfer of graphene, the material of interest in the experiments. Numerous methods have been reported for graphene growth, and currently the most common one is Chemical Vapor Deposition (CVD) in a high temperature furnace with a catalytic metal substrate [13]. Catalytic metals such as copper and nickel provide surface sites for precursor gas molecules to sit and dissociate from their original state. This leaves behind a network of carbon atoms that bond with each other to form graphene.

This hexagonal bonding is naturally limited to a monolayer when copper is used owing to its low solid solubility of carbon. Once all surface copper atoms are weakly bound with carbon atoms, the growth ceases [14], [15], [16]. Copper is also a relatively cheap metal and easy to handle. For our purposes, graphene is grown on Alfa Aesar (AA) copper foils in the Atomate furnace in the Micro and Nanotechnology Laboratory (MNTL) clean-room at the University of Illinois, Urbana-Champaign (UIUC). The flow was maintained at 100 standard cubic centimeters per minute (sccm) of methane (CH_4) and 50 sccm of hydrogen (H_2) in the furnace for 25 minutes at 1000 ^oC. Large area graphene, with grains on the order of a few microns, is consistently obtained with this method.

Following the growth, the graphene was transferred to a substrate of choice. First, the copper with graphene on it was cut into required sizes (10 mm by 10 mm usually). Subsequently, poly(methylmethcrylate) (PMMA) was used as a polymer scaffold for support of the graphene film [17], [18]. Two versions of PMMA, which differed in their polymer lengths, named 495 and 950 were spun on one after the other onto the graphene/copper substrate. After applying a few drops of the PMMA, the spinner was set to 3000 revolutions per minute (rpm) and the spin took place for 30 seconds. After each layer was applied, the sample was heated at 200 ^oC for 2 minutes to firm up the polymer and remove any excess vapor and solvents. In the next step, a Reactive Ion Etch (RIE) tool (operations explained further below) was used to remove poor quality graphene from the underside of the sample. Now, the top side of the copper has graphene coated with PMMA

and the bottom is bare, exposed copper. The sample is now ready to be etched such that the copper is removed and the graphene is left floating with the support of the polymer scaffold. For this, the copper sample is placed in iron (III) chloride ($FeCl_3$) solution to etch the copper from the underside. It is left in the solution overnight to ensure complete removal of the copper.

Now, the graphene is ready for the next stage of transfer i.e. onto a substrate. In order to ensure the films are clean of $FeCl_3$ residue, the freestanding PMMA coated graphene is transferred to a deionized (DI) water bath for 15 minutes. This transfer step was performed using glass slides that were cleaned with Piranha solution made of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) in a 3:1ratio. This ensures that the slides do not introduce contaminants to the delicate graphene films. Next, the films are moved over to a modified SC-2 solution for 15 minutes, as outlined in the Radio Control of America (RCA) process [19]. The make-up is 20:1:1 of H_2O:HCl:H_2O_2. This solution is meant to remove any metal particulates from the copper etch step. Finally, another DI water bath step ensures removal of molecules introduced in the modified SC-2 step. The films are now ready for transfer onto a substrate.

This process is done carefully by getting the substrate right under the film in the DI bath, and wicking it off the surface of the water. Now, the graphene/PMMA film will be sitting on the surface of the silicon (Si) sample. The last step is to get rid of any excess water that the transfer introduced and remove the polymer support. To remove the moisture and reduce wrinkles from surface tension on the graphene, the substrate with the film can be either spun at 3000 rpm for 30 seconds or be allowed to dry in air for about 2 hours. This choice depended on the application; the first choice is rougher on the graphene and introduces more tears. It is not the ideal path when making devices. For the graphene etch mask, the films were rid of excess water by first spinning them as their conductivity was not of importance. The samples were then heated, first at 60 ^oC and then at 150 ^oC for 10 minutes each. The sample was now ready for a chloroform bath (two baths of 30 minutes each or one bath of about 2 hours) to remove the PMMA scaffold that was supporting the graphene all along. A simple degrease (of methanol, acetone, isopropyl alcohol) afterwards

to remove any organic particulates then yielded the prepared sample of graphene on Si. The process flow is shown below in figure 6.

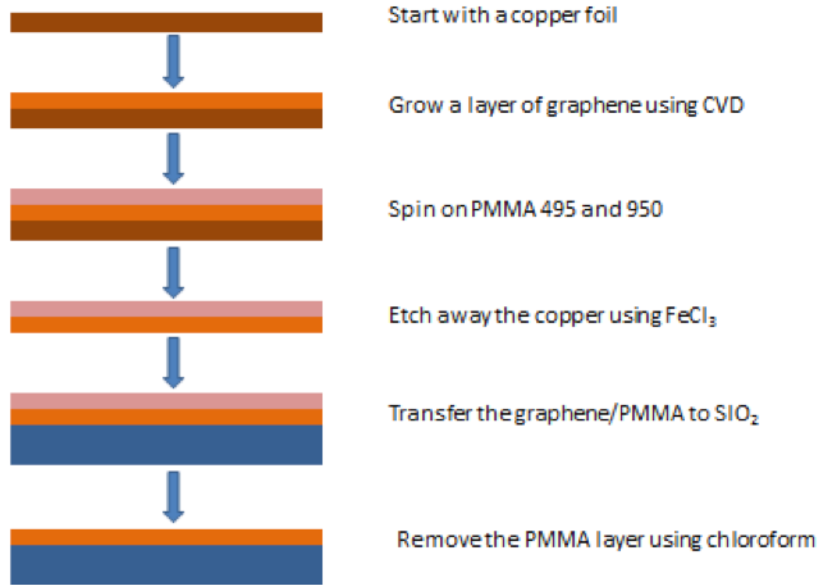


Figure 6: Steps from growth on copper to final transfer of graphene onto substrate.

2.2 Substrate Preparation and Patterning

To obtain a clean silicon surface for the etch experiment, we used 90 nm pre-grown SiO_2 on Si(100) wafers and etched them to remove the oxide. The wafers were first cleaved with an artificial diamond scribe to an appropriate sample size (about 10 mm by 10 mm) and left in 10:1 H_2O:HF (hydrofluoric acid) solution for about 5 minutes. This was sufficient to completely strip the oxide and leave a hydrogen passivated silicon surface. This passivation holds for a few hours after it is performed. The samples were Piranha cleaned to rid the surface of organic contaminants, but this was later stopped to prevent the surface from becoming too hydrophobic. That stressed the graphene after transfer by inhibiting the natural adhesive force that helped the film sit with minimal tensile strain and made transferring more difficult.

For the etch mask, a patterned graphene layer was needed. The entire process flow is shown in figure 7. After transfer, a micro-scale mask fashioned using traditional photolithography

techniques was used. First a layer of Shipley 1813 positive (develops upon exposure to UV) photoresist (PR) was applied onto the graphene/silicon sample. As is the usual case, a surfactant to bind the organic PR polymer to the substrate surface was first used. In this case, it was polymethylglutarimide (PMGI). PMGI was applied and spun on the sample at 3500 rpm for 30 seconds. It was then baked at 150 ^{o}C for 5 minutes to remove excess moisture and promote adhesion of PMGI to the surface. PR was then spun at 5000 rpm for 30 seconds, followed by a soft-bake at 110 ^{o}C for 70 seconds to remove excess water and solvents from the polymer. The mask was aligned using a contact aligner in MNTL and exposure with a UV light source took place for 4 seconds. The PR was then developed using MF-319 (metal-free) PR developer for 50 seconds to react away the exposed PR. The graphene was now exposed in areas and was ready to be etched and patterned.

Etching of the graphene took place in the RIE chamber. Oxygen (O_2) at about 30 sccm of flow and 90 Watts (W) of power was used for about 30 seconds to react with the exposed graphene. Finally, the excess PR was stripped with acetone in a sonication bath. One of the steps was also placing metal pads (with labels for identifying the graphene channels). The evaporation took place with the same photolithography steps, with the added step of metal evaporation (with titanium/gold). Their electrical properties were inconsequential as they were simply identifiers. The steps to produce the pattern are highlighted below in figure 7. In order to simplify the steps, a TEM grid was later used as a shadow mask (figure 8). Placing the TEM grid over the graphene/silicon sample and exposing it under UV produced a grid pattern as shown in the figure 8. The resultant pattern had a pitch of either 10 or 20 microns. The squares of the grid formed the exposed silicon areas while the grid itself was made of graphene.

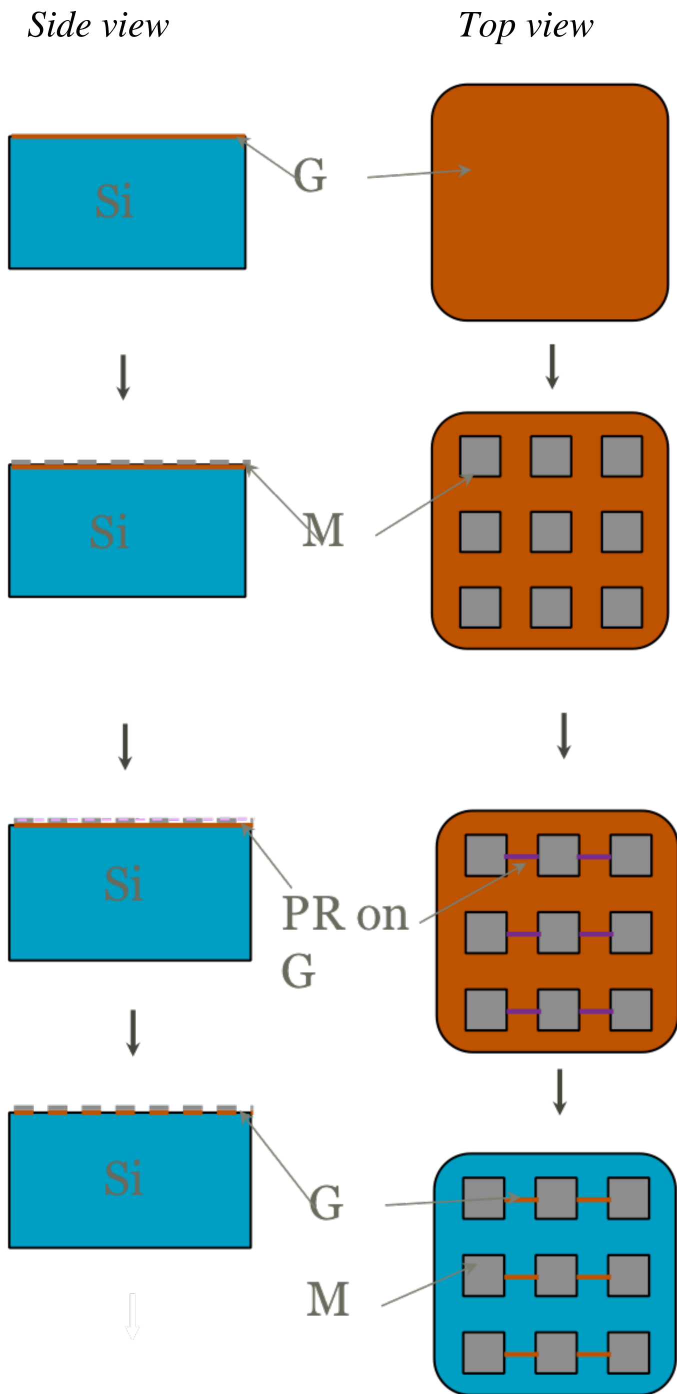


Figure 7: Patterning of graphene in preparation of an etch mask.

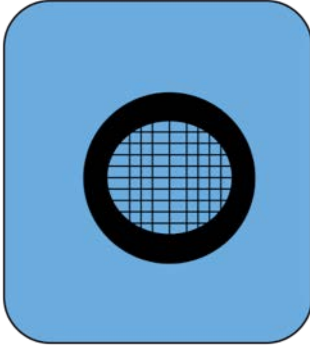


Figure 8: Graphene (black) and silicon (blue) grid pattern with TEM grids.

2.3 Imaging and Characterization

Raman

Raman spectroscopy is a widely used technique for learning the chemical and structural make-up of a material in a non-intrusive way. It primarily relies on Stokes scattering, where phonon vibrations between virtual energy states are perceived and used to quantify the intensity of vibrational peaks. These peaks correspond to particular attributes of a system.

The bands of interest with graphene are the G, 2D and D bands. The G band occurs as a result of E_{2g} symmetry in graphene [20] and shows up at 1580 cm^{-1}. Laser excitation energy has a small part to play in this wavenumber. The G' or 2D peak, which is a result of a double-resonant process involving the π-electron cloud, falls at around 2700 cm^{-1}. The intensity of this peak relative to the G peak is indicative of the number of graphene layers. For a monolayer, the intensity ratio (I_{2D}/I_G) should be around 2 (or more, in the case of a higher-quality film). The D peak, which falls at around 1350 cm^{-1}, is more colloquially known as the defect peak and will be minimal so long as the delocalized π-cloud is mostly undisturbed. Once extra bonding with the carbon atoms takes place, utilizing the free electrons, the D peak starts to spike due to an increase in inter-valley scattering.

SEM

A scanning electron microscope (SEM) uses a beam of collimated electrons to get the topography information of a surface. The electrons interact with the sample's atoms and information from the backscattered electrons (BSE) is used to come up with an image of

the surface. High resolutions in the tens of nanometers are achieved in the SEM of the Imaging Technology Group (ITG) at Beckman Institute (BI).

AFM

An atomic force microscope (AFM) makes use of a small tip mounted on a cantilever to gauge the surface topology. The AFM that was used for imaging in these experiments (in the STM lab of BI) had a cantilever oscillating at its resonant frequency and a feedback loop to tell the tip to pull away or go closer to the surface, depending on how far the surface was from it (tapping mode). A laser shining on the tip was used to read its vertical position and image the surface. Relying on the mechanical movement of the arm means that the AFM is a slower way to get data, though useful things such as the step height are acquired. Imaging was done at each stage of the process (after transfer, after etch etc.) as much as possible to keep track of the sample and understand the effects of the processes.

2.4 Etch

2.4.1 Xenon Difluoride

A known technique for silicon etch, and concurrently graphene fluorination, is the vapor phase etch using xenon diuoride (XeF_2) [12], [21]. The process of fluorination/etch was carried out in a Xactix system at MNTL. The chamber (shown in figure 9) is pumped down to vacuum before performing the etch. Graphene exposed on one side to XeF_2 for just a few minutes gets instantly fluorinated [12]. It is important to note the selectivity of Si to SiO_2 when it comes to XeF_2 etching. As Williams and Miller indicate [21], while silicon is etched quite quickly with XeF_2, there is no chemical selectivity toward SiO_2. Hence, etch would be imperceptible in areas where native oxide grows over the exposed silicon. Silicon exposed to oxygen rich environments has reported growth of up to 10 Å (Angstroms) at room temperature [22]. If there is moisture or oxygen in the environment, one can expect at least about 2-5 Å of native oxide to be present on the surface. It is imperative to remove this weak oxide as there are no mechanisms to break it down during XeF_2 etch.

Figure 9: Xactix system at MNTL. Etch takes place in the circled chamber. Image Courtesy: MNTL clean-room website.

A chemical step utilizing 10:1 H_2O:HF solution is used to treat the sample prior to XeF_2 exposure. Following this, the sample was placed in the pressure chamber and pumped down. XeF_2 vapor was introduced into the chamber by opening a valve to a solid XeF_2 source. Due to its low vapor pressure, gaseous XeF_2 flows into the chamber. Nitrogen (N_2) was also introduced into the system as a buffering agent. It is common practice to allow an inert gas (such as N_2) into the system to aid the movement of reaction by-products away from the etch surface; this helps to maintain reaction kinetics. The partial pressures of XeF_2:N_2 was 1 Torr:35 Torr. This is in the range of medium vacuum. The etch was performed three times for 60 seconds each, totaling 180 seconds. After each etch cycle, the system was evacuated to rid it of XeF_2, N_2 and the by-products. The balanced chemical reaction is given in equation 2:

$$2XeF_2 + Si \rightarrow SiF_4 + 2Xe \quad (2)$$

2.4.2 RIE

Reactive Ion Etch (RIE) systems make use of plasmas generated by a high-frequency RF signal (usually at 13.56 MHz) to do a directional etch. Plasma RIE can broadly be classified into capacitively coupled plasma (CCP) and inductively coupled plasma (ICP) RIE

systems. The systems are further described below.

CCP RIE: In this version of RIE, the bottom plate is left floating and it has no DC discharge outlet. The high-frequency RF signal applied between the bottom and top plates is usually has a few hundred watts of energy. The high rate of signal switching strips the incumbent gas mixture of its electrons as they oscillate back and forth between the two plates. These electrons move around the chamber due to the field, and strike the walls and the plates. However, since only the bottom wafer plate is DC isolated, a negative charge builds up in it. Charge from electrons hitting chamber walls etc. is dissipated to ground. This accelerates the positively charged radicals from the gas mixture, which were stripped of electrons, toward the bottom wafer plate. Hence, directional etch can result due the field. Sputtering also occurs as a result of the kinetic energy from the traveling molecules. It is at once also evident that the density of the plasma and the energy of the radicals are proportional to each other – application of a higher energy signal causes greater stripping of electrons (more radicals) and also increases the charge on the wafer plate (greater acceleration as a result). This can be considered a drawback of CCP RIE, as opposed to ICP RIE where the kinetic energy and density of radicals are decoupled.

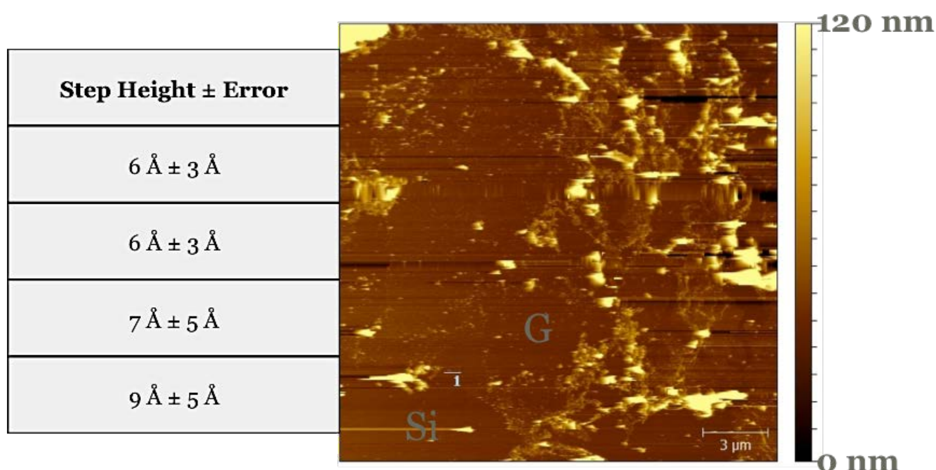
ICP RIE: The main difference with ICP RIE is that much lower radical energies are possible, inciting lesser etch damage. The plasma is struck in a separate chamber and a bias to the sample is applied in a different chamber. During plasma generation, the bias between the plates goes to about 250 V, as is the case with CCP RIE as well. However, the energy of the radicals incident on the sample could be as low as 1 W, since a low bias can be applied in the second chamber where the sample is. Directionality without etch damage can be achieved, though etch rates may be much slower than CCP RIE. Using Freon-14, or carbon tetrafluoride (CF_4), the chemical reaction would look like the following:

$$4CF_2 + Si \rightarrow SiF_4 + 2C_2F_6 \quad (3)$$

3 RESULTS AND DISCUSSION

3.1 Xenon Difluoride

The pattern transfer from the graphene mask to the silicon substrate is characterized below and the effectiveness of each method is analyzed. The first step of the process was to use a simple technique as a control for assessing the success of the mask. Xenon difluoride (XeF_2) etch (mechanism explained previously) was used first. The initial data of the graphene film is briefly presented. In figure 10, the film shows step heights of less than 1 nm under the AFM, which corresponds to a monolayer. Values much lower than this are suspect, since it would be close to the resolution of the scope.



Step Height ± Error
6 Å ± 3 Å
6 Å ± 3 Å
7 Å ± 5 Å
9 Å ± 5 Å

Figure 10: Step height of graphene on silicon under the AFM.

Raman data provided insight into its quality and also confirmed an I_{2D}/I_G ratio of between 1 and 2, as noted in table 1. Folds or wrinkles in the graphene layer can cause this ratio to be lower than predicted for a monolayer.

Table 1: Tabulated data of graphene under Raman. Red laser (632 nm) was used.

Sample #	2D (cm⁻¹)	G (cm⁻¹)	2D (fwhm)	G (fwhm)	2D (intensity)	G (intensity)	2D/G
#1	2669.4	1576.1	41.05	18.875	816.75	548.988	1.4694
#2	2670.8	1576.7	41.1	28.9	592.79	373.263	1.6249

SEM images help show the pattern of the graphene and metal. The thin strips between the

large, labeled pads are graphene. Some waves caused by wrinkles of the film can be observed in figure 11.

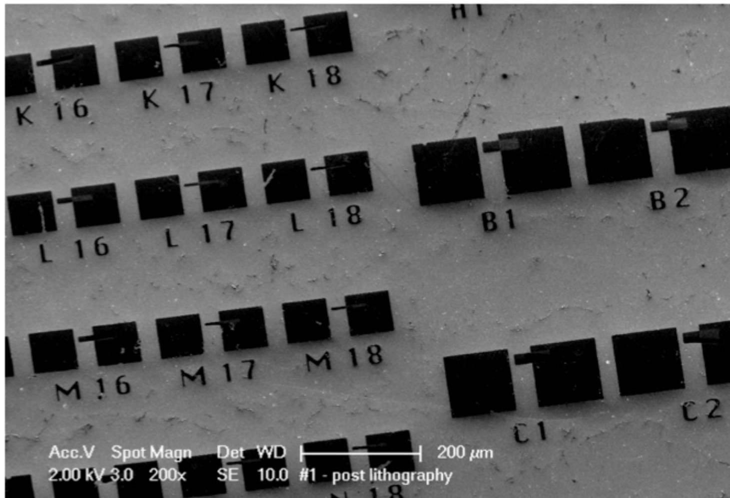


Figure 11: Patterned graphene under the SEM. Large square pads are metal (Ti/Au) and small strips between them are graphene.

After etch, the sample was imaged and characterized using SEM, AFM and Raman spectroscopy. The SEM image of the resultant etched sample is shown in figure 12.

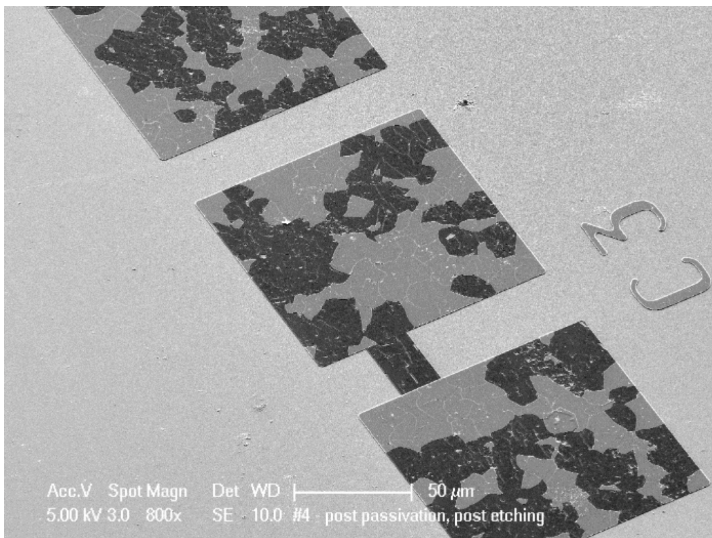


Figure 12: SEM of one pad and graphene channel after XeF_2 etching. Darkest regions are graphene, lightest regions are Si/native oxide. Big square pads are delaminating metal areas.

Figure 12 does not reveal much about the etch, except to show that there is some

delamination of the metal after etching. This is possible due to the hydraulic forces from the wet step to remove native oxide. Owing to the weak adhesion of metal on graphene (inorganic on organic), the metal could have delaminated. The exposed graphene is visible as the dark areas, which is the same shade as the graphene channel. A slight shift in surface topology can still be seen, since the metal areas are at a higher level than the bulk substrate.

Figure 13 more clearly depicts the etch of silicon. There is a definite height difference as shown, and the pitting is characteristic of an etch from XeF_2. Owing to the relatively low concentration of XeF_2 vapor, the area around each XeF_2 molecule, or a cluster of XeF_2 molecules, acts as a local center of etch. This locally (and globally) isotropic etch would tend to cause pits in the surface, making it rougher. The surface can be smoothened by running the etch at a higher XeF_2 partial pressure. This was, however, not attempted since the goal was to verify that two separately known processes (etch of Si and fluorination of graphene) can occur concurrently without affecting each other. Further examination of this follows.

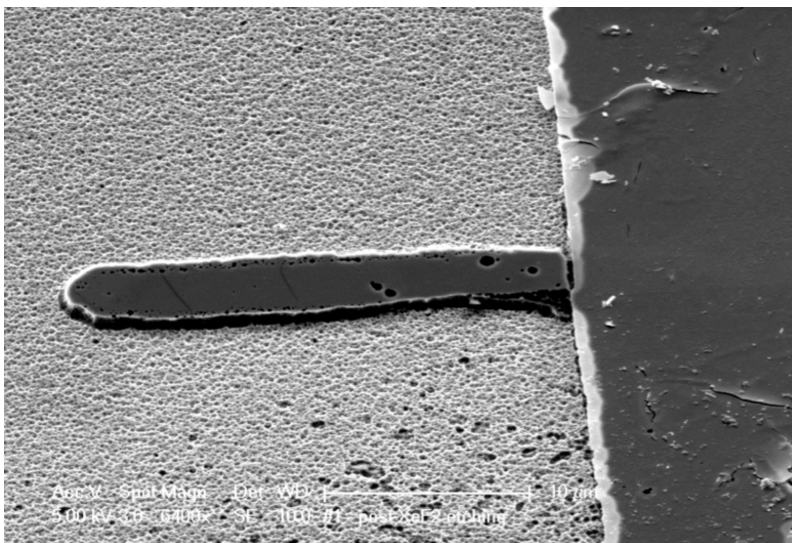


Figure 13: Close-up SEM image of the etched sample. Height difference and surface roughness are apparent, indicating etch.

While etch was evident, it was not necessarily consistent. The processing steps and the quality of the graphene had a role on how the pattern retention turned out. Grain boundaries in the graphene layer seem to have provided avenues for the etchant molecules to seep

through and etch the silicon underneath, also delaminating the graphene mask in the process. This is a plausible explanation judging by the widening of cracks on the graphene channel and the corrugated nature of the silicon beneath it from the SEM images in figure 14. This theory was not readily verifiable as grain boundaries are not easily observable under an SEM or AFM. Grain boundaries are more reactive and are often the source of functionalization and etching, as evidenced by the work of Zhang et al. [23], where hydrogen was used to etch graphene along grain boundaries and produce single crystal islands. A milder version of a similar mechanism could be taking place with the grain boundaries and XeF_2. These cracks could also be the result of wrinkles and tears from transfer since they are not consistent with all parts of the graphene. Should it be a result of grain boundaries, it would more likely be observed on all or most graphene channels, which was not the case. Hence, it is possible, and more likely, that human error from processing is causing the inconsistency. The next step of verification was using Raman spectroscopy to confirm the functionalization of graphene.

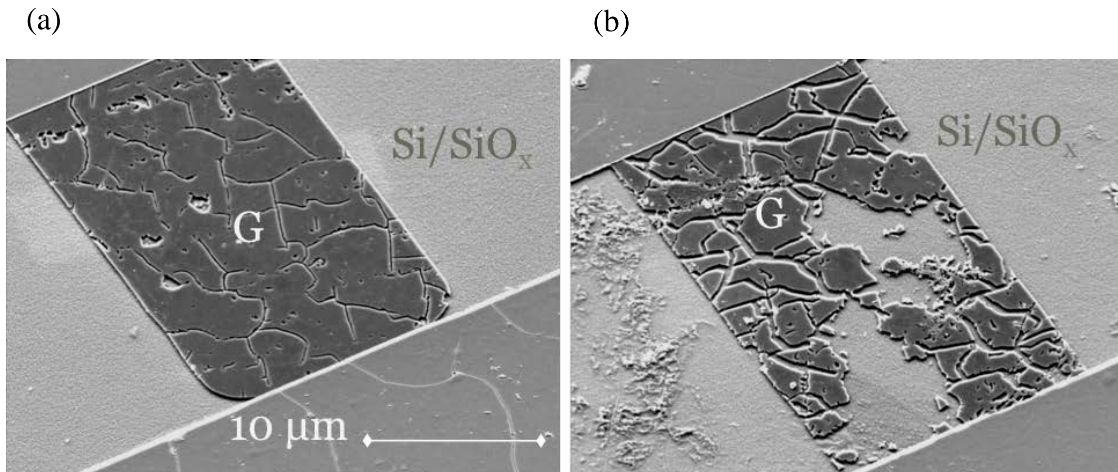


Figure 14: SEM images from around the same area showing a lack of pattern retention, possibly due to cracks from grain boundaries or tears/wrinkles from transfer.

When a monolayer of graphene is imaged using Raman, as was previously shown, the dominant peaks are the 2D and G peaks. Now, with the localization of electrons due to the sp_3 hybridization of carbon atoms to form C-F, the D peak value is much higher, as visualized in figure 15. Hence, expected functionalization of graphene with fluorine is shown. Finally, AFM imaging using the tapping mode AFM found in our lab was employed

to look at the step height from the etch. The results corroborated with previous evidences of etch, showing about 200 nm of silicon removal. The following image illustrates the etch height. In figure 16, the images were taken at separate locations and show how the top of the graphene differs from the bulk etched silicon. The dark areas are the silicon while the bright areas are graphene. One of the limitations of this process is undercut. Undercut results from an isotropic etch, as with XeF_2, and widens features more than needed.

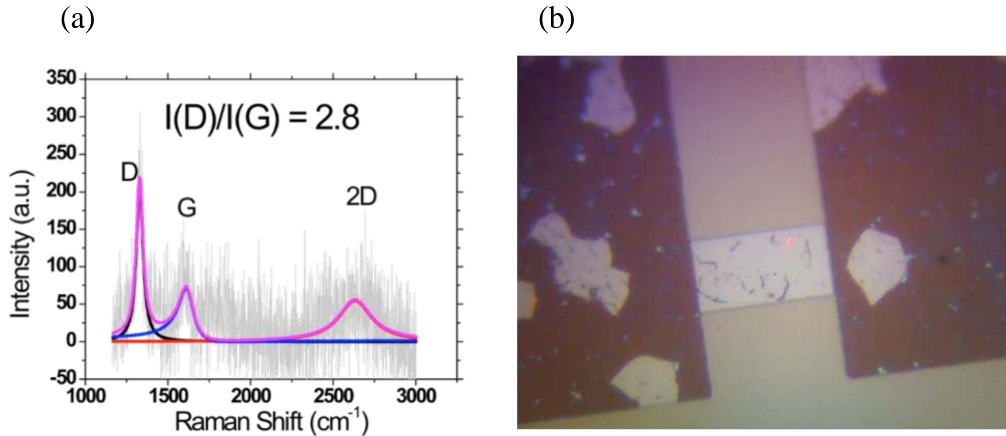


Figure 15: Raman spectrum with red (632 nm) laser. Image (a) is the spectrograph of relevant peaks. Image (b) shows the optical image of the surface and the laser spot on the graphene channel.

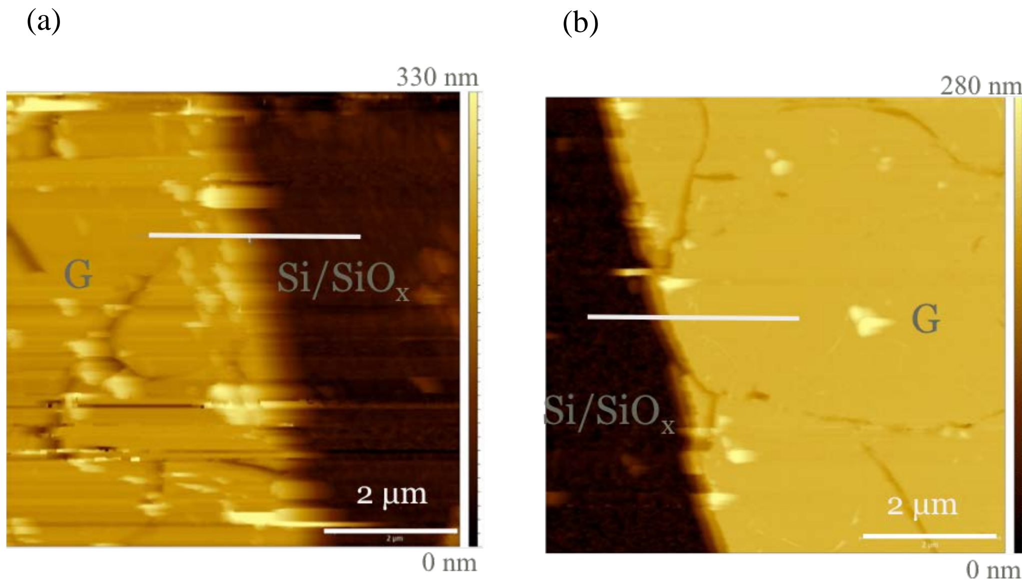


Figure 16: Two AFM images showing similar heights. (a): 160±20 nm. (b): 190±9 nm. The heights are measured across the gold lines.

Figure 17 illuminates this characteristic of XeF_2 etch – there is a wide berth between where

the graphene should theoretically end and where the mask actually covers the surface. A depth profile greater than the bulk etch can also be imagined from the trench adjacent to the masks end. One can imagine XeF_2 molecules accumulating near the graphene/silicon edges and not having much room to move around (laterally). Hence, the molecules can tend to remain in the tight spot a little longer, effectively inciting more reactive with the silicon. Thus, a trenching effect could result. Delamination of graphene and metal is also a challenge to address. Graphene is flaking away in certain areas possibly due to hydrostatic forces from the various liquid steps. These include application of PR, development of PR in a solvent, stripping of PR (with mild sonication) and a HF dip step to remove native oxide. Hence, such causes for variances need to be minimized to learn more conclusively the capabilities and limitations of the graphene etch mask. Nonetheless, we can gauge the robustness and suitability of graphene to withstand such mechanical wear from the above-mentioned processes.

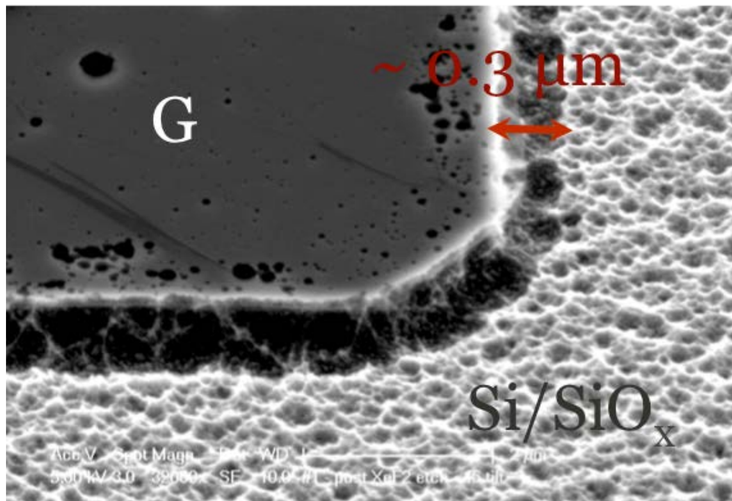


Figure 17: SEM image at high magnification showing undercut of silicon from XeF2 etch.

3.2 Reactive Ion Etching

3.2.1 CCP RIE

In a bid to fnd an anisotropic etch and remove a wet step, Reactive Ion Etching (RIE) was put forth as the next logical step. The first instance of the RIE was with Capacitively Coupled Plasma (CCP) RIE. This was carried out in the Plasma Freon RIE chamber in the clean-room of the MNTL. This time, a TEM grid was used as a shadow mask to remove

the metallization step from the equation and simplify alignment during photolithography. The resultant pattern prior to being subject to any etch is shown below in figure 18. This graphene pattern on silicon was then placed in the Freon RIE machine. The conditions were set to the mildest possible in the machine to ensure minimal sputter damage. The etch was carried out for about 20-30 seconds with 60 W of power, 30 mTorr of chamber pressure and about 21 sccm of CF_4 gas flow. These conditions were borrowed from many other previous works [12], [24] that fluorinated graphene. A lower parameter set could not be used with the CCP RIE since a plasma could not be struck.

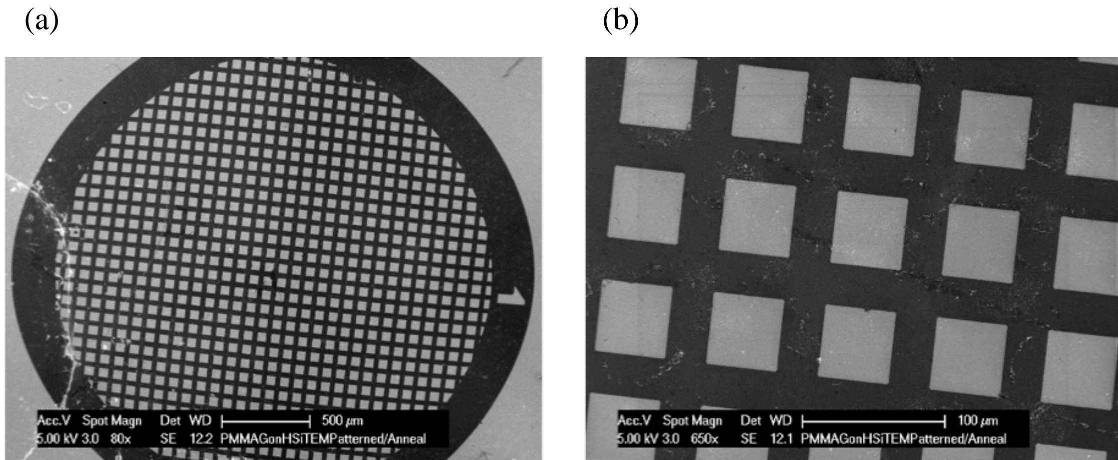


Figure 18: SEM images of TEM shadow mask grid pattern of graphene. Dark areas are graphene, lighter regions are silicon. Left shows an overall view while right is a close-up of how the squares look.

This etch proved detrimental to the graphene mask, as most of the graphene ended up being removed. Physical sputter due to the energetic radicals, as predicted, was sufficient to bombard the single atomic layer. Two results evident from this cycle were that (1) the graphene offered some resistance to the incumbent radicals as seen by the contrast between previously covered areas and exposed squares in the SEM images in figure 19, and (2) there seems to be an edge affinity to the graphene removal, which suggests a semi-chemical process. The corners of the graphene junctions are radially going inward, as illustrated more in figure 19, which could be attributed to the ability of the end atoms to bond with the radicals and be whisked away. Many trials with Freon (CF_4 and CHF_3) gases were performed to yield useful results.

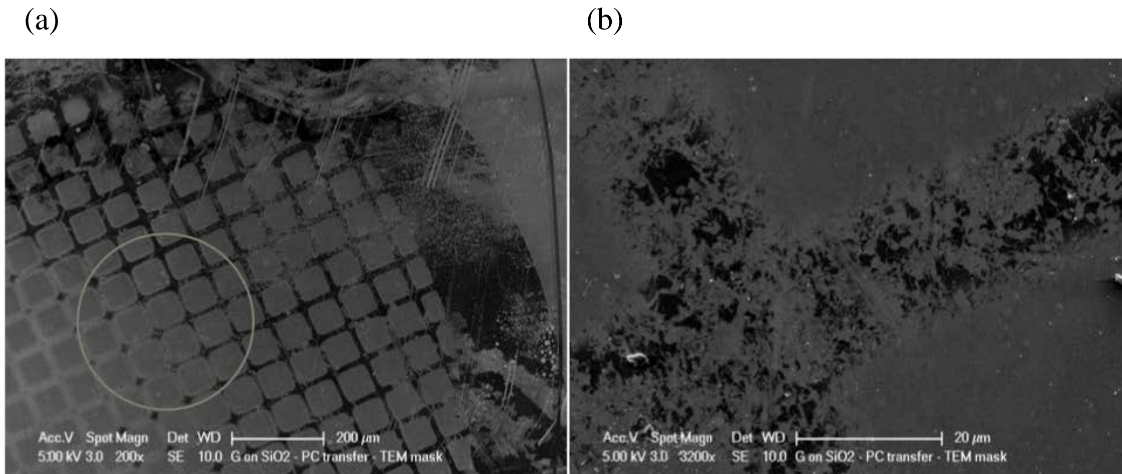


Figure 19: Post etching SEM images with CCP RIE using CF_4. Sputter damage and edge affinity can be observed. The white circle highlights areas with the radial inward trend.

Unfortunately, the physical nature of the etch meant this path had to be abandoned. A modification to this RIE process was to try doing it facedown (FD). The idea was borrowed from Tahara et al, where much less defect damage was reported on FD fluorinated graphene sheets [25]. The set-up is shown below in figure 20.

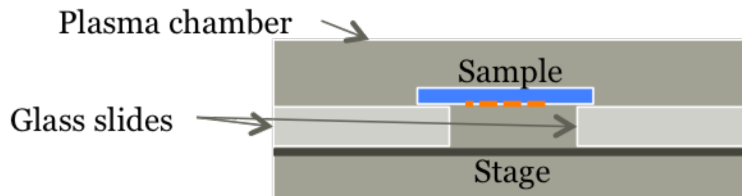


Figure 20: Facedown (FD) RIE set-up to minimize direct sputter. The orange dashed line symbolizes the graphene pattern.

With the graphene pattern facing the bottom plate, and the sample suspended between two glass slides, radicals could get under to etch the silicon. The etch is hypothesized to certainly be slower due to the decreased exposure to the path of the radicals, and possibly more isotropic since the same directionality from the field is no longer present.

However, FD RIE was ineffective is causing any noticeable etch (figure 21). This was visible to the naked eye since the pattern did not become any more pronounced after the process. Graphene is practically invisible on silicon due to its almost total transparency. Etching of the features makes the grid pattern prominent due to the depth difference. The

absence of this optical contrast made AFM and Raman data very difficult to procure.

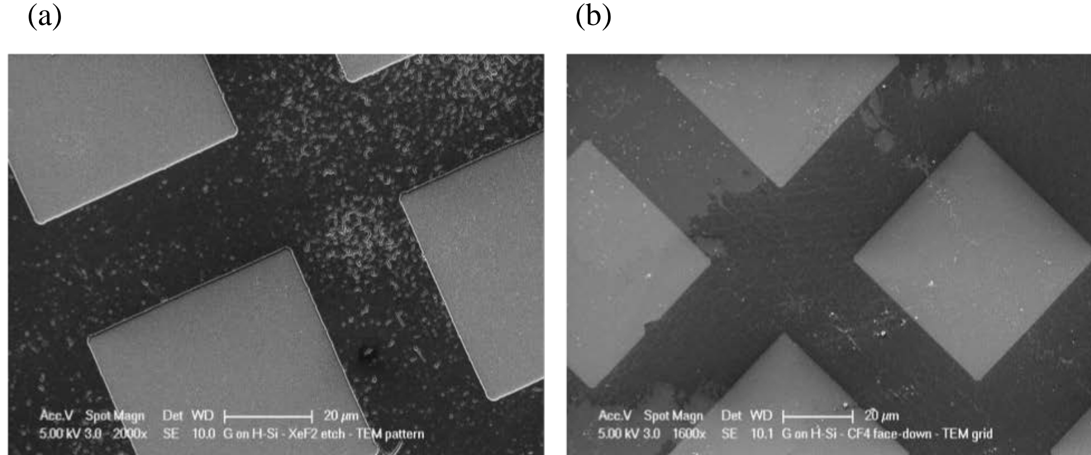


Figure 21: (a) XeF_2 for control and (b) FD RIE performed on graphene grid pattern. There is no consistent pattern retention with FD RIE.

An HF step was performed before FD RIE to remove the native oxide, should the lack of physical sputter be inhibiting any form of etch. It was in vain as no change was observed with the step. A more feasible option, ICP RIE, was considered instead.

3.2.2 ICP RIE

To be gentler on the graphene, ICP RIE was tried next. The ICP RIE Plasma machine was found in the MNTL clean-room. The conditions were 10 W of power, 10 mTorr of chamber pressure and 5 sccm of CHF_3 flow. CHF_3 was used instead of CF_4 due to the latter's unavailability in the ICP RIE machine. As a first order characterization of etch effects, this choice of gas has little effect.

First, SEM data post CHF_3 etching is presented below in figure 22. Two runs were performed for different times. One was at the above mentioned conditions for 2 minutes and the other one was at the same conditions for 10 minutes. The next two SEM images in figure 22 show the aftermath.

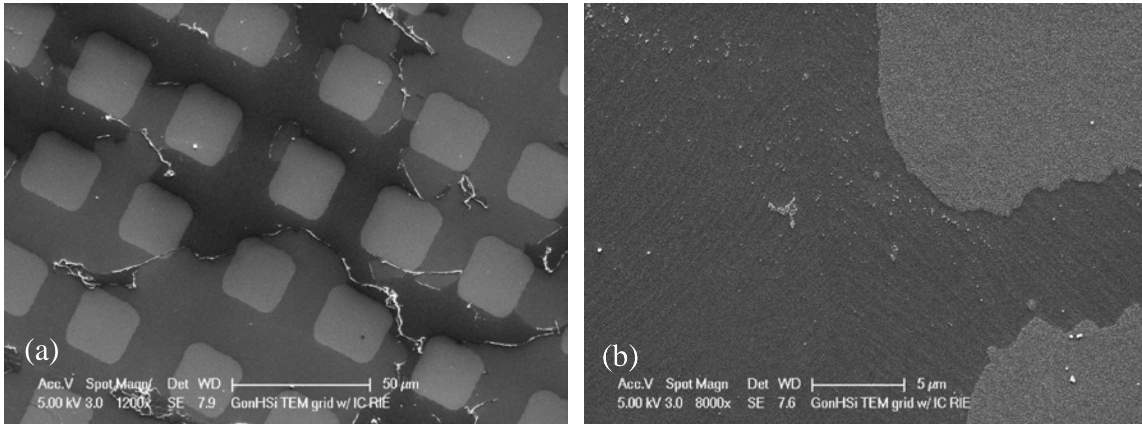


Figure 22: 2 minutes (a) and 10 minutes (b) of ICP RIE etching. Graphene coverage seems to disperse slowly within 2 minutes, and surface seems altered after 10 minutes.

It is noted that the graphene is slowly being removed. After 2 minutes, there is very sporadic coverage of graphene, as represented by the darkest parts of figure 22-a. The lighter regions, in (a) and (b) of figure 22, are the exposed areas from the TEM grid pattern. They are silicon areas with some native oxide due to ambient exposure. Graphene coverage was even more remote after 10 minutes of ICP RIE. This was a strange case, since there was more graphene left on the silicon after CCP RIE, which is harsher on the graphene. Nonetheless, AFM was used to find the step height of the etch.

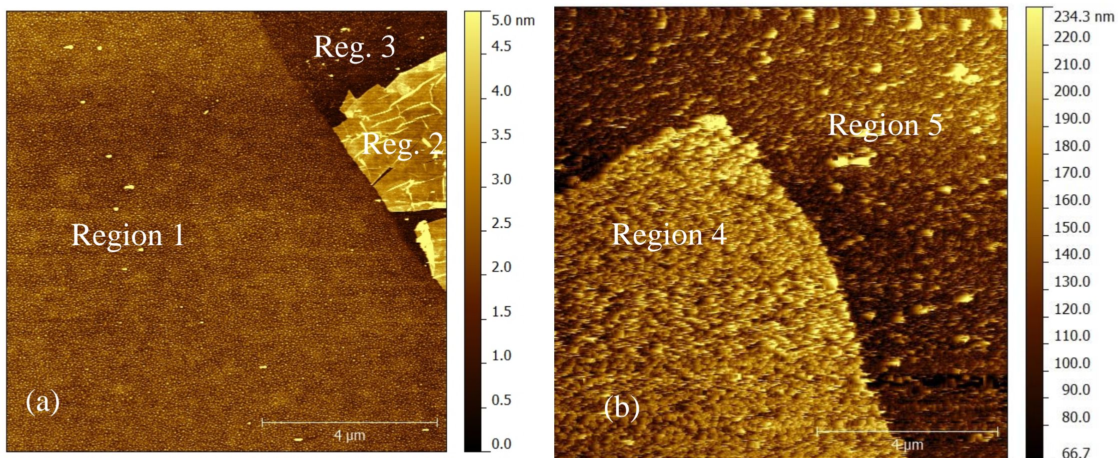


Figure 23: (a) 2 minutes and (b) 10 minutes of ICP RIE etching under AFM. Step height is ~1-2 nm in (a) and ~120 nm in (b).

It is obvious from the AFM data that etching happened after 10 minutes of exposure. In the case of 24-a, we were fortunate to find an area where there was graphene (the lightest

region or region 2) as most of it had disappeared. The step height between regions 1 and 2, i.e. exposed silicon which would be mildly oxidized and graphene, is about 1.7 nm. This is close to the atomic layer height of graphene and could be inflated slightly due to folds, wrinkles, edge artifacts and resolution limits of the AFM. The step between regions 1 and 3, which is probably slightly etched silicon, is about 0.8 nm. This shows very little etching at 2 minutes but nothing as yet can explain the disappearance of graphene. The height between regions 4 and 5 is 120 nm. This is evidence of a lot of etching, though the mask has been inverted. This inversion of the mask can be explained by native oxide being present over the exposed silicon area (region 4 in figure 23-b) and shielding the removal of silicon. Since graphene is being removed from the grids (region 5), either due to the chemistry with the radicals or poor coverage and adhesion with the surface. The root mean square (RMS) surface roughness extracted from AFM measurements show that region 4 is much rougher than region 1, both of which are supposed to be exposed silicon (with some native oxide). Region 1 has a roughness of ~0.6 nm whereas RMS roughness of region 4 is ~30 nm. Despite the masking of silicon in the square areas by native oxide, there is some alteration to the surface which is not clear as to why. Region 5, which in this case is passivated silicon without any shield, has a RMS roughness of ~25 nm, which is relatively close to the RMS roughness value of region 4. Despite the difference in etch, the two regions seem to have been affected in a similar manner on the surface. An explanation for this could be that the native oxide is thin (order of a few to tens of angstroms), and the native oxide layer could be interspaced with silicon atoms displaced from the bulk lattice [26]. These could be bonding with the incoming radicals and be etched, causing the corrugation. After a certain point, when all these intermediary atoms have been removed by fluorine radicals, the native oxide that remains continues to provide protection to the bulk silicon lattice underneath. This can explain the similarity in RMS surface roughness and the step height between regions 4 and 5.

To further conclusively confirm the absence of graphene in the etched samples, Raman spectroscopy was performed. As expected, no graphene bands, namely the 2D and G peaks at 2700 cm^{-1} and ~1600 cm^{-1} respectively, were found in the sample with 10 minutes of etching.

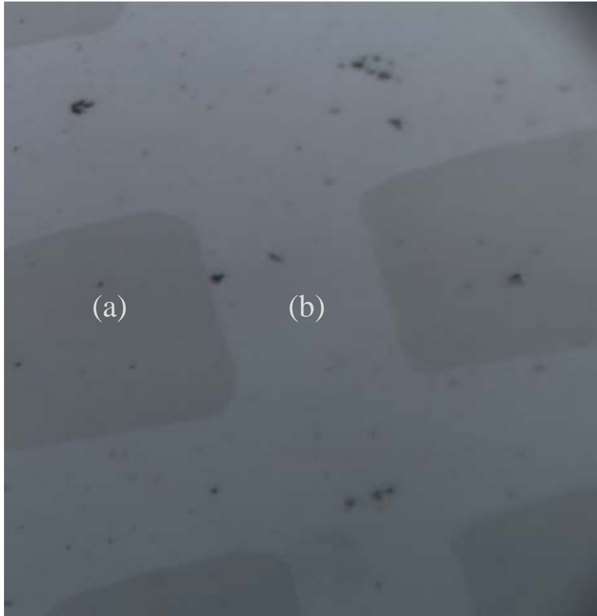


Figure 24: Optical image under microscope before Raman on the sample that was etched for 10 minutes.

Figure 24 shows the optical image under 50x zoom. The darker square regions, as already mentioned, are exposed silicon areas that would have had native oxide from the ambient grown on them. The lighter regions should have graphene, but as shown by SEM, do not retain it. This is confirmed by Raman spectroscopy of the region, as shown in figure 25.

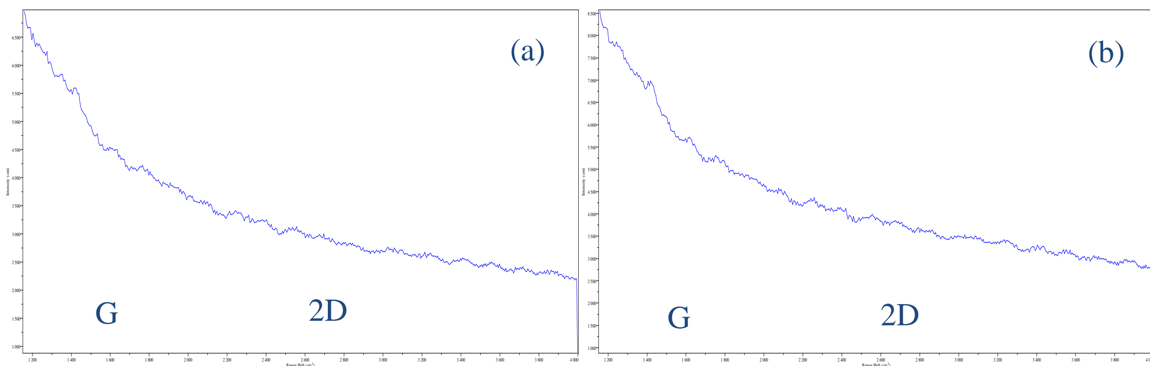


Figure 25: Raman data of (a) dark square area and (b) lighter area corresponding to figure 24. 2D and G bands are missing in both regions, showing that there is no graphene anywhere.

To verify if the incoherent effects were due to etch type or the graphene, xenon difluoride (XeF_2) etching was performed on samples prepared with the same graphene used for ICP RIE. Since XeF_2 etching is gentle on the graphene and formed the initial benchmark for graphene masking of silicon, it would indicate if the RIE etch was inherently unreliable for this purpose. Not too surprisingly, similar artifacts were observed with XeF_2 as well.

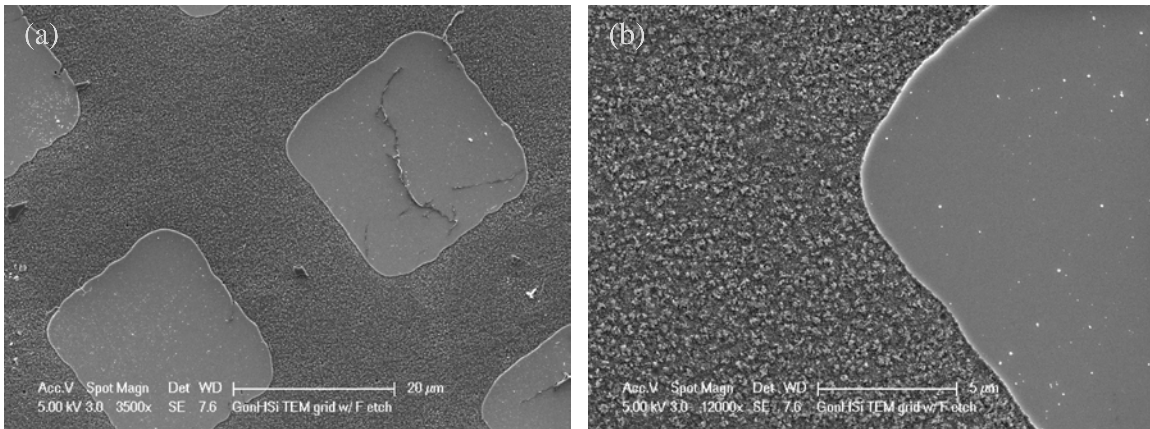


Figure 26: SEM images of the graphene/silicon TEM patterned sample after XeF_2 etching.

This reversal in etch mask is again observed as noticed by the corrugation on the "graphene" areas of the pattern in figure 26. The square pads, which were exposed by the graphene mask, came out smooth and unscathed. Comparing this to figure 21-a, it is clear that the graphene is not acting as the primary mask. The graphene is protecting the hydrogen passivation of the silicon beneath it, which prevents any native oxide growth. Upon fluorination, a poorly grown film has etchants seep under it and remove the silicon, delaminating the graphene from the top surface in the process. The square pads, which were exposed to air all along, have no chemistry with the fluorine molecules to react with them. The fluorine species here does not even have physical energy from momentum to get under the native oxide surface and etch the sub-layer silicon.

The RMS surface roughness and the step height from AFM are indicative of the lack of effect of the process on the square pads. Figure 27 shows the edge of a square and the RMS roughness within the square is ~5 nm, which is in the ballpark of that of native oxide. In the bulk, the RMS roughness is ~30 nm, which is similar to what was obtained from ICP RIE etching. The step height is ~300 nm, which shows substantial etch of silicon. The conditions followed were similar to those used previously – partial pressures of XeF_2:N_2 were 1 Torr:10 Torr and etch was done in three cycles of 60 seconds each. This signifies a relatively high etch rate, and one much larger than for ICP RIE.

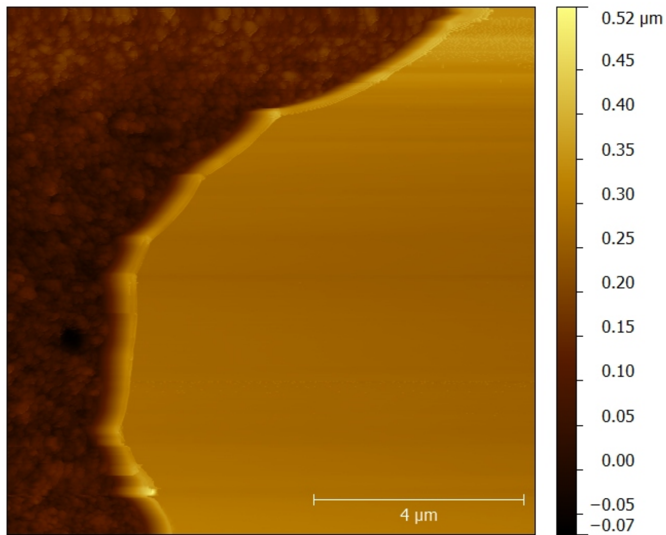


Figure 27: AFM post XeF_2 etching of graphene/silicon using graphene from same growth. Step height was ~300nm.

Hence, it is evident that the process was compromised with a poor batch of graphene and/or bad transfer. Other projects utilizing this graphene growth suffered from unreliability and lack of quality and there was reason to believe that the furnace was contaminated during this period.

4 CONCLUSION AND FUTURE

The graphene etch mask has been demonstrated to be effective for patterning microscale features on silicon using a non-damaging etch. Though the mask has more potential in theory, it requires more experimentation before its practical issues are resolved. Etch conditions have to be finely tuned to ensure the graphene can actually behave as an etch mask. Techniques such as Low Energy Electron Enhanced Etch (LE4), developed originally by Pat Gillis [1], [27], might pave the way for future etch that can couple graphene as an etch mask and use a directional, gentle etch. In the near future, carbon nanotubes (CNTs) could also act as an etch mask due to their easy, proven bottom-up synthesis and strength. However, they will not have the same conformity as graphene, a desirable feature when it comes to nanoscale patterns. Removal of the graphene mask post-etching is also a challenge that would need a solution for sustainable use in the future. At this juncture, this is a positive step toward a novel, cost-effective silicon etch mask that might be able to support nano-fabrication of FinFETs.

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