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Research on Pulsed Power Generation Based on Inductive Energy Storage (IES)

A Dissertation

By

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ABSTRACT

Pulse power technology is an effective means to produce extreme physical conditions. These conditions include high current strong electric field, ultra high voltage strong electric field and gas discharge plasma. These features enable pulse power to produce some special effects and thus bring unique applications. These applications can greatly improve the human ability to transform nature and improve the well-being of human life. While, with people demand more and more of their quality of life, pulsed power technology has extended its applications from traditional fusion and defense fields to many industrial areas, such as food processing, water treatment, laser pumping, and even cell manipulation [1]. At the same time, reliable and durable pulsed power sources are being developed in order to meet the requirements of industrial applications. This technical trend has pushed forward the evolution of not only the components but also the circuit methods of pulsed power generation. Pulsed power generation starts from energy storage. Although the capacitive energy storage (CES) has been the dominating method so far, it has been long since people realized that inductive energy storage (IES) could be more efficient and compact[2]-[4].In this article, we study the circuit topology of the IES pulse generator. This study is divided into five parts. The first part is the introduction, which mainly summarizes the progress of the development of the pulse power source circuit, and finds that the current research and application of the IES topology are not much. The second part, the pure inductor energy storage circuit is studied. Its advantages and shortcomings of IES are deeply recognized. In the third part, several new circuits proposed, there are called IES pulse forming line adders. The experimental results show that they can output nanosecond square wave pulse and more efficient with the load

matching easily. In the fourth part, in order to improve the energy density of the device, the IES Blumlein line is studied. Then, on this basis, a compact IES Blumlein line adder is developed.

Key Words Pulsed power systems, pulse generation, inductive energy storage, transmission lines, semiconductor switches.

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CHAPTER I: INTRODUCTION

1.1 An overview of pulse power technology

1.1.1 History and present situation

Pulse power technology is a new science and technology in the past 60 years. If only from the literal meaning, it is difficult to understand its connotation Because there are many ways to generate electric pulse square wave, such as the control method in power electronic power supply, PWM modulation is a typical electric pulse square wave, and for example, a variety of square wave generators in the field of electronic communications, it is obvious that the two case of appeal does not belong to the category of pulse power. It is clear that two cases of appeal are not in the category of pulse power. In fact, in the history of the birth and development of the so-called pulse power technology, its power is often high power. Therefore, the long term "pulse power technology" is actually "high power pulse technology". A large number of researchers also call it "strong relativistic particle beam" or “high power particle accelerator” according to their load and application place [2].

The concept of relativistic electron beam in the early medieval twentieth Century by Alfonso et al (Alfven), and in 1938, the United States Kingdon and Tanis first published a paper on the microsecond pulse power generated by high-voltage pulse X ray. After a year, the former Soviet Union successfully produced a Marx generator that simulated lightning shock waves in the field of high power rate pulses in 1939. However, the internationally recognized pulse power technology's theoretical formation and practical application owe to the J.C, Martin [2][3] and his team of the British Atomic Energy

Research Center (AWE) in the 60s of last century. Therefore, at the 1981 International Conference on pulsed power, J.C. Martin won the special contribution award in the field of pulsed power ("Erwin Marx" award), in recognition of his special contribution to pulse power technology in the last century.

It can be said that in twentieth Century 60 to 80s, pulse power technology developed rapidly. At that time, the development of the pulse power is the arms race that the United States and the Soviet Union extended to the cold war. At this time, the Americans will take the lead in pulsed power technology produced by pulsed X ray for simulation of nuclear explosions, built a large pulse device Hermes II in the 1967 United States Sandia National Laboratory (1TW). In late 70s, due to the inertial confinement fusion scheme is proposed and advocated by the US star wars, various countries have produced their own "high power scientific device", such as: Angara 5 device and LIU-10M, which were built by the former Soviet Union's Institute of Atomic Energy and the Institute of Experimental Physics, respectively. France's Thalie and AIRIX. But, Japan and Germany's political and historical reasons, the pulsed power technology will not be applied to the military, so their device used for nuclear fusion research, there are some the representative devices. For instance, the researchers at Osaka University in Japan make the Raiden-IV. The ETIGO-series [2] were built by the Nagaoka University of Technology. And in Germany, nuclear technology research center do the KAKTUS device. China is also an important force that cannot be ignored in building large-scale pulsed power devices. From the early 1960s, the research team with Mr. Wang Ganchang as the core began to explore the new flash pulse X ray photography based on pulsed power technology, and built the first large device flash -I in China in 1979. In 80s, China's pulse power business has also been

developing rapidly. In 1990, the scientific research team led by Dr. Qiu Aici in Northwest Institute of nuclear physics developed the low impedance accelerator flash-II in China.Table I enumerates some of the international pulse power devices. From the data in the Table I, the United States is the leader of the world's major scientific devices. From the nuclear arsenal National Laboratory (Sandia National Laboratory -SNL, Laurence Livermore National Laboratory, -LLNL) to the company (physical international company -PI, Maxwell) has the ability to develop high power pulse device. It is not difficult to find some interesting phenomena from Table 1. Some large pulse power devices seem to be related to geopolitics and national strength. Let's take note of three interesting points of time, 1965, 1991, and 2000, respectively. 1945-1965 was a period between the end of World War II and the beginning of the cold war. The center of this time science is western society. At this time, the British have a solid foundation, and the Americans are beginning to develop rapidly. In the 1965-1991 years, the United States and the Soviet Union began the "hegemony of the two camps", the so-called period of the cold war. Obviously, the Western leader is already the United States, when the American large power pulse device is completely surpassing any country in the West. Notable Soviet Union has developed a series of devices during this period, and some of the technical routes are different from those in the US, especially in inductive energy storage and short pulse. Unfortunately, after the disintegration of the Soviet Union in 1991, the development of these technologies was slowed. As we turn our eyes back to East Asia, Japan's large pulse power devices are internationally advanced in 1980s and 90s. This seems to be related to the high wealth created by the rapid economic development of Japan from 1961 to 1992. And China has almost nothing to build throughout the 1980s,

in the large pulse power devices. To know this period of time, China's "reform and opening up" has just started and ended the ten years of social turmoil. But after 21 Century, the world is only China and the United States that can build more than 5MA large pulse power devices. Does it mean that the era of G2 is coming?

Looking at the devices in Table 1 from another perspective, some countries in the world are obviously less interested in large pulse power devices, entering the 21st century. The development of peace is the theme of the world, and developing large pulsed power devices for military and nuclear fusion applications has not been as important as before. But in recent ten years, the application of high power nanosecond short pulses in industry has been paid much attention by many scholars all over the world. In the field of biomedicine, the research team in the United States Old Dominion University shows that the strong nanosecond electric field can induce biological effects of some cells. On the one hand, a strong nanosecond electric field can cause the death of cells in the cells of human cells [5][6]. On the other hand, changing the duration of the nanosecond pulse and the number of pulses can cause coagulation of the platelets [5][6].These means that nanosecond pulse technique brings new ways to cancer treatment and homeostasis. In environmental protection, In the field of environmental protection, the Kumamoto University study suggests that less than tens of nanoseconds can form high frequency pulse discharge can be applied to flue gas denitrification [1].Research at the Nagaoka University of Technology shows that a mixed discharge of nanosecond gas and liquid, produced by strong oxidizing substances, can be used to treat industrial waste water [8].In the automobile industry, the ignition of nanosecond discharge can overcome the limitation of the traditional ignition mode and reduce the fuel consumption and reduce

the emission of polluted gas[8].The promise of these attractive application prospects is the development of compact, all solid state, high frequency, and short pulse generator[1][9].

Table 1: International high power pulse device[2][3][7]

Name	**Countries and organizations**	**Main technical parameters (technical route)**	**Time**
Mini B	U.K.Atomic Weapons Research Establishment(AWE)	2.2 MV, 50 kA, (High impedance)	1964
SWARF-II	U.K.AWE	10 MV,100 kA (High impedance)	1986
Magpie	U.K.AWE	1.5MA (Multiple devices parallel)	?
Hermes-II	USA SNL	10-12MV,0.17MA,80ns (High impedance)	1968
Hermes-III	USA SNL	20MV,0.8MA,40ns (Induction voltage adder)	1989
PBFA-I	USA SNL	1.9MV,4.5MA,40ns (36 branches parallel)	1980
PBFA-II	USA SNL	4MV,10MA,40ns (72 branches parallel)	1985
PBFA-Z/ZR	USA SNL	2.5MV,20-26MA,40ns (36 branches parallel)	1996-2010

Gambl-I	USA Naval Research Laboratory (NRL)	0.75MV,0.5MA,50ns (Low impedance)	1968
Gambl-II	USA NRL	0.9MV,1.3MA,50ns (Low impedance)	1970
Mercury	USA NRL	6MV, 0.36MA,50ns (Induction voltage adder)	2004
ETA	USA LLNL	4.5MV,10kA,50ns (Induction voltage adder)	1979
ATA	USA LLNL	50MV,10kA,70ns (Induction voltage adder)	1984
Blackjack5	USA Maxwell	3MV,3.5MA,50ns (Low impedance)	1978
Pithon	USA PI	2MV, 3.5MA,50ns (Low impedance)	1975
DECADE	USA PI	1.5MV,17MA,50ns(Multiple devices parallel)	1983
Thalie	France	10-15MV, 0.2MA,70ns (High impedance)	1974
AGLAE-II	France	0.7MV,1.7MA,35ns (Low impedance)	1981
AIRIX	France	16-20MV,3.5MA,60ns (Induction voltage adder)	2000
ИГУР	Former Soviet Union and Russia	6MV,80kA,20-150ns (IES)	1978

Эмир	Former Soviet Union and Russia	7.5MV,0.2MA,20-200ns (IES)	1990
TOHYC-II	Former Soviet Union and Russia	1MV,1MA,60ns (Low impedance)	1979
Angara-5-1	Former Soviet Union and Russia	3MV,3-5MA,90ns (8 branches parallel)	1989
Liu-10	Former Soviet Union and Russia	14MV,50kA,20ns (Induction voltage adder)	1977
Liu-10M	Former Soviet Union and Russia	25MV,50kA,20ns(Induction voltage adder)	1983
Liu-30	Former Soviet Union and Russia	40MV,0.1MA,20ns	1989
Reiden-IV	Japan, Osaka University	1.4MV,1.4MA,50ns (Low impedance)	1978
ETIGO-II	Japan, Nagaoka University of Technology	3MV,0.46MA,50ns (Low impedance)	1986
ETIGO-III	Japan, Nagaoka Univ.Tech.	8MV,5kA,30ns (Induction voltage adder)	1996
ETIGO-IV	Japan, Nagaoka Univ.Tech.	0.5MV, 13kA,200ns,1HZ (Magnetic pulse compression)	2000

Flash-I	People's Republic of China (P.R.C), China Academy of Engineering Physics (CAEP)	8MV,0.1MA,80ns (High impedance)	1979
Flash-II	P.R.C., (Northwest Institute of nuclear technology)	0.9MV,0.9MA,70ns (Low impedance)	1990
LIA-10	P.R.C.,CAEP	12MV,3.5kA,70ns (Induction voltage adder)	1993
ShenLong-I	P.R.C.,CAEP	20MV,3.5kA,70ns (Induction voltage adder)	2003
ShenLong-II	P.R.C.,CAEP	3MV,>2kA,2MHZ (Induction voltage adder and transmission line delay)	2015
PTS-I	P.R.C.,CAEP	3MJ,8-10MA (24 branches parallel)	2013

1.1.2 Definition, system composition, and implementation

Pulse power technology, in a broad sense, is a science and technology aimed at obtaining short-time high power electrical pulses. It has the feature that the stored energy is loaded in a single or repeated form in the form of a short electric pulse. The traditional pulse power is often required to reach the following electrical parameters: The power is generally above 1GW, and the maximum is in the order of 10^{14}W, the voltage range from10kV to 50MV, the current from1kA to 10MA, the di/dt from 1kA/μs to100kA/ns,

and du/dt from 1kV/μs to100kV/ns. Due to the rise of industrial applications, the traditional electrical parameters are difficult to cover fast pulse and short pulse generator.

Therefore, a new definition method has been put forward by some scholars. This method synthesizes the characteristic parameters of electric pulse, and the specific method is as follow. P_{max}, V_{max}, I_{max} and t_r represent short pulse power capacity, voltage peak value, current peak value and rise time of electric pulse. Then the pulse power technology can be quantitatively expressed as equation 1-1. K_{pr} is the rate of increase of electrical power, in other words, the rate of providing pulse power.

$$K_{\mathrm{pr}} = \frac{P_{\max}}{t_{\mathrm{r}}} = \frac{V_{\max} I_{\max}}{t_{\mathrm{r}}} > 10^{13}\,\mathrm{W/s} \qquad [1\text{-}1]$$

If the physical meaning of equation 1-1 is represented by a graph, it is shown as shown in Figure 1 (a). As shown in Figure 1 (a), if a high power output is to be achieved, an effective method is the energy compression.

The typical pulse power system is shown in Figure 1 (b). It is composed by a primary charging power, an energy storage unit, a pulse forming network, a switch, and a load. Primary charging power is the power source of the whole system. DC power is usually used. The energy storage unit has two forms, the electric field energy storage and the magnetic field energy storage. Their equivalent circuits are shown in Figure 2. For electric field energy storage, a capacitor C is used to store energy. When the switch S is

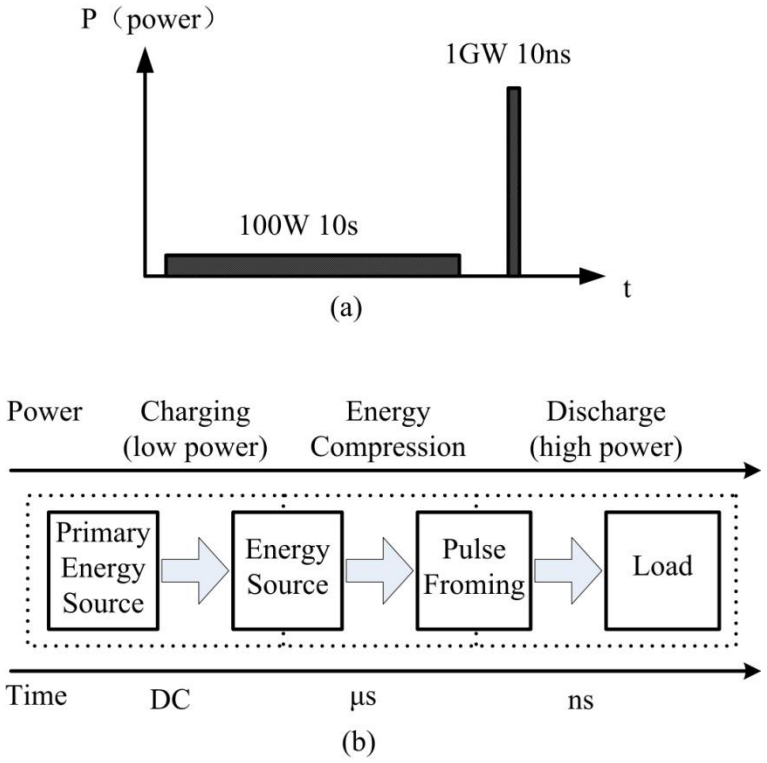


Figure 1: A schematic diagram of definition and system composition.(a) Definition (b) system composition

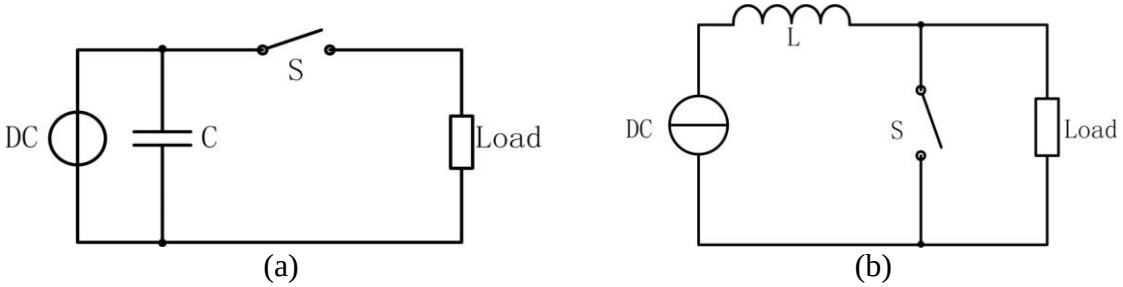


Figure 2: Capacitive energy storage and inductive energy storage.(a) CES (b) IES

opened, the capacitor C will be charged by the constant voltage source. When the voltage on the capacitor C is charged to the switch S is closed, and the capacitor will be discharged to the load. As the load and energy storage element are parallel, the output voltage is equal to the charge voltage. If the closing time of the switch S is far shorter than the opening time of the switch, the output current is far higher than the charging

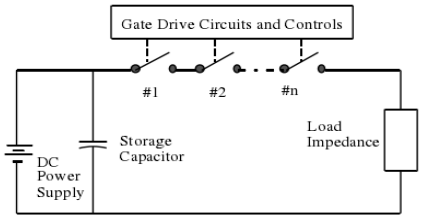
current, according to the energy conservation law. Therefore, the circuit in Figure 2 (a) can be used to obtain the current amplification. While, the magnetic field energy storage is shown by using an inductor as a energy storage element, in Figure 2 (b). So magnetic field energy storage is also called inductive energy storage (IES) circuit. For the IES circuit, the primary DC charging power supply is a constant current source in the ideal case. When the switch S is closed, the inductor L is charged by the current source. When the current in the inductor reaches the preset current, the switch S is opened, and the inductor discharge to the load. Because the inductor L is connected in series with the load, the output current is equal to the charge current in the ideal case. If opening time of the switch S is far shorter than the closing time, the output voltage will be higher than the charge voltage, according to the conservation of energy law.

1.1.3 The development of nanosecond compact solid state pulse power technology

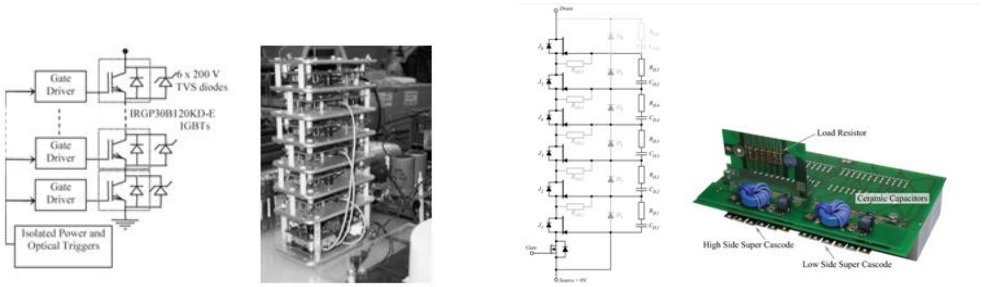
From the previous description, it is not difficult to find that industrial applications require pulse power sources to have the following characteristics. First, it can output short, fast and rectangular pulse. Secondly, the size of the device smaller is the better when the output power is satisfied. Once more, the pulsed power source should have the ability with high reliability and high repetition. Finally, it should have low cost and high efficiency. The development of all solid state pulse power sources is an effective way to achieve the above requirements. The primary problem that hinders the development of all solid state pulse power technology is the limited power capacity of the switches [9].

In recent ten years, scholars from all over the world have invested a lot of enthusiasm in developing all solid state pulse power technology, not only in energy storage components

and switches, but also in the innovation of circuit methods. First of all, it is easy to think of the switch series, based on the circuit making generator in Figure 2 (a). For example, USA scholars use IGBTs in series make a generator with a voltage 6.5kV [10].This circuit has a simple structure. However, multiple switches have to divide the voltage evenly during the operation, and the potential of the switch on the high voltage side is floating. If one of the switches is broken, it will cause the overall overvoltage of the system and eventually cause the system to collapse. The schematic diagram of the switch component is shown in Figure 3(b). In order to solve the problem of floating voltage, the German scholars have developed the switch in series. The SiC-JFETs is used in series to make a generator with a voltage 5kV and a pulse width 50ns,as shown in Figure 3(c) [11]. But, it cannot solve the problem of system stability, because of single switch breakdown.



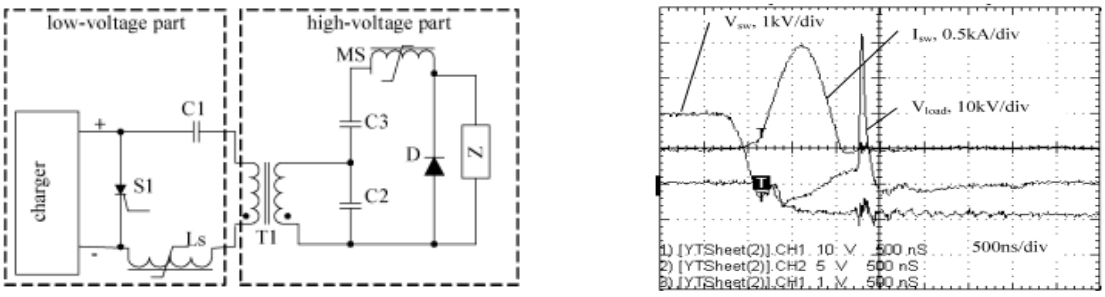
(a)



(b) (c)

Figure 3 Semiconductor switch series circuit. (a) Nanosecond solid-state pulse power source based on switch series. (b) 6.5 kV series IGBTs.(c) 5 kV/50 ns series SiC JFETs[10][11]

Secondly, the invention of magnetic switch effectively solves the problem of insufficient switching power capacity. For example, the Israeli research team developed a 45kV nanosecond generator using magnetic compression and fast recovery diodes, as shown in Figure 4 [12].Although the circuit is easy to obtain high power output, the output waveform is not ideal, not an ideal rectangular wave, as seen in Figure 4 (b). Furthermore, when the circuit is designed, the circuit parameters are fixed, and all the output parameters are difficult to adjust.

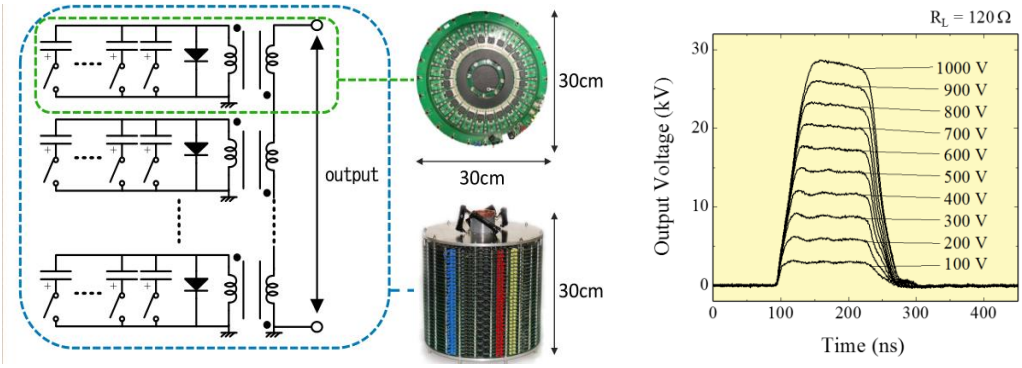


(a) (b)

Figure 4 45kV Magnetic compress circuit (a) The circuit principle diagram (b) Output waveforms[12]

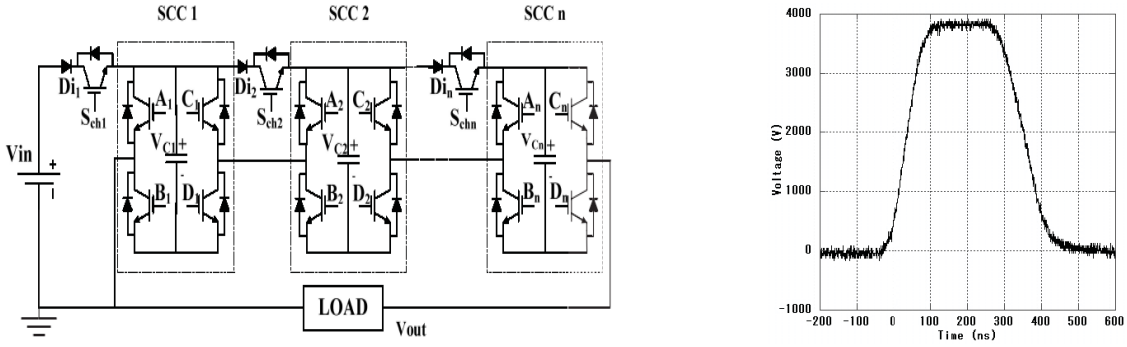
Because of the obvious shortcomings of these circuits, recently, pulsed power system design method has shifted rapidly toward modular concept. Instead of designing and building a pulsed power machine from the beginning, it is more desirable to construct a pulsed power system from pre-manufactured modules. Most of the recently reported solid-state MARX-type or LTD-type generators are developed based on this concept. Modular concept relies on the feasibility of voltage adding and power adding. As a result, the system no longer requires a “main” switch that must be able to handle the total output voltage and output power of the whole system. Therefore, the significance of the pulsed power system modularity is not only on lowering the system cost but also, more

importantly, on the extension of the operation parameters far beyond the limit of a single device. With this in mind, the research team at the Nagaoka University of Technology developed the 30kV solid state LTD[13], as shown in Figure 5. And the research team at the Kumamoto University developed 4kV bipolar Marx[14] for gas discharge, as shown in Figure 6. And researchers from Chongqing University in China have developed the Blumlein line module adder [15] for cancer treatment, as shown in Figure 7.



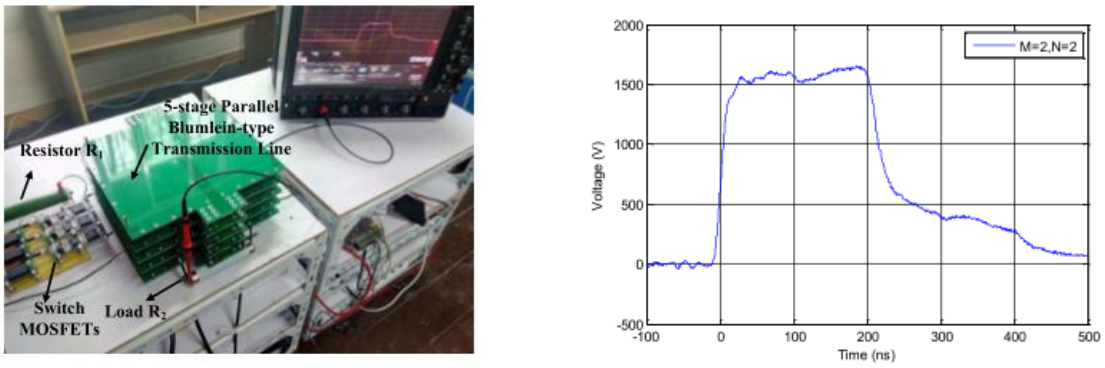
(a) (b)

Figure 5 30kV solid state LTD (a) The circuit principle diagram (b) Output waveforms[13]



(a) (b)

Figure 6 4kV bipolar Marx(a) The circuit principle diagram (b) Output waveforms[14]



(a) (b)

Figure 7 Blumlein line module adder(a) The Physical diagram (b) Output waveforms[15]

It has been long since people realized that inductive energy storage (IES) could be more efficient and compact [16].But the development of the high voltage nanosecond generator based on the inductive energy storage is very slow. Only circuits based on semiconductor opening switch (SOS) and drift step recovery diode (DRSD) are reported [17].Although Russian scholars exploit these special switches to develop a 1MV 50ns pulse generator [17]. However, the purchase channels of these switches are difficult, so the cost is high. The efficiency of the device is less than 60%, and the output waveform is not an ideal rectangular wave [17].

1.2 Research purpose and significance

IES is an important development direction of pulse power technology. The energy storage density of IES is several tens times higher than the CES. Under the condition of a certain volume of the pulse power source, the IES can output a higher energy than the CES. It is easier to miniaturize the system when the output energy is required. The obstacle that has hampered IES has been the lack of suitable opening switches, because high-voltage, high-speed, and high-efficiency opening switch has not been developed yet.

The pulse source using magnetic pulse compression and special switch has no advantages in efficiency, waveform and cost. The new circuit method used IES should be put forward to develop the nanosecond compact solid state pulse power technology. It should have the following features. Fist, it can output the rectangle wave, which has improved the unsatisfactory waveform of the traditional IES circuit. Next in importance, it can output less than 50 nanosecond pulse width pulses to meet the demand for industrial applications for short pulses. Once more, its voltage is superimposed to meet the high electric field applications. In the end, it should be efficient and low cost relative to traditional inductive energy storage circuits. Some successful experiences should be used for reference. On the one hand, the development of the MOSFET switch has been able to turn off less than 10 nanoseconds, but less power capacity limits its application. On the other hand, the application of modular concept in capacitive energy storage has greatly promoted the popularization of CES. The new inductive energy storage circuit in this paper will introduce these useful concepts and create a new circuit method to enrich the compact nanosecond solid state pulse source.

This research has great significance, not only to guide the future design of nanosecond pulse source, but also promoting the development of nanosecond high repetition rate pulsed power technology. As well as compact, ideal rectangular wave, high voltage ratio and high stability pulse power source have important practical significance for environmental protection, health care, or food industry. It will also bring considerable social and economic benefits.

1.3 Research methods and main works

1.3.1 Research methods

1. Theoretical analysis

According to the theoretical analysis, the circuit principle is studied by the method of circuit analysis for the IES pulse power source. The internal relations of CES and IES are discussed by a symmetric analysis method.

2. Experimental study

Based on the theoretical research and computer simulation design, a variety of prototype platform of inductive energy storage pulse power source is set up, and the correctness of the theoretical analysis is verified.

1.3.2 Main works

On the basis of in-depth analysis and study of traditional IES pulse power source, the paper fully recognizes the characteristics and defects of the inductive energy storage circuit. Several new inductive energy storage circuits are proposed by using the dual principle to change the traditional pulse forming line (PFL). Experiments show that these circuits can output rectangular waves, which are better than the output waveform of traditional inductive power source power source. These circuits are easier to achieve load matching and achieve higher efficiency. After the introduction of the concept of modularization, the pulse adding is realized. These circuits can be called IES-pulse forming line (IES-PFL) adder and Inductive Blumlein Line adder.

The main structure of the thesis is as follows:

- In the first chapter, the history of pulse power technology is combed, and then the nanosecond all solid state high frequency pulse power technology is investigated. On the basis of this, the purpose and significance of this study are expounded. Finally, the main work of the paper is briefly introduced.

- In the second chapter, the theoretical knowledge of IES, the charging and discharging process, the energy efficiency, the discharge waveform, and power adding of the traditional IES are elaborated and analyzed. Then, we show its advantages and disadvantages through experiments, and make a summary and analysis. At the same time, some simple power adder experiments are presented, which makes us realize the necessity of improvement.

- In the third chapter, the relationship between the IES and the CES is studied by using the dual principle. Since then, some new circuit topologies are proposed, which can be called IES-pulse forming line (IES-PFL) adder and Inductive Blumlein Line adder. The feasibility of these circuits is verified by simulation and experiment.

- In the fourth chapter, the core purpose is compactness, short pulse and bipolar output. A compact Inductive Blumlein Line adder is proposed. Here, the strip-line is designed as the transmission line, and the silicon carbide MOSFET is used as an opening switch. In the case with the 4 module, a short pulse is obtained, with 15 ns 2kV. And this new type of circuit can get the negative voltage output only by the geometric folding.

- The fifth chapter is a conclusion and prospect.

CHAPTER II: SIMPLE INDUCTIVE ENERGY STORAGE (IES) PULSE POWER SOURCE AND ITS VLOTAGE ADDING EXPERIMENT

2.1 The simple IES circuit principle base on semiconductor switch

2.1.1 Comparison of CES and IES

Before explaining the basic principle of the inductive energy storage pulse power source, it is better to understand the difference between the capacitive energy storage and the inductive energy storage.

Capacitive energy storage refers to the storage of energy in an electrostatic field after the capacitor is charged. For example, a flat plate capacitor, its energy density ω_C is as follow:

$$\omega_C = \frac{\frac{1}{2}CU^2}{V} = \frac{\frac{1}{2}\varepsilon\frac{S}{d}E^2d^2}{Sd} = \frac{1}{2}\varepsilon E^2 \qquad [2\text{-}1]$$

The symbols in the equation represent the following: C-Capacitance, U-Voltage between plates, V-Capacitor volume, ε-Dielectric constant, S-plat area, d-Distance between plates, E- Electric field strength between plates

The inductive energy storage is to store the energy in a magnetic field produced by the current in the inductance coil. For example, a spiral inductor its energy density ω_L is as follow:

$$\omega_L = \frac{\frac{1}{2}LI^2}{V} = \frac{\frac{1}{2}\mu n^2 V\left(\frac{B}{\mu n}\right)^2}{V} = \frac{1}{2}\frac{B^2}{\mu} = \frac{1}{2}\mu H^2 \qquad [2\text{-}2]$$

The symbols in the equation represent the following: L- Inductance, I-Current in the inductor, V-Inductor volume, μ-Magnetic permeability, n-Turn number of coil, B-, Magnetic induction intensity, H- Magnetic field intensity.

It is known from equation 2-1 and 2-2 that the capacitance density ($\varepsilon E^2/2$) is obviously limited by the electric field intensity of the medium, and it is easy to break, when the the medium is charged with high voltage for a long time. Therefore, the long charging time of CES is also limited to the increase of its energy storage density. However, the density of inductive energy ($B^2/2\mu$) is only related to the magnetic induction intensity B, and the high electric field only appears at the output terminal. Therefore, the electric field intensity has almost no limitation on the inductive energy storage, and its energy storage density is almost limited by the electromagnetic force. Therefore, under reasonable numerical conditions, it is known that the density of the IES is several times the CES. It has been shown that the cost of IES is only 10% of CES for energy storage above 5MJ [2].

2.1.2 Operation principle of IES pulse source

The operating principle circuit of the traditional IES pulse source is shown in Figure 8. The basic operation process is as follows: When the primary energy storage unit of C is charged to the working voltage, the switch S is closed. The inductance L can be charged by the capacitor C. When the current reaches the maximum value, the switch EEOS opened, at this time, the current in the circuit is suddenly cut off, causing a high voltage on the inductor L. The high voltage is applied to the sharpening switch Gap, and when

the voltage is higher than the breakdown voltage of the sharpening switch, the switch Gap is closed. Then, the voltage is applied to the load, and driving the load to work.

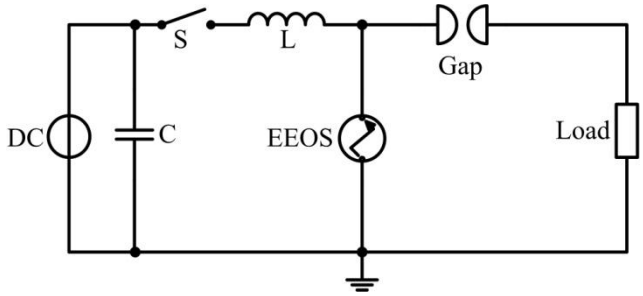


Figure 8 Circuit principle diagram of traditional IES

In the traditional circuit, the electric exploding wire is used as the main opening switch. The advantage of this switch is that its power capacity is large, and it can withstand high voltage after opened. The disadvantage is that the switch speed is slow and it cannot be closed, so some auxiliary switches are needed. As shown in Figure 8, in order to output a nanosecond pulse, it is necessary to sharpening switch Gap and control switch S.

The MOSFET switch is used to replace the electric exploding wire as the main opening switch, and the inductive energy storage circuit can be simplified, as shown in Figure 9. The switching speed of the MOSFET can be less than 10ns, so a short nanosecond pulse can be get without using sharpening switch Gap. The MOSFET, as a fully controlled switch, can perfect all the functions of the closing switch S and the opening switch EEOS, without considering the power capacity of the switch. The operating principle of the circuit is as follows. When the MOSFET switch is closed, the constant voltage source composed by capacitor and voltage source charges the inductance L, and the current in the inductor rising. Because the diode reverses bias, there is not voltage on the load.

When the current reaches a predetermined value, the MOSFET switch is opened, and the current in the inductor flows through the diode to the load.

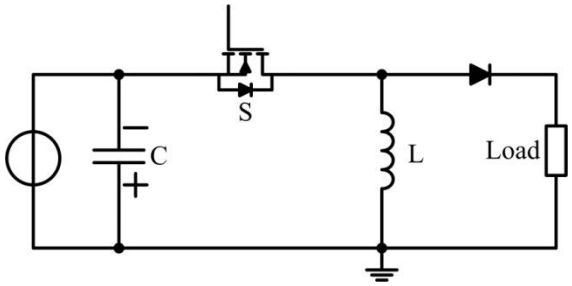


Figure 9 Schematic diagram of a simple IES circuit based on MOSFET switch

2.1.3 Charging process of IES circuit based on semiconductor switch

If the capacitor is large enough and the closing time of the MOSFET switch is not long, the voltage on the capacitor is basically unchanged at this time. Therefore, the inductor charging process can be equivalent to the first order circuit as shown in Figure 10. The meaning of the symbol in the Figure 10 is as follows: U_0-charging voltage, R_1-Line resistance (including resistance of wire and inductance coil), R_S-The on resistance of the semiconductor switch MOSFET, L-Inductance.

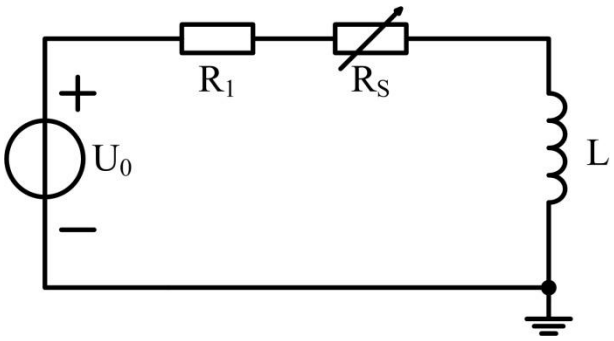


Figure 10 Charging equivalent circuit model of IES based on semiconductor switch

According to the principle of circuit analysis, it is assumed that the charging current is I, and the state of the circuit can be expressed in the following equation [2-3]. The charging current can be obtained by the equation [2-3]. $I = \frac{U_0}{R_1 + R_S}(1 - e^{-\frac{R_1+R_S}{L}t})$

$$U_0 = I(R_1 + R_S) + L\frac{dI}{dt} \quad [2\text{-}3]$$

From the calculation formula, the low circuit resistance is often needed to obtain high charge current. When the line resistance is low enough, the voltage on line resistance in equation [2-3] can be ignored. At this time, the rising rate of charging current is basically constant (U_0/L).

2.1.4 Discharge process of IES circuit based on semiconductor switch

After the MOSFET is disconnected, the energy storage inductor is discharged to the load. This process can be divided into two stages, as shown in Figure 11. This process is as follows. When the current of the energy storage inductor L is I, the MOSFET switch begins to open and it changes from a low resistance to the high resistance. This change obviously takes some time. During this period of time, the discharge process is shown in Figure 11 (a), and the energy storage inductor L discharges to the switch and the load. Then, the switch is completely off. At this time, because the leakage current of the switch is very small, it can be considered that the energy storage inductor L only discharges to the load, as shown in the Figure.11 (b). Because of the energy loss on the switch discharge, the current I* is smaller than the charging current I. The whole discharge time

is proportional to opening time of the switch and the time constant (L/R_{load}) of the inductor L discharge.

(a) (b)

Figure 11 Equivalent circuit diagram of discharge process using IES based on semiconductor switch (a) The switch is not completely turn off (b)The switch is completely turned off

2.2 A simple IES circuit experiment based on MOSFET switch

The experimental design of a simple inductive energy storage circuit based on MOSFET switch is designed to verify the theoretical discussion, and to further understand the advantages and disadvantages of the IES circuit. In order to extend the application to high voltage in the future, the opt-coupler isolation is used, and the power supply is isolated from the transformer, which is shown in Figure 12.

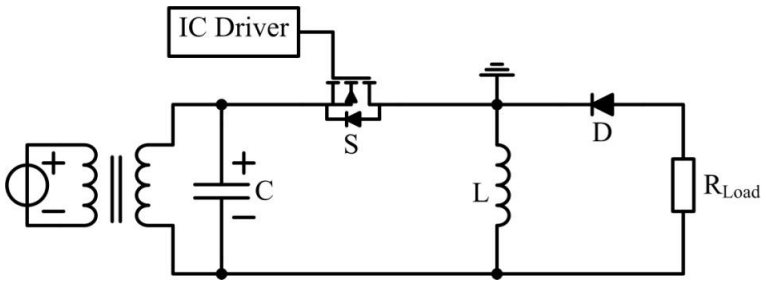


Figure 12 Schematic diagram of experimental circuit using IES based on MOSFET

The experimental design is as follows. The trigger control signal is the digital signal generator (GD535), and it can produce the control signal with 2 microseconds to control

the switch on. The charge uses a DC isolation converter, which converts the voltage from 5V into 12V to charge a 47μF capacitor C. Part of the components used in the experiment are shown in Table 2.

Table 2 Some components used in the experiment of simple IES base on MOSFET

Components	Manufacturer	Model	Main parameters
MOSFET	STMicroelectronics	STW23N85K5	V_{DSS}=850V I_{D25}=19A(DC) t_f=8ns
Driver Chip	Microchip	TC4429	V_{max}=20V I_{peak}=6A
Isolated DC-DC converter	TRACOPOWER	NMJ0515SAC	V_{OUT}=12V V_{IN}=5V P_{OUT}=10W Isolated Voltage=5kV
Opto-coupler	Avago Tech.	HCPL-0601	Isolated du/dt=15kV/μs High speed:10MBd
Murata	Chemicon	Murata RCE	50V,10 μF
Diode	STMicroelectronics	STTH310	V_{rev}=1kV I_{max}=3A(DC)
Inductor	/	/	1μH

According to the circuit shown in Figure 12, and the use of components in Table 2 to build a laboratory platform, the control switch is turned off after 2μs. When the load is 500 ohm pure resistance, the output voltage waveform and charging current waveform are shown in Figure 13.

From the experimental results, the advantage of inductive energy storage is voltage amplification. As the experiment did, when charge current is nearly 16A, the output of about 800V was obtained at a load 500 ohms, and the charge voltage was only 12V. The increase of the charge current is Linear on the inductance with 1μH is basically matching the theoretical deduction. According to Ohm's law, the peak output current is about 1.6A,

and it is less than 16A of the charging current. This phenomenon, as described in the previous theory, the current in the inductor partially discharges to the switch with the process of the switch opened.

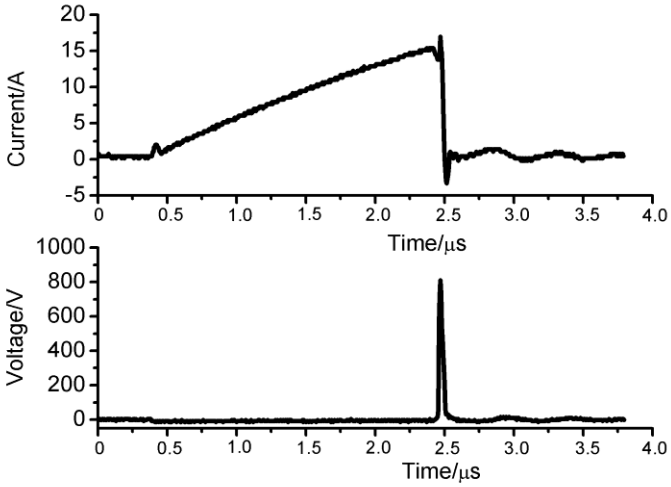
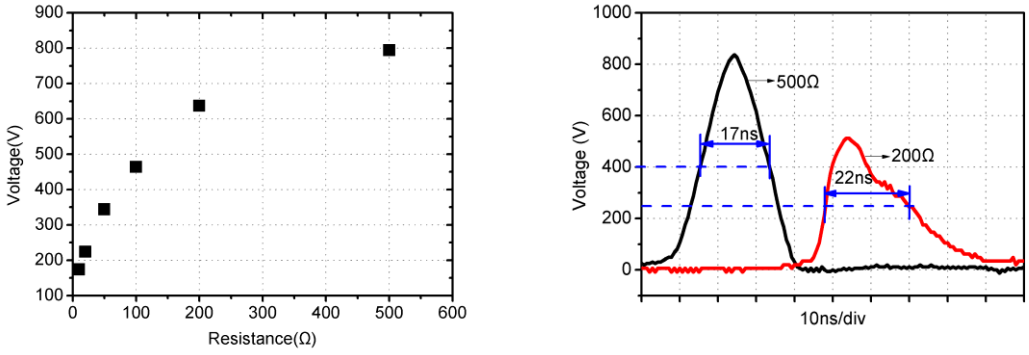


Figure 13 Charge current and output voltage waveform using simple IES based on MOSFET with 500Ω load



(a) (b)

Figure 14 Output voltage using simple IES based on MOSFET with different loads (a) Peak voltages (b) Voltage waveforms

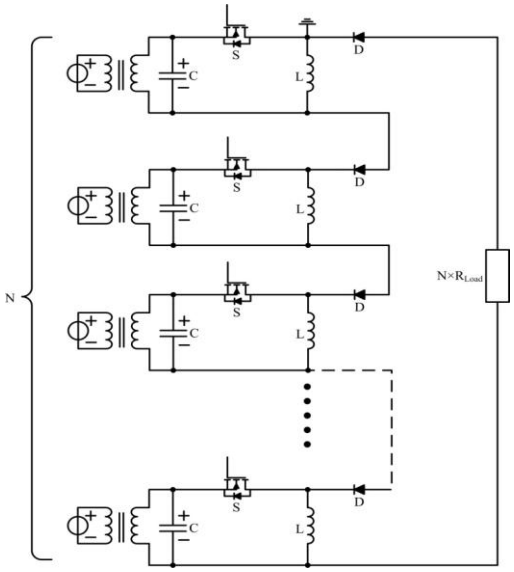
The relationship between the peak output voltages and the different loads can be obtained by maintaining the constant charging current and changing the load resistance, as shown

in Figure 14. As we can see from Figure 14 (a), the output voltage increases with the increase of load, but the nonlinearity increases. Compare the output voltage waveforms of different loads in Figure 14 (b). When the load is 200 ohms, the voltage fall part is close to the exponential waveform longer than 500 ohms, and the rise time of voltage is basically the same as the rise time of 500 ohms. This phenomenon indicates that the inductor discharge is divided into two parts, the first part is the phase of the output voltage rising, and its time is completely determined by the switch off speed. The latter part is the voltage drop stage, and its time is related to the time constant of the inductance discharge, and the lower the load resistance the longer the longer. This is matching with the inference in 2.1.4.

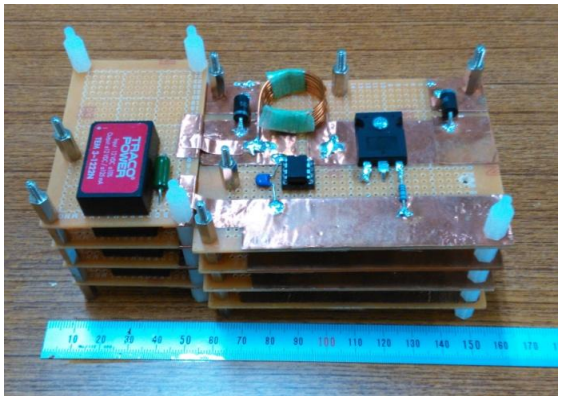
2.3 Voltage adder experiment using simple IES circuit based on MOSET

In order to obtain higher voltage output and short pulse, it is obviously impossible to increase the load resistance only. There are two reasons. On one hand, the peak voltage of switch is limited, for example, the peak voltage of MOSFET used in experiment is 850V, while the output voltage with 500 ohms is 800V, which is close to the limit value of switch. In order to obtain higher voltage output and short pulse, it is obviously impossible to increase the load resistance only. There are two reasons. On one hand, the peak voltage of switch is limited, for example, the peak voltage of MOSFET used in experiment is 850V, while the output voltage with 500 ohms is 800V, which is close to the limit of switch. On the other hand, from the results in Figure 14 (a), the increase rate of the voltage load is slowing down with the increase of load.

In order to obtain higher output voltage, the basic concept of Marx circuit is used for reference, and the inductor is connected in series in series. At the same time, the resistance of the load is increased with the inductor increasing, which ensures the discharge time constant as L/R_{load}. The schematic diagram and the physical diagram of the experimental circuit are shown in Figure 15.



(a)



(b)

Figure 15 Voltage adder using simple IES circuit based on MOSFET. (a) The circuit principle diagram (b) Physical diagram

In the experiment, we select 4 modules to stack in series, and the circuit of each module is the same as that used in the 2.2. The load resistance in the experiment increases from 500 ohms to 2000 ohms. The load resistance in the experiment increases from 500 ohms to 2 thousand ohms.

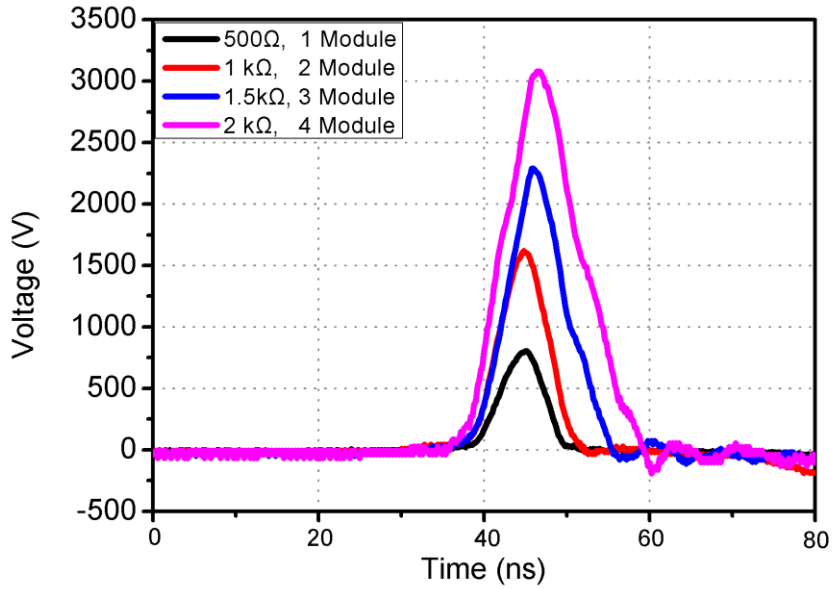


Figure 16 Output voltage waveforms of the voltage adder using simple IES circuit based on MOSFET.

From the results of Figure 16, the increase of the output voltage can be obtained by connecting the modules of the IES circuit in series connection. However, the peak value of the voltage is not multiplied by the number of modules. And the width of the pulse has a tendency to widen with the number of modules increasing, especially in the part of the voltage fall. Obviously, these shortcomings are caused by the simple using pure inductors. In the series, we wanted the total inductance to be multiplied with the number of modules. However, it must be noted that in the process of inductor series, several important details are ignored. First, in the process of series, the inductance of the loop is increasing. This

will lead to the tail of the voltage during the discharge process. What is more serious is the process of inductance in series, if the coupling between inductors as shown in Figure 17, the total value will lead to mutual inductance deviation from ideal multiplier. It is assumed that the inductance of the inductor is L, the coupling inductance is M, and the inductance in series is the same as that in Figure 17. The sum of the two inductors at this time is not 2L but 2 (L+M). Obviously, the total amount of the inductor deviates from the ideal value, so the time constant of the series of two modules is not L/R_{load}, but $(L+M)/R_{load}$. This causes the width of the discharge pulse to long.

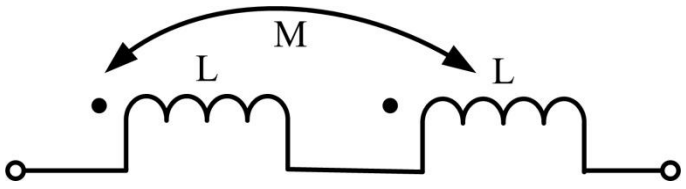


Figure 17 A schematic diagram of the coupling effect between inductors

2.4 Summary and discussion

In this chapter, the basic knowledge of inductive energy storage is introduced, and the working principle of the traditional inductive energy storage pulse power source is discussed in detail. On the basis of the study of traditional inductive energy storage pulse power technology, a simple inductive energy storage circuit based on MOSFET switch is designed. The advantages and defects of the inductive energy storage circuit with MOSFET are fully demonstrated by theoretical analysis and experimental analysis. Because of the limited power capacity of MOSFET, it is difficult to meet the application of high pressure in the future. Therefore, in the light of the traditional Marx circuit, we propose a voltage adder based on a simple inductive energy storage circuit. The

characteristics of the voltage adder are studied by experiments. The research work in this chapter can be summed up as the following.

- Through the experiment, we find that the simple inductive energy storage circuit uses MOSFET as an opening switch, which can simplify the traditional inductive energy storage circuit.

- Using MOSFET switches and inductive energy storage, we can get nanosecond short pulses, and get voltage gain easily. As we did in experiments, we can amplify the voltage of 12V to 800V.

- The disadvantage of inductive energy storage is that the load matching is difficult, and it is difficult to get a standard rectangular pulse.

- Although the accumulation of the module can further improve the voltage, the peak output voltage is not an ideal increase, and the pulse width is widened with the increase of the number of modules. It is obvious that the coupling between inductors cannot be ignored.

CHAPTER III: VOLTAHE ADDING OF IES PLUSE FORMING LINES [19][20]

In the chapter II, a simple inductive energy storage circuit is discussed. Its advantage is that the voltage gain can be obtained, but the output waveform is not ideal. In order to improve the output waveform, some new pulse forming circuits are discussed in this chapter. Both methods use inductive energy storage (IES) instead of traditional capacitive energy storage (CES), which means that the PFLs are charged by current instead of voltage. One of the methods (Type A) used an additional transmission-line-transformer (TLT) to achieve the output voltage adding from multiple PFLs, while the other method (Type B) combined the functions of PFL and TLT into one set of transmission lines.. Both methods have advantages and disadvantages over each other and both methods are believed to have certain significance in pulsed power generation.

3.1 Basic principle of IES pulse forming line (PFL) circuits

3.1.1 Symmetry geometric topology principle applied to IES circuit

The new circuit is not created by imagination, so the IES pulse forming line circuits are inspired by the traditional CES pulse forming lines and symmetry principle. From the analysis of the second chapter, we have already known that the energy storage density of a capacitor is $\varepsilon E^2/2$, and it is $\mu H^2/2$ with the IES. In other words, their mathematical expression of the energy storage density is same, if physical meaning is ignored. The propagation of electromagnetic waves should follow the Maxwell equation group [], as shown in [3-1]. It is not difficult to find that the electric field and the magnetic field are symmetric in the mathematical form from the equation group.

$$\begin{cases} \nabla \bullet E = 0 \\ \nabla \times E = -\mu \dfrac{\partial H}{\partial t} \\ \nabla \bullet H = 0 \\ \nabla \times H = \varepsilon \dfrac{\partial E}{\partial t} \end{cases} \qquad [3\text{-}1]$$

The essence of the pulse power source circuit is the storage and propagation of the electromagnetic energy. Therefore, we have reason to suspect that there is some symmetry in the geometric topology of the CES circuit and the IES circuit. It is not difficult to find that the node voltage equations of the CES circuit, as shown in Figure 2(a), which has the same mathematical form as the loop current equations of the IES circuit, as shown in Figure 2(b).Specific to the circuit topology as shown in Figure 18.

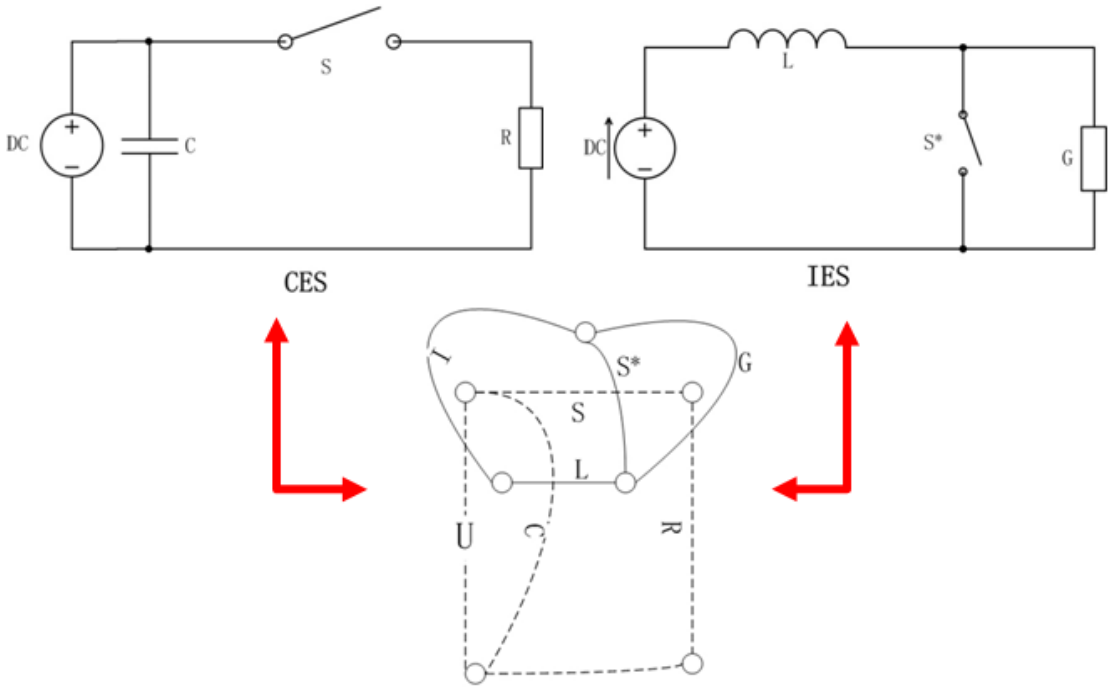


Figure 18 Symmetric geometric graphs of CES and IES

The components and branches in the CES circuit are expressed in the dotted line, and the voltage nodes in the circuit are expressed in the hollow circle, which is the dotted line diagram shown in Figure 18. Each loop in the dashed graph corresponds to a hollow circle, and the circles are connected by solid lines. As shown in Figure 18, a solid line diagram is obtained. This solid line diagram is the IES circuit corresponded from the CES. This corresponding relationship can be summed up as shown in Table 3.

Table 3 Symmetric relation table between the CES and IES

CES	**IES**
node	loop
series and parallel	parallel and series
capacitance (C)	inductance (L)
charge (q)	magnetic linkage (ψ)
impedance (Z)	admittance (Y)
voltage charging	current charging
current amplification	voltage amplification
switch (off-on)	switch (on-off)
open circuit	short circuit

This kind of relationship and method can be extended to other derivative circuits. As in Figure 19, if this method be applied to the magnetic pulse compression circuit (MPC), as everyone knows, the new IES circuit called electric pulse compression circuit (EPC) can be obtained. If the symmetric law is applied to the Marx circuit, the new IES circuit called XRAM circuit [21] can be obtained..

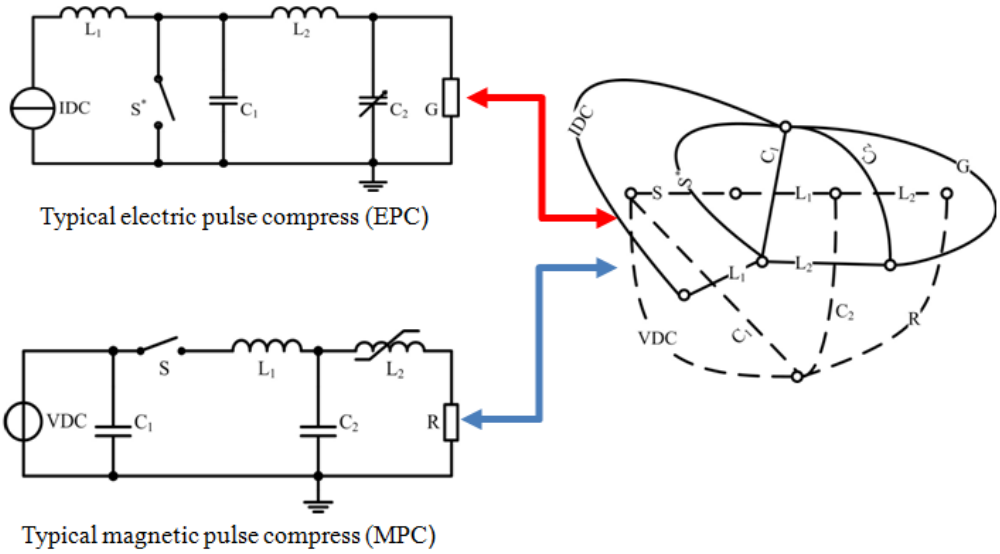


Figure 19 Typical electric pulse compress (EPC) from magnetic pulse compress (MPC) by symmetric principle

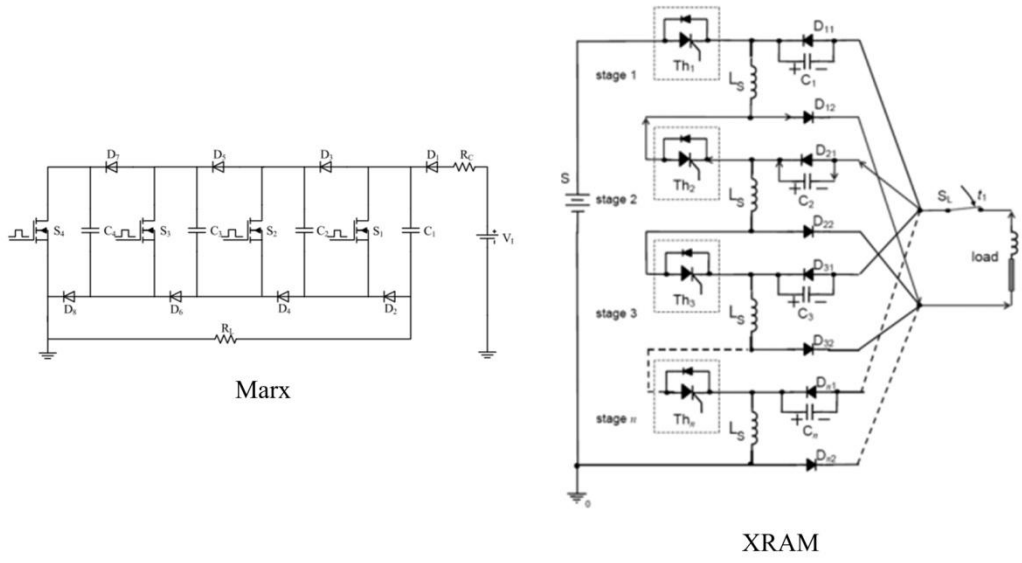
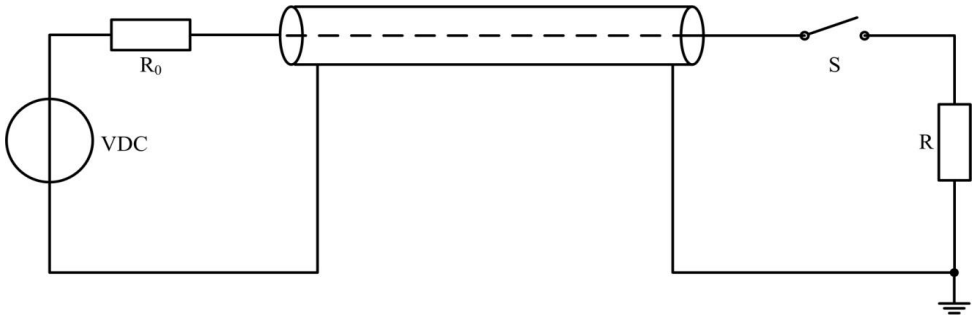


Figure 20 XRAM circuit[21] and Marx circuit

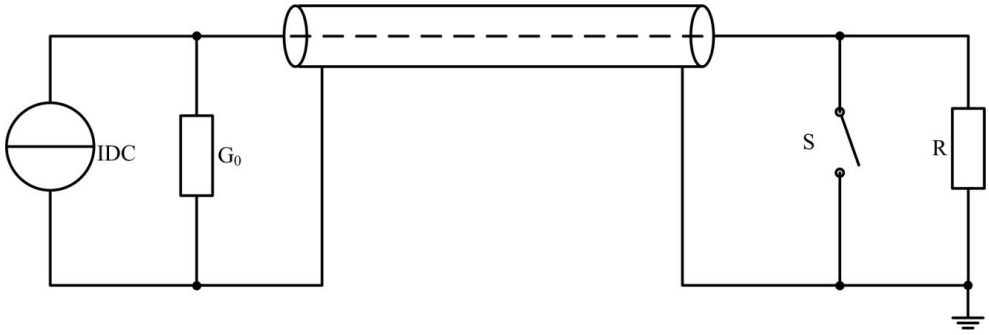
Figure 12 shows a typical Marx, and a XRAM circuit. It is well known that the Marx circuit topology is essentially "capacitor parallel charging and series discharge." Its functions are low voltage input and high voltage output. Using the symmetry law in Table 3, there is a new IES circuit whose topology is "series charging and parallel discharge", from the Marx, and its functions are low current input and high current output. The circuit topology and its characteristics derived from the symmetry law are confirmed in the paper [21] .

3.1.2 Traditional CES-PFL and Type A IES-PFL

In the chapter II, from discussion and experiment, we find that it is difficult to obtain a rectangular pulse, only using pure inductor, with the simple IES circuit. However, it is easier to obtain the rectangular pulse with the simple CES circuit, using pure capacitor. The main reason is that, in a CES circuit, the switch can be opened to cut the pulse tail, so that a rectangular wave can be obtained. While, in the IES circuit, when the switch is opened, the pulse is output, as well as, the switch loses control of the pulse. This means that the inductor is fully discharged, pulse tail forming an exponential wave. In the past, we can use a simple method to get the rectangular pulse, without the switch being opened to eliminate the tail of the pulse. The specific circuit is shown in Figure 21(a). A rectangular wave can be obtained by discharging a matching load with a fully charged transmission line. This circuit is called capacitance energy storage pulse forming line. Using the principle of symmetry, a new pulse forming circuit is obtained. It can be called Type A IES forming line. The energy storage element of the pulse forming line is the inductor inside the transmission line, and the control switch is an opening switch.



(a)



(b)

Figure 21 The schematic diagram of the traditional CES pulse forming line and the type A IES pulse forming line (a) Traditional CES pulse line (b)Type A IES pulse forming line

From the circuits of Figure 21, it is not difficult to find that the transmission line is the core device, so it is necessary to make a brief analysis of the transmission line to understand the characteristics of the pulse forming line. Assuming that the transmission line is ideal, it is considered that the transmission line is good conduction and the insulation performance of the dielectric is good, and the resistance and conductance of the lossy line are ignored. So the circuit in Figure 21 (a) can be equivalent to the transmission in Figure 22. It can be seen that the transmission line is made up of numerous small inductors and capacitors. Through the circuit analysis of the circuit in Figure 22, it is assumed that the unit's microelement (L and C) length is dx. The characte-

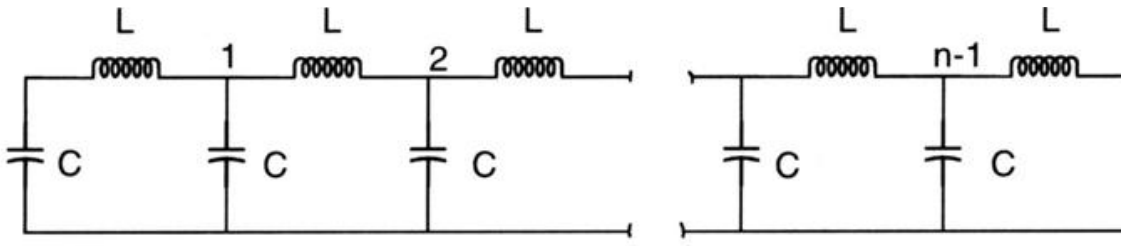


Figure 22 Equivalent circuit model of transmission line

-ristic equations of the micro inductors and capacitors and the two order partial differential equations of the voltage are listed: [3-2]. The meaning of the symbol in the equation is as follows. du-The voltage drop, between the output and input of the micro-element. di- The current drop, between the output and input of the micro- element. And the form of the solution of the two order partial differential equation in the equation is a function: u(x+vt) and u(x-vt).Its physical meaning is a set of electromagnetic waves with the opposite direction and equal amplitude.

$$\begin{cases} du = -L\dfrac{di}{dt}\bullet dx \\ di = -C\dfrac{du}{dt}\bullet dx \end{cases} \Rightarrow \frac{\partial^2 u}{\partial x^2} = \frac{1}{\sqrt{LC}}\frac{\partial^2 u}{\partial t^2} \qquad [3\text{-}2]$$

So, several important physical quantities can be obtained. They are the propagation speed of the wave v, the impedance of the wave Z, and the delay time (τ) of the transmission line using the line length with *l*, as shown in [3-3]

$$\begin{cases} v = \dfrac{1}{\sqrt{LC}} \\ Z = \sqrt{\dfrac{L}{C}} \\ \tau = l\sqrt{LC} \end{cases} \qquad [3\text{-}3]$$

When the impedance of the load is equal to the impedance of the transmission line, in other words, the impedance matching, the maximum power output can be obtained [2][3].The circuit shown in Figure 21 (a) assumes that the inside and outside radius of the coaxial transmission line is r_0 and r, while the maximum electric field intensity that the transmission line and switch can withstand is E, and the maximum voltage is U=E (r_0-r). Therefore, the output voltage U_{load}, Output pulse widthT, the output power P_C and the power density ω_C are as follows [3]. X=R/Z, Z=(ρ/2π)ln(r_0/r), T- Output pulse width

$$\begin{cases} U_{load} = \dfrac{UR}{R+Z} \\ P_C = \left(\dfrac{U}{R+Z}\right)^2 R = \dfrac{U^2}{Z}\left[\dfrac{X}{(1+X)^2}\right] \\ \omega_C = \dfrac{E^2}{\rho}\left[\dfrac{X}{(1+X)^2}\right] \\ T = 2\tau \end{cases} \qquad [3\text{-}4]$$

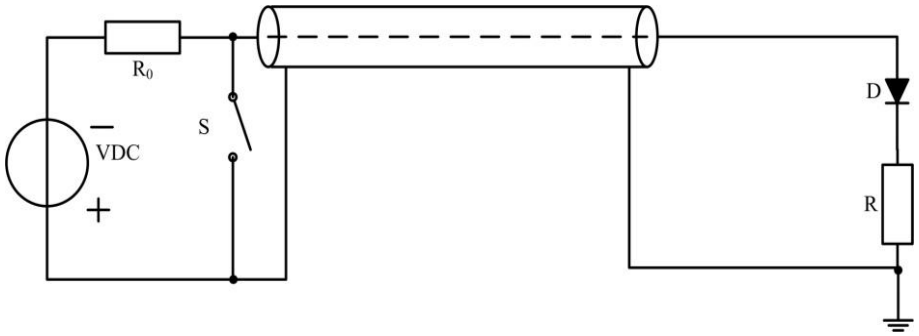
According to the symmetry rule, the output parameters of Figure 21 (b) can be obtained as follows. I-charging current, G=1/R, Y=1/Z, σ=1/ρ, T- Output pulse width

$$\begin{cases} I_{load} = \dfrac{IG}{G+\mathrm{Y}} = \dfrac{IZ}{Z+R}, U^*_{load} = R \times I_{load} = IZ\left[\dfrac{X}{(1+X)}\right] \\ P_L = \dfrac{I^2}{Y}\left[\dfrac{X^*}{(1+X^*)^2}\right] = I^2 Z\left[\dfrac{X}{(1+X)^2}\right] = \dfrac{\left(U^*_{load}\right)^2}{Z}\dfrac{1}{X} \\ \omega_L = \dfrac{H^2}{\sigma}\left[\dfrac{X^*}{(1+X^*)^2}\right] = \dfrac{\left(E^*\right)^2}{\rho}\dfrac{1}{X} \\ T = 2\tau \end{cases} \qquad [3\text{-}5]$$

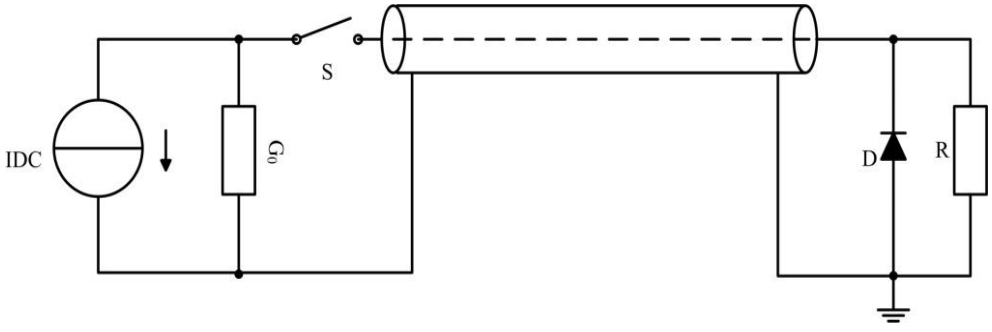
Under the condition of impedance matching(X=1), if the electric field intensity is the same (E=E*,U=U^*_{load}), the power (P_L) and power density (ω_L) of the IES pulse forming line can be 4 times of CES pulse forming line (P_L=4P_C, ω_L=4ω_C). Considering the same output pulse width, the energy density of the IES pulse forming line is higher than that of the CES pulse forming line with the same dielectric material in the transmission line.

3.1.3 Derived CES-PFL and Type B IES-PFL

There is a derivative circuit of such a CES pulse forming line, which is far away from the load, as shown in Figure 23 (a). According to the symmetry law, a new IES forming line circuit can be called type B IES pulse forming line, as shown in Figure 23 (b).



(a)



(b)

Figure 23 Circuit schematic diagram of derived CES pulse forming line and type B IES pulse forming line (a) Derived CES pulse forming line (b) Type B IES pulse forming line

For the analysis of circuit characteristics in Figure 23, we use the classical wave process analysis and the symmetry law. With the switch S just closed as the starting point, the circuit, in the Figure 23(a), can be divided into 4 stages. As shown in Figure 24, it is assumed that the initial charging voltage is U_0. The characteristic impedance of the transmission lines (AB) is Z. The one-way propagation time of transmission line is τ_0. In the case of load matching, we analyze the wave process in the transmission line.

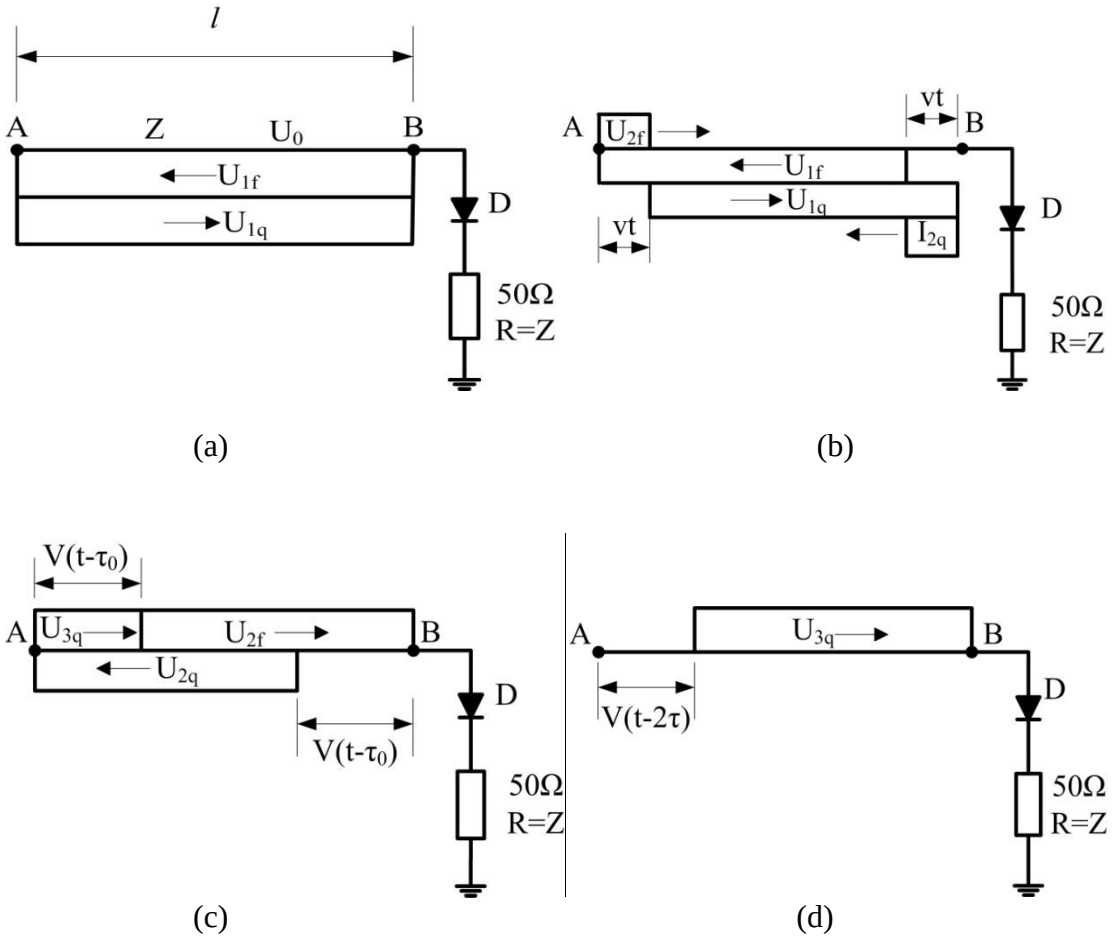


Figure 24 Wave propagation analysis of the Derived CES pulse forming line (a) t=0 (b) $0<t\leq\tau_0$ (c)$\tau_0<t\leq2\tau_0$ (d) $2\tau_0<t\leq3\tau_0$

The process is as follows:

1) When t=0,the switch S is not closed, The transmission line AB is charged to U_0. This voltage U_0 can be seen as two voltage wave composed with the opposite direction and same amplitude, as shown in Figure 24 (a).

2) When t=0, the main switch S is closed, and leading to the A point is short circuit. However, due to the diode reverse blocking, B point is open circuit. Therefore, the voltage wave U_{1f} in the A point emerges reflection wave U_{2f}, because the negative total reflection, this process continues to a τ_0 time. On the other hand, at the point of B, the voltage wave U_{1q} has a positive total reflection, emerges the reflection wave U_{2q}. When $0<t\leq\tau_0$, at the A and B points, the voltage has changed. During this period of time, A point voltage is 0.B point voltage is 0, because no current flows through. The specific process is shown in Figure 24 (b).

3) When $t=\tau_0$, at this time the U_{2f} reaches the B point. Because the load resistance and the transmission line impedance matching, then the voltage does not generate any reflection. When $\tau_0<t\leq2\tau_0$， the U_{2f} to the load discharge generates the voltage at the B point. $U_B=U_{2f}=U_0/2$. While, the wave head of the U_{2q} reaches the A point, and the negative total reflection occurs, bring about a reflection wave U_{3q} arise. The voltage of the A point is maintained as $U_A=0$. The specific process is shown in Figure 24(c).

4) When $t=2\tau_0$, the U_{2f} discharge is completed on the load R. At the same time, the wave head of the U_{3q} reaches the B point. Because of the resistance matching, there is no reflection. When $2\tau_0<t\leq3\tau_0$, at A point, the voltage is zero. However, at the B

point, the voltage will be maintained. $U_B = U_{3q} = U_0/2$. The specific process is shown in Figure 3 (d).

The following conclusion can be obtained from the analysis of the above wave process. For the circuit in Figure 23 (a), there are the following characteristics under the condition of load matching: The output voltage is half the charge voltage ($U_B = U_0/2$,). The output voltage pulse width is $2\tau_0$ ($\tau_0 < t < 3\tau_0$). The current flowing through the switch is U_0/Z. According to the symmetry law, the output characteristic parameters of the type B IES pulse forming line circuit can be obtained. The output current is half the charge voltage ($I_B = I_0/2$), so the output voltage is $ZI_0/2$. The output voltage pulse width also is $2\tau_0$ ($\tau_0 < t < 3\tau_0$). The voltage on the switch is I_0Z.

3.2 Experiment with IES pulse forming lines

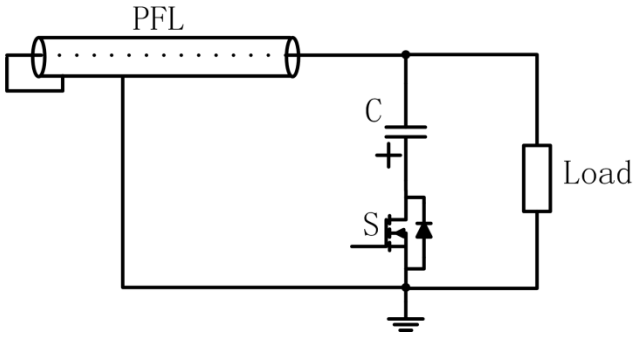
From the previous analysis, in contrast to CES where the energy is stored by applying a voltage between two conductors, IES is carried out by driving a current through them. For instance, in case of a transmission line, inductive energy can be stored by creating a current in the line and can be released by interrupting it. There are two kinds of IES forming line circuits called type A and B.

When the charging current is I_0.If we compare Type A with Type B, we see that, after opening, the switch has to withstand the voltage of $I_0Z/2$ for Type A and I_0Z for Type B. In other words, the maximum output voltage of Type B is only half as high as the voltage the switch can hold. However, the location of the switch for Type A is right next to the load while it is at the other end of the PFL for Type B, although a diode is required for

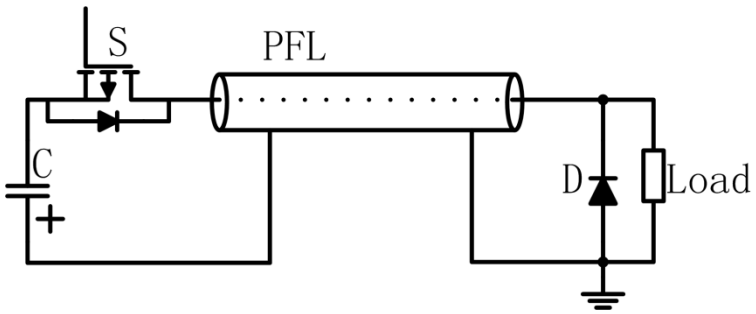
the latter case in order to carry the initial energy-storage current. In order to further verify the characteristics of the two circuits, some discharge experiments were designed.

3.2.1 Experiment plan

Figure 25 shows two examples of pulse forming line using inductive energy storage, both circuits consist of an initial energy storage capacitor, a switch (MOSFET), and a transmission line (PFL). In either case the inductive energy storage is done by switching on the MOSFET and letting the capacitors discharge through the transmission line. When the current reaches a certain value, the switch is turned off initiating a wave propagation process which is different between each other in two cases.



(a)



(b)

Figure 25 Circuit diagrams of two examples of pulse forming lines using inductive energy storage (IES-PFL) (a) Type A (b) Type B

Simple experiments have been carried out to demonstrate the behavior of the circuits shown in Figure 25. The main components used in the experiments are shown in Table 4. The control signals of the trigger switch are derived from the Field-Programmable Gate Array (FPGA). Specific programs and designs are displayed in the appendix.

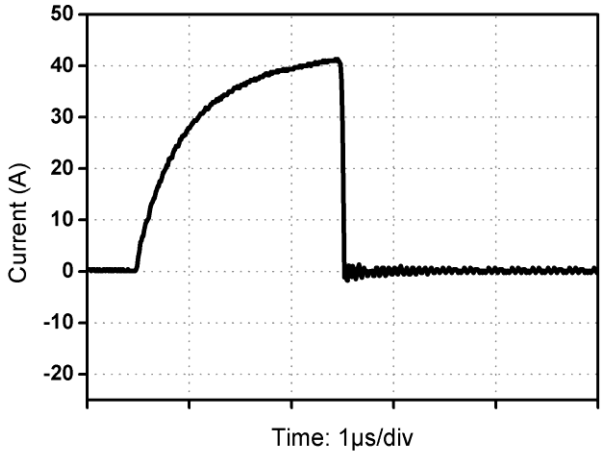
Table 4 Main components used in the experiments with IES pulse forming lines

Components	Manufacturer	Model	Main parameters
Coaxial cable	BELDEN	RG174/U	Z = 50 Ω *l* = 2m for Type A *l* = 4m for Type B
Switch (MOSFET)	IXYS	DE475-102N21A	V_{DSS}=1kV I_D=24A (DC)
Diode	CREE SiC	C4D20120A	V_{RRM}=1.2kV I_F=20A (DC)
Capacitor	Nichicon (Electrolytic)	UVK2A471MHD	100V, 470μF
	Chemicon (Ceramic)	KTD101B335M55A0T00	100V, 3.3μF

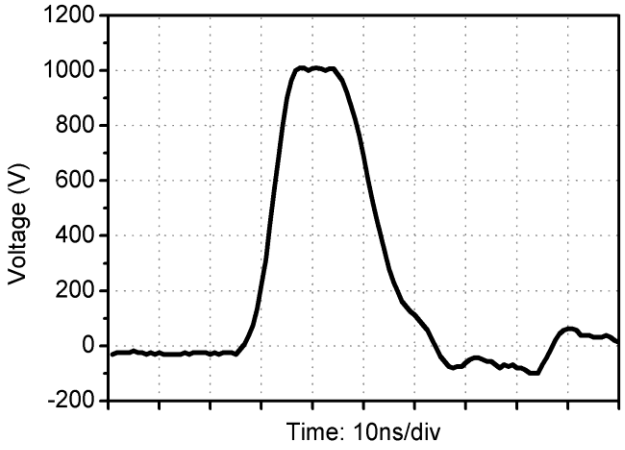
Z- Coaxial cable characteristic impedance; *l*- Coaxial cable length; V_{DSS}- Maximum drain-source voltage; I_D- Maximum drain current; V_{RRM}- Maximum repetitive peak reverse voltage; I_F- Maximum continuous forward current

3.2.2 Experimental results and discussions

For circuit Type A, the results are shown in Figure 26. A 2-m long coaxial cable was charged with a current of 40 A when the switch was turned off. Figure 26a shows the current waveform obtained at the left-hand side of the PFL with a current transformer (CT) and Figure 26b shows the voltage waveform across the 50-Ω load obtained with a voltage probe. As the current was cut off by the switch, an output pulse was generated by the PFL and delivered to the load. The amplitude of the peak output voltage reaches ~ 1 kV with a pulse width (full-width at half-maximum, FWHM) of ~ 20 ns. It is noted that the charging voltage of the capacitor was only 70 V.



(a)

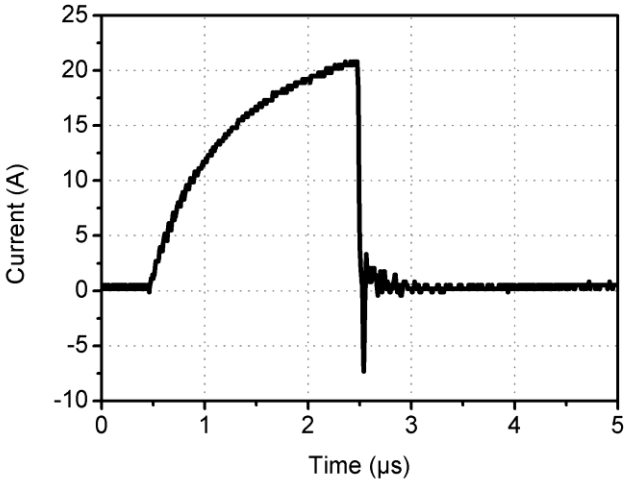


(b)

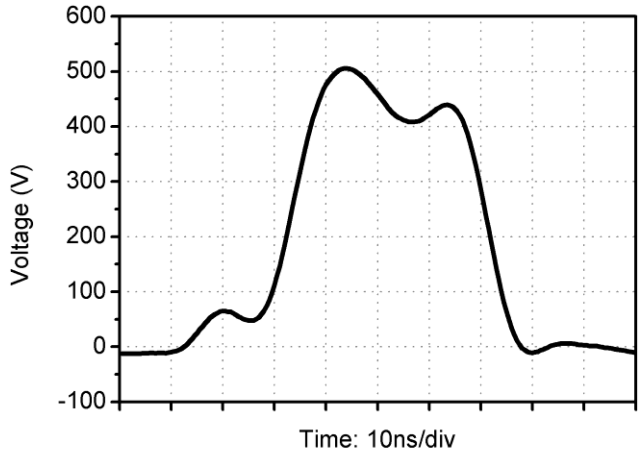
Figure 26 Waveforms of PFL current and load voltage (Type A). (a) Charging current (b) load vltage

For circuit Type B, the results are shown in Figure 3. A 4-m long coaxial cable was charged with a current of 20 A when the switch was turned off. Figure 3a shows the current waveform obtained between the switch and the PFL while Figure 3b shows the voltage waveform across the load. It is seen that, as the switch opened, the current was cut off. After about one transit time of the PFL, a voltage pulse appeared across the load.

The peak load voltage was ~ 500 V, although the voltage across the switch is expected to have reached ~ 1 kV. The capacitor charging voltage was 43 V.



(a)



(b)

Figure 27 Waveforms of PFL current and load voltage (Type B) (a) Charging current (b) load vltage

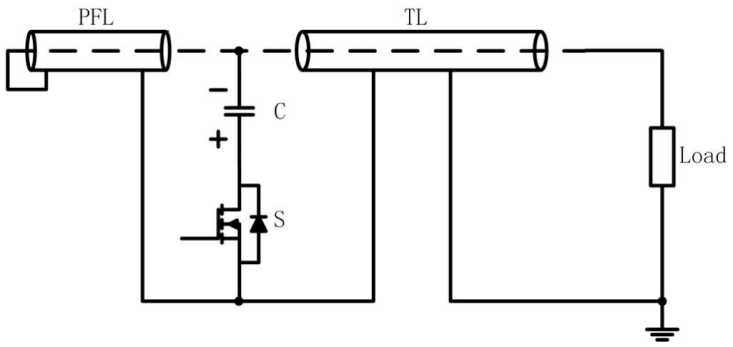
The experimental results shown in Figures 26 and 27 have demonstrated the IES-PFL behavior of circuits Type A and Type B, respectively. The pulse widths are generally consistent with the cable lengths, although the voltage rise-time is longer than that of the switching device. It is considered that the circuit stray capacitance and the diode (for Type B) have caused the lengthening of the rise-time.

3.4 Voltage Adding

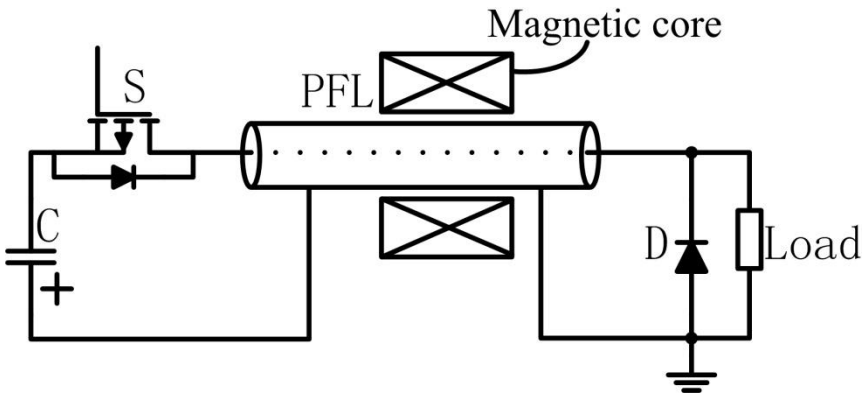
Voltage adding will become necessary if the application requires a higher voltage than that a single switching device can handle. In fact, the typical operation voltage of a semiconductor switch is on the order of kilovolt while most of the industrial applications of pulsed power require voltages higher than 10 kV.

3.4.1 Isolation mode of IES pulse forming lines

The key technology for multiple low-voltage modules to get high voltage output is to ensure voltage isolation between modules. For two kinds of IES pulse forming line voltage adder, different isolation methods are used, as shown in Figure 28 (a) (b). For the A type inductive energy storage circuit, a new transmission line TL is added on the basis of the original circuit. If the transmission line TL is long enough to make the delay time between the output and input pulse longer than the pulse width, when a voltage on the load, the voltage on the switch is basically zero. Because this way use a transmission line delay to isolate the input and output, which can be called time isolation. In this case, we take TL as 6m, the voltage waveform on the switch and on the load （50Ω）, as shown in Figure 29.



（a）



(b)

Figure 28 Schematic diagram of isolation for IES pulse forming lines (a) Time isolation for Type A IES-PFL (b) Magnetic core isolation for Type B IES-PFL

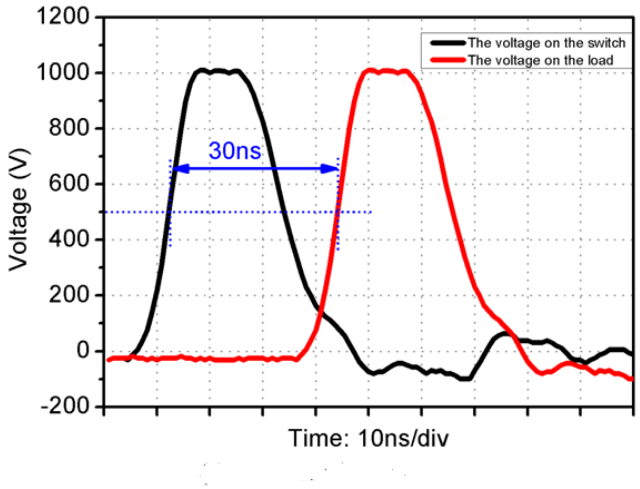


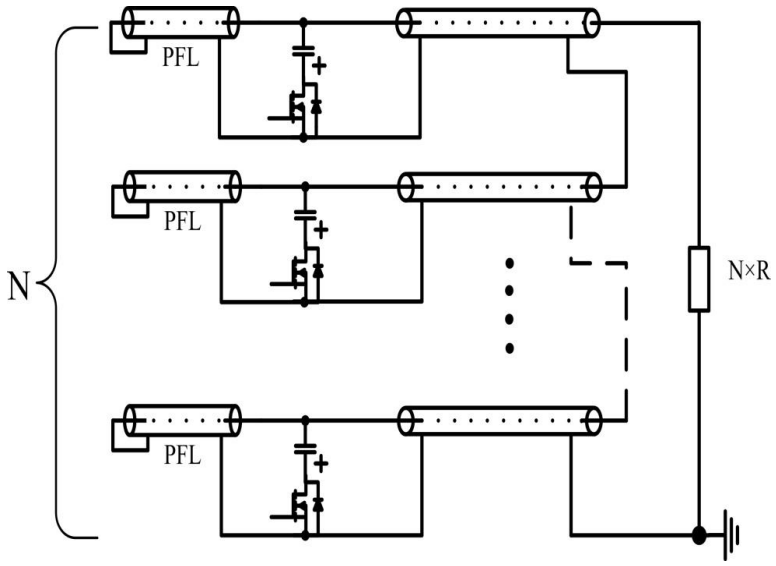
Figure 29 Experimental results of time isolation for Type A CES-PFL

For the circuit in Figure 28 (b), a core is added on the basis of the B type IES-PFL circuit, if core is large enough ($\int Bds > U_{out} \triangle t$),Voltage pulses give priority to load discharge, not on the switch side. B: Magnetic core saturation flux density. S: Magnetic core cross section area. U_{out}:Output voltage. Δt: Output pulse width

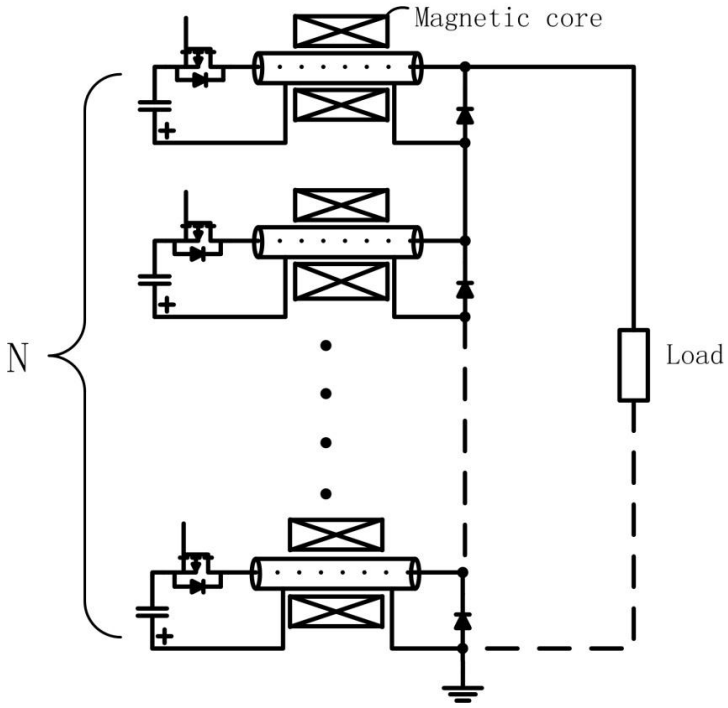
3.4.2 Experimental results and discussion of voltage adding

Figure 30(a) shows an example of voltage adding circuit, which combines the circuit Type A with a transmission-line-transformer (TLT), as we did in Figure 28(a). The TLT provides transit-time isolation between the primary circuits and the secondary circuit so that the primary circuits can be operated on the ground level. This is very important because otherwise the insulation requirements will largely increase the system complexity and limit its operation voltage. The magnetic cores can be omitted if the transmission lines are longer than the pulse length, although most developers prefer shorter lines isolated by magnetic cores which work just as well as longer lines without cores. These basic concepts are as we discussed in 3.4.1.

On the other hand, the voltage adding of the circuit Type B can be realized by simply stacking many of them together, as shown in Figure 30b. It is important that the left-hand side of the transmission lines are operated on the ground level. By comparing Figure 3b with Figure 3a, we can say that the transmission lines in the circuit of Figure 30b play the roles of both PFL and TLT. In other words, the circuit of Figure 30b combines two sets of transmission lines of Figure 30a into one set. However, for the circuit of Figure 30b, the magnetic cores are indispensable because the transmission lines cannot be longer than the pulse length.



（a）



(b)

Figure 30 Circuits for voltage adding based on IES-PFLs. (a) Type A and (b) Type B.

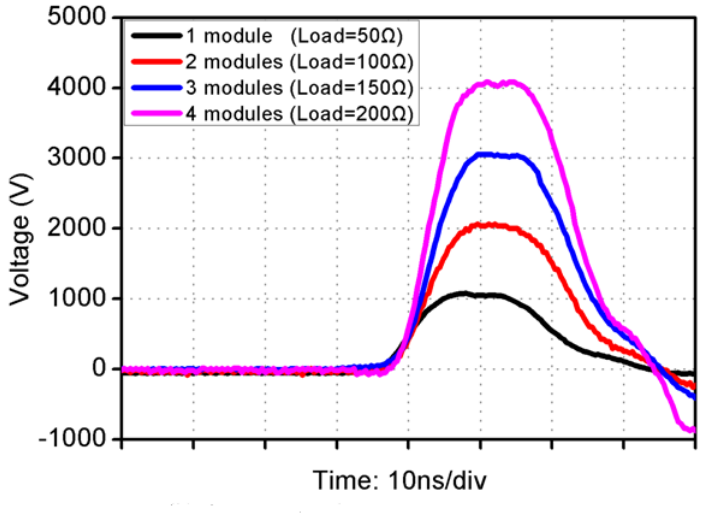
Voltage adding of multiple modules inevitably requires switching synchronization between them. It is therefore expected that the switching jitter be much smaller compared with the rise-time of the output pulse. In our case, for the rise-time on the order of 10 ns, we have confirmed that the MOSFET jitter is lower than 1 ns.

As initial demonstration experiments, simple circuits have been put together to prove the behavior of the circuits shown in Figure 30. For both circuit Type A and circuit Type B, four identical units as that described in Section II are stacked together, while same cables have been used for TLT of Figure 30a.

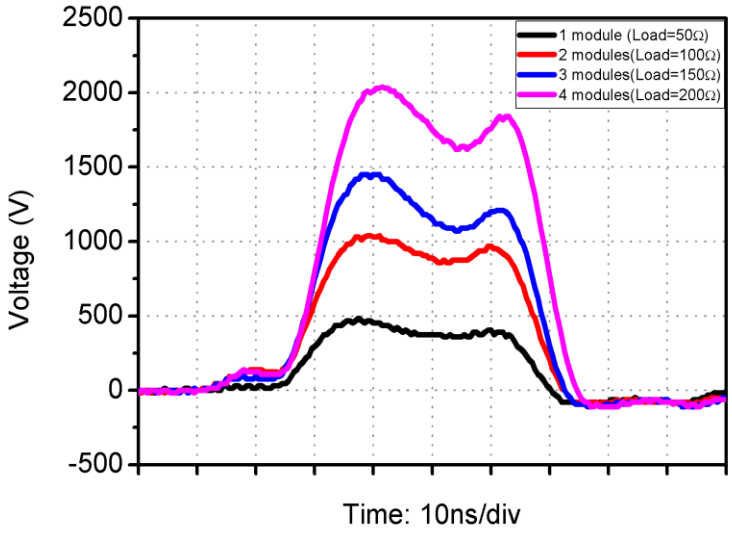
Figure 31 shows the experimental results, with 4 modules adding. The peak output voltage obtained across the load resistor increased nearly proportionally with the number of stages, reaching ~ 4 kV for Type A and ~ 2 kV for Type B. Although there exist some rise-time and oscillation problems, which are attributed to the stray parameters and load mismatch, we believe the results shown in Figure 31 have provided enough evidence that voltage adding can be carried out by using the methods shown in Figure 30.

In order to estimate the IES circuit efficiency, we have compared the output energy per pulse to the load with that stored in the PFL before the switch opened. The results are 86.5% for Type A and 90.7% for Type B, respectively. Detailed evaluations are to be carried out, whereas the omission of the second set of transmission lines, which plays the role of TLT for the circuit of Figure 4a, may have helped circuit Type B on improving energy efficiency. It is noted that the efficiency given above is only for that from PFL to the load, not including the loss caused during energy transfer from the initial capacitor to

the PFL. Figure 32 shows the physical diagram of the two IES-PFL 4 module voltage adder.

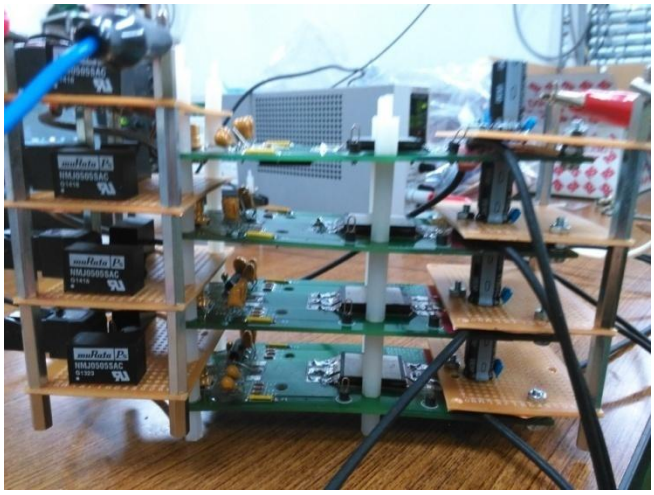


(a)

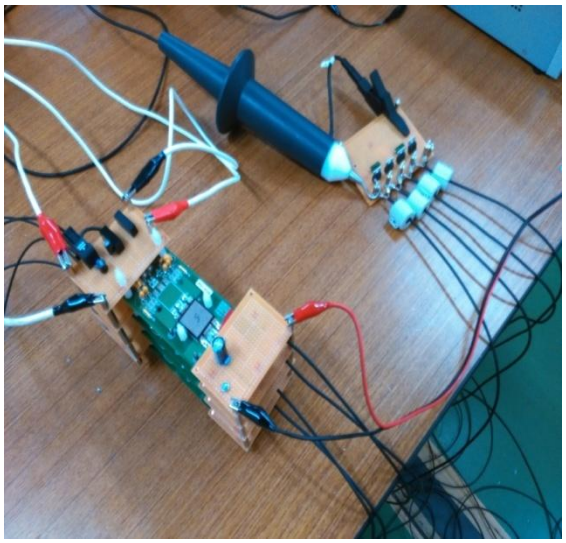


(b)

Figure 31 Waveforms of output voltage obtained with the circuits shown in Figure 30a Type A and Figure 30b Type B.(a) Figure 30a Type A (b) Figure 30b Type B



(a)



(b)

Figure 32 The physical diagram with 4 modules adding (a) Figure 30a Type A (b) Figure 30b Type B

3.5 Summary and discussions

In this chapter, two types (Type A and Type B) of circuits using pulse forming line (PFL) with inductive energy storage (IES) have been studied experimentally.

Circuit Type A places the opening switch next to the load so that the load can receive the same voltage rise and amplitude as the switch. However, when voltage adding is carried

out while placing all switches on the ground, an isolation circuit, such as a transmission line transformer (TLT), is required.

Circuit Type B places the switch on the opposite side of transmission line. As a result, the load receives the output voltage half as high as the switching voltage and after a delay of transit time. However, the voltage adding can be carried out straightforwardly by stacking the unit circuits together while keeping all switches on the ground. In circuit Type B, the transmission lines play the roles of both PFL and TLT.

Simple experiments have been carried out to demonstrate the behavior of both types of circuits, with voltage adding up to 4 stages. The results have proved circuit functions of both pulse-forming and voltage adding, although problems in rise-time and oscillation are to be solved.

The purpose of this study is to carry out the proof-of-principle experiment for IES-PFL. For simplicity, coaxial cables have been used as the transmission lines. It is expected that, for practical system design, strip lines will likely be used for geometric convenience and impedance flexibility.

The circuits presented in this paper have been designed following the concept of modularity. Therefore, the circuits are expected to be expandable by simply stacking many modules together, while keeping internal operation of each module unaffected. For series stacking, the final output current is the same as that of each module, which is determined by the PFL impedance and the current capacity of the switch. The output voltage, on the other hand, is proportional to the number of modules connected in series.

The limitation on the number of modules eventually comes from the insulation and coupling issues. The high-voltage output requires certain measures on breakdown prevention. At the same time, the structure design demands impedance continuation which may become a real challenge for the case of very high voltages.

Impedance matching is a key issue for the circuits described above. It may affect the rise-time, the pulse width, the peak power, and the efficiency that can be obtained at the load. However, for many real applications, especially those involve gas discharges, the load impedance is not always well defined and may be time-dependent. Therefore, it is necessary to keep in mind that the actual performance of any pulsed power generator based on these circuits will unavoidably depend on the load.

Finally, it is noted that IES has been widely used for pulsed power generation, although for most cases the storage elements were simple inductors. Compared with simple inductors, PFL operated in IES mode has the advantage in square-wave output. In addition, as we have proved in this paper, the PFL can play the role of isolation as those in TLT.

CHAPTER IV: PULSED VOLTAGE ADDER BASED ON INDUCTIVE BLUMLEIN LINES[20][22]

The coaxial cable using inductive energy storage can output the rectangle wave, which is not the same as the simple using pure inductor, which only output exponential wave. In the chapter III, a new pulse generator circuit using IES-PFL with single line is described. However, this technology still needs further development. On the one hand, the output current of the generator is only half of the charge current when single line is hired. On the other hand, as shown in Fig. 23(b), a diode is used in the inductive pulse forming line. It is worth noting that with this circuit, the main switch and the load are separated through the transmission line. The circuit can be output directly through series connection, to achieve a higher voltage, as shown in Fig.30(b) and 31(b).

However, the use of diode has also brought some problems. The ideal diode is expected, but not realistic. During charging of the transmission line, the diode is forward conduction. When the switch (S) is switched off, a short pulse is generated. This pulse is transmitted to the load through the transmission line and the diode must be switched off in reverse direction, which is expected. It is well known that diode reverse recovery takes time. Because diode reverse recovery time is not enough, this circuit structure is not suitable for short pulse generator, even with Schottky diode.

In this chaper, we discuss a developing circuit topology of inductive pulse forming line (IPFL) voltage adder based on inductive Blumlein line. The new circuit has been proposed and experimentally demonstrated. The circuit principle is explained based on the analogy with capacitively charged Blumlein lines. In the experiments, strip-lines have

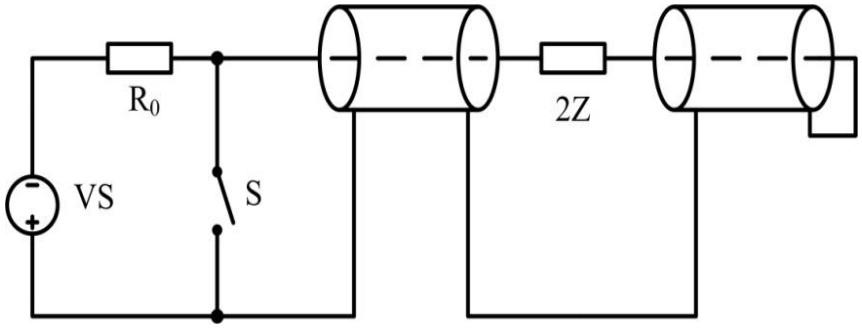
been used for inductive energy storage and SiC power devices have been used as the opening switches. The experimental results have proved both the circuit behavior and the voltage adding by using multi-module stack. This circuit method is expected to become a new approach to compact and repetitive pulsed power generation.

4.1 Inductive Blumlein line

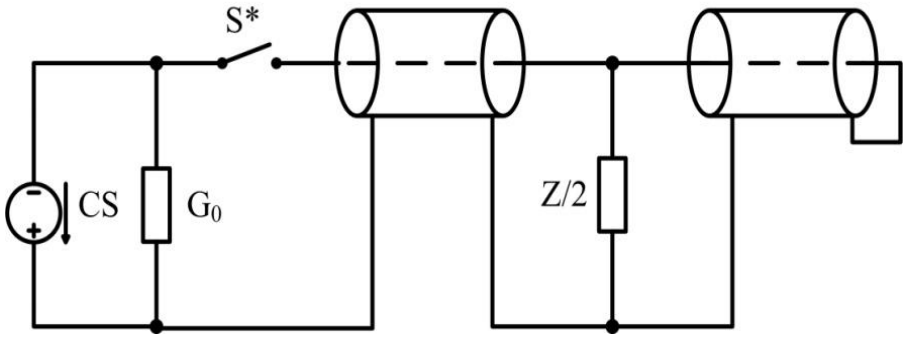
4.1.1 Basic principle

The schematic diagram of the inductive Blumein line circuit is shown in Figure 33 (b). Its circuit structure can also be obtained from the famous Blumein line circuit, as shown in Figure 33(a), by the symmetry law. For the Blumein line circuit, the voltage charge is used, the load and the transmission line are connected in series, and the end of the transmission line is open circuit. While, in the inductive Blumein line circuit, the current charge is used, transmission line and load in parallel and the end of the transmission line is short circuit. The output characteristics of Blumein line circuit are well known. Its output voltage is equal to the charge voltage in the transmission line, when the impedance of the load and the transmission line is matching. The matching resistance of the load is two times of the single transmission line impedance. The output pulse width is two times the time constant of the transmission line. The delay time between the output voltage and the voltage on the switch is same as the time constant of the transmission line. According to the law of symmetry, The output characteristics of the inductive Blumein line are as follows. Its output current is equal to the charge current in the transmission line, when the impedance of the load and the transmission line is matching. The matching resistance of the load is half of the single transmission line impedance. However, the time

characteristics are not change. Table 4 shows the characteristics of these two circuits in Figure 33. Table 5 shows the characteristics of these two circuits shown in Figure 33.



(a)



(b)

Figure 33 The circuit principle diagram of Blumein line and inductive Blumein line circuit (a) Blumein line (b) Inductive Blumein line

Table 5 Characteristic parameter table of Bumlein line and Inductive Bumlein line

Bumlein line	Inductive Bumlein line
Changing voltage U_0	Changing current I_0
Matching resistance R=2Z	Matching resistance R=Z/2
Output voltage $U_{load}=U_0$	Output current $I_{load}=I_0$
The current through the switch U_0/Z	The current on the switch I_0Z
Output pulse width $2\tau=2l/(LC)^{1/2}$	Output pulse width $2\tau=2l/(LC)^{1/2}$
Output delay $\tau= l/(LC)^{1/2}$	Output delay $\tau= l/(LC)^{1/2}$

Z- Impedance of transmission line. L- Transmission line inductance. C-Transmission line capacitance

4.1.2 Principle experiment

A simple discharge experiment was designed to verify the inference in 4.1.1 and to show the characteristics of the IES pulse forming line. The experimental scheme is shown in Figure 34. The experiment uses a 2 m long coaxial cable as a transmission line. The MOSFET switch is the DE475-102N21A produced by IXYS. A capacitor charged with is used to replace the constant current source in Figure 33. In order to achieve the load matching condition, the load is selected to be 25 Ohm.

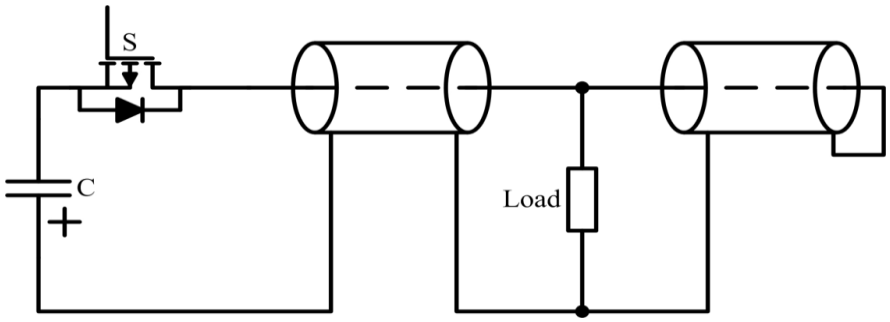


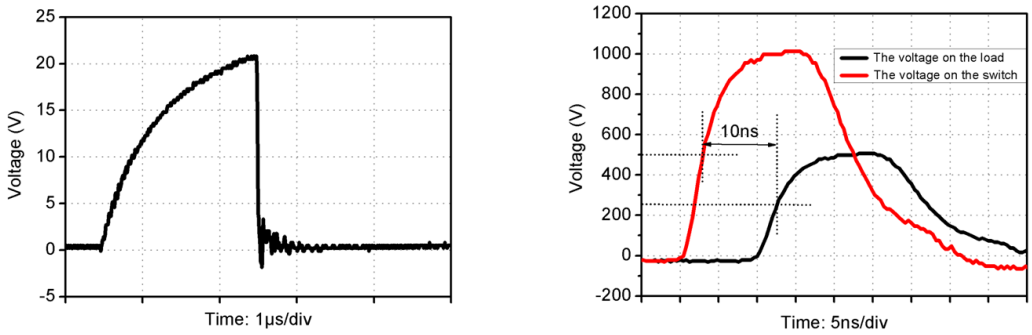
Figure 34 Experimental circuit diagram of inductive Blumlein line

Table 6 Main components used in the inductive Blumlein line discharge experiments

Components	Manufacturer	Model	Main parameters
Coaxial cable	BELDEN	RG174/U	Z = 50 Ω, *l* = 2m
Switch (MOSFET)	IXYS	DE475-102N21A	V_{DSS}=1kV I_D=24A (DC)
Diver IC	CREE SiC	IXRFD630	V_{Typ}=15 V, I_{Typ}=28 A
Capacitor	Nichicon (Electrolytic)	UVK2A471MHD	100V, 470μF
	Chemicon (Ceramic)	KTD101B335M55A0T00	100V, 3.3μF

With the load resistance is 25 Ω, the 26 V constant voltage is used to charge the inductor in the transmission line. The charging time is 2 μs, when the current rises to about 20A, as shown in Figure 35(a). At the same time, the control switch is opened, and the voltage

waveform on the load and switch is shown as shown in Figure 35(b). It is not difficult to find out from Figure 35 that when the charging current is around 20 A, the voltage on the matched load 25Ω is about 500V (Figure 35 (b) black curve). This proves that the IES Blumlein line is used and the output current is equal to the charge current. The output voltage is half of the voltage on the switch, and the output voltage has a delay of 10 ns relative to the voltage on the switch. The half pulse width of the output voltage is 20 ns. The experimental results are in agreement with the theoretical analysis in 4.1.1.



(a) (b)

Figure 35 Experimental results of inductive Blumlein line circuit discharge

4.2 Inductive Blumlein line module based on solid strip line and silicon carbide(SiC) MOSFET

In the chapter III, the shortcoming of the pulse forming circuits, which are discussed, is that the output current is only half the charge current. In order to improve this shortcoming, we discussed the inductance energy storage circuit in 4.1. Its output current is basically the same as the charging current. It can be seen from the experimental results and theoretical analysis. However, there is also a small limitation, even though they have many advantages. For example, in the market, the impedance of the coaxial cable is often

set. In other words, we can only get 50 ohm or 75 ohm transmission line, form the commercial market. What is more serious is that the size of the traditional pulse generator cannot be further compressed, with insulating material using low dielectric constant. This is a fundamental constraint. In order to further compress the volume of the generator, the transmission line composed with high dielectric constant insulation material is expected. But that brings a problem. The transmission line with high permittivity means the impedance is low. In other words, the output current will increase. A fast switch which can withstand large current is very important. The SiC switch is obviously more appropriate than the silicon switch, because its switching speed and current carrying capacity are better [24].Now SiC MOSFET and high dielectric constant banded lines are employed to make a more compact new pulse power square wave generator module using inductive Blumlein line.

The generator module consists of three parts, the energy storage transmission line, the function generator, and the switch module.

4.2.1 Solid-state stripline

In this case, the classic parallel plate transmission line is employed. The geometric structure of a strip line is shown in Figure 36. The gray part is a conductor. The yellow part is dielectric material. The length of the transmission line is about 1 meter. The width (W) of a conductor is approximately 16mm. The distance (d) between conductors is approximately 2mm. The insulating material is made of polyvinyl chloride board. In order to simplify the calculation, the edge effect is neglected. The classical formula [4-

1][4-2][4-3] is used to obtain the impedance, unit time length and per-meter inductance of the transmission line.

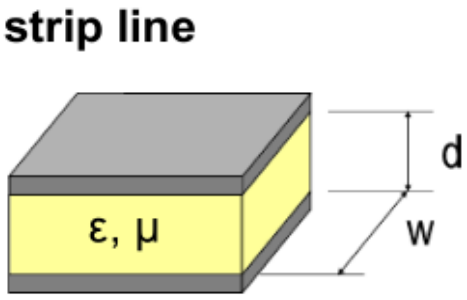


Figure 36 A schematic diagram of the geometric structure of a strip line

$$Z = (\mu_r \mu_0 / \varepsilon_r \varepsilon_0)^{1/2} (d / w) \quad [4\text{-}1]$$

$$\tau = \sqrt{\mu_r \mu_0 \varepsilon_r \varepsilon_0} \quad [4\text{-}2]$$

$$L_{per} = \mu_r \mu_0 d / w \quad [4\text{-}3]$$

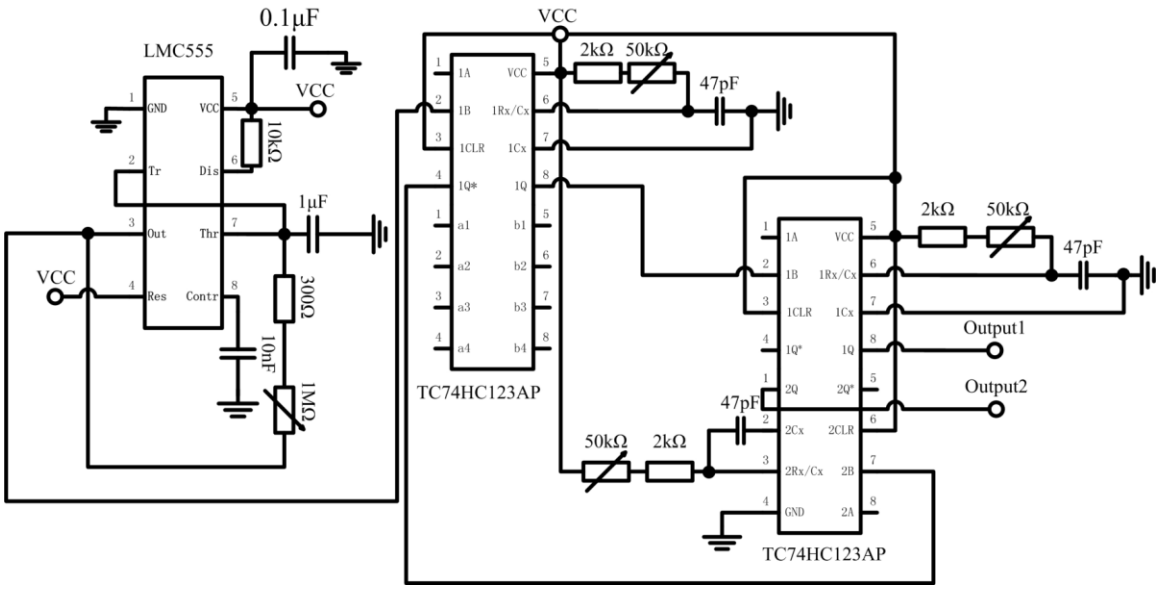
The theoretical parameters of the transmission line are shown in table I.

Table 7 Tansmission line parameters using solid state strip line

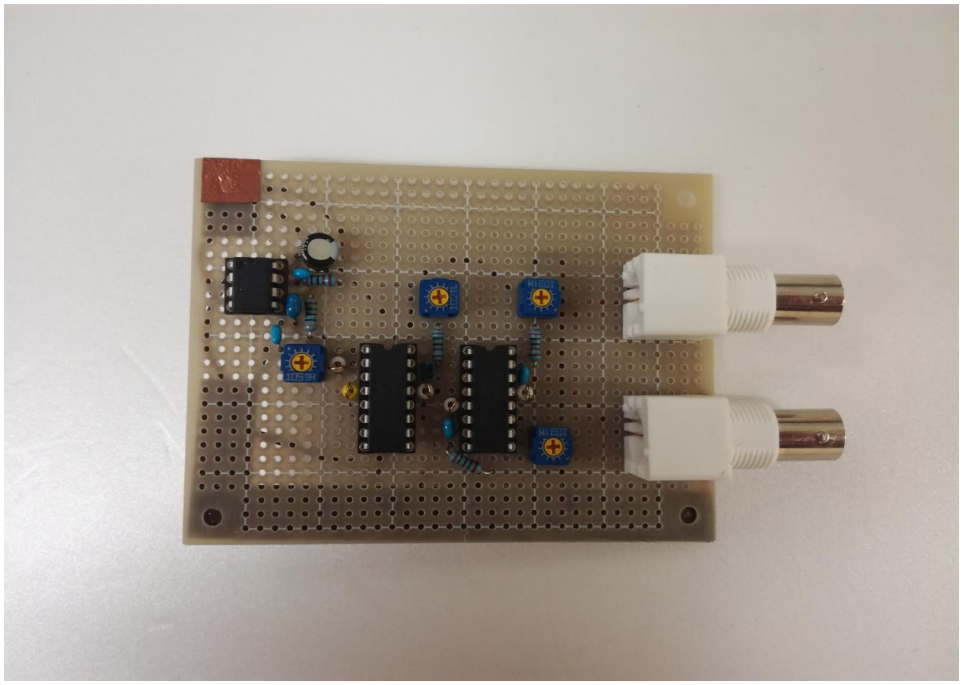
Geometry of Solid-State Strip-Line	Length	1 m
	Width	16 mm
	Thickness	2 mm
Relative Permittivity	4.0	
Characteristic Impedance (Z)	25.9 Ω	
Transit Time (τ)	6.7 ns	

4.2.2 Function generator

The main function of the function generator is the "high level" of a digital logic whose amplitude is 5V, the pulse width can be adjusted and the frequency is adjustable, for the switch driver IC. The schematic diagram of the specific circuit is shown in Figure 37.



（a）



(b)

Figure 37 Circuit schematic and physical diagram of a function generator（a）Circuit schematic diagram（b）physical diagram

Its basic design idea is to produce a self oscillating square wave heavy frequency signal through a 555 timer, which is the output frequency of the function generator. Adjusting

the resistance of 1M ohm in Figure 37a, the frequency of the output of the generator can be adjusted. And the monostable flip-flop, TC74H123AP, controls the output of the pulse width by adjusting the 50kΩ resistance, as shown in Fig.37(b). The main design output parameters of the function generator are shown in Table 8.

Table 8 Design parameters of function generator

Number of output	Output voltage	Frequency	Delay between the output ports	Output pulse width
2	5V	≦25kHZ	0-2.5μs	0-2.5μs

4.2.3 Silicon carbide MOSFET switch module

The opening switch is the key component. As with all inductive energy storage circuits, the ideal opening switch often requires a low on resistance and a fast turn off time. In the semiconductor switch, MOSFET switch has advantages in switching speed. For a long time, the on resistance of silicon MOSFET is a disadvantage, especially in the case of the high current. The on resistance of wide bandgap semiconductor device is lower than traditional silicon devices. The SiC MOSFET, manufactured by CREE Inc., is selected as the opening switch with comprehensive consideration. In order to optimize the characteristics of SiC MOSFET, drive chip requires strong drive capability. Therefore, the driver chip IXRFD631 which can provide 30A high current is selected. The main components and parameters of the switch module are shown in Table 9.Figure 38 is the circuit schematic diagram of the switching module. Optical fiber is used, so that the control signal and the main switch are isolated, reducing interference, and increasing the system reliability. The SiC MOSFET switch is driven by driving the IC: IXRFD630,

which is composed of MOS tube complementary circuit. It can provide 30A instantaneous current, to ensure the rapid opened of the SiC MOSFET. The isolated DC (VCC) provides the 15V voltage to drive the SiC MOSFET.

Table 9 Major components of the switch and driver

Components	Manufacturer	Model	Main parameters
SiC MOSFET	CREE	C3M0065090J	V_{DSS}=900V I_{D25}=35A(DC) $R_{DS(on)}$=65mΩ t_f=6ns(R_G=2.5Ω)
Driver Chip	IXYS	IXRFD630	V_{max}=30V I_{peak}=30A
Ceramic capacitance	Chemicon	/	10μF,100nF,10nF, 1nF
Optical Module	Hitachi	DR9300	DC ~ 50 Mb/s
Isolated DC	muRata	NMJ0515SAC	V_{OUT}=15V V_{IN}=5V P_{OUT}=1W

V_{DSS} – Drain-Source Breakdown Voltage, I_{D25}- Continuous Drain Current with Junction Temperature at 250C, R_{DS}(on) – Drain-Source On-State Resistance; t_f-Fall Time of the SiC MOSFET, V_{peak} – Breakdown Voltage of Driver Chip, I_{peak} - Transient Peak Current of Driver Chip.

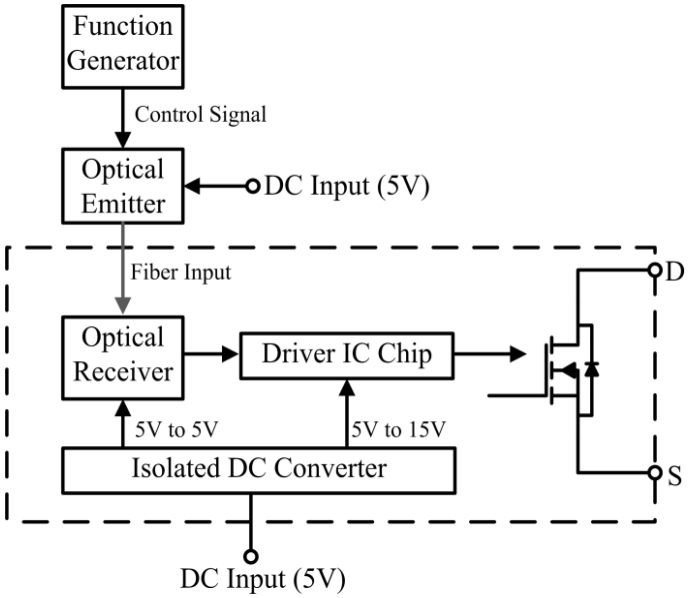


Figure 38 Circuit diagram for the control of MOSFET

Typical input control signal and gate signal for silicon carbide switch are shown in figure 39. A control signal with a pulse width about 2μs and a amplitude about 5V is input into the drive IC through the optical fiber. The control signal is amplified by driving the integrated circuit to about 15V and input to the gate of the SiC MOSFET. There is a small overshoot in the rising section of the gate pulse signal, and the stray inductance in the connection may be the main cause. The signal pulse shows no obvious oscillation in the falling section, as shown in Figure 39, which indicates that the SiC MOSFET switch can be switched off effectively.

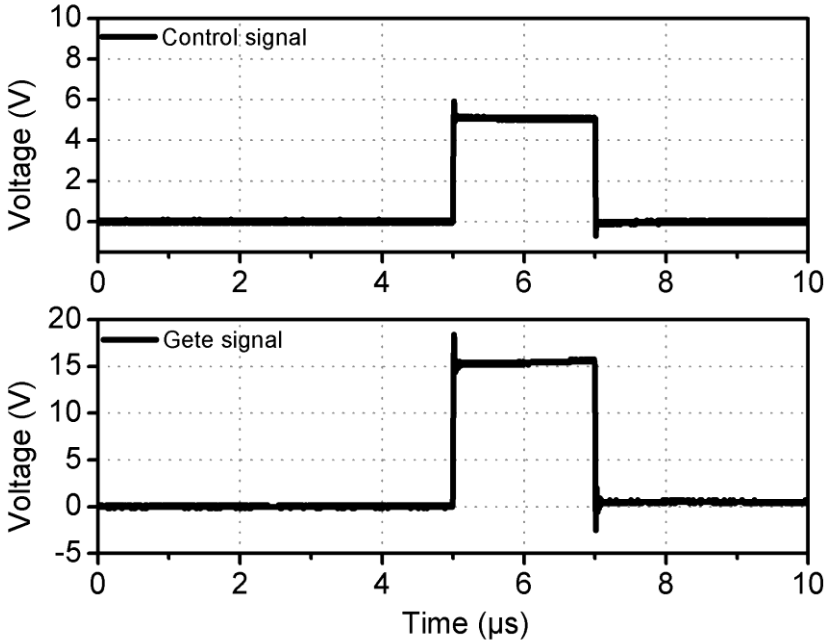


Figure 39 SiC MOSFET Switch Modular input control signal and gate signal test waveform

4.2.4 Experimental results of single module discharge using IES Blumlein line

Experiments have been carried out in order to verify the pulse generation by the circuit of Fig. 40 as described above. In the experiments, the voltage is probed by using LeCroy PPE6kV and the current is measured by using PEM CWT/6BMini. The waveforms are

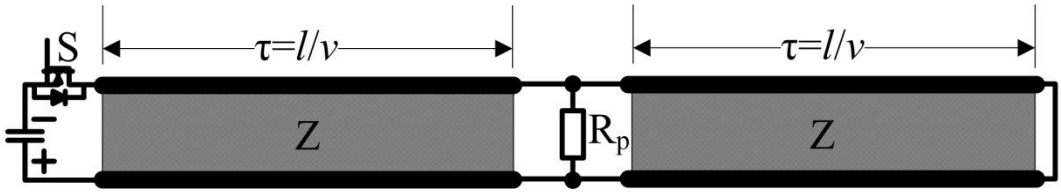


Figure 40 Schematic diagram of single module circuit using IES Blumlein line

recorded by using digital oscilloscope LeCroy WaveJet 324A. Figure 4 shows the typical waveform of the charging current. A capacitor of 200 μF has been used as the initial energy storage, which is charged to a DC voltage of 26V. When the switch is turned on, the current starts to rise resulting in inductive energy storage in both transmission lines. It is seen in Fig. 41 that the current reached ~ 40 A in about 2μs before the switch is suddenly turned off.

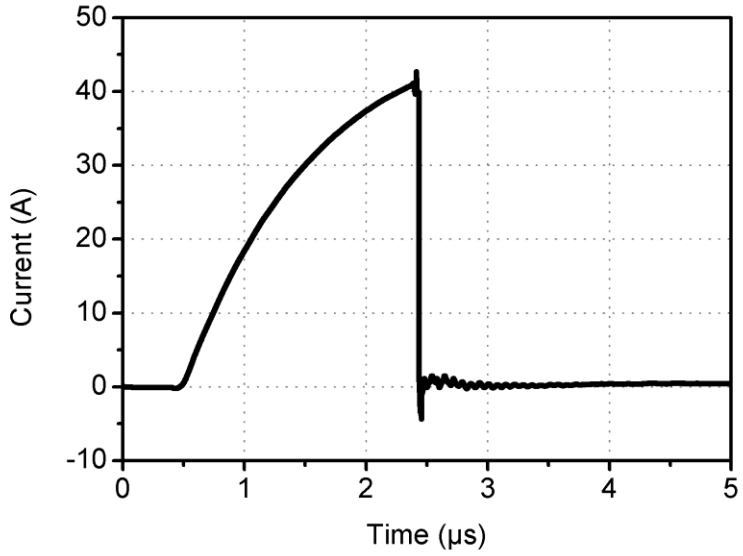


Figure 41 The waveform of MOSFET current, obtained with capacitor charging voltage of 26 V.

Figure 42 shows the waveform of the output voltage obtained on the 12.5Ω load. It is seen that the peak voltage reached ~ 450 V, corresponding to a load current of ~ 36 A, with a full-width at half-maximum of ~ 13 ns. It is noted that the waveform shown in Fig.

42 is far from an ideal square-wave pulse. The limited rise- and fall-times are caused by the switching device and the stray inductance of the circuit. However, this result has suitably proved the expected output of an inductive Blumlein line as described in the last section.

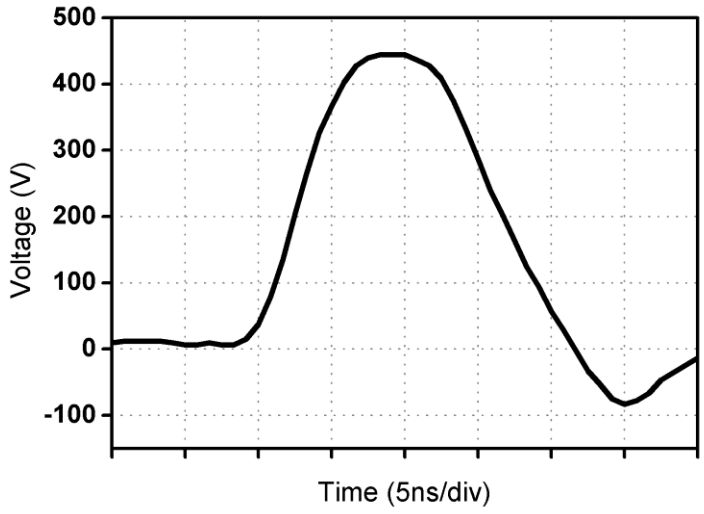


Figure 42 The waveform of output voltage, obtained on the 12.5 Ω load.

4.3 Inductive Blumlein line voltage adder

The next goal of this development is to obtain voltage adding by stacking multiple circuits of inductive Blumlein lines, as illustrated in Fig. 43. In principle, we can stack many circuits (modules) of that shown in Fig. 40. When all switches are turned on, a common voltage source can drive an IES current through all the modules because they are effectively connected in series. When all switches are turned off simultaneously, the behavior of each module should be exactly as described above and the output voltage should add up across the load, given that it matches with the stack.

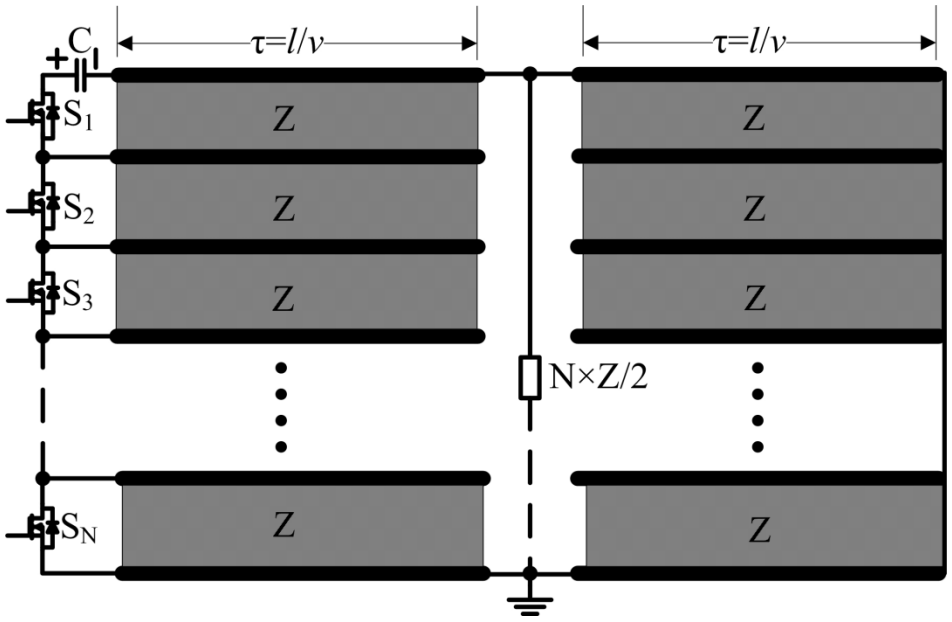


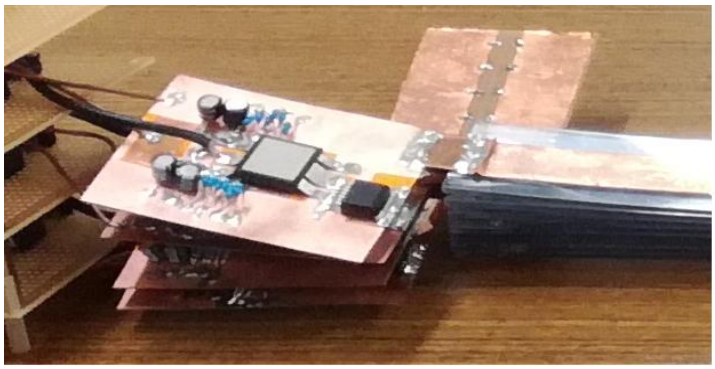
Figure 43 Circuit diagram of voltage adder using inductive Blumlein lines.

A simple proof-of-principle experiment has been carried out. Four identical modules of inductive Blumlein lines have been stacked together as shown in Fig. 43. A capacitor of 200μF was charged to 107V before all MOSFETs were switched on. It raises the current to ~ 40 A when the switches are turned off.

Figure 44 shows the photograph of the 4-stage stacked inductive Blemlein lines. The transmission lines on the right-hand side of the load, as seen in Fig. 43, are located under those on the left-hand side. So, a total of eight 1-m long strip-lines are stacked on top of each other and the load is seen on the right-side end in the picture.

Figure 8 compares the output voltage waveforms obtained with different numbers of modules. The load resistance is also varied in order to approximately match with the lines. It is seen that the peak output voltage is almost proportional to the number of modules.

(a)



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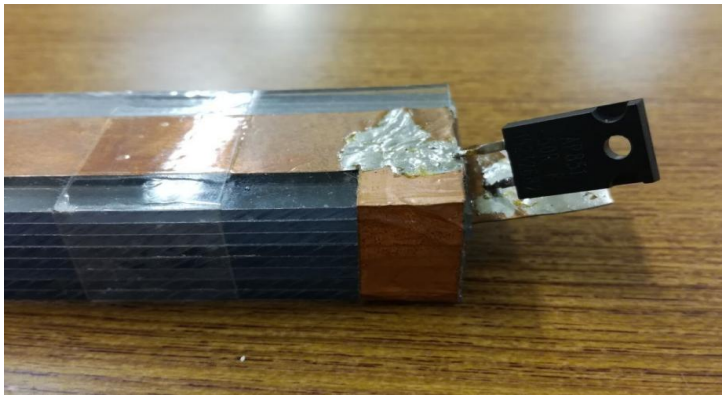

(c)

Figure 44 Photograph of a voltage adder using inductive Blumlein line using 4 modules. (a) Overall diagram of the device (b) Switch connection diagram (c) Load connection diagram

As in the last section, the results shown in Fig. 45 have at least proved the voltage adding

that we have obtained by using stacked inductive Blumlein lines.

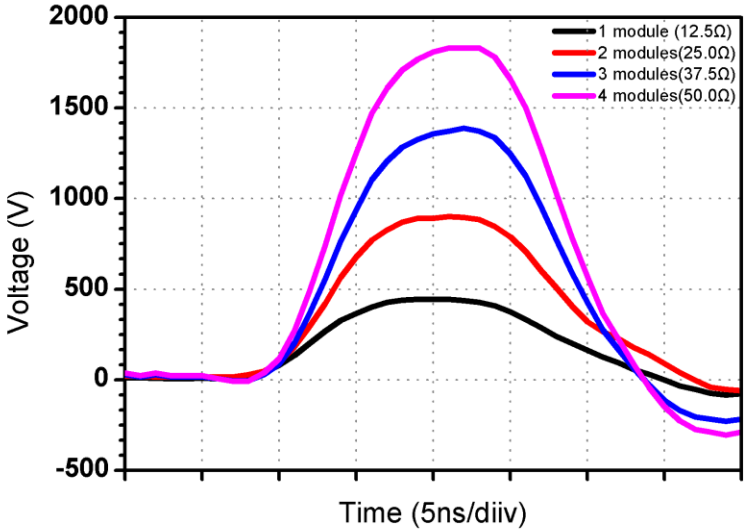

Figure 45 The waveforms of output voltage obtained with different numbers of modules and different load resistances using IES Blumlein line

Another interesting phenomenon is when the load connection is shown in the circuit in Figure 46. At this point, the device runs in a single line mode and the output voltage is negative, as shown in Figure 47. The pulse width is two times the pulse in Figure 45

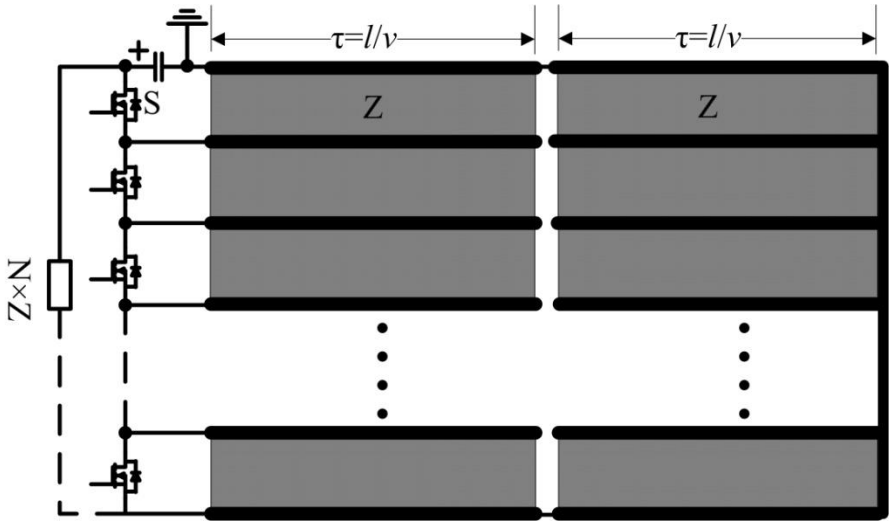

Figure 46 Circuit diagram of voltage adder using IES-PFL with single line

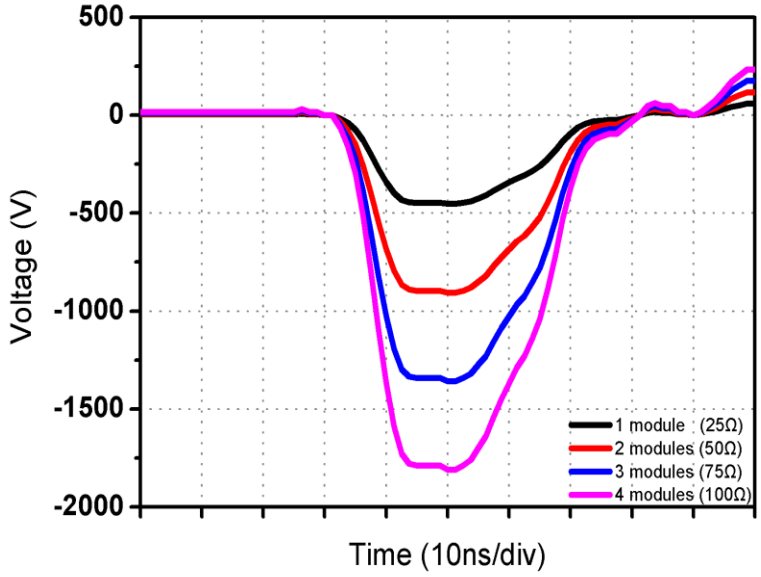

Figure 47 The waveforms of output voltage obtained with different numbers of modules and different load resistances using IES-PFL with single line

4.4 Summary and discussion

In this chapter, A circuit configuration using IES pulse forming lines, which is called inductive Blumlein line, has been proposed and experimentally demonstrated. Single circuit (module) operation has been carried out by using a combination of strip-lines and SiC semiconductor switch. It is also proved that, by stacking multiple modules together, voltage adding can be obtained by using inductive Blumlein lines. This result has indicated the possibility of a new approach to compact and repetitive pulsed power generation. It has to be added that the experiments reported above have yielded relatively low output voltage. For the single-module experiment, the output voltage is limited to be lower than 450 V.because the switch we are using is limited to be operated under 900 V and the switch bears a voltage twice as high as load voltage [19].

For the stack, on the other hand, the module number (and the output voltage) is eventually limited by the DC-DC converters that isolate all switches from each other and from the ground.

In order to increase the output voltage by using this circuit scheme, we have to solve the problem of driver power supply. This can be done, for example, by using isolation transformers. Another more interesting way to do this would be making use of the local resource which, in this case, is the IES current. Other than the driver power supply problem, we do not see any real issue that prevents us from increasing the number of modules, and therefore the output voltage, for the stacked inductive Blumlein lines. Therefore, we are expecting this circuit method to be widely used in future pulsed power applications.

Finally, pulse length is a very important factor, which can be varied by the physical length of the transmission lines. High-permittivity materials have recently become available and there have been attempts of using them in PFLs [22]. It is expected that these new materials will drastically reduce the size and increase the flexibility of the Blumlein lines

CHAPTER V: CONCLUSION

In this thesis, the basic research on all solid state inductive energy storage pulse power technology is carried out for future industrial applications. Based on theoretical analysis and experimental verification, a series of new inductive energy storage circuits are proposed. These circuit modules, voltage adder for what we do, they are fully illustrated in high repetition rate pulsed power generator has the potential to become the compact generators. It is of great significance not only to the improvement of the pulse power technology, but also to the engineering practice.

5.1 The main research work and achievements

- Through the analysis and experiment of the traditional inductive energy storage circuit, the characteristics and limitations of the inductive energy storage are fully realized.

- A method of geometric figure theory is applied to the design of IES pulse generator. By deformation of typical CES circuits, some new IES circuits can be obtained, as we have discussed.

- The IES-PFL adder has been studied, experiments show that this method can overcome the shortcomings of the output waveform is not ideal, compared to the traditional inductive energy storage generator. It has potential as a candidate for future pulsed power generators, to achieve high voltage through multiple series. And it does not need the core to boost the voltage, so it is more compact and lighter. In the experiment, we only use 4 modules to get the result that the voltage change ratio

is close to 30. The short pulses are obtained with peak voltage 4kV and pulse width 20 nanosecond, as well as, 2kV with 40ns.

- Voltage adder using IES Blumlein line with solid stripline and SiC MOSFET is proved feasible. It is a compact pulse source, and it is easy to get negative pulse. A short pulse with a pulse width of about 14 ns is obtained. The peak voltage is about 1.8kV and can continue to increase through the series.

5.2 Main problems and work prospect

To further compress the volume of the device, we need to study the new transmission line structure. The process of voltage adding at the present stage is limited by the isolation voltage of DC –DC converter.Another more interesting way to do this would be making use of the local resource which, in this case, is the IES current.

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Appendix I FPGA control program

```
/ ----------------------------------------------------------------------

//  COPYRIGHT NOTICE

// Module: pulse_gen

// Author: Yu Liang

// Description: Pulse generate module

// Features:

// 1.The output pulse frequency can be adjusted

// 2.The output pulse width can be adjusted

// 3.It can be reset by "reset"

// ----------------------------------------------------------------------

// Code Revision History :

// Version: |Mod. Date:   |Changes Made:

// V1.0     |2017/10/21   |Initial ver

// ----------------------------------------------------------------------
```

```
module pluse_gen
(
input                                clk_50,
input                                RESET,
output  reg                  pluse_out
);
parameter f= 1;//Frequency
parameter n = 50000000/f;
parameter div_n = n-1;
parameter plusewidth = 2000;//Unit nanosecond
parameter duty_n = plusewidth/20;
reg      [25:0] cycle;
reg      [25:0] duty;
reg      [25:0] cnt;
//Control cycle and frequency
always @(posedge clk_50 or negedge RESET)
```

```
begin
  if(!RESET) cycle<=0;
  else if(cycle < div_n)  cycle <= cycle + 1;
  else  cycle <= cycle;
end
//Control duty cycle
always @(posedge clk_50 or negedge RESET)
begin
  if(!RESET) duty<= 0;
  else if(duty < duty_n)  duty <= duty + 1;
  else  duty <= duty;
  end
//counter for cycle
always @(posedge clk_50 or negedge RESET)
begin
        if(!RESET)
```

```
                cnt<=0;
        else
                if(cnt>=cycle) cnt<=0;
                else cnt <= cnt + 1;
end
//pulse generate with duty
always @(posedge clk_50 or negedge RESET)
begin
        if(!RESET)
                pluse_out<=1'b0;
         else if(cnt<duty) pluse_out<=1'b1;
         else if(duty>=cycle) pluse_out<=1'b0;
         else pluse_out<=1'b0;
end
endmodule
```

Appendix II Publication of papers

- Journal Articles:

1. Liang Yu, Yu Feng, Weihua.J et al. Voltage Adding of Pulse Forming Lines Using Inductive Energy Storage[J]. *IEEE Trans.Dielectr. Electr. Insul.* , vol.24, no.4, pp.2211-2215, Aug. 2017.

2. Liang Yu, Weihua.J et al. Repetitive Pulsed Power Generator based on inductive-energy-storage PFL[J]. *High Power Laser and Particle Beams*, vol.30, no.2, pp.1-5, Feb. 2018

3. Liang Yu, Taichi Sugai , Akira Tokuchi , and Weihua.J. Pulsed Voltage Adder Topology Based on Inductive Blumlein Lines [J]. *IEEE Trans. Plamas Sci.* to be published

- Conference Papers

1. Yu Feng, Liang Yu, Weihua Jiang, Research on transient characteristics of SiC-MOSFET switch[C],conference on gas discharge, plasma science and technology, and pulsed power technology, Saga University,Japan,2016

2. Liang Yu, Taichi Sugai, and Akira Tokuchi, et al. Voltage Adding of Inductive Energy Storage Circuits[C], conference on gas discharge, plasma science and technology, and pulsed power technology, Saga University,Japan,2016

3. Liang Yu, Weihua.J, Power Adding of Inductive Energy Storage Circuits for Application to Gas Discharge[C], 21st International conference on gas discharges and their appllications, nagoya university, Japan, 2016

4. 酒　澤政，余 亮、須貝　太一、江 偉華：「パルスパワー伝送線路のインピーダンス制御と評価」，電気学会東京支部新潟支所研究発表会，2017 年 11 月 11 日

5. 曹 竣淳、余 亮、須貝　太一、江 偉華「小型 MARX 回路の開発と応用」電気学会東京支部新潟支所研究発表会、2017 年 11 月 11 日