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Adaline-Based Control of Capacitor Supported DVR for Distribution System

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ABSTRACT

In this paper, a new control algorithm for the dynamic voltage restorer (DVR) is proposed to regulate the load terminal voltage during various power quality problems that include sag, swell, harmonics and unbalance in the voltage at the point of common coupling (PCC). The proposed control strategy is an Adaline (Adaptive linear element) Artificial Neural Network (ANN) and is used to control a capacitor supported DVR for power quality improvement. A capacitor supported DVR does not need any active power during steady state because the voltage injected is in quadrature with the feeder current. The control of the DVR is implemented through derived reference load terminal voltages. The proposed control strategy is validated through extensive simulation studies using the MATLAB software with its Simulink and SimPower System (SPS) toolboxes. The DVR is found suitable to support its dc bus voltage through the control under various disturbances.

Keywords: Power quality, Custom power devices, Dynamic voltage restorer, Artificial neural network

1. Introduction

Power quality issues in the distribution system are widely addressed in the literature^[1-6] due to the sensitive and critical loads such as precise manufacturing process, automation etc. A new group of devices like distribution static compensator (DSTATCOM), dynamic voltage restorer (DVR) and unified power quality conditioner

(UPQC) are developed and used for improving power quality in the distribution system under the generic name of custom power devices^[2]. The shunt connected DSTATCOM is used for improving the power quality of the supply current and the series connected DVR is used for improving the power quality of the load terminal voltage. The UPQC is meant for improving power quality of both current and voltage. Power quality problems include voltage sags, swells, transients and other distortions to the sinusoidal supply voltage waveform and these problems are compensated using the DVR^[1]. Some attempts have been made to develop protection and technologies of DVR^[7-8]. There are number of custom power devices installed at the consumer premises to

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protect the sensitive loads as per the standards such as IEEE-519 [9].

A DVR is connected between the supply and sensitive load, so that it can inject the compensating voltage into the distribution line. Therefore, the DVR can provide an effective solution for compensating voltage sag, swell, harmonics and unbalance in supply voltage. There are several methods like pre-sag compensation, in-phase compensation and phase-advanced method for compensation [10-20]. A capacitor supported DVR does not need active power during steady state because the voltage is injected in quadrature with the feeder current [20]. However, its disadvantage is that the restored voltage may not be in-phase with the voltage before the power quality event. In order to achieve the pre-sag/pre-swell voltage, the DVR should inject or absorb active power to the distribution system. However, capacitor supported DVR is used when the phase jump, caused by the quadrature voltage injection, is affordable.

One of the most important issues is voltage sag. It is a sudden reduction in the voltage for short duration usually caused by faults on transmission and distribution systems. Similarly, the sudden increase in voltage for a short duration is called voltage swell. The harmonics in voltage and unbalance in voltage are also among power quality issues. The DVR can provide an effective solution for all these power quality problems. The DVR is proposed as an important controller in the custom power park [21]. Some topologies of the DVR are compared in [22]. The analysis, design and voltage injection schemes of capacitor supported DVR is discussed in the literature [2, 20] and the different control strategies are developed for the control of DVR [12-26]. The instantaneous reactive power theory (IRPT) [4], synchronous reference frame theory (SRFT) [6, 22], sliding mode controller [10], space vector modulation [15], symmetrical components [20] etc., based control techniques for series compensator are reported in the literature.

The SRFT based algorithm reported in [22] is advantageous because calculations are performed in the rotating reference frame. But, the computation involves conversion from stationary frame to rotating frame and then the reference signals from rotating frame to stationary frame. The IRPT algorithm [4] for the reference signal

generation involves the conversion from three-phase to two-phase and vice versa. In this paper, a new control algorithm is developed based on unit templates [27] and Adaline based neural network [28]. It is for the control of capacitor supported DVR for compensation of voltage sag, swell, harmonics and unbalance in supply voltage. The extensive simulations are performed using MATLAB software with its Simulink and SimPower System (SPS) tool boxes for verifying the proposed control algorithm of DVR.

2. Principle of Operation of DVR

The schematic diagram of a capacitor supported DVR is shown in Fig. 1. Three voltage sources (v_{sa} , v_{sb} , v_{sc}) represent the 3-phase supply system and the series source impedance are shown as $Z_a (L_a, R_a)$, $Z_b (L_b, R_b)$ and $Z_c (L_c, R_c)$. The terminal voltages (v_{ta} , v_{tb} , v_{tc}) have power quality problems and the DVR uses injection transformers (T_r) to inject voltages (v_{Ca} , v_{Cb} , v_{Cc}) to get undistorted load voltages (v_{La} , v_{Lb} , v_{Lc}). A voltage source converter (VSC) along with a dc capacitor (C_{dc}) is used as a DVR. The switching ripple in the injected voltage is filtered using a series inductor (L_r) and a parallel capacitor (C_r). The considered load is a three-phase lagging power factor load and the data of the load is given in Appendix.

The ripple filter is designed based on the switching frequency. It is designed that the capacitor offers a low impedance path for the switching ripple and the series inductor should provide high impedance for the switching ripple. The reactance given by the capacitor and the inductor at half of the switching frequency ($f_s = 10$ kHz),

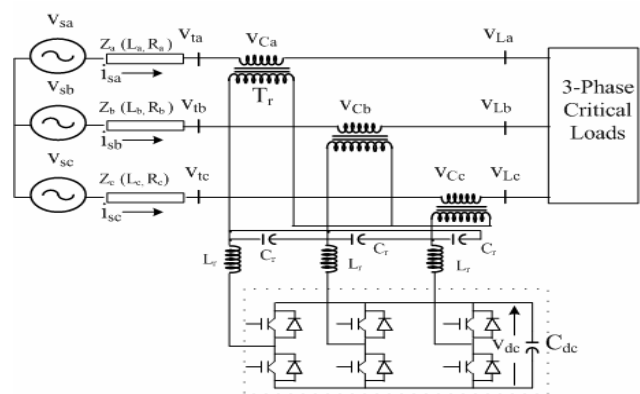


Fig. 1. Schematic diagram of capacitor supported DVR.

ie, $f_r = f_s/2 = 5 \text{ kHz}$ is calculated as,

$$X_{Cr} = 1 / (2 * \pi * f_r * C_r) = 1 / (2 * 3.14 * 5000 * C_r) \tag{1}$$

$$X_{Lr} = 2 * \pi * f_r * L_r = 2 * 3.14 * 5000 * L_r \tag{2}$$

Considering, $X_{Cr} = 3 \Omega$, $C_r = 10.61 \mu\text{F}$
 $X_{Lr} = 100 \Omega$, $L_r = 3.18 \text{ mH}$

These values of ripple filter elements are initially used for simulation and by iteration it is found that, $L_r = 3.5 \text{ mH}$, $C_r = 10 \mu\text{F}$ is suitable for minimum ripple at the output of DVR.

Fig. 2 shows the phasor diagram of the DVR operation for the compensation of sag, swell and unbalance in supply voltage. The load terminal voltage and current during pre-sag condition are represented as $V_{L(\text{presag})}$ and I_s' as shown in Fig. 2(a). After the sag event, the terminal voltage (V_{ta}) is lower than pre-sag condition. The voltage injected by the DVR (V_{Ca}) is used to maintain the load voltage (V_{La}) at the rated magnitude and this has two components, V_{cad} and V_{caq} . The voltage in-phase with current (V_{cad}) is to regulate the dc bus voltage and also to meet the power loss in the VSC of DVR. The voltage in

quadrature with the current (V_{caq}) is to regulate the load voltage (V_{La}) at constant magnitude. During swell in voltage, the voltage injection (V_{Ca}) is such that the load voltage lies in the locus of the circle as shown in Fig. 2(b). The unbalance compensation when voltage sag occurs in two phases is shown in Fig. 2(c). The unbalanced terminal voltages are (V_{ta} , V_{tb} , V_{tc}) and the injection voltages in each phase (V_{Ca} , V_{Cb} , V_{Cc}) are such that the line voltages (V_{La-Lb} , V_{Lb-Lc} , V_{Lc-La}) are equal in magnitude and are displaced by 120° .

3. Control Strategy of DVR

The main aim of a DVR is to inject a voltage in series with the supply for regulating the load terminal voltage. The proposed control algorithm is based on unit templates and Adaline based artificial neural network (ANN) [28] for fundamental voltage extraction. The proposed control scheme is shown in Fig. 3. The reference load voltages (v_{La}^* , v_{Lb}^* , v_{Lc}^*) are derived from the sensed load terminal voltages (v_{La} , v_{Lb} , v_{Lc}), supply currents (i_{sa} , i_{sb} , i_{sc}), terminal voltages (v_{ta} , v_{tb} , v_{tc}) and the dc bus voltage (v_{dc}) of DVR as feedback signals. The sag, swell, harmonics and unbalance in terminal voltages are compensated by controlling the DVR. The load voltage is regulated and the waveform is controlled to be sinusoidal.

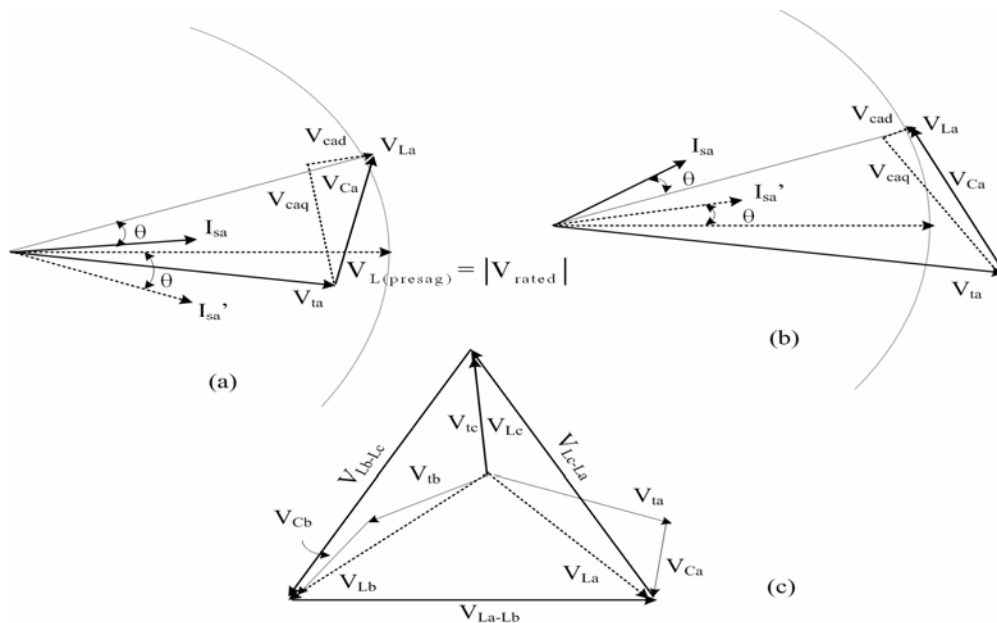


Fig. 2. Phasor diagram for capacitor supported DVR. (a) voltage sag (b) swell (c) unbalanced sag

3.1 Control Algorithm

There are two proportional-integral (PI) controllers used to estimate the in-phase and quadrature components of the injected fundamental voltage by the DVR. Three phase unit templates (u_a, u_b, u_c) are derived in-phase with the supply currents (i_{sa}, i_{sb}, i_{sc}). The dc bus voltage of the DVR is regulated using a PI controller over the sensed dc bus voltage (v_{dc}) and reference value (v_{dc}^*) of DVR. This PI controller output is considered as the amplitude (V_d^*) of the in-phase component of the injection voltages ($V_{Cad}^*, V_{Cbd}^*, V_{Ccd}^*$).

The other PI controller is used to derive the amplitude (V_q^*) of the quadrature component of the injection voltages ($V_{Caq}^*, V_{Cbq}^*, V_{Ccq}^*$) of the DVR by using it over the amplitude of sensed load voltage (V_{Lp}) and reference value (V_{Lp}^*) of the load voltage. To estimate reference load voltages ($v_{La}^*, v_{Lb}^*, v_{Lc}^*$), the fundamental components of terminal voltages ($v_{ta1}, v_{tb1}, v_{tc1}$) are extracted from the sensed terminal voltages (v_{ta}, v_{tb}, v_{tc}). The algebraic sum of the in-phase components ($V_{Cad}^*, V_{Cbd}^*, V_{Ccd}^*$), the quadrature components ($V_{Caq}^*, V_{Cbq}^*, V_{Ccq}^*$) and the positive sequence fundamental of terminal voltages ($v_{ta1}, v_{tb1}, v_{tc1}$) are added and these added voltages are considered as the reference load voltages ($v_{La}^*, v_{Lb}^*, v_{Lc}^*$). A pulse width modulation (PWM) controller is used over the reference ($v_{La}^*, v_{Lb}^*, v_{Lc}^*$) and sensed load voltages values (v_{La}, v_{Lb}, v_{Lc}) to generate

gating signals for the IGBT's (insulated gate bipolar transistors) of the VSC of DVR. The PWM carrier wave (triangular) frequency is set at 10 kHz. The gating pulses switch the IGBT's of the VSC for the compensation of sag, swell, unbalance and harmonics in terminal voltage to provide sinusoidal balanced load voltages.

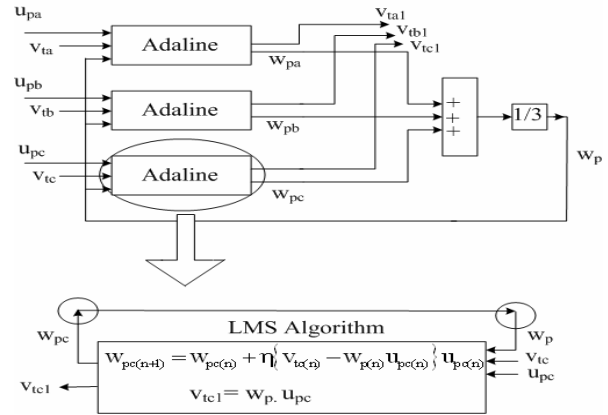


Fig. 4. Block diagram for fundamental voltage extraction using Adaline based ANN.

3.2 Artificial Neural Network (ANN) Method for Extraction of Fundamental Component

The extraction of balanced positive sequence fundamental frequency components of terminal voltages ($v_{ta1}, v_{tb1}, v_{tc1}$) is carried out using Artificial Neural Network (ANN) based on least mean square (LMS)

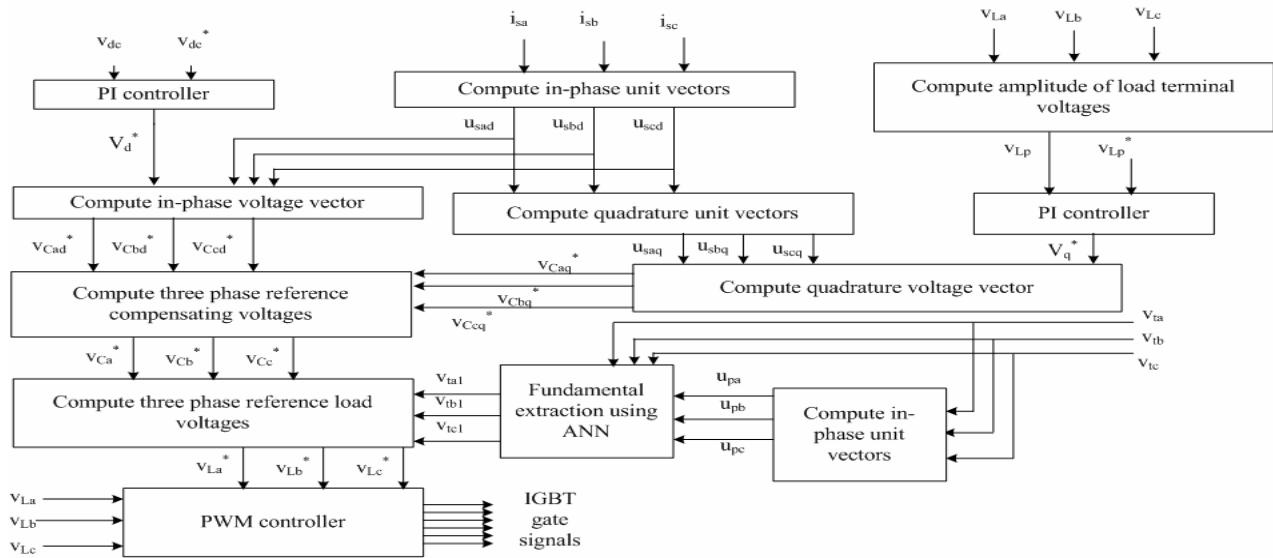


Fig. 3. Proposed control strategy for the capacitor supported DVR.

algorithm known as Adaline (adaptive linear element) technique [28]. Fig. 4 shows the block diagram of the Adaline approach, which is based on online estimation of weights corresponding to active fundamental frequency component. The ANN control algorithm is based on the positive sequence extraction of the component vector in-phase with the unit vector template. The unit vector templates (u_{pa} , u_{pb} , u_{pc}) are derived from sensed terminal voltages (v_{ta} , v_{tb} , v_{tc}). To estimate the positive sequence fundamental component of the terminal voltages (v_{ta1} , v_{tb1} , v_{tc1}), the sensed terminal voltages (v_{ta} , v_{tb} , v_{tc}) and unit templates (u_{pa} , u_{pb} , u_{pc}) in-phase with terminal voltages are required. Two phase unit voltage vectors are derived using a PLL (phase locked loop) over the terminal voltage and then the unit three phase voltage vectors (u_{pa} , u_{pb} , u_{pc}) are derived as,

$$\begin{bmatrix} u_{pa} \\ u_{pb} \\ u_{pc} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} \sin \omega t \\ \cos \omega t \end{bmatrix} \quad (3)$$

where, $\sin \omega t$ and $\cos \omega t$ are obtained using the PLL. Estimates of the fundamental of terminal voltage for each phase can be chosen as,

$$v_{tc1} = w_p \cdot u_{pc} \quad (4)$$

where, w_p is the average weight estimated and u_{pc} is the

unit template.

The estimation of the weight in n th sampling period for each phase is given as per eqn. (2) as,

$$w_{pc(n+1)} = w_{pc(n)} + \eta \{ v_{tc(n)} - w_{pc(n)} u_{pc(n)} \} u_{pc(n)} \quad (5)$$

where w_{pc} , v_{tc} and η are the weight estimated, the terminal voltage and the convergence coefficient respectively. The average weight (w_p) is calculated as the average weight estimated in each phase (w_{pa} , w_{pb} , w_{pc}).

$$w_p = (w_{pa} + w_{pb} + w_{pc})/3 \quad (6)$$

The factor, η decides the rate of convergence and accuracy of estimation. The practical range of η lies in between 0.1 and 1 and the considered value is 0.2 in this work.

4. MATLAB Based Simulation of DVR System

Fig. 5 shows the MATLAB model of the DVR connected system. The supply voltage is realized by using a three-phase supply voltage and the source impedance is connected in its series. In order to simulate the disturbances at the PCC voltage (v_{ta} , v_{tb} , v_{tc}), an additional load is switched on with a circuit breaker. The considered load is a lagging power factor load. The DVR is connected in series with the supply using an injection transformer. The VSC of DVR is connected to the

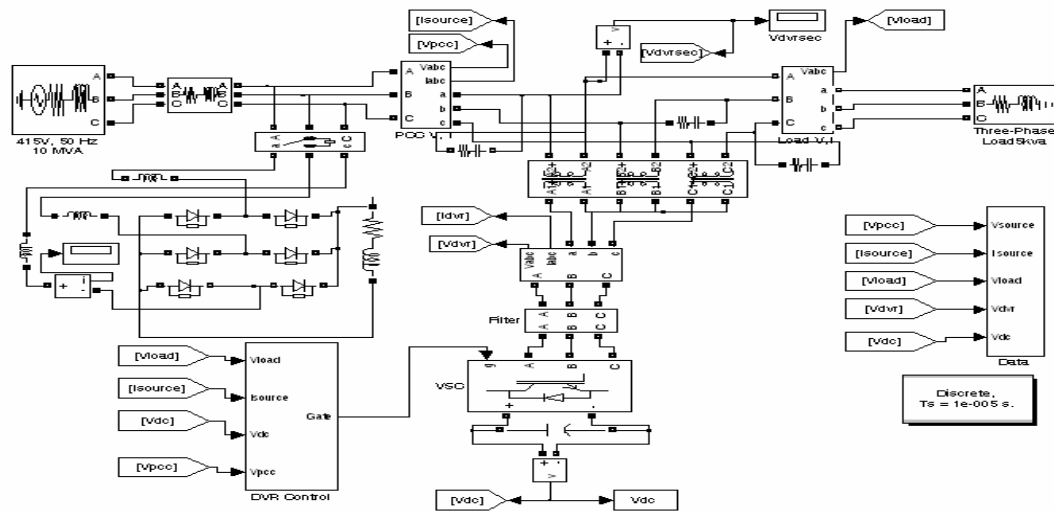


Fig. 5. MATLAB block diagram of DVR connected system.

transformer along with a ripple filter. The dc bus capacitor is selected based on the transient energy requirement and the dc bus voltage is selected based on the injection voltage level. The dc capacitor decides the ripple content in the dc voltage. The system data are given the Appendix.

The control algorithm for the DVR is modeled in MATLAB and it is given in Fig. 6. The control scheme shown in Fig. 3 and Fig. 4 are modeled here. The reference load voltages are derived from the sensed terminal voltages, supply currents, load voltages and the dc bus voltage of DVR. A pulse width modulation (PWM) controller is used over the reference and sensed load voltages values to generate gating signals for the IGBT's of the VSC of DVR.

5. Results and Discussion

The performance of the DVR for different supply disturbances is tested under various operating conditions. The proposed control algorithm is tested for different power quality events like voltage sag (Fig. 7), voltage swell (Fig. 8), balanced and unbalanced sag in terminal voltage (Fig. 9) and harmonics in supply voltage (Fig.10). The proposed control algorithm is able to mitigate the above mentioned power quality problems successfully. A balanced sag in source voltage of 30% in the terminal voltage (v_t) is introduced at 0.30 seconds and it occurs for 5 cycles of ac mains as shown in Fig. 7. The terminal voltage (v_t), ANN based extracted fundamental voltage (V_{t1}), DVR voltage (v_C), load voltage (v_L), source current (i_s), amplitude of terminal voltage (V_t), the amplitude of load voltage (V_L) and the dc bus voltage (v_{dc}) are also

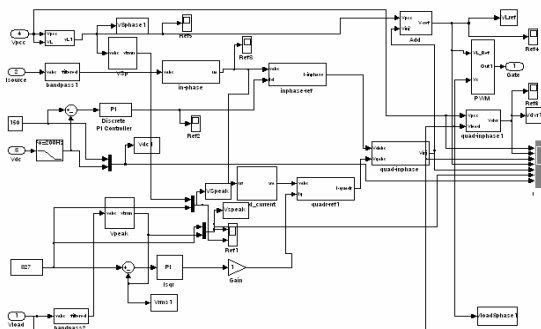


Fig. 6. MATLAB model of the ANN based control scheme of DVR.

shown in Fig. 7. The DVR injects a voltage (v_C) in series with the terminal voltage (v_t). The load voltage (v_L) is regulated at the rated value, which demonstrates the satisfactory dynamic performance of DVR.

The dynamic performance of the DVR for a swell in terminal voltage is given in Fig. 8. The terminal voltage (v_t), ANN based extracted fundamental voltage (V_{t1}), DVR voltage (v_C), load voltage (v_L), source current (i_s), amplitude of terminal voltage (V_t), the amplitude of load voltage (V_L) and the dc bus voltage (v_{dc}) are also shown in Fig. 8. The load voltage (v_L) is regulated at rated value, which shows the satisfactory performance of the DVR. The dc bus voltage is regulated at the reference value, though a small fluctuation occurs during transients.

The performance of DVR for unbalance in supply voltage is shown in Fig. 9. The unbalanced voltage sag in one phase is introduced first followed by unbalanced voltage sag in two phases and the balanced sag in all phases. The performance of the DVR is observed to be satisfactory in all these cases. The DVR injects unequal voltages (v_C) so that the load voltage (v_L) is regulated to a constant magnitude. The terminal voltage (v_t), ANN based extracted fundamental voltage (V_{t1}), DVR voltage (v_C), load voltage (v_L), source current (i_s), amplitude of terminal voltage (V_t), the amplitude of load voltage (V_L) and the dc bus voltage (v_{dc}) are also shown in Fig. 9, to demonstrate the satisfactory behavior of DVR.

The harmonics compensation in load voltage is achieved and depicted in Fig. 10. The terminal voltage (v_t), ANN based extracted fundamental voltage (V_{t1}), DVR voltage (v_C), load voltage (v_L), source current (i_s), amplitude of terminal voltage (V_t), the amplitude of load voltage (V_L) and the dc bus voltage (v_{dc}) are also shown in Fig. 10. The terminal voltage (v_t) is distorted by switching on and off the non-linear load and the load voltage (v_L) is sinusoidal and constant in magnitude due to the injection of harmonic voltage (v_C) using the DVR. The load voltage (v_{La}) has a total harmonic distortion (THD) of 1.67% (Fig. 11(a)) at the time of disturbance and the voltage at PCC (v_{ta}) has a THD of 7.27% (Fig. 11(b)). The source current is sinusoidal with a THD of 0.20% (Fig. 11(c)). These results demonstrate the capability of DVR for the compensation of harmonics in supply voltages along with sag, swell and unbalance compensation.

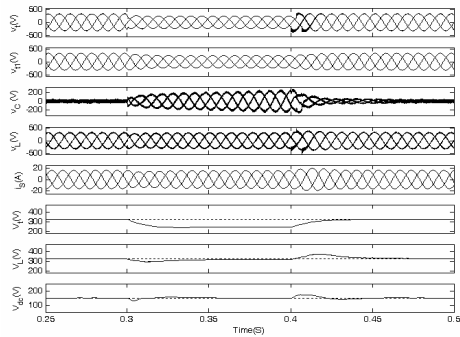


Fig. 7. Voltage sag compensation using ANN controlled DVR.

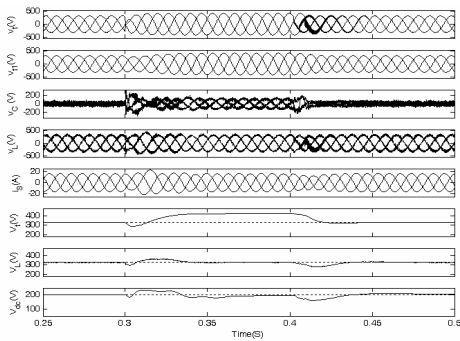


Fig. 8. Voltage swell compensation using ANN controlled DVR.

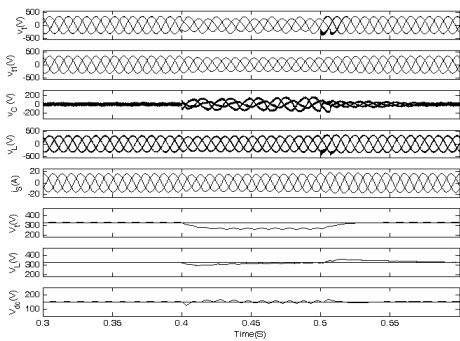


Fig. 9. Unbalanced Voltage sag compensation using ANN controlled DVR.

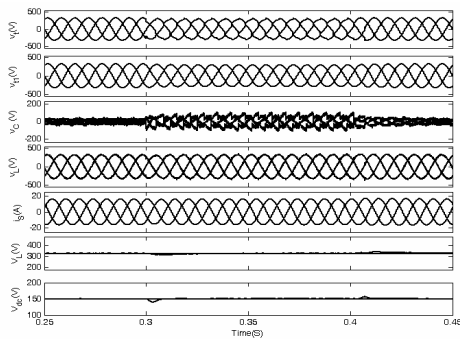


Fig. 10. Voltage harmonic compensation using ANN controlled DVR.

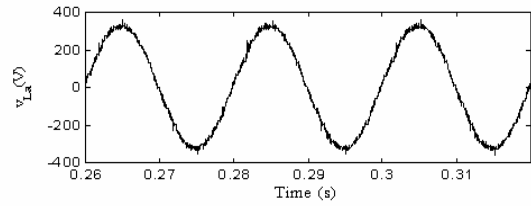


Fig. 11. (a) Load voltage and harmonic spectrum.

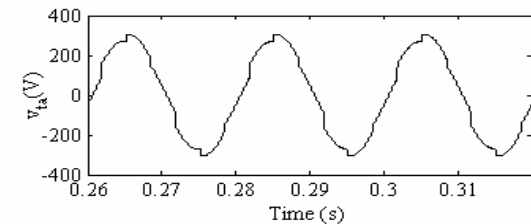


Fig. 11. (b) Terminal voltage and harmonic spectrum.

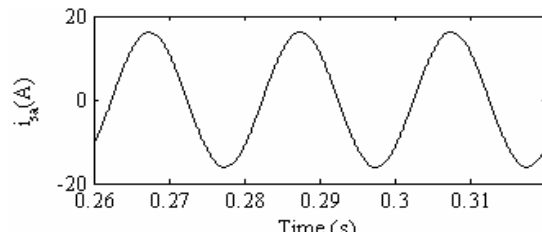


Fig. 11. (c) Supply current and harmonic spectrum.

6. Conclusions

An Adaline (adaptive linear element) Artificial Neural Network (ANN) based new control strategy has been proposed for the DVR. The proposed control scheme of DVR has been validated for the compensation of sag, swell, unbalance and harmonics in terminal voltages. The fundamental component of the terminal voltage was extracted using the Adaline based neural network technique. The performance of the DVR has been observed to be satisfactory for compensation of various power quality disturbances like sag, swell, unbalance and harmonics in terminal voltage. Moreover, it has been found capable of providing self-supported dc bus of the DVR through power transfer from the ac line at fundamental frequency.

Appendix

The parameters of the system considered are:

AC source voltage: 415 V, 50 Hz

Line Impedance: $L_s=3.5$ mH, $R_s=0.01$ Ω

Loads: (i) Linear: 10 kVA, 0.707 pf lag

DVR:

Ripple filter: $L_r=3.5$ mH, $C_r=10$ μ F

DC bus capacitance of DVR: 1000 μ F

DC bus voltage of DVR: 150 V

DC bus voltage PI controller: $K_{pd}=0.1$, $K_{id}=0.8$

Load voltage PI controller: $K_{pq}=0.2$, $K_{iq}=0.5$

PWM switching frequency: 10 kHz

Series Injection Transformer: Three numbers of single-phase transformers of each of rating 5kVA, 200V/400V.

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