Optimal microscale water cooled heat sinks for targeted alleviation of hotspot in microprocessors

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Abstract Hotspots in microprocessors arise due to non-uniform utilization of the underlying integrated circuits during chip operation. Conventional liquid cooling using microchannels leads to undercooling of the hotspot areas and overcooling of the background area of the chip resulting in excessive temperature gradients across the chip. These in turn adversely affect the chip performance and reliability. This problem becomes even more acute in multi-core processors where most of the processing power is concentrated in specific regions of the chip called as cores. We present a 1-dimensional model for quick design of a microchannel heat sink for targeted, single-phase liquid cooling of hotspots in microprocessors. The method utilizes simplifying assumptions and analytical equations to arrive at the first estimate of a microchannel heat sink design that distributes the cooling capacity of the heat sink by adapting the coolant flow and microchannel size distributions to the microprocessor power map. This distributed cooling in turn minimizes the chip temperature gradient. The method is formulated to generate a heat sink design for an arbitrary chip power map and hence can be readily utilized for different chip architectures. It involves optimization of microchannel widths for various zones of the chip power map under the operational constraints of maximum pressure drop limit for the heat sink. Additionally, it ensures that the coolant flows uninterrupted through its entire travel length consisting of microchannels of varying widths. The resulting first design estimate significantly reduces the computational effort involved in any subsequent CFD analysis required to fine tune the design for more complex flow situations arising, for example, in manifold microchannel heat sinks.

Keywords: Microchannels, Hotspot-targeted cooling, Electronics cooling, Hotspots

1. Introduction

Moore's law has driven the performance increase in microprocessors over the last many decades (Moore, 1965). However, the inability to follow the Dennard scaling for supply voltage while downscaling the transistor has progressively increased chip heat flux dissipation densities (Dennard et al., 2007). This in-turn has shifted the focus of heat transfer community from air cooling to single and two-phase liquid cooling to maintain chip reliability (JEDEC, 2010; Sharma et al., 2012). Starting with the seminal work of Tuckerman and Pease (Tuckerman and Pease, 1981), extensive research has been done on liquid cooling including investigations on traditional microchannel (TMC) heat sinks and manifold microchannel (MMC) heat sinks. In TMC heat sinks, the coolant enters the heat transfer structure through a single inlet and leaves through a single outlet (Lee et al., 2005). In MMC heat sinks, the coolant circulates through multiple and alternating inlet and outlet slot nozzles thus improving the heat transfer at comparatively lower pressure drops. (Copeland et al., 1997; Escher et al., 2010; Kermani et al., 2009; Ryu et al., 2003; Sharma et al., 2013).

Most of the research on liquid cooling of chips has focused on maximum junction temperature $\left(T_{J,max}\right)$ reduction under uniform heat flux dissipation conditions. However, it is also necessary that the chip temperature is spatially as uniform as possible (i.e. approaching the isothermal chip condition). Large temperature gradients increase thermal stresses in the chip to substrate or heat sink

interface, reduce electronic reliability in regions of high temperature and create circuit imbalances in CMOS devices (JEDEC, 2010). A few studies have focused on reducing temperature non-uniformity across the microprocessor $\left(\Delta T_{J,max} = T_{J,max} - T_{J,min}\right)$; however, under a uniform chip heat flux map (Barrau et al., 2010; Hetsroni et al., 2002; Rubio-Jimenez et al., 2012).

The large increase in chip heat flux dissipation in the last decade has resulted in an industry-wide shift towards multicore microprocessors (Esmaeilzadeh et al., 2012). In a typical multicore microprocessor, the heat flux dissipation in the cores (termed as hotspots) is multiple times higher than the rest of the chip (termed as background) thus increasing the criticality of chip temperature non-uniformity as compared to serial microprocessors. A few single phase liquid cooling approaches have been proposed in the past for preferential cooling of hotspots (termed as hotspot-targeted cooling) with varying degree of success (Brunschwiler et al., 2009; Lee and Garimella, 2005; Lee et al., 2013)

Embedded liquid cooling (ELC), in which the coolant is circulated through microchannels etched into the backside of the chip, is an effective approach to target the hotspots. ELC compares favorably against conventional backside attached cooling which suffers from high resistance due to thermal interface material (TIM) (Dang et al., 2006; Etessam-Yazdani et al., 2008; Mingyuan and Huang, 2007).

In this paper, we propose a one-dimensional model for estimation of a novel; single-phase liquid-cooled, hotspot targeted microchannel heat sink for modern day microprocessors. The model provides a computationally efficient method to quickly obtain hotspot-targeted microchannel and flow rate distributions. The model is formulated as a generalized design method and is applicable to ELC as well as conventional heat sinks on one hand and TMC as well as MMC heat sinks on the other.

2. Analytical design method

Consider an arbitrary microprocessor power map as shown in Fig.1. In the figure, each shaded area represents a region dissipating a different level of heat flux that is multiple times higher than that dissipated in the unshaded area (background).

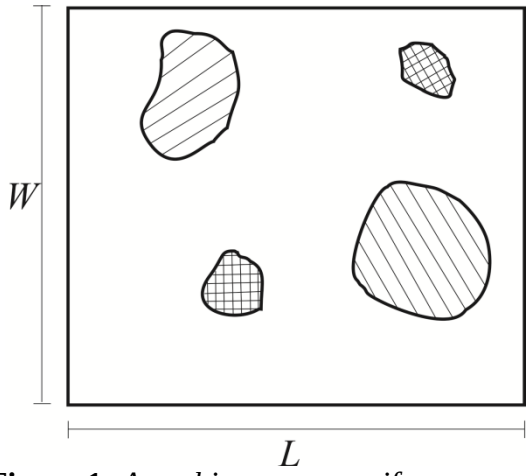


Figure 1: *An arbitrary non-uniform power map with regions of high heat flux*

This power map can be discretized such that each cell of the discretized map encompasses an area of nearly constant heat flux. Figure 2(a) illustrates the coarsest level of discretization for the power map in Fig. 1 and Fig. 2(b) illustrates the $(i,j)^{th}$ cell and the nomenclature adopted in this work for the discretized power map.

The discretization can be refined depending upon the desired resolution of the calculated temperature map. However, the highest degree of refinement is limited by the following constraint:

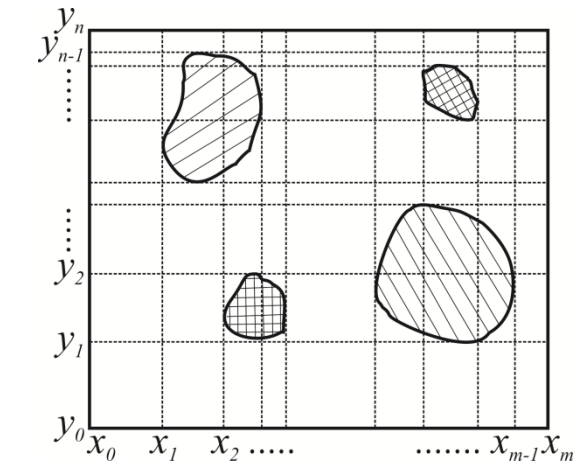
$$\Delta y_i \geq w_{c,max} + w_{w,max} \qquad (1)$$

With the flow direction as shown in Fig. 2(b), the average coolant temperature in the $(i,j)^{th}$ cell is given by Eq.(2) and the average junction temperature, assuming negligible heat spreading, is obtained in Eq.(3) below:

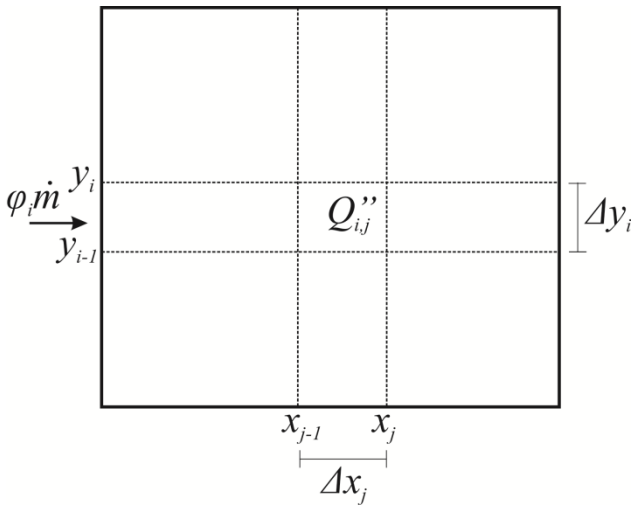
$$T_{f,(i,j)} = T_{f,in} + \sum_{k=1}^{j-1} \frac{Q''_{(i,k)} \Delta y_i \Delta x_k}{\dot{m} cp_f} + \frac{Q''_{(i,j)} \Delta y_i \Delta x_j}{2\varphi_i \dot{m} cp_f} \qquad (2)$$

$$T_{J,(i,j)} = T_{f,(i,j)} + Q''_{(i,j)} R_\lambda + Q''_{(i,j)} R''_{\alpha,(i,j)} \qquad (3)$$

where, R_λ , the total conduction resistance between junctions and base of microchannels,



(a)



(b)

Figure 2: (a) *Discretization of the power map* **(b)** *(i,j)th cell of the discretized power map*

is given by summation of all the conduction resistances in series (such as those of silicon chip thickness, TIM and heat sink base):

$$R_{\lambda} = \sum_{l} \frac{\Delta z_l}{\lambda_l} \tag{4}$$

$R''_{\alpha,(i,j)}$ is the convective resistance for heat transfer to the coolant. Accounting for the fin resistance and assuming adiabatic fin tops, $R''_{\alpha,(i,j)}$ is given by (Escher et al., 2010):

$$R''_{\alpha,(i,j)} = \frac{w_{c,(i,j)} + w_{w,(i,j)}}{\alpha_{(i,j)} w_{c,(i,j)} + 2\alpha_{(i,j)} h_c \gamma_{(i,j)}} \tag{5}$$

where $\gamma_{(i,j)}$, the fin efficiency, is given by:

$$\gamma_{(i,j)} = \frac{\tanh(m h_c)}{m h_c}, \; m = \sqrt{\frac{2\alpha_{(i,j)}\left(w_{w,(i,j)} + h_c\right)}{\lambda_w w_{w,(i,j)} h_c}} \tag{6}$$

and $\alpha_{(i,j)}$, the heat transfer coefficient can be calculated as:

$$\alpha_{(i,j)} = \frac{Nu_{D,(i,j)} \lambda_f}{D_{c,(i,j)}} \tag{7}$$

$D_{c,(i,j)}$ is an equivalent length scale for the microchannel cross-section and its definition depends upon the form of correlation available for $Nu_{D,(i,j)}$.

With these thermal characteristics of the heat sink in place, the design of the hotspot-targeted heat sink involves determination of geometrical parameters $w_{c,(i,j)}, w_{w,(i,j)}$ and operational parameters $\dot{m}$, φ_i such that, $T_{J,max}$, as well as chip wide temperature gradient $\Delta T_{J,max}$ are minimized, while satisfying the following constraints

$$\begin{aligned} & w_{c,min} \le w_{c,(i,j)} \le w_{c,max} \\ & w_{w,min} \le w_{w,(i,j)} \le w_{w,max} \\ & \Delta P \le \Delta P_{limit} \end{aligned} \tag{8}$$

The geometrical and operational design parameters are determined by separately considering the three terms in Eq. (3) as discussed in the following subsections.

2.1 Determination of φ_i

The first step in minimizing $T_{J,max}$ and $\Delta T_{J,max}$ is minimization of bulk resistance that drives the increase in coolant temperature $T_{f,(i,j)}$ (the first term in Eq. (3) and given by Eq.(2)). This is achieved by equalizing the fluid temperature rise $T_{f,(i,m)} - T_{f,in}$ for all n rows. This gives, *n* equations in *n* unknown variables φ_i:

$$\begin{aligned} & \sum_{i=1}^{n} \varphi_i = 1 \\ & \text{for } i = 2 \text{ to } n \\ & \frac{\Delta y_i}{\varphi_i}\left(\sum_{k=1}^{m-1} Q''_{(i,k)} \Delta x_k + \frac{Q''_{(i,m)} \Delta x_m}{2}\right) = \\ & \frac{\Delta y_1}{\varphi_1}\left(\sum_{k=1}^{m-1} Q''_{(1,k)} \Delta x_k + \frac{Q''_{(1,m)} \Delta x_m}{2}\right) \end{aligned} \tag{9}$$

With φ_i determined as above, $T_{f,(i,j)}$ in

Eq. (3) are fixed. The second term $Q''_{(i,j)}R_\lambda$ is fixed for a given power map and cooling architecture. Hence, only the convective resistance term $Q''_{(i,j)}R''_{\alpha,(i,j)}$ can be controlled which leads to determination of the channel widths $w_{c,(i,j)}$ as explained in the following subsection.

2.2 Determination of $w_{w,(i,j)}$ and $w_{c,(i,j)}$

The channel wall widths $w_{w,(i,j)}$ can be independently fixed such that the overall pressure drop is minimized as below:

$$w_{w,(i,j)} = w_{w,min} \tag{10}$$

As a result, the distribution of junction temperatures $T_{J,(i,j)}$ is determined only by the distribution of channel widths $w_{c,(i,j)}$ through the convective resistance term in Eq.(3). This term is minimized under the following condition:

$$Q''_{(i,j)}R''_{\alpha,(i,j)} = Q''_{max}R''_{\alpha,min} = Q''_{min}R''_{\alpha,max} \tag{11}$$

where the minimum convective resistance $R''_{\alpha,min}$ can be fixed as below:

$$R''_{\alpha,min} = \frac{w_{c,min} + w_{w,min}}{\alpha_{max} w_{c,min} + 2\alpha_{max} h_c \gamma_{min}} \tag{12}$$

Eqs. (11), (5) and (10) result in $nm-1$ non-linear equations for $nm-1$ unknowns $w_{c,(i,j)}$:

$$\frac{w_{c,(i,j)} + w_{w,min}}{\alpha_{(i,j)} w_{c,(i,j)} + 2\alpha_{(i,j)} h_c \gamma_{(i,j)}} = \frac{Q''_{max}R''_{\alpha,min}}{Q''_{(i,j)}} \tag{13}$$

with $\gamma_{(i,j)}$ and $\alpha_{(i,j)}$ given by Eqs. (6) and (7).

Since the channel widths change along flow direction, it is important that the coolant flows uninterrupted in every row (i.e. does not run into a wall). This is ensured by simply modifying $w_{c,(i,j)}$ values from Eq. (13) such that the microchannel pitch in any (i,j)th cell $w_{c,(i,j)} + w_{w,min}$ is related to the pitches in adjacent upstream and downstream cells, $w_{c,(i,j-1)} + w_{w,min}$ and $w_{c,(i,j+1)} + w_{w,min}$, through integral multiples.

2.3 Determination of $\dot{m}$

The only design parameter that remains to be determined is the total coolant flow rate $\dot{m}$. $\dot{m}$ can be determined such that the maximum pressure drop in the microchannels does not violate the pressure drop constraint in Eq. (8) i.e.:

$$\max_i \left(\Delta P_i\right) \le \Delta P_{limit} \tag{14}$$

Pressure drops ΔP_i can be expressed in terms of Fanning friction factor, as below:

$$\Delta P_i = \sum_{j=1}^{m} \frac{2\mu \left(f\,\mathrm{Re}_D\right)_{(i,j)} \Delta x_j}{D^2_{c,(i,j)}} \left(\frac{\varphi_i \dot{m}\, p_{(i,j)}}{\rho_f \Delta y_i A_{c,(i,j)}} \right) \tag{15}$$

where $p_{(i,j)} = w_{c,(i,j)} + w_{w,min}$ is the microchannel pitch and $A_{c,(i,j)} = w_{c,(i,j)} h_c$ is the channel cross-sectional area. Equations (14) and (15) determine highest allowable $\dot{m}$.

2.4 Coolant distribution according to φ_i

Since the pressure drops ΔP_i are bound to be different, the flow distribution φ_i can only be realized if the flow resistances of all parallel *n* rows are equal. This can be achieved by introducing additional resistances in all rows such that:

$$\Delta P_i + \Delta P_i^* = \max_i \left(\Delta P_i\right) = \Delta P_{limit} \tag{16}$$

where ΔP_i^* is the pressure drop due to the additional flow resistance introduced in the ith row. This is a key idea in our approach to hotspot targeted cooling.

The additional resistances can be flow throttling zones either in the manifold that supplies the coolant or within the microchannel structure itself in the form of fine channels. In the latter case, however, it has to be ensured that the flow throttling channels do not interrupt the flow as discussed in section 2.2. Additionally, the throttling zones have to be positioned such that the enhanced cooling caused by the fine microchannels does not affect $\Delta T_{J,max}$. Note that $\Delta P_i^* = 0$ for the ith row with $\Delta P_i = \max_i \left(\Delta P_i\right)$. Similar to Eq.(15), ΔP_i^* can also be expressed as below:

$$\Delta P_i^* = \frac{2\mu\left(f\,\mathrm{Re}_D\right)_i^* L_i^*}{\left(D_i^*\right)^2}\left(\frac{\varphi_i \dot{m}}{\rho_f A_i^* N_i^*}\right) \qquad (17)$$

where the superscript '*' indicates geometrical and operational parameters for the flow throttling zone.

2.5 Developed flow assumption

For traditional heat sinks, the flow can be assumed to be fully developed inside the microchannels. Hence, $w_{c,(i,j)}$ values determined by Eq. (13) are independent of $\dot{m}$ and the heat sink design is completed in a single iteration.

2.7 Developing flow

In more complex flow geometries such as MMC sinks, the flow inside the microchannels is developing for a large part of the channel length. In this case, the heat transfer coefficients $\alpha_{(i,j)}$ and hence the microchannel widths $w_{c,(i,j)}$ are no longer independent of $\dot{m}$. This necessitates the following recursive procedure to determine the optimal geometrical and operational parameters: (a) Assume $\dot{m}$ (b) determine $w_{c,(i,j)}$ using Eq. (13) (c) revise channel widths to ensure uninterrupted flow (d) check the pressure drop constraint in Eq. (14). If the inequality (14) is satisfied, then increase $\dot{m}$ and repeat steps (a)-(d). These steps are repeated till the highest $\dot{m}$ is reached that satisfies the constraint(14).

3. Exemplar design for an arbitrary power map cooled by TMC heat sink

In this section, we illustrate the use of the one-dimensional model to design a hotspot targeted embedded TMC structure. We consider a highly non-uniform power map shown in Fig. 3.

The coolant is assumed to be water with the constant properties: ρ_f = 998.2 kg/m^3, μ_f = 0.001 Pa.s, and cp_f = 4180 J/kgK. The thermal conductivity of Silicon is also assumed to be constant (λ_l =150 W/mK). Following design constraints have been adopted, $w_{c,min} = w_{w,min}$ = 30 μm, ΔP_{limit} =0.5 bar. The unetched chip thickness Δz_l and microchannel height h_c are 225 μm and 300 μm respectively. Flow is assumed to be fully developed and the correlations for Nu and $f\,\mathrm{Re}$, for rectangular channels, are adopted from Shah and London (Shah and London, 1978). These correlations are defined in terms of hydraulic diameter; hence:

$$D_{c,(i,j)} = \frac{2w_{c,(i,j)}h_c}{\left(w_{c,(i,j)} + w_{w,min}\right)}$$
$$D_i^* = \frac{2w_{c,i}^* h_c}{\left(w_{c,i}^* + w_{w,i}^*\right)} \qquad (18)$$

where $w_{c,i}^*$ and $w_{c,i}^*$ are channel and wall widths of the flow throttling channels.

Using the coarsest level of discretization similar to Fig.2, and following the sections 2.1 and 2.2, we obtain a set of non-linear system of equations for $w_{c,(i,j)}$ (Eq.(13)) that is solved using MATLAB. The $w_{c,(i,j)}$ values so obtained are modified to ensure uninterrupted coolant flow (refer section 2.2). The resulting hotspot-targeted w_c distribution is shown in Fig. 4.

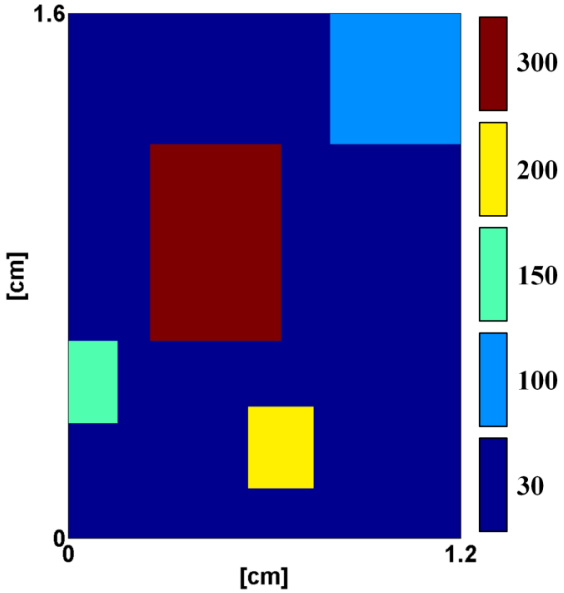


Figure 3: *An exemplar non-uniform power map with heat flux dissipation in W/cm^2.*

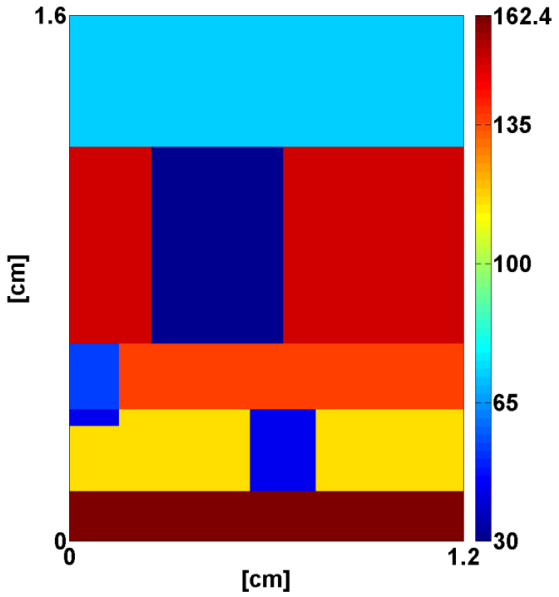


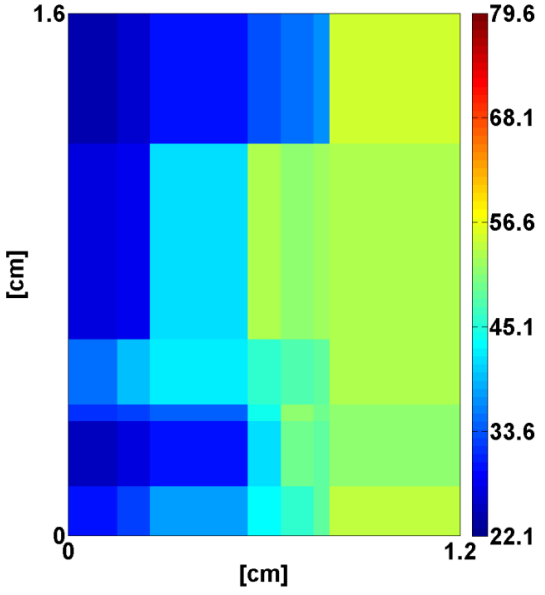
Figure 4: *w_c distribution for the power map in Fig. 3*

The ΔP_{limit} constraint limits $\dot{m}$ to 1.17 g/s (0.07 l/min). Figure 5(a) shows the temperature map of the chip corresponding to the hotspot targeted microchannel structure at 0.07 l/min. The performance of the optimal design is compared against a base case consisting of uniformly fine, embedded microchannels (w_c =30 μm) and uniform flow distribution. The base case performance for the same pumping power as the design in Fig. 4 is shown in Fig. 5(b).

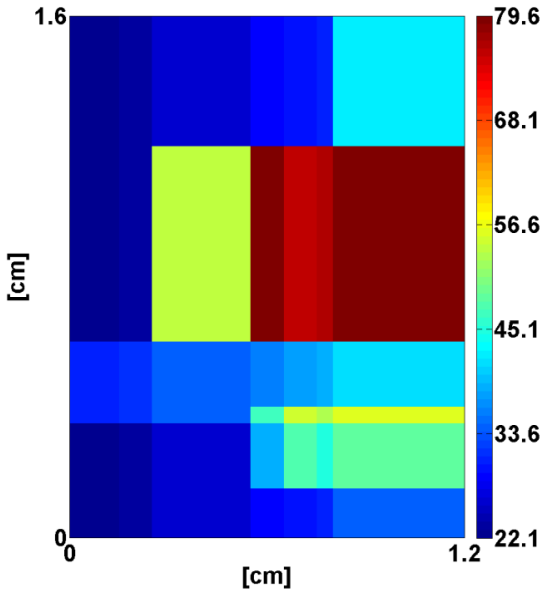
Figure 5 illustrates that, as compared to the base case, hotspot-targeted design reduces $T_{J,max}$ from 79.6℃ to 55.3℃ and $\Delta T_{J,max}$ from 57.5℃ to 31.4℃ - an improvement of 45%.

Following section 2.4, the pressure equalization is achieved by introducing flow throttling zones in the microchannel structure. The throttling zones are positioned towards the coolant outlet and are formed by merging every two channels in each row into a fine microchannel of 30 μm width, i.e. $w^*_{c,i}$ =30 μm and $w^*_{w,i} = 2\left(w_{c,(i,m)} + w_{w,min}\right) - w^*_{c,i}$. Throttling zone lengths L^*_i are obtained using Eq.(16). Figure 6(a) shows the microchannel structure along with flow throttling zones in black color. Figure 6(b) shows the temperature map for the complete design which clearly shows that the additional cooling from the throttling zones does not adversely affect the performance of the hotspot targeted design.

In future work, this design approach will be validated against results from experiments on embedded liquid cooled test chips.

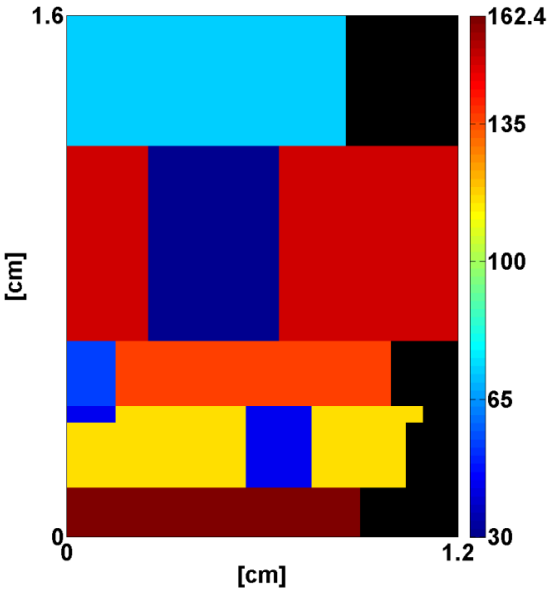


(a)

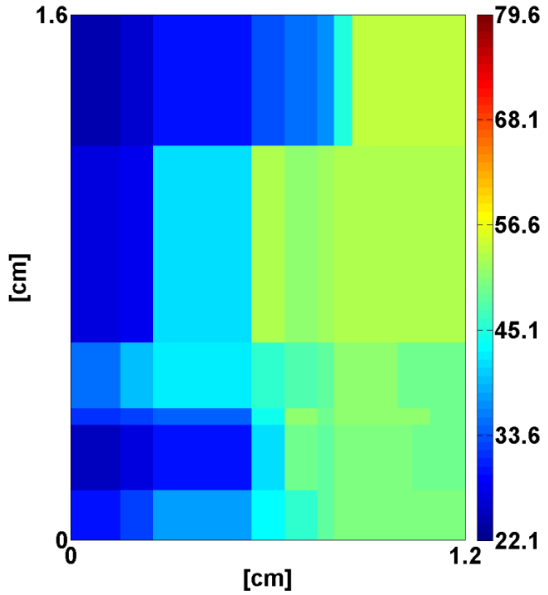


(b)

Figure 5 *Temperature maps* **(a):** *hotspot-targeted design* **(b)** *base case. The same temperature scale for both the figures illustrates reduction in $T_{J,max}$ and $\Delta T_{J,max}$. Coolant flows from left to right.*



(a)



(b)

Figure 6(a): *Throttling zones towards coolant outlet* (*compare with* **Fig. 4**) **(b)** *Temperature map for the design shown in* **Fig.6(a)** (*compare with* **Fig. 5(a)**)

4. Conclusions

A 1-dimensional model for quick design of a single-phase, liquid cooled, hotspot-targeted microchannel heat sink has been presented. The model is a generalized design method for developed and developing flow situations encountered in TMC and MMC heat sinks respectively, for arbitrary chip power maps for serial and multicore microprocessors and for conventional as well as embedded cooling. The potential of the model has been demonstrated for a non-uniform chip power map cooled by an embedded TMC structure.

Nomenclature

A_i^*	cross-sectional area of each parallel flow path in the throttling zone (m^2)
D	equivalent cross-sectional length scale (m)
$\dot{m}$	total coolant flow (kg/s)
h_c	microchannel height (m)
i, j, k	indices
L_i^*	length of throttling zone in i^{th} row (m)
n, m	number of rows and columns in the discretized power map
N_i^*	number of parallel flow paths in throttling zone
Nu_D	Nusselt number defined for D
$Q''_{i,j}$	heat flux in the $(i,j)^{th}$ cell (W/m^2)
ΔP	pressure drop (Pa)
R_λ	conduction resistance (m^2K/W)
R_α	convection resistance (m^2K/W)
T_J	junction temperature (K)
T_f	coolant temperature (K)
w_c	microchannel width (m)
w_w	microchannel wall width (m)
Δz_l	thickness of l^{th} layer (m)
α	heat transfer coefficient (W/m^2K)
φ_i	fraction of $\dot{m}$ directed into the i^{th} row
γ	fin efficiency
λ_f, λ_w	fluid and solid thermal conductivities in heat sink (W/mK)
λ_l	thermal conductivity of l^{th} layer in heat transfer path from junctions to microchannel base (W/mK)

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