

## Performance analysis of ultrathin junctionless double gate vertical MOSFETs

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### Article Info

#### Article history:

Received Mar 29, 2019

Revised May 24, 2019

Accepted May 30, 2019

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#### Keywords:

Channel length

$I_{ON}/I_{OFF}$  ratio

Off-state current

On-state current

Subthreshold slope

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### ABSTRACT

The main challenge in MOSFET minituarization is to form an ultra-shallow source/drain (S/D) junction with high doping concentration gradient, which requires an intricate S/D and channel engineering. Junctionless MOSFET configuration is an alternative solution for this issue as the junction and doping gradients is totally eliminated. A process simulation has been developed to investigate the impact of junctionless configuration on the double-gate vertical MOSFET. The result proves that the performance of junctionless double-gate vertical MOSFETs (JLDGVM) are superior to the conventional junctioned double-gate vertical MOSFETs (JDGVM). The results reveal that the drain current ( $I_D$ ) of the n-JLVDGM and p-JLVDGM could be tremendously enhanced by 57% and 60% respectively as the junctionless configuration was applied to the double-gate vertical MOSFET. In addition, junctionless devices also exhibit larger  $I_{ON}/I_{OFF}$  ratio and smaller subthreshold slope compared to the junction devices, implying that the junctionless devices have better power consumption and faster switching capability.

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## 1. INTRODUCTION

Aggressive scaling of conventional MOSFET leads to several short channel effect (SCE) as the channel length ( $L_{ch}$ ) is reduced. Multiple MOSFETs architectures have been introduced [1-5] to realize the Moore's law prediction in producing ultra-small transistors while maintaining excellent electrical performance. As the transistor size is continuously scaled down, the formation of extremely intricate junctions between source/drain and channel regions offers a real challenge to chip designers. But still, an ultrathin and narrow body configuration is believed to be a significant alternative for extreme MOSFET scaling. The double-gate vertical MOSFET is one the MOSFET configurations that offers the maximum control of the electrostatic field in the channel region by the two side gates. The reduction of  $L_{ch}$  and pillar (body) thickness could further improve the controllability of both gates upon the electrostatic potential in the ultrathin channel [6]. As a result, the channel experiences lesser electrical interference between the source and drain region that subsequently leads to the improvement of on-state current ( $I_{ON}$ ), leakage current ( $I_{OFF}$ ) and subthreshold slope (SS). The double-gate vertical MOSFET, though having better immunity to SCE, are yet far from perfect and encounter similar challenges like conventional bulk MOSFET. For instance, the requirement of new doping approaches, advanced source/drain and channel engineering are required to form ultrashallow source/drain (S/D) junctions with high doping gradient [7].

Recently, a lot of junctionless [8-13] MOSFET configurations have been proposed to eliminate the adversity arisen from ultrashallow junction formation. The key feature of junctionless MOSFET configuration is to eliminate the presence of junction between the source/drain and channel region where both regions are doped with the same polarity dopant, either n-type or p-type material. The junctionless configuration absolutely neglects the adversity of having high doping gradient, hence considerably diminishing the complicated fabrication process. Therefore, the working principle of junctionless transistors is based on depletion-mode and it heavily relies on the geometrical design, process parameters and work function (WF) engineering.

Numerous research groups are working on studying, analyzing and optimizing multiple types of junctionless transistor in order to improve the electrical performances as well as the fabrication cost. Colinge *et al.* (2009) [14] are the first researcher groups that discovered and studied the fundamental and physical properties in junctionless transistor. They found that the N+ and P+ silicon-on-insulator (SOI) based nanoribbon are less sensitive to thermal budget issue than conventional MOSFET since they contained no junction and no doping gradients [15]. The simple process fabrication with excellent subthreshold slope and drain induced barrier lowering (DIBL) are the main advantages of the junctionless device. Akram *et al.* (2014) [16] have investigated the impact of multiple parameter variations on the device characteristics in 20 nm p-type double-gate junctionless tunnel field transistor (p-DGJLTFET). It is observed that the optimized parameters along with the utilization of high-*k* dielectric material (TiO<sub>2</sub>) of 20 nm gate length yields excellent device characteristics with I<sub>ON</sub>~0.3 mA/μm, a low I<sub>OFF</sub> of ~30 fA/μm, a high I<sub>ON</sub>/I<sub>OFF</sub> ratio of ~1x10<sup>10</sup>, a subthreshold slope (SS) point of ~49 mV/decade at a supply voltage of -1 V and at room temperature. Lakshmi and Srinivasan (2015) [6] have studied the influence of process variations on unity cut-off frequency (f<sub>t</sub>) in both conventional and junctionless gate-all-around (GAA) transistors via TCAD simulation. The results show that the f<sub>t</sub> was more sensitive to gate length and S/D doping, less sensitive to gate oxide thickness, ovality and channel doping and least sensitive to gate work function (WF) variations. Riyadi *et al.* (2016) [17] have investigated the impact of gate material and process on subthreshold performance of junctionless FET (JLFET), by comparing four sets of gate material and process techniques. Based on the results, it was observed that the V<sub>TH</sub> value for all JLFET types heavily depended on the channel doping concentration as well as the WF. The SS value for JLFETs was generally lower than SOI based device, with the slope which was closed to ideal value of 60mV/decade. This is mainly due to the bulk transport mechanism in which the conducting channel is fully occupied by the majority carriers, in contrast to the surface conduction experienced in conventional MOSFET and SOI FET.

Archana *et al.* (2017) [18] have derived the analytical modeling of junctionless surrounding gate MOSFET based on existing model. Based on the derived model, multiple characteristics and behavior of the device such as surface potential, V<sub>TH</sub>, SS were plotted against channel length, radius and doping concentration. The result revealed that the V<sub>TH</sub> rolls off as the channel doping concentration was increased. In addition, the variation of V<sub>TH</sub> and SS were explicitly noticed when the channel length was scaled down below 20 nm. This clearly indicates that the junctionless device is significantly related to process and geometrical parameters as it shrinks into nano scale regime. The study of structural and geometrical variability on the performance junctionless transistors have also been conducted recently by khorramrouz *et al.* (2018) and Ambika and Srinivasan *et al.* (2018) [19, 20]. Based on their observation, the structural and geometrical parameters such as thickness of silicon, thickness of insulator, channel length and etc. did contribute significant changes in the electrostatic and analog performance of the devices. Carrillo-Nunez *et al.* (2018) in their report [21] have investigated the effect of channel length variation on the junctionless silicon nanowire transistor. Based on the results, the reduction of the channel length slightly deteriorated the device performance in term of on-state and off-state current due to weakened electrostatic control. The variation of structural and geometrical parameters does not only affect the DC performance but also defining the RF characteristics of the junctionless device [22-25]. Based on the aforementioned literatures, junctionless configuration is definitely one of the alternative device configurations that allow the continuity of transistor scaling with minimal degradation of electrical performances. Several focal research areas can be drawn from the previous literatures such as the impact of geometrical design, process variations and high-*k*/metal-gate application on the transistor performance [26-30]. This paper will focus on the performance analysis of ultrathin Junctionless Double Gate Vertical MOSFETs (JLDGVM) by comparing their electrical characteristics with the Junctioned Double Gate Vertical MOSFETs (JDGVM).

## 2. METHODOLOGY

This section will describe about numerical models used to attain simulation solutions via Silvaco TCAD tools. Then, the 2D process simulation for ultra-thin JLDGVMs is conducted via Athena module as the process flow of the device is presented in Figure 1. The process simulation consists of the ultrathin

pillar formation, the high- $k$  metal-gate (HKMG) deposition, source/drain implantation and metallization. The device simulation is finally employed via Atlas module in order to extract the  $I_D$ - $V_G$  characteristics.

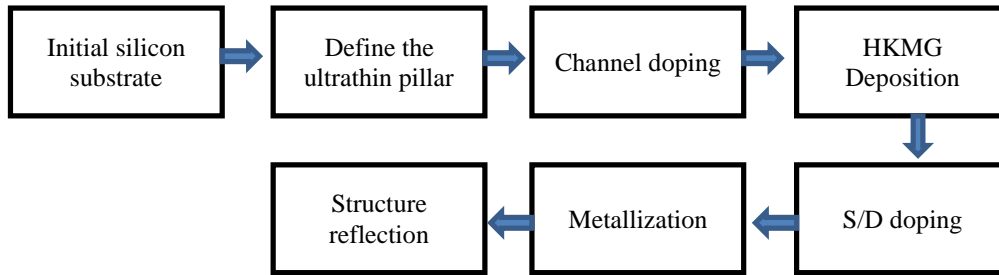


Figure 1. Simulated process flow for ultrathin JLDGVM design

### 2.1. Numerical models

The transport model is based on drift-diffusion model since it is suitable for designing the device with low power density specification. The drift-diffusion model is basically employed for carrier transport in semiconductors and is defined by the basic semiconductor equations. Current density for electrons and hole is given by (1) and (2):

$$J_n = -qn\mu_n \nabla \psi_n + qD_n \nabla n \quad (1)$$

$$J_p = -qp\mu_p \nabla \psi_p + qD_p \nabla p \quad (2)$$

The  $\mu_n$  and  $\mu_p$  stand for the electron and hole mobilities, where as  $\psi_n$  and  $\psi_p$  stand for the electron and hole quasi-Fermi potentials respectively. The  $q$  and  $D$  are used to indicate the absolute value of the electronic charge and diffusion coefficient correspondingly. The three main equations for carrier transport in the semiconductor devices are known as Poisson equation, the electron and hole continuity equations. The poisson equation is denoted as:

$$-\nabla^2 \psi = \frac{q}{\epsilon} (N_D - n + p - N_A) + \rho_{trap} \quad (3)$$

where  $\epsilon$  is the electrical permittivity,  $n$  and  $p$  are the electron and hole densities,  $N_D$  is the donor ion concentration,  $N_A$  is the acceptor ion concentration, and  $\rho_{trap}$  the charge density contributed by traps and fixed charges. Continuity equations for electron and hole are denoted as:

$$\nabla \cdot J_n = qR + q \frac{\partial n}{\partial t} \quad (4)$$

$$\nabla \cdot J_p = qR + q \frac{\partial p}{\partial t} \quad (5)$$

where  $R$  represents the net recombination rate for electrons and holes. Modeling the carrier mobilities of the JLDGVM are subjected to surface scattering extreme carrier-carrier scattering, and quantum mechanical size quantization effects. These effects need to be taken into account in order to execute the device simulation. Lombardi CVT model is opted to be employed in ATLAS module for accurate simulation of non-planar MOSFET like JLDGVM. In this model, the mobility parts consist of the transverse field, doping dependent and temperature dependent which are given by three combined components as follows:

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \quad (6)$$

where  $\mu_{AC}$ ,  $\mu_b$  and  $\mu_{sr}$  are the surface mobility limited by scattering with acoustic phonons, mobility limited by scattering the optical intervalley phonons and mobility limited by surface roughness respectively. The surface mobility of electron and hole are formulated by:

$$\mu_{AC,n} = \frac{BN.CVT}{E_{\perp}^{EN.CVT}} + \frac{CN.CVT.N^{TAUN.CVT}}{T_L E_{\perp}^{DN.CVT}} \quad (7)$$

$$\mu_{AC,p} = \frac{BP.CVT}{E_{\perp}^{EP.CVT}} + \frac{CN.CVT.N^{TAUN.CVT}}{T_L E_{\perp}^{DP.CVT}} \quad (8)$$

where BN.CVT, CN.CVT, DN.CVT, EN.CVT, TAUN are the default electron mobility parameters and BP.CVT, CP.CVT, DP.CVT, EP.CVT, TAUP are the default hole mobility parameters, which are preset by the Silvaco Atlas. The symbol  $T_L$ ,  $E_{\perp}$  and  $N$  stand for the temperature, perpendicular component of electric field and total doping concentration, respectively.

The mobility model is combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes models. This recombination model is opted in order to take the phonon transitions effect into account due to the presence of a trap (or defect) within the forbidden gap of the devices. The numerical model of SRH recombination is shown as follows:

$$R_{SRH} = \frac{pn - n_{ie}^2}{TAUPO \left[ n + n_{ie} \exp\left(\frac{ETRAP}{KT_L}\right) \right] + TAUNO \left[ p + n_{ie} \exp\left(\frac{ETRAP}{KT_L}\right) \right]} \quad (9)$$

where ETRAP,  $T_L$ ,  $n_{ie}$ , are the difference between trap energy level and the intrinsic Fermi level, intrinsic carrier concentration and lattice temperature in Kelvin, respectively. Meanwhile, TAUNO and TAUPO are the electron and hole lifetimes which are user definable in the material statement in Atlas module. This model will be activated as the SRH parameter of the model statements are defined in Atlas module.

## 2.2. Device simulation

The schematic structure of JLDGVM and JDGVM are illustrated in Figure 2. The structures of these devices are based on the ultrathin silicon pillar/body in order to operate in fully depleted mode. Both devices are designed based on the similar geometrical parameters in which the channel length ( $L_{ch}$ ), pillar thickness ( $L_p$ ) and hafnium dioxide ( $HfO_2$ ) thickness are set to 11 nm, 9 nm and 3 nm respectively. All the detailed geometrical and process parameters utilized for both devices are summarized in Table 1. In term of process parameters, the silicon substrate of n-channel JLDGVM is heavily doped with concentration of  $1 \times 10^{18} \text{ cm}^{-3}$  of n-type dopant (Arsenic). On the other hand, the silicon substrate is heavily doped with the concentration of  $1 \times 10^{18} \text{ cm}^{-3}$  of p-type dopant (boron) for p-channel JLDGVM. In contrast, JDGVM design utilizes the opposite dopant type where the silicon substrate is doped with the concentration of  $1 \times 10^{14} \text{ cm}^{-3}$  of p-type dopant (boron) for n-channel device and with the concentration of  $1 \times 10^{14} \text{ cm}^{-3}$  of n-type dopant (arsenic) for p-channel device. This is because the working principle of n-channel JDGVM and p-channel JDGVM are based on N-P-N (Inversion-mode) and P-N-P (Accumulation-mode) respectively.

Table 1. Parameters used in the simulated devices

Parameter	Units	JLDGVM		JDGVM	
		n-type	p-type	n-type	p-type
Channel Length, $L_{ch}$	nm	11	11	11	11
Pillar Thickness, $L_p$	nm	9	9	9	9
High- $k$ material thickness, $T_{high-k}$	nm	3	3	3	3
Channel doping, $N_{ch}$	$\text{cm}^{-3}$	1.0E18	1.0E18	1.0E14	1.0E14
S/D doping, $N_{sd}$	$\text{cm}^{-3}$	1.0E18	1.0E20	1.0E18	1.0E14
Metal work-function, WF	eV	4.5	4.7	4.5	4.7

The source and drain regions of the JLDGVM are heavily doped with the same type of dopant used in the channel region where  $1 \times 10^{18} \text{ cm}^{-3}$  concentration of n-type dopant (Arsenic) and  $1 \times 10^{20} \text{ cm}^{-3}$

concentration of p-type dopant (boron) are implanted for n-channel JLDGVM and p-channel JLDGVM, respectively. This is important in order to form the junctionless configurations that require an  $N^+-N^+-N^+$  (n-channel) and a  $P^+-P^+-P^+$  (p-channel) doped structure for the source, channel and drain region. The S/D doping for JDGVM is in contrast with the JLDGVM where  $1 \times 10^{18} \text{ cm}^{-3}$  concentration of n-type dopant (Arsenic) and  $1 \times 10^{14} \text{ cm}^{-3}$  concentration of p-type dopant (boron) are employed for n channel JDGVM and p channel JDGVM, accordingly. The physical high- $k$  dielectric thickness ( $T_{\text{high-}k}$ ) of 3 nm is considered for both JLDGVM and JDGVM devices in order to keep the equivalent oxide thickness (EOT) intact. The  $\text{HfO}_2$  is a dielectric material applied for both devices as it has permittivity 4–6 times higher than that of silicon dioxide.

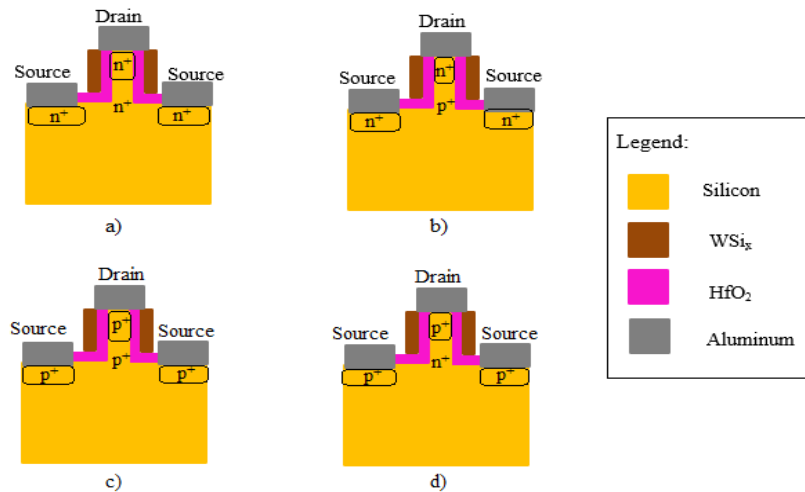


Figure 2. 2D structure of double-gate vertical MOSFETs, (a) n-JLDGVM (Junctionless), (b) n-JDGVM (Inversion-mode), (c) p-JLDGVM (Junctionless), (d) p-JDGVM (Accumulation mode)

Having a larger dielectric constant would enable thicker insulator to be used for leakage reduction while retaining fast reaction of the device. The presence of two metal gates (tungsten silicide) that wrap the ultrathin pillar would help in producing an accelerating force to drive the charge carrier into the channel, thus improving the on-current ( $I_{\text{ON}}$ ) as well as suppressing the SCE. For both type of devices, the metal work functions of n-type and p-type device are taken as  $\text{WF}=4.5 \text{ eV}$  and  $\text{WF}=4.7 \text{ eV}$ , respectively. The doping profile across the JLDGVM device is shown in Figure 3 where the net doping for silicon, hafnium dioxide, tungsten silicide and aluminum has been clearly displayed.

The ATLAS module provides specific characteristics such as the  $I_{\text{D}}-V_{\text{G}}$  curve that enable the extraction of critical device characteristics such as threshold voltage ( $V_{\text{TH}}$ ), drive current ( $I_{\text{ON}}$ ), off-leakage current ( $I_{\text{OFF}}$ ),  $I_{\text{ON}}/I_{\text{OFF}}$  ratio and subthreshold slope (SS). The device simulation condition [31] as shown in Table 2 is used to generate  $I_{\text{D}}-V_{\text{G}}$  transfer characteristics for DC characteristics extraction. All the investigated characteristics are extracted and computed from the generated  $I_{\text{D}}-V_{\text{G}}$  transfer characteristics. In the next section, the simulation results for JLDGVM and JDGVM devices were then analyzed, compared and further discussed.

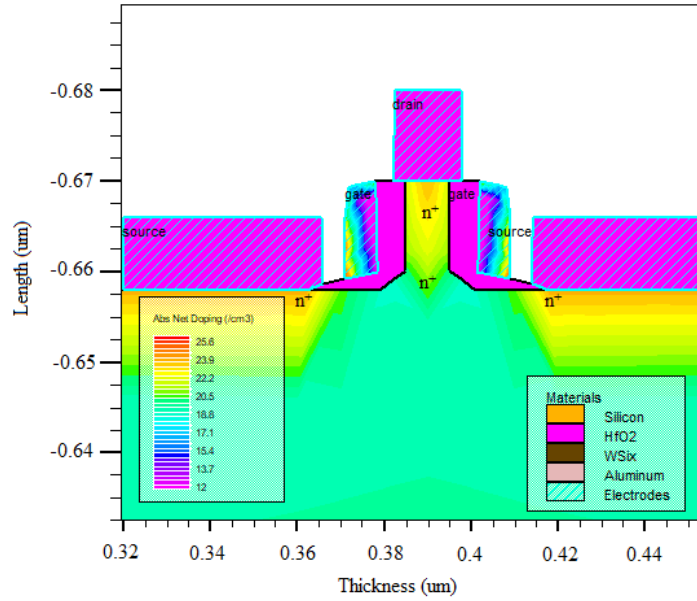


Figure 3. Contour Mode of n-JLDGVM layout

Table 2. Device simulation condition

Electrical Characteristics	Drain Voltage, $V_D$ (V)	Gate Voltage, $V_G$ (V)		
		$V_{Initial}$	$V_{Step}$	$V_{Final}$
Threshold Voltage ( $V_{TH}$ )	1.0	0	0.1	2.0
On-state Current ( $I_{ON}$ )	1.0	0	0.1	2.0
Off-state Current ( $I_{OFF}$ )	1.0	0	0.1	2.0
Subthreshold Slope (SS)	1.0	0	0.1	2.0

### 3. RESULTS AND ANALYSIS

In this section, all the simulation results and its discussion are briefly described for both JLDGVM and JDGVM devices. In order to study and analyze the performance of JLDGVM and JDGVM devices, the  $V_{TH}$  values of both devices were tuned at 0.25 V. In other words, all the investigated characteristics were normalized to the fixed  $V_{TH}$  value for unbiased performance evaluation. The variation of  $I_D$ - $V_G$  transfer characteristics of both JLDGVM and JDGVM devices, shifting the curves to the positive x-axis for n-channel and to the negative x-axis for p-channel is depicted in Figure 4.

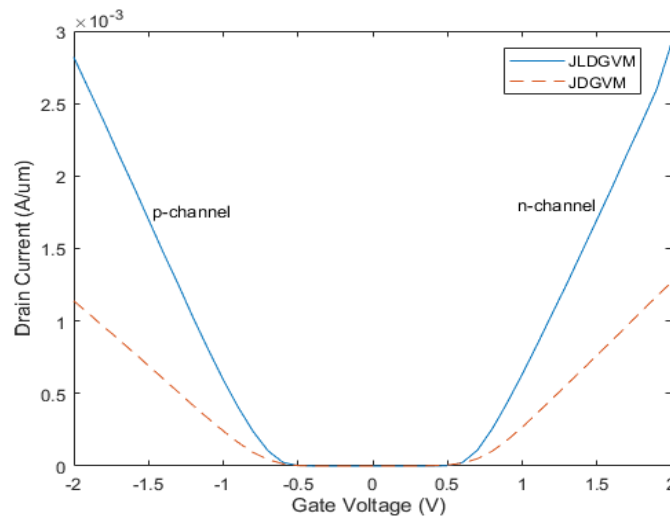


Figure 4.  $I_D$ - $V_G$  transfer characteristics of both JLDGVM and JDGVM

Based on the graph, it is clearly shown that the  $I_D$  of both n- and p-channel JLDGVM were significantly larger than JDGVM. The  $I_D$  of the n-JLDGVM and p-JLDGVM could be tremendously enhanced by 57% and 60% respectively as the junctionless configuration was applied to the double-gate vertical MOSFET. Such occurrence is majorly due to the electric field perpendicular to the flow of current in the junctionless configuration is significantly less than in the junctioned configuration. In junctioned configuration, the carriers propagating from source to drain experience much higher phonon scattering due to high electric field which subsequently lead to mobility degradation. Since the electrons/holes mobility in the channel region is significantly associated with this electric field, a much lower electric field featured in the JLDGVM could contribute a significant rise in drain current which is desirable for nanometer-scale complementary metal-oxide semiconductor applications.

Figure 5 depicts the semilog  $I_D$ - $V_G$  transfer characteristics for both JLDGVM and JDGVM. The value of  $I_{ON}$ ,  $I_{OFF}$  and SS of both devices can be extracted from the graph. It is shown that the  $I_{ON}$  magnitudes for the n- and p-channel JLDGVMs are approximately 50% higher than the JDGVMs. The majority carriers in the JDGVM's channel are heavily scattered due high electric field, whereas, the JLDGVMs experience much lower electric field that significantly increases the electrons/holes volume in the channel, subsequently leading to higher  $I_{ON}$ . In term of off-current ( $I_{OFF}$ ), the n- and p-channel JLDGVMs exhibit approximately 20% and 75% smaller  $I_{OFF}$  than the JDGVMs. This implies the presence of junction in JDGVMs did cause larger effect of band-to-band-tunneling, leading to a significant leakage in the OFF state condition.

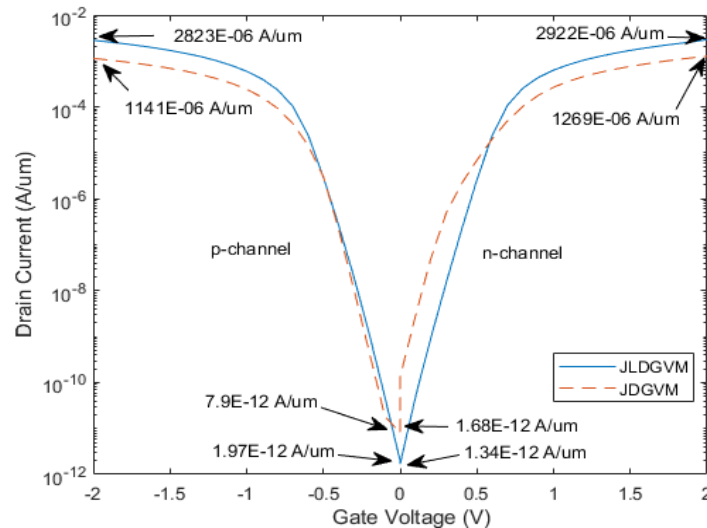


Figure 5. Semilog  $I_D$ - $V_G$  transfer characteristics of both JLDGVM and JDGVM

The  $I_{ON}/I_{OFF}$  ratio is an important figure of merit for having high performance (more  $I_{ON}$ ) and low leakage (less  $I_{OFF}$ ) for the CMOS transistors. Figure 6 depicts the bar graph, indicating the level of  $I_{ON}/I_{OFF}$  ratio between JLDGVM and JDGVM for both types of channel.

Based on the bar graph, the n-channel and p-channel JLDGVM devices exhibit approximately 44% and 90% higher  $I_{ON}/I_{OFF}$  ratio over the n-channel and p-channel JDGVM devices respectively. This implies that the JLDGVM devices feature a better power consumption than the JDGVM devices as the devices could switch instantly from 'OFF' to 'ON' or vice versa at a minimum rate of required gate voltage. The increasing rate of drain current below the threshold limit is defined by a characteristic called the subthreshold slope (SS), which is mathematically derived from the semilog  $I_D$ - $V_G$  transfer characteristics as:

$$SS = -\frac{dV_G}{d(\log(I_D))} \quad (10)$$

where the logarithm is in base 10,  $V_G$  is the gate voltage and  $I_D$  is the drain current. Figure 7 shows the bar graph, indicating the SS values between JLDGVM and JDGVM for both types of channel.

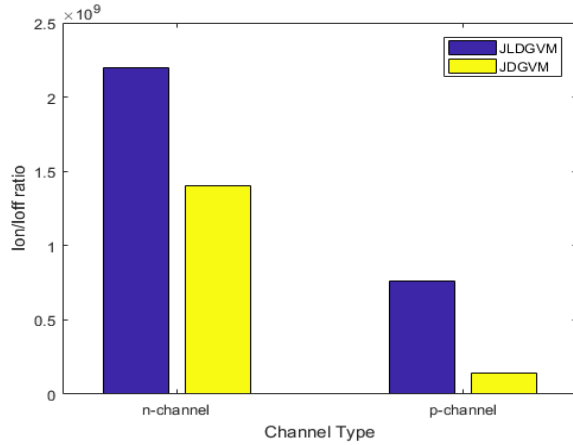


Figure 6. Bar Graph of the  $I_{ON}/I_{OFF}$  ratio for JLDGVM and JDGVM devices

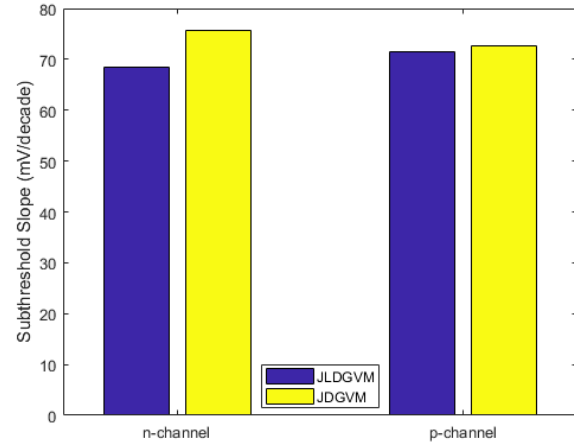


Figure 7. Bar Graph of the  $I_{ON}/I_{OFF}$  ratio for JLDGVM and JDGVM devices

The SS magnitude is commonly monitored to determine the scalability limit of the device in which the changing rate of required gate voltage to increase the drain current by one decade is measured. Based on Figure 7, the n-channel and p-channel JLDGVM devices exhibit approximately 9.8% and 1.5% lower SS value than the n-channel and p-channel JDGVM devices respectively. The smaller SS indicates that the device has lower power consumption as it only requires minimum changes in  $V_G$  to increase one decade of  $I_D$ . Hence, the device with smaller SS (JLDGVM) would reach saturation mode much faster than the device with larger SS (JDGVM). For instance, the SS value for n-channel JLDGVM is 68.4 mV/decade, implying that a 68.4 mV increase of  $V_G$  would contribute approximately a tenfold increase in the  $I_D$  as shown in Figure 5. Therefore, in order to switch the current from its off-state ( $1.34E-12$  A/ $\mu$ m) to the on state ( $I_D=7.9E-9$  A/ $\mu$ m at threshold), a swing in  $V_G$  of

$$68.4mV \times \log \frac{7.9E-9A}{1.34E-12A} = 0.258V$$

is required. Similar to n-channel JDGVM, the SS value is measured at 75.8 mV/decade, thereby switching the current from its off-state ( $1.68E-12$  A/ $\mu$ m) to the on state ( $I_D=2.7 E-7$  A/ $\mu$ m at threshold) requires a swing in  $V_G$  of

$$75.8mV \times \log \frac{2.7E-7A}{1.68E-12A} = 0.395V$$

is required. This implies that the n-channel JLDGVM can be turned on from its off-state much faster than the n-channel JDGVM.

In practice, the gate control over the channel region might not be perfect due to electrostatic coupling between the gate and the ultrathin channel. This issue is mainly aroused due to the geometry-related process parameters such as channel length ( $L_{ch}$ ) and pillar thickness ( $T_p$ ), which, on the other hand, significantly deteriorate the performance of JLDGVMs. Since controlling process variations become the crucial factor in deciding the JLDGVM's performances, several optimization approaches [32-34] can be conveniently employed for further improvement.

#### 4. CONCLUSION

In summary, the DC behaviours and performances of junctionless double-gate vertical MOSFETs (JLDGVMs) are compared with the junction double-gate vertical MOSFETs (JDGVMs). The performance evaluation of JLDGVMs and JDGVMs are made in terms of on-state current, off-state current,  $I_{ON}/I_{OFF}$  ratio and subthreshold slope. Junctionless devices are observed to experience less short-channel effects than the junction devices. Comparison of  $I_D$ - $V_G$  transfer characteristics are made between junctionless devices and junction devices, and the benefits of bulk transport in junctionless devices are clearly portrayed via the tremendous improvement of the drain current as the gate voltage is increased. Junctionless devices also have larger  $I_{ON}/I_{OFF}$  ratio and smaller subthreshold slope compared to the junction devices, implying that



the junctionless devices have better power consumption and faster switching capability. For future work, the impact of process parameters towards AC behavior of the JLDGVMs will be further investigated. In addition, optimization approaches could be deployed for further enhancing the device performances.

#### ACKNOWLEDGEMENTS

The authors would like to thank to the Ministry of Higher Education (MOHE) for sponsoring this work under project (FRGS/1/2017/TK04/FKEKK-CeTRI/F00335) and MiNE, CeTRI, Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for the moral support throughout the project.

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