

## Simulation study of single event effects sensitivity on commercial power MOSFET with single heavy ion radiation

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### ABSTRACT

High-frequency semiconductor devices are key components for advanced power electronic system that require fast switching speed. Power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the most famous electronic device that are used in much power electronic system. However, the application such as space borne, military and communication system needs Power MOSFET to withstand in radiation environments. This is very challenging for the engineer to develop a device that continuously operated without changing its electrical behavior due to radiation. Therefore, the main objective of this study is to investigate the Single Event Effect (SEE) sensitivity by using Heavy Ion Radiation on the commercial Power MOSFET. A simulation study using Sentaurus Synopsys TCAD software for process simulation and device simulation was done. The simulation results reveal that single heavy ion radiation has affected the device structure and fluctuate the I-V characteristic of commercial Power MOSFET.

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## 1. INTRODUCTION

The development of advanced technology in power electronic application nowadays has influenced the electronic devices to be updated. Power electronic application such as space borne system, remotely operated underwater vehicle (ROV) and the military system can be categorized as harsh environment applications. The implementation of power electronic application in this critical environment has exposed the electronic device with radiation pollution and it can seriously compromise the mission. Therefore, in order to withstand in harsh environment application, it is compulsory for electronic devices to be reliable with radiation environment. Predominantly, Power MOSFET was the most well-known electronic devices used in many power electronic application in this century. The ability to withstand at high frequency and fast switching speed application has made the Power MOSFET the most selected electronic device among other devices. At the beginning of the 1980s, the first generation of Power MOSFET was explored and introduced with several structures [1, 2]. However, most of them have been deserted in favor of the Vertical Diffused MOS (VDMOS) structure (also called Double-Diffused MOS or simply DMOS). Basically, the structure of Power MOSFET is different from lateral MOSFET because most of power devices structure is vertical and not planar. With a vertical structure, the doping and thickness of the N epitaxial layer determine the voltage rating of the transistor, while the channel width will determine the current rating. This makes this device practicable to be installed in both high blocking voltage and high current within a compact piece of silicon [3]. Hence, due to this advantages, most of the vertical MOSFET was designed for switching applications and they are used in both on-state and off-states [4-10].

However, the implementation of Power MOSFET under continuous radiation and high temperature will reduce device performance. Generally, the radiation effect can be classified into two major problem which depends on the time of exposure and the level of radiation energy. Firstly, it will create permanent damage to the device called as Total Ionizing Dose (TID). TID effects are cumulative degradation of devices due to hole trapping in gate oxide and isolation oxide, which changes the threshold voltages and increases leakage current of the device. Secondly, Single Event Effect (SEE) which happens instantaneously if the amount of radiation energy is enough to make device broke. SEE effects are due to a single ion strike, further classified into two major catastrophes which are Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR). SEB effect results in the drain to source shortening and SEGR effect damage the gate oxide dielectric. Therefore, there is a necessity to enhance the performance of power MOSFETs in space applications [11-24]. Hence, the motivation of this research work is to study the effect of particle radiation on commercial Power MOSFET by using single heavy ion radiation source.

The remaining part of the paper is organized as follows: Section II will discuss the device structure and simulation description. This section divided into four major part; geometrical consideration, material properties, simulation work setup, and reliability test model setup. Next, Section III will present the simulation result and the discussion. Finally, the paper will be concluded in Section VI.

## 2. DEVICE STRUCTURE AND SIMULATION DESCRIPTION

### 2.1. Geometrical consideration

Power MOSFET manufacturer has begun moving away from the traditional DMOSFET that does not have to reduce electrical field at the gate oxide interface Figure 1 to the Power MOSFET that has reduced electrical field at the gate oxide interface Figure 2. The basic construction of traditional DMOSFET consists of a gate, source and drain wheres the gate contact placed under gate oxide. This will make the device suffering from possible hot carrier injection during long-term blocking operation, in which the drain is placed under a high positive bias. Besides, the high electrical field combined with any imperfection in the interface material and gate oxide could result in a gate oxide failure. The related MOSFET device in Figure 1 illustrates the needs for modification to the transistor design that reduce the electrical field at the gate oxide interface and increase maximum current flow in the on-state with the ability to block incident voltage in reverse biases operation [25].

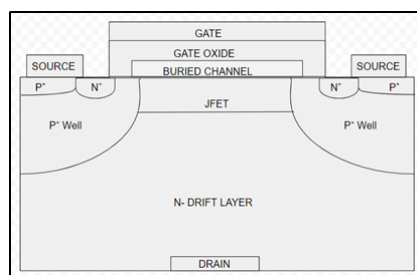


Figure 1. Traditional DMOSFET without reducing the electric field at the gate oxide interface

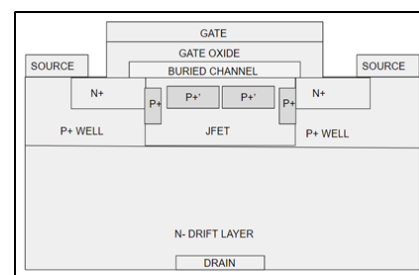


Figure 2. DMOSFET with reducing electric field at the gate oxide interface

The alternative design for the transistor with the implementation of the P+ region within a JFET region in order to reduce electrical field at the gate oxide interface shown in Figure 2. JFET region generally is an active portion of an N-type drift layer which may include an N-type dopant and is located between two P-type wells. In addition, JFET region also may refer to a region in contact with the channel region coming up to the surface of the P-type wells by applying a gate voltage. Moreover, the JFET region makes up the conduction path for the electron with the N+ source region, the channel region, the N-type drift region, the substrate and the drain electrode. Under operation condition at which a high bias is applied to the drain and which the gate is held near ground potential, a high electrical field is created in the gate oxide that placed just above the JFET region [25].

Figure 2 shows a transistor device having reduced electrical field at the gate oxide interface with the enactment of P+ region within a JFET region in order to improve device reliability during long-term blocking operation in which the drain is placed under a high positive bias. Hence, due to the lower gate oxide field, it will minimize the possibility of hot carrier injecting into the gate oxide.

## 2.2. Material properties

Power MOSFETs are important and are used in most of the electronic devices that people use on a daily basis. Analyzing all of the materials used in the creation of a Power MOSFET transistor shows that this seemingly simple but it is actually very complicated and the industry is constantly finding better ways to make it smaller and more efficient. As new technology presents itself, the materials that are used in the MOSFETs are replaced by more efficient ones. Researcher are constantly finding new ways to make it smaller as this equates to most other electronic devices becoming smaller as well. This makes finding exactly what is inside a transistor difficult. The three main components are substrate, gate, and the terminal. Originally, the substrate material is made with silicon crystal doped with other element. Depending on the element the silicon is doped with, the transistor is n-channel or p-channel. In a p-channel transistor, the substrate is silicon crystal doped with boron, and the surrounding material is doped with phosphorus. However, the terminals can be doped with a material that has three valence electrons and the surrounding material can be doped with a material that has five valence electrons as long as it is small enough to fit into the silicon structure. Different elements have been favored over the century based on performance and cost. For the substrate of Power MOSFET, the materials available are silicon, germanium and gallium arsenic. Nevertheless, among these, Silicon is the best material for substrate because it has a wider band gap and high intrinsic resistivity. Besides, silicon also easy to oxidize to form high-quality silicon dioxide and it is a cheap element. Meanwhile, Gallium Arsenic has higher mobility than silicon but it less stable during thermal processing and it contains much higher defect density during the fabricating process. Silicon substrate in surface orientation is used due to its advantage to produce electrically clean oxide interface because has the fewest atom per area. Hence, lower interface state and further leads to lesser charge defects. Therefore, silicon is chosen as a substrate for the fabrication process [26, 27].

Besides, metal polysilicon can also be used as a gate element. Polysilicon chosen because of the capability to form a self-aligned gate. This is the main reason for the cost and time reduction when at step align the gate to the substrate. Moreover, polysilicon is able to withstand at high temperature compared to the metallic gate since polysilicon has a higher resistance to temperature. When metal used as gate materials, gate voltage are largely due to the high work function difference between a metal gate and silicon channel but threshold voltage can still be overcome by the applied gate voltage. As the transistor dimension is scaled down, the applied voltage is also brought down to reduce gate oxide breakdown, hot electron injection and power consumption. A transistor with a high threshold voltage would become non-operational under this condition. Hence, polysilicon becomes the modern gate material because it works function different is close to zero, making threshold voltage lower and ensuring the transistor can be turned on. The best material for contact should be a high conductivity material. The current technologies used aluminum and copper as the contact materials because of their materials properties. Aluminum is selected because it is lighter than copper. Besides, the price for aluminum also cheaper than copper hence the manufacturing cost will be reduced. However, copper has high conductivity than aluminum, around 36% then aluminum but it highly diffused which can cause reliability problem such as electro migration at high temperature [26, 27].

## 2.3. Simulation work

In this paper, Synopsys Technology Computer Aided Design (TCAD) mixed simulation is used to study the effect of radiation on Power MOSFET. First, the process began with Process Simulation basically is a process to design the geometrical of the devices. In TCAD Synopsys, Sentaurus Structure Editor (SDE) tool is used for this process and was connected with Graphical User Interface (GUI) to input process step. Several fabrication techniques available in the industry can be done such as oxidation, deposition, epitaxy, etch and implantation by using this software. Next, creating the mesh process will be continued. Mesh is important because it decides the quantity of calculation node which effect simulation result directly. Mesh can be organized by using command file or GUI with SDE. Third, the created structure will be linked to Sentaurus Device (SDevice) to perform the device simulation. SDevice can read the structure by structure grid file and parameter files. At this time, SDevice can start device simulation based on physic model listed in command. Fourth, the result will be viewed by using Tecplot tools. Tecplot tool is combined with the image of structure patterns in inspect with plotting graph of electrode current and Voltage. Table 1 shows the designing process by using SDE. Design of NMOS and PMOS is identical for example the grown oxide, polysilicon gate, spacer and electrode thickness are the same for both NMOS and PMOS. The different only species of dopant, dose, and energy during implantation in well formation, channel implantation, LDD, and halo implantation and source-drain implantation [28].

After completing the designing process, SDevice tool is used to analyze all the work from Process simulation and this process is called as Device Simulation. First, all the file needs to be set up and read from the previous tool during the operation of SDE and the file name must be in concurrence with the program regulation based on the default value. Second, the physics formula needs to be assigned into the simulation

calculation and mathematical model need to assign accordingly with the default setting of this program. Next, the construction of the diagram to be extracted must be added such as energy band diagram and carrier distribution diagram. Then, the calculation of parameter value by the combination of the aforementioned physics model and mathematical model. In addition, Poisson equation is used to substitute the code of electron and hole, and then eQuantumPotential must be added for correction. Other than that, the Initial Step =  $1e-3$  refers to the first point to be calculated will be  $1e-3$  unit away from threshold voltage else, the voltage pitch will be reduced to continue with the search for the value that can be converged. For this research work, N-Channel Power MOSFET is design by using the software simulation as shown in Figure 2 [28].

Table 1. Process simulation by using Sentaurus Synopsys

Process	Description
Initial Substrate	Silicon with boron/phosphorus concentration used as substrate body.
Well Formation	Well, the region is formed by dopant implantation.
Channel Implantation	Annealing process to repair the implantation damage and activate the implanted dopants. The dopant is implanted again to adjust $V_{th}$ .
Gate Oxidation & Oxide Growing	Grown the oxide layer on the substrate which acts as an insulating layer. Deposited polysilicon on oxide layer to form a gate terminal
Gate Formation & Gate Re-oxidation	Polysilicon oxidized again to growth oxide layer around the gate
Lightly Doped Drain and Pocket Implantation	Lightly doped drain (LDD) and pocket implantation to reduce hot carrier effect and drain induced barrier lowering effect respectively
Spacer Formation	Deposited and pattern nitride to form a spacer layer, where its thickness is corresponding to the gate thickness.
Electrode Contact Formation	Form electrode at the gate, source, and drain by deposit aluminum layer

#### 2.4. Reliability test

In a harsh environment, there are two types of radiation which is particle radiation and photon radiation. For this study, particle radiation is used as radiation source by using single heavy ion radiation model. Radiation happens when a high-energy particles penetrate a semiconductor device, they will generate a trail of electron-hole pairs by depositing their energy. These charges may cause a large enough current to switch and it will effect the I-V characteristic of the device. The important factors that influence the generation of the electron-hole pair are; the energy and type of the ion, the angle of penetration of the ion and lastly the relation between the linear energy transfer (LET) and the number of pairs created [28, 29].

For this research, a physics model for radiation has been setup and will be tested on the Power MOSFET by using Cobalt-60 radiation source with 25 MeV decay energy. A simple model for the heavy ion impinging process is shown in Figure 3 where as  $l$  is the length of the track,  $w$  is the width or radius and  $T(t)$  is the temporal variations of the generation rate. The generation rate caused by heavy ion is computed by (1) [28].

$$G(l, w, t) = G_{LET}(l)R(w, l)T(t) \quad (1)$$

Based on (1),  $G_{LET}(l)$  is the linear energy transfer generation density and its unit is pairs/cm<sup>3</sup>. Linear energy transfer is the amount of energy that an ionizing particle transfers to the material traversed per unit distance. It describes the action of radiation into matter. Next,  $T(t)$  is defined as a Gaussian function as shown in (2) where  $t_o$  is the moment of the heavy ion, and  $S_{hi}$  is the characteristic value of the Gaussian [28].

$$T(t) = \frac{2 \cdot \exp\left[-\left(\frac{t-t_o}{\sqrt{2} \cdot S_{hi}}\right)^2\right]}{\sqrt{2} \cdot S_{hi} \sqrt{\pi} \left(1 + \operatorname{erf}\left(\frac{t_o}{\sqrt{2} \cdot S_{hi}}\right)\right)} \quad (2)$$

$$R(w, l) = \exp\left(-\frac{w}{w_t(l)}\right) \quad (3)$$

Besides that, the spatial distribution  $R(w, l)$  can be defined as an exponential function (default) as shown in (3), where  $w$  is a radius defined as the perpendicular distance from the track. The characteristic distance is defined as  $W_{t,hi}$  in the Heavy Ion statement and can be a function of the length  $l$ . Once a model is developed, all the specification need to put in the software SDevice under physic modeling part [28].

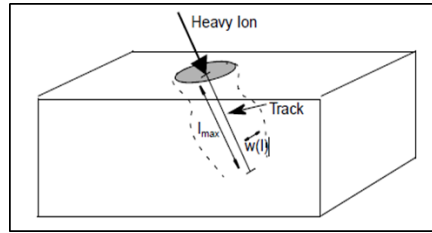


Figure 3. Heavy ion model

### 3. RESULTS AND DISCUSSION

This section discusses about the result from simulation work by using Sentaurus Synopsys software. First part provides the topology of radiation incident on the Power MOSFET device. Next, the explanation of single heavy ion radiation effect on the power MOSFET by using two variable which are; (a) Time-based study (Dose Time) and (b) Linear Energy Transfer (LET) based study (Dose Rate).

#### 3.1. Radiation incident on the power MOSFET device

The implementation of Power MOSFET device in harsh environment application has exposed the device to withstand with various kind of the radiation type. Radiation are divided into two type which are; particle and photons radiation which are generally differentiated based on their mass and energy level. Particle radiation usually give more significant impact to the device because of their high energy level and mass. Radiation incident happened when high-energy particles penetrate a semiconductor device and deposited their energy by producing new electron-hole pairs. Then, the generated electron-hole pair will accumulate and form a channel along the incident track. Figure 4 shows the device with radiation exposure by using a single heavy ion module. As can be seen, the red color area is the area that single heavy ion travel into the device and caused a high saturation of heavy ion charge density which is about  $2.348 \times 10^{18} \text{ cm}^{-3}$ . Meanwhile, the blue color represents the area that has the least heavy ion charge density which is about  $1 \times 10^{-30} \text{ cm}^{-3}$ . Therefore, the area that radiation incident occur has higher generation rate and it caused a high saturation of heavy ion charge density.

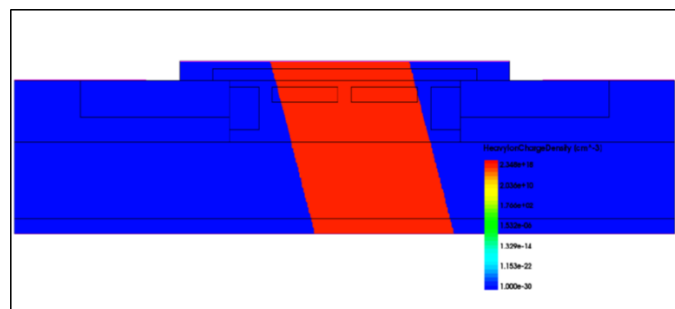


Figure 4. Single heavy ion penetration into devices

#### 3.2. Device structure of power MOSFET

The result in Figure 5(a) show the device structure of the virgin device with normal electric field distribution when 5V bias is applied at the gate terminal. As can be seen, the JFET region and gate oxide have higher electric field when the device is on-state because the electron will form depletion area to transfer the charge from source to the drain. The result of single heavy ion penetration on Power MOSFET structure in this experiment shown in Figure 5(b) with gate bias of 5V. For this condition, the period of heavy ion penetration on the device used is  $1 \times 10^{-3}$  second and 25MeV of LET. As can be seen, the radiation particle has changed the device structure of Power MOSFET by increased the electrical field density especially in the pathway between drain to source. Compared with virgin MOSFET in Figure 5(a), the electric density is slightly higher, and the area of the saturated electrical field is increased drastically near to the drain terminal. Besides, the radiation has merged the high electric field density in the JFET region and gate oxide. The

biggest challenge of Power MOSFET device in harsh environment application is to maintain the electrical characteristic of the device and keep the fully system running.

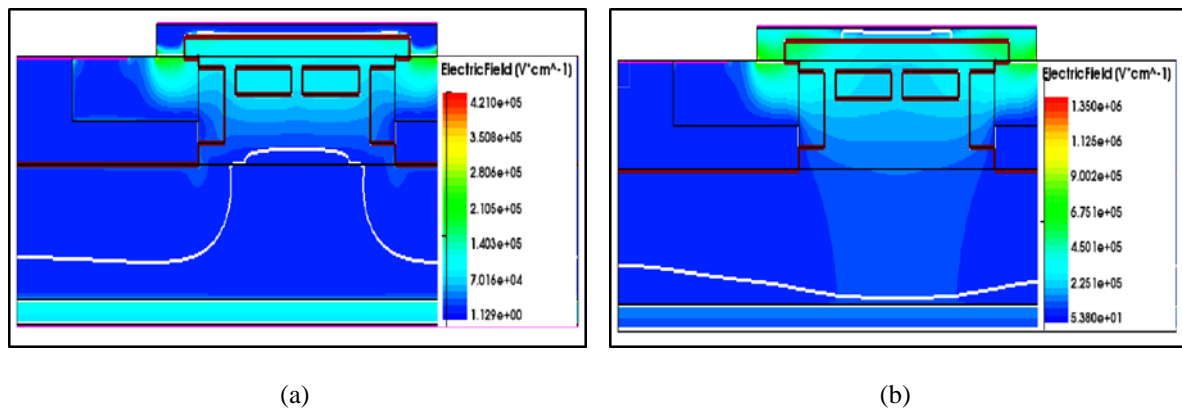


Figure 5. The layout of Power MOSFET after exposed to radiation, (a) Time based study, (b) Linear Energy Transfer (LET) based study

### 3.3. Electrical performance of power MOSFET

For the electrical performance, the graph of  $I_{DS}$  vs  $V_{DS}$  for time-based study and LET study are shown in Figure 6(a) and Figure 6(b) during off-state operation. For the time-based study, the dose level used for the radiation source is 25 MeV and the time of radiation exposure is varied: 0ms, 25 ms, 50ms, 75ms, and 100ms. From the result, a drastic effect of radiation exposure on the value of  $I_{DS}$  vs  $V_{DS}$  can be observed. The blue colored line represents the virgin MOSFET and the other color represent the device with the radiation. From the obtained result, the value of  $I_{DS}$  is somehow shifted from  $1 \times 10^{-14}$  A/cm<sup>2</sup> (Virgin) to more than  $1 \times 10^{-16}$  A/cm<sup>2</sup> after the radiation exposure during off-state region  $V_G=0$  V. This decrement was not good for Power MOSFET because it will affect the device when it in the on-state period wheres gate bias applied. Since, SEE is an instantaneous effect, hence no matter how long the time of radiation penetration onto device it still affected the device performance if the value of radiation energy is enough.

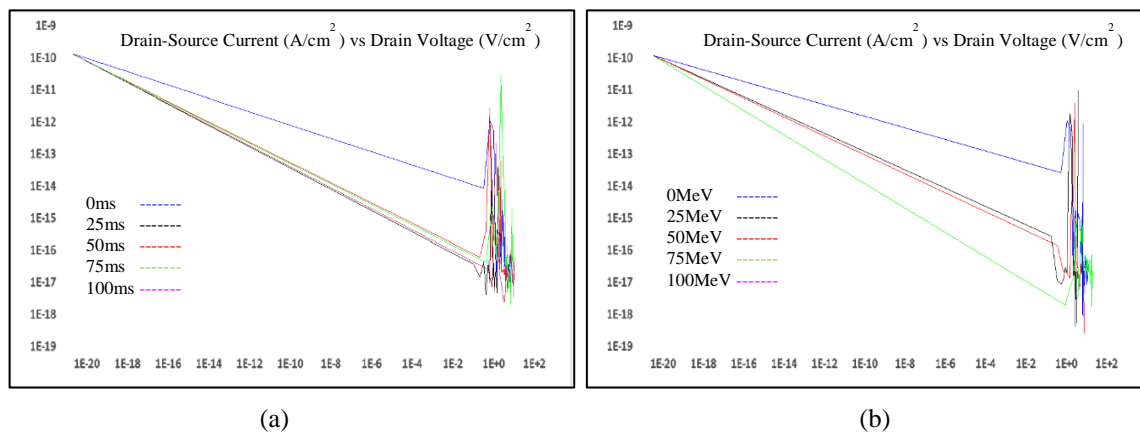


Figure 6. Graph of Drain-Source Current ( $I_{DS}$ ) vs Drain-Source Voltage ( $V_{DS}$ ) with reliability test, (a) Time based study, (b) Linear Energy Transfer (LET) based study

Moreover, Figure 6(b) shows the effect of heavy ion radiation on the device by using the LET-based study. As the previous experiment, blue color represents the virgin device and other colors represent the device that been penetrated to the appropriate value of LET. From the obtained result, there was a significant effect on the value of  $I_{DS}$  vs  $V_{DS}$  between each of device sample. As the value of LET is increased the value of  $I_{DS}$  will decrease during the off-state region  $V_G=0$  V. For this experiment, the analysis of electrical performance taken during off-state region because the research work target is to do the Single event burnout

(SEB) test to the power device. SEB is the device degradation phenomena that happened during off-state region where the value of  $I_{DS}$  is shifted gradually after radiation. As conclusion, the heavy ion radiation has localized the SEB failure mechanism in Power Device structure and the electrical performance of the device.

#### 4. CONCLUSION

This paper reveals the effect of single heavy ion radiation on the Power MOSFET using software simulation. First, the research begins with the designing process parallel with GUI by using process simulation Sentaurus Structure Editor (SDE) to design the commercial Power MOSFET. Then, the research continued with the device simulation to study the effect of radiation before and after radiation exposure by using Sentaurus Device Simulation (service). Following that, Tecplot tool was used to present the device layout and I-V characteristic. From the study, the radiation exposure toward electronic device will lead the device to malfunction. From the time-based study, it shows that even though the time for radiation penetration on the device is short (microsecond) but it still will give a great impact to the device itself. Besides, for LET-based study, the change of I-V characteristics is depends on the value of LET. The higher the LET, the higher the shifting in  $I_{DS}$  and more impact to the device performance. Therefore, investigation of the Single Event Effect (SEE) sensitivity by using Heavy Ion Radiation on the Power MOSFET has provide some useful knowledge about the device.

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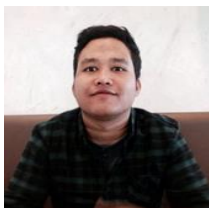
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