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Low insertion loss of surface mount device low pass filter at 700 MHz

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ABSTRACT

The paper involved with the design, simulation and fabrication of 6th order elliptical-based Surface Mount Device (SMD) LPF with cutoff frequency at 700 MHz. Fabricated LPF is consisted of four PCB layers which components of SMD are soldered on the top layer. Another three layers is for grounding and shielding, power supply and grounding void. The four layers is crucial to avoid interference between components. The research has find out that the momentum simulation is definitely required to improve the signals response compared to a normal simulation by ADS software. The comparison between momentum simulated versus measured and normal simulated versus measured is 0.2 dB and 29 dB correspondingly. Such huge difference leads to conclusion that momentum simulation is saving time without having much struggles and efforts to get optimum readings. The Proposed SMD LPF has a very low insertion loss of 0.965dB with a transition region of 195 MHz which is good steepness to avoid any image frequency.

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1. INTRODUCTION

RF filters of all types form an important element within a variety of scenarios, enabling the required frequencies to be passed through the circuit while rejecting those that are not needed. It is not possible to achieve the perfect pass filter in reality and there is always some loss within the pass band, and it is not possible to achieve infinite rejection in the stop band. Also, there is a transition between the pass band and the stop band, where the response curve falls away, with the level of rejection rises as the frequency moves from the pass band to the stop band [1].

In microwave systems, low-pass filters (LPF) are dedicated to attenuate undesired frequencies or spurious by stepped LPF and stub LPF. However, these technique leads to the gradual cutoff response at the passband. Increasing the number of orders could enhanced transition band of LPF. Nonetheless, passband insertion loss and size of the LPF will get bigger. Few methods have been introduced to solve these problems. Ref. [2, 3] proposed an LPF deployed a lumped element composed of capacitor with a section of transmission line. Coupling lines [4], stepped-impedance hairpin resonators [5], capacitors with multiple orders LPF [6], varactor and lump components are among other techniques [7-13].

This paper provides the surface mount device LPF design with low loss insertion loss for TV White Space (TVWS) Application [14-16]. The development of LPF aims to simplify analytical studies on the LPF by using ADS momentum simulation. Section 2 describes the design of LPF and analyses the circuit design using ADS software. Discussion of the results obtained from the simulation and measurement are described in Section 3. Section 4 concludes the paper.

2. LOW PASS FILTER (LPF) DESIGN & FABRICATION METHOD

Figure 1 shows the circuit diagram design for the LPF using Cadence Allegro software. The proposed LPF has been designed using inductors and capacitors arranged in pi network. In order to provide a greater slope or roll off, cascaded LPF sections are deployed which is consisted of a 6th order elliptical design with a cutoff frequency at 770 MHz.

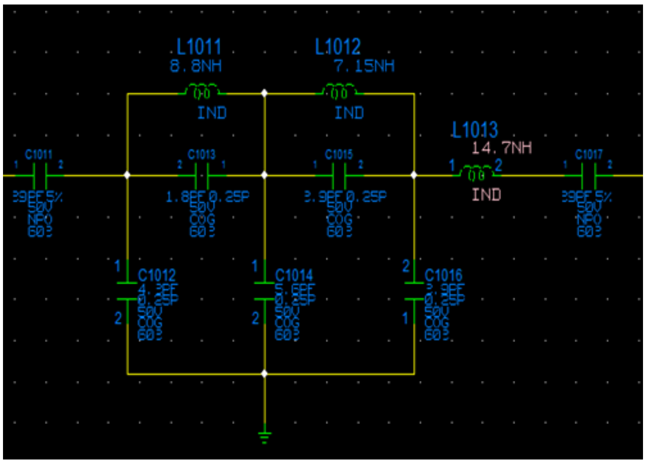

Figure 1. Schematic circuit diagram of LPF at 700MHz

For Pi section filter, each section has one series component and either side is a component to the ground. In the case of a LPF the series component are inductors whereas the components to ground are capacitors. The inductances and capacitances of inductors and capacitors based on constant-k type which are obtained from (1) to (3):

$$L = Z0/(\pi\ fc)\ H \tag{1}$$

$$C = 1/(Z\_(0\ )\ \pi\ fc\ )\ F \tag{2}$$

$$f_c = 1/(\pi\ \sqrt{LC})\ Hz \tag{3}$$

where: Zo=Characteristic impedance in ohm
C=Capacitance in Farad
L=Inductance in Henry
fc=Cutoff frequency in Hertz

The close tolerance components such as Murata components and Coilcraft components have been identified to ensure the required performance between simulated and fabricated is obtained. It is crucial to identify and finalize every single material or parts to be used to fabricate proposed LPF prior to the schematic and PCB design stage.

In industrial practice, usually, a so-called build of material (BOM) needs to be prepared to capture and structure all those parts in a list which will help to design the schematic and PCB layout properly and systematically. Basically, a BOM will be expected to include the following information: Reference Designator, Manufacturer Part Number (PN), Description of Item and Manufacturer, as shown in Table 1.

PN and reference designator of each component are already determined in BOM, the respective PNs are picked from Cadence library and the reference designator will be defined accordingly before placing the component in the schematic. Otherwise, the component has to be created based on the mechanical drawing in the datasheet and added to the Cadence library for being used in the schematic.

Table 1. BOM list of 700MHz LPF

Num	Ref Des	Value	MFR PN	Manufacturer
1	C1031	39pF	GRM1885C1H390JA01D	MURATA
2	C1032	4.3pF	81-GQM1885C2A4R3BB01	MURATA Capacitors
3	C1033	1.8pF	81-GQM1885C2A1R8BB01	MURATA Capacitors
4	C1034	5.6pF	81-GQM1885C2A5R6BB01D	MURATA Capacitors
5	C1035	3.9pF	81-GQM1885C2A3R9BB01D	MURATA Capacitors
6	C1036	3.9pF	81-GQM1885C2A3R9BB01D	MURATA Capacitors
7	C1037	39pF	GRM1885C1H390JA01D	MURATA
8	L1031	8.8nH	1606.8_L_	CoilCraft
9	L1032	7.15nH	1606.7_L_	CoilCraft
10	L1033	14.7nH	0908SQ.14N_L_	CoilCraft

LPF schematic diagram must be made available that shows the connection of the parts on the board. Each part on the schematic should have a reference designator that matches the one shown in the BOM. Cadence provides schematic layout programs that will allow automatic generation of the BOM, as shown in Figure 1.

Once schematic is completed, PCB layout design will be the next process. The main PCB of proposed LPF is designed to have 4 copper layers: TOP layer, GND layer, PWR layer and BOTTOM layer. TOP and BOTTOM are the most outside layer of the PCB which is exposed or accessible for the components to be mounted on it. TOP layer is the only layer that mounted with the components listed in the BOM.

Figure 2 shows cross section structure of the PCB while Figure 3 shows the PCB layout of the LPF at the top layer of the four layers PCB. The special process of PCB layout called momentum starts off with the preparation of layout information defined in Cadence Allegro to be exported into ADS to simulate the EM-behavior as nets, traces, ports, transmission line, padstack and grounding. The momentum includes effects of those signals to reach a maximum similarity of the physical fabricated board where the normal simulation of ADS only includes the response of only lump components like resistors, capacitors and inductors.

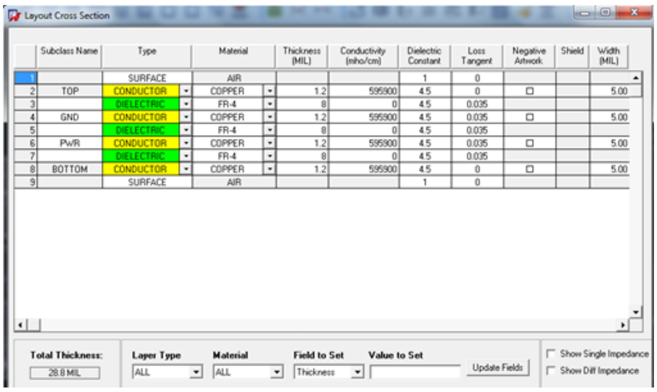

Figure 2. PCB structure of proposed LPF

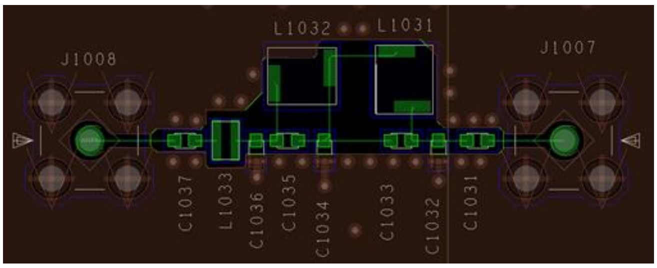

Figure 3. PCB layout of proposed LPF at 700MHz

L1032 and L1031 are wire wound inductor. Both inductors are seen perpendicular to each other. The arrangement is purposely made such a way to minimize or cancel out the mutual inductance between two inductors when they are positioned close to each other. Once the schematic diagram and PCB design are in place, Gerber file can be generated by Cadence to allow the fabrication of the bare board. Test setup of the prototype LPF is depicted by Figure 4.

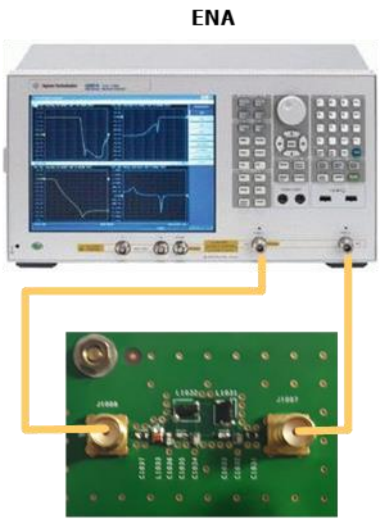

Figure 4. Test setup of fabricated proposed LPF at 700MHz

3. RESULTS AND ANALYSIS

Figure 5 shows a normal ADS simulated and the measured response of the LPF. From this figure, it is noticeable that the measured response is not correlated with the simulated response with obviously huge differences. Marker m 11 denotes the insertion loss for both responses at 700MHz where the difference between their performances appears to be around 29dB.

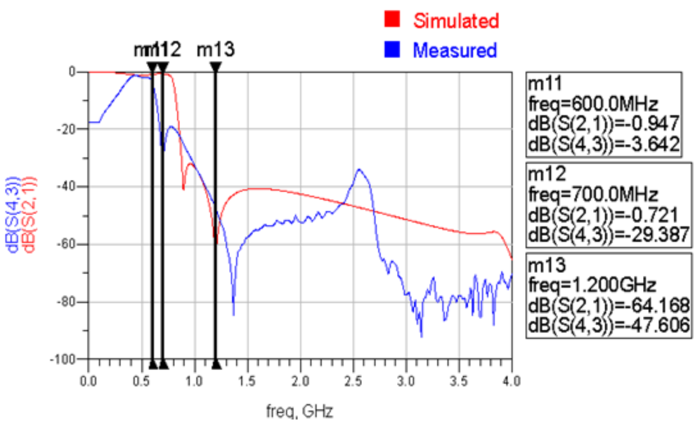

Figure 5. Momentum simulation vs measured insertion loss of proposed LPF at 700MHz

To address this discrepancy, the LPF circuit layout which is designed in Cadence Allegro is converted to a file that imported to ADS to perform momentum simulation to create a simulation model of the layout. The layout model is currently integrated into the entire circuit simulation including the lump components to perform S-parameters simulation for frequency response performance analysis.

If the LPF is not able to meet the design goal by optimizing the lump component due to layout limitation, then changes on the layout in Cadence Allegro might be required and the momentum simulation process may need to start over. The entire process will be done until the best performance is obtained in ADS simulation based on S-parameter performance.

With this practical approach, the PCB prototype fabrication or material cost, as well as optimization effort on real hardware, can be reduced a lot as layout limitation issue can be addressed earlier during PCB design with necessary changes on the layout or component footprint to provide the best performance in circuit simulation.

Figure 6 shows the frequency response of proposed LPF with a cutoff frequency of 700MHz. The marker m8 denotes the cutoff frequency at 700MHz which insertion loss of -0.965dB. This means that the 700MHz signal will lose power by 0.965dB when it passes through the LPF. The pass band region (bandwidth) for the filter is up to 700MHz whereby the signal below the cutoff frequency is allowed while others is rejected or attenuated including harmonic signals denotes as m9. Stop band cutoff frequency which falls at 895MHz. The transition region for this LPF is 195 MHz (from 700MHz to 895MHz).

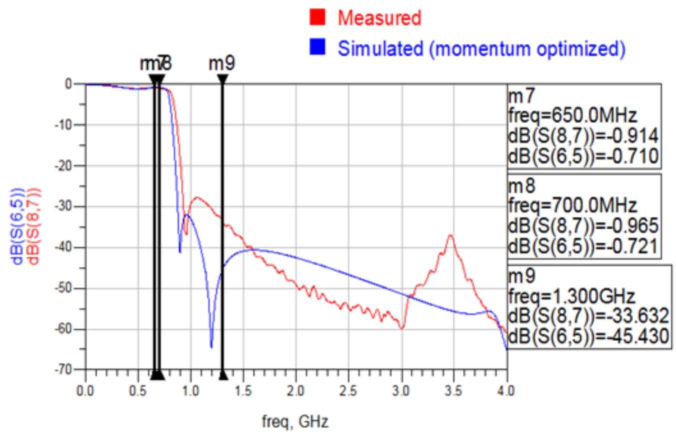

Figure 6. Momentum simulation vs. measured insertion loss of proposed LPF at 700MHz

Both simulated and measured response of the LPF filter is very much correlated. For instance, marker m8 denotes the insertion loss of both responses at 700MHz in which the difference between them is just about 0.2dB.

4. CONCLUSION

A low insertion loss of SMD LPF is presented in this paper. The proposed LPF competency is proven through insertion loss of 0.965dB with excellence steepness towards stopband. The loss gradient between measured and simulated is only at 0.2 dB. Momentum simulation deployed is this research prior to fabrication has shortened the time duration to get an optimum loss, a good rolloff margin and transition region compared to a normal simulation. Momentum does simulate EM-behaviour by counting the padstack, transmission line, grounding and shielding compared to the normal simulation which only counts responses solely based on RLC components.

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Khairil Anuar Khairi received his M.Sc in 2018 from Universiti Malaysia Perlis in the field of Communication and Computer Engineering. Currently, he works as Lead Test Development Engineer in Jabil. Previously, he works as senior RF & Electronics Design in Motorola Solutions for almost 12 years. His expertise is in Testing, RF designs and RF engineering.

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