A low quiescent current low dropout voltage regulator with self-compensation

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ABSTRACT

This paper proposed a low quiescent current low-dropout voltage regulator (LDO) with self-compensation loop stability. This LDO is designed for Silicon-on-Chip (SoC) application without off-chip compensation capacitor. Worst case loop stability phenomenon happen when LDO output load current (I_{load}) is zero. The second pole frequency decreased tremendously towards unity-gain frequency (UGF) and compromise loop stability. To prevent this, additional current is needed to keep the output in low impedance in order to maintain second pole frequency. As I_{load} slowly increases, the unneeded additional current can be further reduced. This paper presents a circuit which performed self-reduction on this current by sensing the I_{load}. On top of that, a self-compensation circuit technique is proposed where loop stability is self-attained when I_{load} reduced below 100µA. In this technique, unity-gain frequency (UGF) will be decreaed and move away from second pole in order to attain loop stability. The decreased of UGF is done by reducing the total gain while maintaining the dominant pole frequency. This technique has also further reduced the total quiescent current and improved the LDO's efficiency. The proposed LDO exhibits low quiescent current 9.4µA and 17.7µA, at I_{load} zero and full load 100mA respectively. The supply voltage for this LDO is 1.2V with 200mV drop-out voltage. The design is validated using 0.13µm CMOS process technology.

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1. INTRODUCTION

In recent years, the technology trend in biomedical engineering have tremendously increased the market demand for portable, wearable and implantable devices [1-3]. The requirement on complete functional integration semiconductor chip such as Silicon-on-Chip (SoC) in low power environment has becoming more important [4]. The advanced in transistor process technology that continuously required for a lower supply voltage with limited power consumption budget has put circuit designer into formidable challenges, especially the power management module [5, 6]. Low dropout linear regulator (LDO) is one of the most important unit in the power management module which has a clean supply but lower power efficiency compare switching regulator. LDO is suitable to regulate sensitive circuitries such as analog or RF modules [7]. The requirement of low power SoC had put LDO circuit design into challenge because the high capacitance external off-chip capacitor which is used for stability compensation had to be removed [8, 9]. Figure 1 shows a conceptual LDO design for SoC application.

There are many reported LDO design to resolve the stability issue of integrated LDO in SoC. Jacob Day and Donald Y.C.Lie suggested to use NMOS transistor instead of PMOS to implement a source follower in order to obtain low output impedance at the output of LDO [10]. This method sustain low impedance at output node and keep this pole at higher frequency. However the trade-off is the higher dropout voltage is required by NMOS pass transistor, thus lower efficiency is obtained. An additional low-impedance loading network at output node of LDO has also been suggested [11]. This method is able to maintain a competitive low dropout voltage using PMOS as output stage and sustain low impedance at the output node. However, excessive amount of current is needed by this circuit to sustain the output in low impedance. Thus, the higher quiescent current has resulting a lower efficiency LDO design.

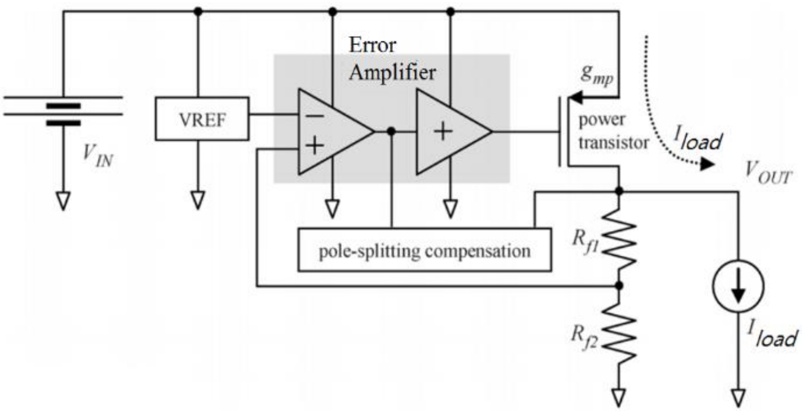


Figure 1. Conceptual LDO design for SoC application

To attain the issue of high quiescent current in LDO, there are research studies had been done, such as reduced the dropout voltage or reduce the low quiescent current during operation mode [12, 13]. However not many researches were being done to reduce quiescent current particularly during very small output load current, which means during its idle state. According to the statistic, electronics devices are under stand-by or idle mode at most of the time. Analog circuitries particularly LDOs are the major modules that constantly consuming current even in its idle state in order to keep the power supply working for the rest of the circuities. Therefore, this compromises the efficiency performance since the stand-by quiescent current carries a higher weight in efficiency. The efficiency percentage is given by

$$\eta = \frac{V_{out} I_{load}}{V_{in}(I_Q + I_{load})} \cdot 100\% \tag{1}$$

where I_Q is quiescent current and I_{load} is the output load current. Therefore reducing quiescent current to maintain a higher efficiency at very small or zero output load current is deemed to be important. Prior to this, this paper is focus on reducing the LDO's quiescent current even during output load current is near to zero, A method had been suggested by using self-reduction quiescent current circuitry [14]. This circuitry uses minimum quiescent current during high output loading current in order to obtain a better efficiency. It only allows adequate amount of additional current to be supplied to attain LDO stability during very low output load current. An improved version of such circuitry design is proposed in this paper. In this work, a sense and control circuit with low-impedance circuit is introduced. The circuit enables a self-adjusted minimum quiescent current to sustain the low output impedance during output load current is very small. At the same time, a self-compensation method is used to sustain the stability. This self-compensation mechanism has also contributed to the further reduction of total quiescent current.

2. PROPOSED LDO CIRCUIT DESIGN

2.1. Schematic and circuit implementation

The schematic of the proposed LDO circuit design is shown in Figure 2 and Figure 3. The proposed circuit is mainly consists of biasing circuit, transconductance amplifier (OTA), pass transistor power PMOS (M_P), low-impedance circuit, sensing and control (SAC) circuit, and feedback network (resistors R_1 and R_2). As shown in Figure 2, the biasing circuit is formed by transistor M_{b1}, M_{b2} and resistor R_b that supply bias current to the rest of the circuitry. The OTA amplifier consists of an input differential amplifier (M_1~M_5) and a gain stage amplifier (M_7~M_{10}). Transistor M_6 is biased from the SAC circuit to control an auxiliary current for the differential amplifier. The output of the gain stage forms a push-pull stage to charge and discharge the gate capacitance of the power PMOS, M_P. The gate capacitance of M_P is large due to the huge transistor size of this power PMOS to regulate the tremendous amount of current to the output load circuit. M_P output impedance, r_{op} is given by (2), where λ is the channel length modulation.

$$r_{op} = \frac{1}{\lambda I_{load}} \tag{2}$$

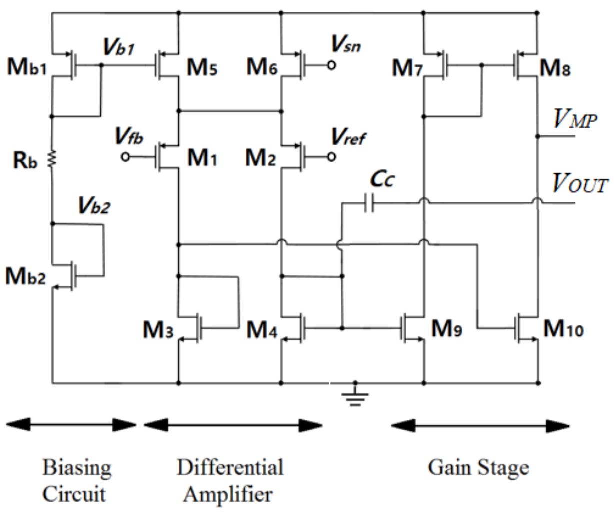


Figure 2. Proposed LDO circuit design (op-amp)

As shown in Figure 3, the low-impedance circuit consists of M_{18}~M_{21}. The source of PMOS transistor, M_{21} is connected to the output node of the LDO to provide a low impedance node. The total output impedance at V_{OUT} node, R_{o3} is given by (3), where $\frac{1}{gm_{21}}$ is the output impedance of M_{21}, and R_L is the output load resistance. The current from M_{12} is mirrored to M_{21} through current mirror M_{14}, M_{18} and M_{20}. Transistor M_{19} is used to keep transistor M_{20} in vigilant to maintain a fast response if M_{18} is turn off.

$$R_{o3} = r_{op}||(R_1 + R_2)||\frac{1}{gm_{21}}||R_L \tag{3}$$

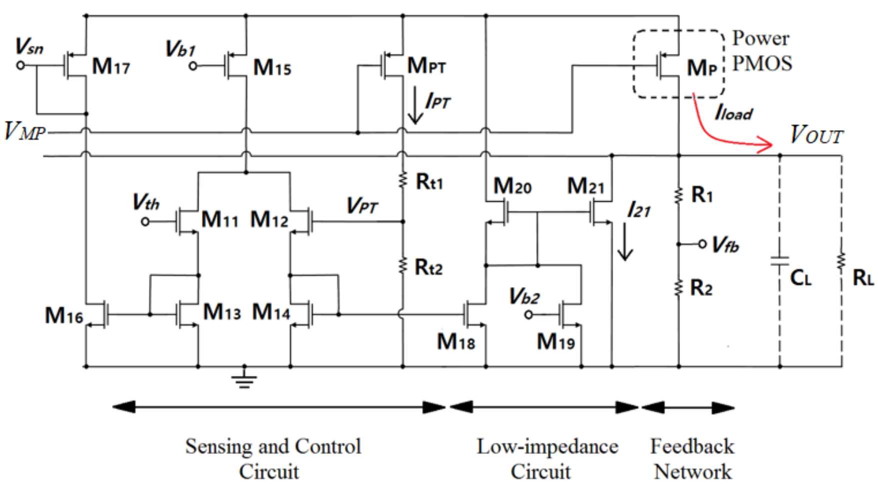


Figure 3. Proposed LDO circuit design

The sensing and control (SAC) circuit consists of sensing circuit (M_{PT}, R_{t1} and R_{t2}) and a differential circuit (M_{11}~M_{15}). The size of sensing transistor, M_{PT} is scaled to a ratio of 100 times smaller than M_P. Changes on output load current, I_{load} that flow through M_P will reflected to M_{PT} with 100 times smaller scale. Voltage level V_{PT} is scaled by the resistor divider R_{t1} and R_{t2} to be compared with a fixed reference voltage, Vth. If I_{load} reduces below $100\mu A$, it reflects to V_{PT}, and start the differential mode comparison operation.

2.2. Stability analysis and circuit operation

Figure 4 shows the open-loop domain configuration of the proposed LDO. It shows total three amplifier stages, which is the differential amplifier, gain stage, and the power PMOS as the third stage. Power PMOS is a common-source amplifier. Each stage corresponding transconductance, output impedance and parasitic capacitance are denoted in the configuration as Gm_1, Gm_2, Gm_3, R_{o1}, R_{o2}, R_{o3}, C_1, C_2, and C_3 respectively.

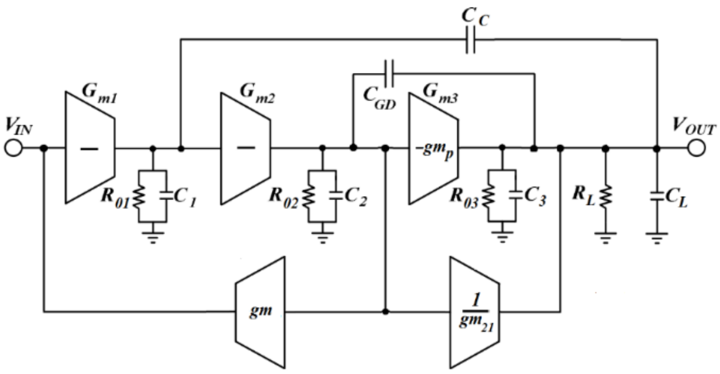


Figure 4. Proposed LDO open-loop configuration

The output impedance of the first stage, R_{o1} is small due to the diode-connected active load which imposed approximately $\frac{1}{gm}$ at its output. Therefore first stage gain A_1 is small and the pole is located at higher frequency and doesn't affect the stability. The second stage has a large output impedance (R_{o2}) due to the active load formed by current mirror circuit. Therefore gain A_2 is higher. At this node, large gate capacitance of power PMOS contributes to a high value C_2 , and therefore the dominant pole (p_{-3dB}) is located at this node. The third stage output impedance, R_{o3} has a wide variation range which depending on the large output load current, as per (2) and (3). Due to the large M_P size, the gm_p is high, thus contributes to high gain A_3. The parasitic capacitance C_3 and output load capacitance C_L contribute to second pole (p_2) frequency and dependent on R_{o3} variation. A compensation capacitor C_c is connected between the output of first and third stage, and gate-drain capacitance of M_P between second and third stage, are giving a pole splitting effect for frequency compensation. The low frequency gain (A_{DC}), dominant pole (p_{-3dB}) and second pole (p_2) are respectively given by:

$$A_{DC} = Gm_1 Gm_2 Gm_3 R_{o1} R_{o2} R_{o3} \tag{4}$$

$$p_{-3dB} = \frac{1}{2\pi R_{02} C_2} = -\frac{1}{2\pi\, g_{mp} R_{02} R_{out}(C_{gd}+C_c)} \tag{5}$$

$$p_2 = \frac{1}{2\pi R_{03}(C_3+C_L)} = -\frac{g_{mp} C_{gd}}{C_{out}(C_{gd}+C_2)} \tag{6}$$

The transfer function, T(s) is given by (7):

$$\mathrm{T(s)} = \frac{v_{fbo\,(S)}}{v_{fbi\,(S)}} \approx \frac{A_{dc} \times \left(1 + \frac{C_c}{2g_{ml}} s - \frac{C_c(C_c + C_{gd})}{2g_{ml}\, g_{mp}} s^2\right)}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + \left[\frac{C_c + C_{gd}}{g_{ml}\left(C_{gd}+C_c\right)} + \frac{C_c C_2 + C_2 C_p + C_{gd} C_p}{g_{mp}\left(C_{gd}+C_c\right)}\right] s + \frac{C_c C_p(C_2 + C_{gd})}{g_{ml}\, g_{mp}(C_c + C_{gd})} s^2\right.} \tag{7}$$

The loop stability analysis to be focused in this work is on the worst case scenario where I_{load} is below $100\mu A$. When I_{load} falls below 100µA, r_{op} becomes very large and so does R_{o3} as shown in (2) and (3). This causes p_2 frequency to reduce tremendously moving toward UGF, and compromise the minimum requirement of phase margin if $p_2 \leq \sqrt{3}\, UGF$. A solution is proposed to reduce R_{o3} using low-impedance circuit. From (3), small value $\frac{1}{gm_{21}}$ from low-impedance circuit dominates R_{o3} instead of r_{op}. If I_{load} reduces below $100\mu A$, the sensing circuit will cause V_{PT} to decrease below Vth. M_{12} will start to draw more current compare M_{11}. As I_{load} reduces, more current will be mirrored from M_{12} to M_{21} to obtain smaller impedance value, $\frac{1}{gm_{21}}$. Thus prevent p_2 from further shifting to lower frequency. If I_{load} is not low enough to compromise the loop stability, only adequate amount of current is used to maintain the loop stability. In other words, self-reduction current is performed when I_{load} starts to increase from zero. However, at worst case stability phenomenon where I_{load} is zero, this current can be high. Instead of using excessive current to maintain p_2 frequency, a self-compensation circuit method is proposed. The total gain is lowered without influencing p_{-3dB} in order to shift UGF to lower frequency, away from p_2 as shown in Figure 5. This is done by the SAC circuit with a current feedback. As I_{load} reduces, V_{PT} decreases, and drain current of M_{11} starts to reduce. Lower current is mirrored from M_{11} to M_6, and reduces the first stage gain.

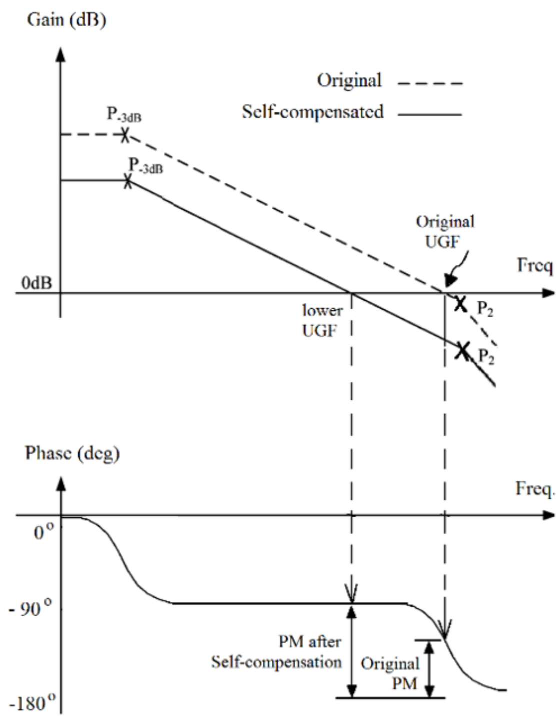


Figure 5. Bode plot for $\boldsymbol{I_{load}}$ < 100µA

Therefore the total gain has been reduced but p_{-3dB} location is not affected. In other words, as I_{load} reduces, a self-compensation mechanism take effect where the UGF is automatically reduces in order to obtain a better phase margin. The proposed SAC circuit has not only reduced the excessive I_{21} at low-impedance circuit, but at same time, it further reduced the tail current at first stage amplifier. This has contributed to the reduction of total quiescent current.

3. RESULTS AND DISCUSSION

The proposed LDO in this work has been implemented using $0.13\mu m$ CMOS process technology. The frequency response at high load current is stable with phase margin higher than 90°. This work focuses on very low output load current phenomenon. The close-loop frequency response of proposed LDO at very low load current is plotted as shown in Figure 6. When the load current is reduced, the decrement of second pole can be seen. It's due to the self-reduction of additional current at low-impedance circuitry. It shows that the gain is decreasing when the load current is reduced to zero, and the UGF shifted to lower frequency and attained loop stability with phase margin higher than $60°$. The $20dB$ gain during zero load current doesn't compromise the application of LDO since it's not in regulating mode. Maintaining adequate phase margin to attain loop stability at zero load current is more important so that a quick response is obtained when the load current is suddenly required at the LDO output. The resulst also shown an almost linear decrement of UGF with the reduction of load current from 100µA.

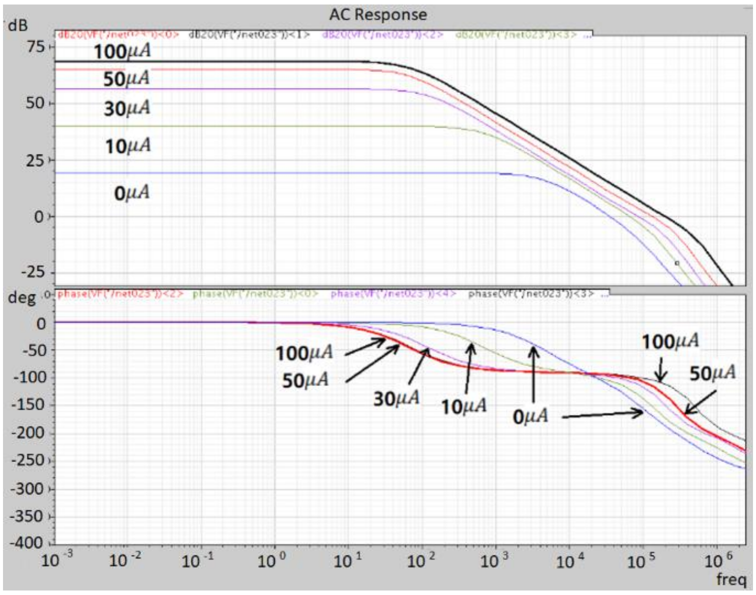
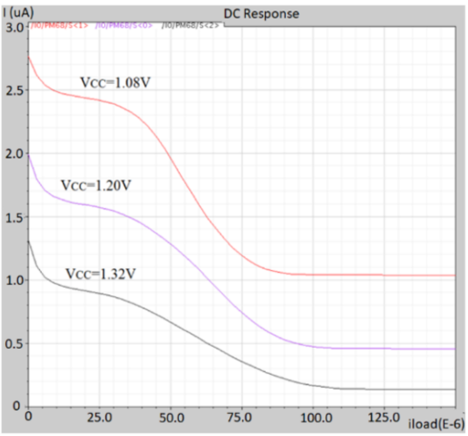
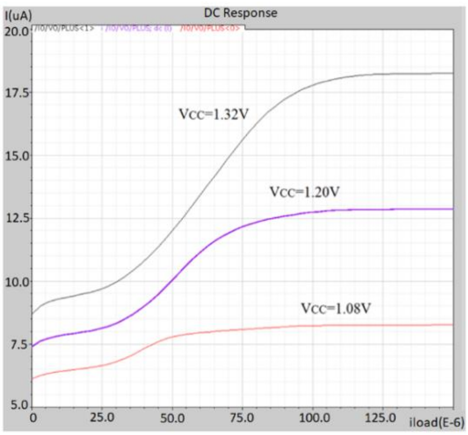


Figure 6. LDO frequency response for very small load current

Figure 7(a) shows the graph of I_{21} versus I_{load}, where I_{21} is the current used to keep output impedance low during small load current. When I_{load} increased from zero to $100\mu A$, I_{21} has reduced from $2.0\mu A$ to $0.5\mu A$ for V_{CC}=1.20V. This shows the self-reduction mechanism of current used in low-impedance circuit. Figure 7(b) shows the graph of total quiescent current, I_Q versus I_{load}. When I_{load} reduces from $100\mu A$, the total quiescent current of LDO has been reduced from $12.8\mu A$ to $7.4\mu A$ for V_{CC}=1.20V. The total quiescent current reduction is around 30%.





(a) (b)

Figure 7. (a) $\boldsymbol{I_{21}}$ (b) $\boldsymbol{I_Q}$, versus $\boldsymbol{I_{load}}$ of LDO

Figure 8 shows the efficiency performance of proposed LDO at load current below 100µA. The result shows 60% efficiency even at very low load current at 25µA. The efficiency has became almost constant at 70% and above when load current increased to 50µA.

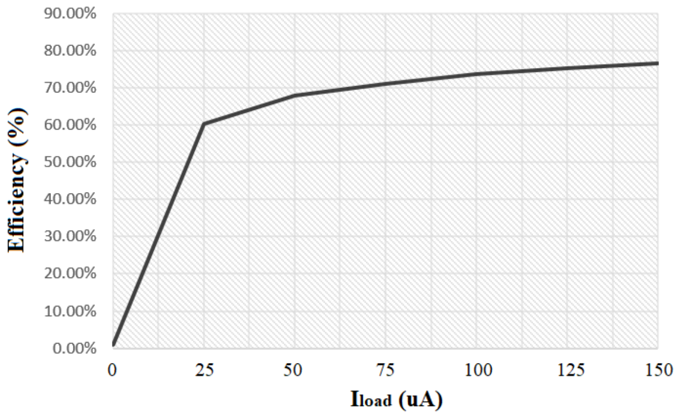


Figure 8. Efficiency versus I_{load}

The die picture of the LDO is shown in Figure 9. Table 1 shows the comparison between the recent reported LDO designs and this work. The reported LDO designs with proximity technology are chosen for the comparison. This LDO is designed to deliver a maximum load current of 100mA. The proposed lower power LDO supply voltage is 1.2V and the output voltage is 1.0V with dropout voltage of 200mV. The total quiescent current is only $9.4\mu A$ at zero output load current, and $17.7\mu A$ at full output load current$100mA$.

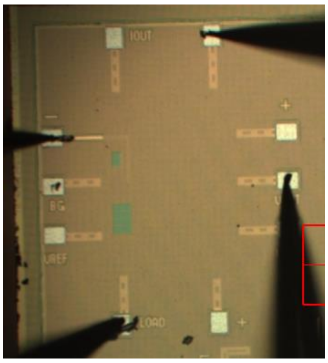


Figure 9. Die picture of proposed LDO

Table 1. Comparison of published LDO results

Published LDO	Technology (µm)	Supply Voltage (V)	Dropout Voltage (mV)	Output voltage (V)	Max. Load Current (mA)	Min. Load Current (µA)	Max. Quiescent Current (µA)	Compensation Cap, Cc (F)
[11]	0.18	1.2	200	1.0	100	0	53.5	10p
[15]	0.13	>1.313	>113	1.2	70	-	93	external
[14]	0.13	1.2	100	1.1	100	-	27	8p
[16]	0.13	1.2	200	1.0	50	50	37.3	-
This work	0.13	1.2	200	1.0	100	0	17.7	8p

4. CONCLUSION

A low quiescent current LDO with self-compensation has been presented in this work. The proposed LDO has improved the loop stability and efficiency issues at worst case scenario where output load current I_{load} is very low. These techniques are implemented by low-impedance circuit and SAC circuits. The variation of I_{load} is sensed and feedback by SAC circuit. Firstly, the current used for keeping output impedance low is self-reduced as I_{load} slowly increases from zero. Secondly, a self-compensation method is introduced for frequency compensation, instead of using excessive current to keep p_2 frequency higher. The current feedback of the SAC circuit has also further reduced quiescent current. The results have shown that this LDO has achieved the goal of reducing quiescent current by adopting current self-reduction technique. On top of that, a self-compensation circuit technique on loop stability has also further decreased quiescent current.The total quiescent current reduction has contributed to a higher efficiency of the LDO at low load current.

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