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Zinc Oxide Thin Film Transistors: Advances, Challenges and Future Trends

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Abstract

This paper presents a review on recent developments and future trends in zinc oxide thin film transistors (ZnO TFTs) together with challenges involved in this technology. It highlights ZnO TFT as next generation choice over other available thin film transistor technology namely a – Si: H (amorphous hydrogenated silicon), poly-Si (polycrystalline silicon) and OTFT (organic thin film transistor). This paper also provides a comparative analysis of various TFTs on the basis of performance parameters. Effect of high –κ dielectrics, grain boundaries, trap densities, and threshold voltage shift on the performance of ZnO TFT is also explained.

Keywords*: ZnO TFT; a – Si TFT; poly – Si TFT; threshold voltage shift*

1. Introduction

The advancement in large area electronics is now driving human civilization. The consumers which were earlier passive have become socially connected through various electronic gadgets like laptops, tablets, phablets, smart phone etc. All these gadgets are getting updated rapidly with the technological advancement. For example in past few decades Television technology was based on the well established cathode ray tube (CRT) technology. However, demand for larger screen size has increased over the past few years with increasing technological advancements along with varying consumer behavior. This demand has led to the increasing popularity of LCD and now LED display technology. Although, the displays like liquid crystal display (LCD) were available for over last six decades, but they were not at all competing with CRT technology. The scenario changed drastically in last decade due to introduction of active matrix LCD (AM-LCD) and active matrix OLED (AM-OLED) devices together with Micro Electro Mechanical System (MEMS) technology (especially smart phone and tablets).

All these display panels are driven by thin film transistors (TFTs) mostly using polycrystalline silicon (poly-Si) or amorphous silicon (a-Si) as an active channel layer [2-4]. But there are also a lot of problems need to be solved in the TFTs, which use silicon as an active channel layer. These TFTs (especially the a-Si ones) actually present some limitations like: low field effect mobility (~1 cm^2/V-s), light sensitivity and light degradation. Utilization of oxide based TFTs can overcome these problems. Oxide semiconductor based thin film transistors have recently been proposed using channel layer of poly crystalline Zinc Oxide (Poly-ZnO). In comparison to a-Si, ZnO provides various advantages. First it can be grown as a crystalline material at relatively lower deposition temperature [5]. Second, it can be deposited on various substrates made of silicon or amorphous glasses [5], which make it possible to realize a total transparent ZnO-TFT. Moreover, the characteristic of ZnO do not degrade in the exposure of visible light because of its direct band-gap. Third, ZnO thin film used as an active channel layer can achieve a higher mobility than a- Si (~12 cm^2 /V-s, compared to < 1 cm^2 /V-s, for a-Si: H produced in similar conditions) [6]. Although, this technology continues to address the AMOLED or AMLCD market, it carries a significant number of issues which demand attention.

This paper is organised as follows: Section 2 highlights the brief history and development of thin film transistor technology, Section 3 consists of factors affecting the performance of ZnO TFT and Section 4 consists of challenges and future trends.

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2. Developments in TFT Technology

The development history of MOSFET and TFTs are almost similar. The concept of MOSFET was first proposed in 1930 by JE Lilienfield [1]. However, this concept took time to commercialize because of the need of sophisticated fabrication techniques. In early time, the TFTs were made of compound semiconductors like CdS or CdSe for high field mobility of the order of 40 cm^2 /V-s [7, 8]. However, because of limitation of fabrication technology mass production of these TFT never realized. Meantime, the researcher started focusing on developing IC technology as it was giving the great deal of miniaturization and enhanced performance. However, IC technology needs single crystal silicon as a substrate to start with, which is very costly. Researchers find this as a motivation and tried to figure out cheaper substrate material and technology to fabricate cheaper transistor. Figure 1 shows the timeline of development of thin film transistor technology. In 1968 Boesen and Jacobs [10] proposed ZnO based FET, these TFT was not having mobility as equal as the new generation ZnO TFT. In the year 1973 CdSe TFT-LCD was successfully demonstrated by TP Brody and Co [8]. In 1979 one more breakthrough came as a-Si: H TFT was fabricated with silicon nitride as a gate dielectric [11] in glass substrate using PECVD (Plasma Enhanced Chemical Vapour Deposition). However, the mobility of these TFT was too low for driving the pixel of OLED display. Not only that, since a-Si: H possesses photoconductive properties hence under light exposure leakage was the issue. Still as soon as the a- Si: H TFTs were invented they were used in LCD display for mass production. To obtain higher mobility, researchers developed a method of depositing polycrystalline silicon in glass substrate which is able to obtain a mobility value as high as 360 cm^2 /V-s [13]. However, it suffers mobility killing scattering at the grain boundaries. Adding to this, the process requires high temperature (~ 600 ^{0}C) anneal for re-crystallization.

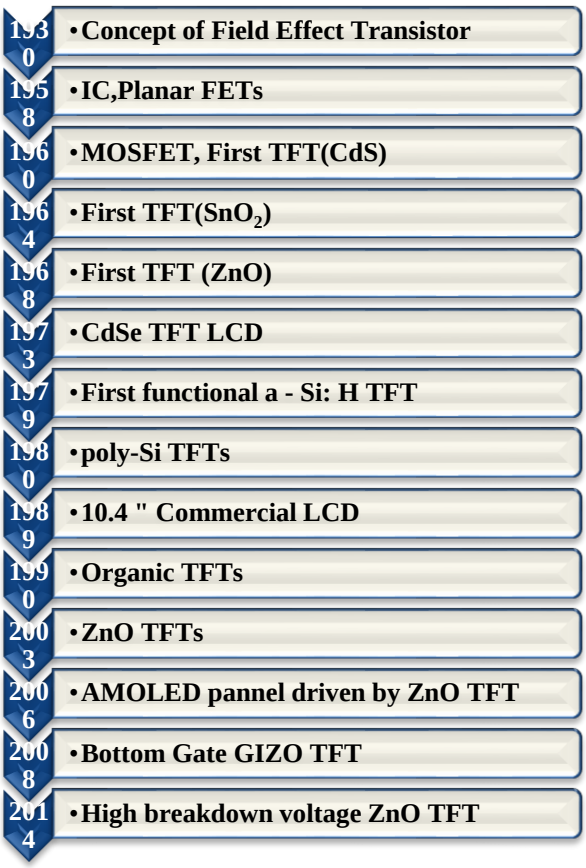

Figure 1. Timeline of TFT technology development

A new class of TFT named as OTFT (organic thin film transistor) was introduced in late 90s. Organic thin films can be easily spin coated or printed on the substrate at the room temperature. Some of the OTFTs have been demonstrated for high field mobility [14-15]. Later, RL Hoffman and Co. [16] demonstrated transparent thin film transistor using ZnO as a channel. ZnO based TFT offers high field effect mobility and immunity towards light sensitivity and light degradation because of its wide band gap. After the year 2003, several reports continued to appear on ZnO based TFTs, bringing innovations to this emerging technology. The most important achievements include fabrication of ZnO thin film at low temperature or even at room temperature, utilization of non vacuum processes, fully transparent ZnO TFT with very less thermal budget and various methods of extraction of field effect mobility. SHK Park et al [40] demonstrated 2.15 inch AM-OLED panel driven by ZnO -TFT. ZnO Thin film was deposited by ALD (Atomic layer deposition). JY Kwon et al in the year 2008 fabricated a Ga_2O_3 – In_2O_3- ZnO (GIZO) TFT with bottom gate topology. It was used to drive 4 –in QVGA AMOLED display. A Ma et al proposed high breakdown voltage ZnO Thin film transistor using ZrO_2 as the gate dielectric. The fabrication process used in this work involves thermal budget less than 130^0c and atomic layer deposition (ALD) technique. A 5 nm thin layer of ZrO2 was used as gate dielectric; this transistor showed enhancement type operation with gate bias voltage less than 2V due to high-κ dielectric.

A comparative analysis of various TFTs is done in Table I. Poly – Si TFT offers higher mobility than a- Si: H, Organic TFT and oxide TFT. However, its performance is affected by high leakage current. ZnO TFT offers good field effect mobility and very good I_{on}/ I_{off} ratio. However, ZnO TFT requires high operating voltage. The threshold voltage of ZnO – TFT can be lowered by the incorporation of high–κ dielectric. Fabrication of OTFT includes very less thermal budget and very simple fabrication technology. The leakage and other properties largely depend upon fabrication process.

Table 1. Comparative analysis of Various TFTS

Performance Parameter	a-Si:H TFT [36]	Poly Si- TFT [37]	Organic TFT [38]	ZnO TFT [39]
μ (cm^2/V-s)	0.8	37	0.02	20
I_{on}/I_{off}	10^7	10^5	10^6	10^9
V_T (V)	4.5	3.4	0.7	6
S (V/ dec)	0.5	1.10	0.17	0.14
I_{off} (A)	10^{-9}	-	10^{-12}	-

3. Factors Affecting the Performance of ZnO TFT

ZnO is a wide bandgap (3.4 eV), *II-VI* compound semiconductor, having a wurtzite structure with lattice spacing *a* = 0.325 nm and *c* = 0.521 nm. ZnO material can be used for numerous applications such as: transparent electrodes, photovoltaic devices, blue and UV light emitters, gas sensors and bulk acoustic wave devices [5]. Intrinsically ZnO is an n-type semiconductor primarily due to presence of oxygen vacancies. The first reported ZnO IGFET in a coplanar configuration was demonstrated by Boesen and Jacobs in the year 1968 [10]. Since then several theoretical and experimental findings has been published that explain the conduction mechanism in ZnO TFTs. Some of the work emphasize on improvement of ZnO thin films [15-18], while some work reported the analytical modeling of ZnO TFTs [17-21]. ZnO thin films have been grown by various growth techniques e.g. RF sputtering, metal organic CVD [22], MBE [23], and pulsed laser deposition (PLD) [24]. A high performance ZnO TFT was successfully demonstrated on a glass substrate by CC Liu et al [25]. RF magnetron sputtering is used to deposit ZnO channel layer, in 10^{-2} torr of Ar/O_2 (15:1). *The need of oxygen gas was to reduce the carrier density of the zinc oxide layer so that TFTs can have positive threshold voltage.* RL Hoffman et al [16] fabricated a ZnO based transparent TFTs with optical transmission of 75% in the visible portion of the EMT spectrum. The current– voltage measurement indicates *n*-type, enhancement-mode TFT with excellent on-to-off ratio (I_{on}/ I_{off}) of 10^7. Threshold voltages (V_T) and channel mobilities (μ_{eff}) of devices fabricated range from; 10 to 20 V and 0.3 to 2.5 cm^2/V-s respectively. Exposure to ambient light has negligible effect on the drain current. On the other hand, exposure to UV radiation results in constant photoconductivity, together with the generation of electron-hole pairs (ehp) by photons with energies greater or

equal to ZnO band gap. HQ Chang et al [26] fabricated transparent TFTs with an a- Zinc Tin Oxide channel layer deposited via RF magnetron sputtering. The post – deposition annealing affects mobility and threshold voltage of device. A mobility of 50 cm^2 /V-s and a drain current on-to-off ratio (I_{on}/ I_{off})) greater than 10^7 is obtained. Zinc tin oxide is an example of a new set of oxide TFT channel materials composed of heavy-metal cations.

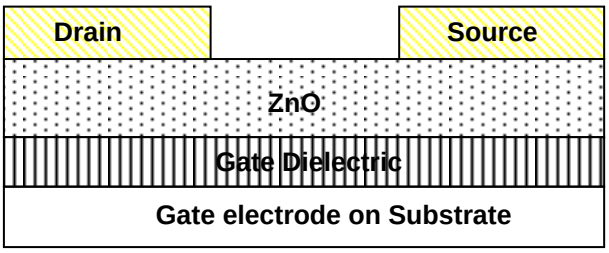

Figure 2. Bottom gate ZnO thin film transistor

Figure 2 shows a schematic view of one of the most popular topology of ZnO -thin film transistor i.e. bottom gate ZnO-TFT. Depending upon the location of source and drain with respect to the channel, TFT structures are defined as coplanar or staggered. If they are on same side then the structure is coplanar and if they are on opposite side then it is staggered. Inside these, bottom and top gate structures exist. If the gate electrode is on the top of structure then this is top gate structure and vice versa. The operation of a TFT is similar as of field effect transistor (FET). The performance of a TFT depends fundamentally on the type of gate insulator and the quality of dielectric- channel interface because of the current flows in the ZnO channel next to the interface. Various studies are done in order to understand the performance of ZnO TFT. These studies are discussed as follows.

A. Integration of ZnO TFT with High-κ Dielectric

The use of thicker high-κ dielectric layers as a gate dielectric reduces gate leakage current without affecting the induced interface charge density. Moreover, since high driving capacity of TFT is needed to drive the OLED pixel, for that high oxide capacitance is required which can be achieved effectively by high-κ dielectric. JJ Siddiqui e. al [27] have studied ZnO thin film transistors with HfO_2 (ϵ_r = 25) as dielectric. The integration of high-k dielectrics in ZnO TFTs as a potential gate dielectric has demonstrated advantages including increased on-to-off current ratios, reduced threshold voltage, and larger transconductance. Several authors [28-30] reported that reduction in leakage current and operating voltage is possible by using various high-κ dielectrics. Various gate dielectric reported which can be used, are Si_3N_4, (BaSr) TiO3, Al_2O_3, ZrO_2, La_2O_3, HfO_2.

B. Modelling of Grain Boundaries and Trap Densities

The performance of ZnO TFT is largely influenced by trap densities and grain boundaries at the interface. According to M Kimura [18], trap densities can be assumed to be uniformly distributed in the ZnO films. The result was obtained using the C-V plot and extraction techniques. The study clarifies that the main reason of trap densities is the presence of donor like trap states originated from Zn antisites and Zn interstitial however; it can be minimized with optimization of deposition techniques and with proper choice of underneath surface. J Nishii et al [17] have modeled grain boundaries (GBs) in ZnO thin film transistors (TFTs) for understanding the grain boundary effects on the device performance. The significant differences between device modeling of the ZnO-based TFT and the poly-Si TFT can be pointed out as:

1) In nanocrystalline ZnO thin film, the developed depletion region around closely spaced grain boundaries overlaps to make potential profiles in the film different from that of poly-Si thin film.
2) Due to probable existence of deep level traps in GBs and wide band-gap (E_g) of ZnO and, the GB barrier height modulation with applied gate bias for ZnO TFTs will be different from that of poly-Si TFTs.

GH Xia et al [31], reported a model for the density of states (DOS) and carrier transport in a poly-ZnO. The GB was modeled as a thin semiconductor layer with defect states parallel to the transverse electric field, with the assumption that the regions on both sides of the GBs were completely defect-free. The DOS $g(E)$ was described as a combination of four components; a) an acceptor-like exponential band tail function, b) a donor-like exponential band tail function c) an acceptor like Gaussian deep state function, d) donor like Gaussian deep state function. Wang et al [32], proposed an analytical solution for GB barrier height in intrinsic polycrystalline semiconductor, later on this model was applied to ZnO TFT. A physical-based analytical solution to the GB barrier height (ψ_B) is developed for polycrystalline TFTs. The explicit solution is obtained using the Lambert W function. The solution is verified by comparing the model with both analytical calculations and experimental ψ_B data of poly- Si TFTs.

C. Threshold Voltage Shift (ΔV_T) in ZnO TFT

Threshold voltage shift is an important performance parameter for many TFT applications. Lesser the shift better is TFT. Extensive Bias-Temperature-Stress (BTS) studies have been carried out on ZnO TFT to track the threshold voltage (V_T), field effect mobility (μ_{eff}), subthreshold slope (SS), grain boundary trap creation (NTG) over time. A change in threshold voltage largely affects the life of an AMLCD display as a shift can cause insufficient driving current to the pixel which in turn results in a dark pixel. All the TFT devices (a- Si, Poly- Si, and Oxide) suffer from threshold voltage shift however a smart change in device topology can reduce this phenomenon. H. Yun [33] fabricated dual-gate and bottom gate ZnO TFTs without any additional processes and analyzed their threshold voltage variation under a negative gate bias stress (NBS). The dual-gate device shows superior electrical performance, such as SS and I_{on}/I_{off}. NBS of V_{GS} = −20 V with V_{DS} = 0 was applied, which resulted in negative threshold voltage (V_T) shift. After applying voltage stress for 1000 s, in dual-gate ZnO TFT the the V_T shift was 0.60 V, while in a bottom-gate ZnO TFT the V_T shift was 2.52 V. *The stress immunity of the dual-gate device was result of modulation in field distribution or potential profile in the ZnO channel due to addition of another gate*. D. Gupta et al [19] investigated the stress – recovery characteristic of ZnO TFTs under gate bias and current-stress conditions. At room temperature a characteristics time of 1.6 x 10^3 − 3.6 x 10^3s during stress and 7.7 x 10^3 − 15.7 x 10^3s during recovery was obtained by following a stretched exponential model under all gate voltage bias and current conditions. The device simulation indicates that threshold voltage shift ΔV_T is mainly caused by the *increase in acceptor like defects of the DOS in the ZnO channel layer*. W. S. Choi [35] studied the effect of threshold voltage shift on TFT scaling. Result shows that the device scaling influences the threshold voltage and subthreshold slope as: *a decrease in the active layer thickness results in an increase in threshold voltage, while the subthreshold slope decreases*.

D. Transport Model of ZnO TFT

Transport model for current conduction in ZnO –TFT is much needed in order to emulate various pixel driver TFT based circuit. F Torricelli et al [34], proposed the multiple-trapping-and-release (MTR)-transport model to describe the transport mechanism in ZnO TFTs. Figure 3 describes MTR model, a charge carrier (shown as filled circle) from the conduction band (CB) is trapped into localized site in the gap, after thermal excitation it can be free to move or return to extended state. Only these carriers are responsible for charge transport.

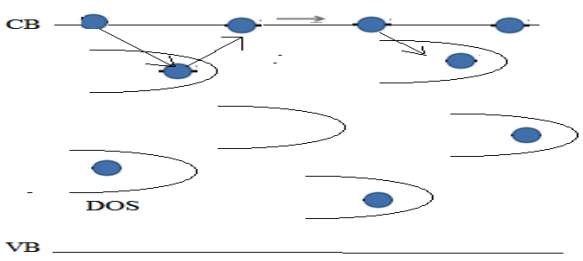

Figure 3. Multiple-tapping and release mechanism

This model was used to define transport properties of ZnO TFT deposited by spray pyrolysis, over wide range of temperatures, biasing condition and at different channel lengths. It is observed that ZnO TFTs field-effect mobility (μ_{eff}) increases with carrier concentration and is temperature activated. Transport properties are strongly influenced by the tail states extend in a wide range of energy

4. Challenges and Future TFT Trends

The rate of progress of TFT technology has been quite commendable. Industry R&D activities have been aiming at improving the throughput, cost and yield of TFTs. Academic research in many institutions has helped in the understanding of device physics and material properties responsible for the TFT performance and the associated technical issues. However, still there are gap in existing research which need to be address:

i. The performance of a TFT depends fundamentally on the type of gate dielectric and the quality of dielectric-channel interface because of the current flows in the ZnO channel next to the interface. However, despite the intensive research on high–κ dielectrics, the performance of the devices with high–κ dielectrics is still rather poor analyzed and compared to those with SiO_2 gate oxides. So a more detailed understanding of the types of gate dielectric and interface is urgently needed.
ii. Various theories and models have been presented for explaining the electrical properties of TFT based on different conduction mechanism of carriers through poly crystalline thin film. But each of these models has their own conditions of validity and also has limited range of applicability. As technology evolves, further model improvement is needed to describe the device characteristics of scaled devices and to account for stochastic effects on characteristic of the device.
iii. As ZnO-TFT is recognized as one of the potential candidates of next-generation active addressing devices for flat panel display (FPD), therefore many research groups are focusing on improving the material properties of ZnO TFT, especially field effect mobility, with different fabrication technologies. It is well known that the threshold voltage stability of TFTs is important in practical applications such as driving an OLED; however, ZnO TFT is rarely investigated on this topic. So stability issues of this device should be investigated property which should provide physical insight to the mechanism which gives electrical instability to these devices.

There has been growing interest in oxide TFTs for the next generation large-area flat-panel display application. According to article published in the year 2007 in the Japanese magazine Nikkei Electronic Asia*, "Transparent Electronic Products soon a reality"* present scenario is of second wave of transparent thin film technology. The impact of thin film technology in electronics industry and its market share will increase with time including other areas of application such as; high definition imagers, UV sensors, high- sensitivity biosensors, transparent conductive p-type transistor, transparent solar cell, CMOS ICs using oxide TFT, high performance ICs, totally transparent high definition displays etc.

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