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Leakage Analysis and Solution of the RFID Analog Front-END

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Abstract

The identification and modeling of different leakage components are very important for estimation and reduction of leakage power, especially low-power applications, such as RFID chip. This paper proposes a theory about leakage mechanism of RFID chip and proves the theory. The one contribution of the paper is the proposed theory about leakage mechanism of RFID chip. The other contribution is that it proves the differences between tape-out verification results and computer simulation results and that to what degree the differences occur for different circuits. And when the source potential is much lower than the substrate potential, tape-out verification results and computer simulation results have larger differences. The test results show that the actual leakage power increases 26.3 times compares with the computer simulation results' when the source potential is -750mV.

Keywords: *RFID, leakage mechanism, rectifier, device model*

1. Introduction

RFID technology is a non-contact automatic identification technology. RFID chips have many features, such as small size, easy to carry, storing large amount of information, non-contact and so on [1]. And RFID chips are widely used in the field of access control system, library management system and vehicle identification system [2].

This paper proposes a RFID chip which is used in the car. The chip transfers the information according to the inductance coupling principle, as shown in figure 1. We tested the chip after it had been fabricated. The oscilloscope displayed the result as shown in figure 2. It illustrated that the chip had all the functions that we had defined. But the performance was poor. For this problem this paper gives a theory that there must be high leakage current between source and substrate. In order to prove this theory, first this paper gives a detailed theoretical analysis. Then we optimized several circuit structures to prove the theory and solve the leakage problem. At last we made tape-out verification and successfully proved the leakage theory.

2. Proposed Leakage Theory

Because of no independent power supply, the chip can only make use of Inductance coupling energy. And the rectifier circuit generates the power supply of the chip. Due to the limited coupling energy, the RFID chip must be low power consumption [3]-[6]. So the testing results shown in Figure 2 indicate that there must be high leakage current in the circuit. Regarding transistor leakage mechanisms paper [7] describes six short-channel leakage mechanisms as illustrated in Figure 3. I_1 is the reverse-bias pn junction leakage; I_2 is the sub-threshold leakage; I_3 is the oxide tunneling current; I_4 is the gate current due to hot-carrier injection; I_5 is the gate-induced drain leakage; and I_6 is the channel punch-through current. The leakage mechanism proposed in this paper is similar to I_1. But it is the forward-bias pn junction

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leakage rather than reverse-bias pn junction leakage. So the proposed leakage theory is that there is high current leakage between source and substrate through forward-bias pn junction.

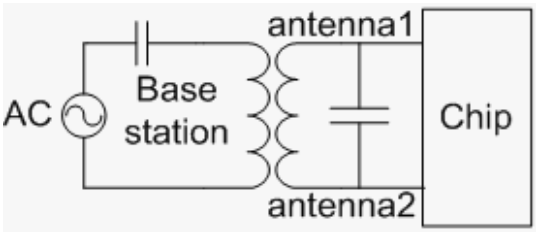

Figure 1. Inductance coupling principle

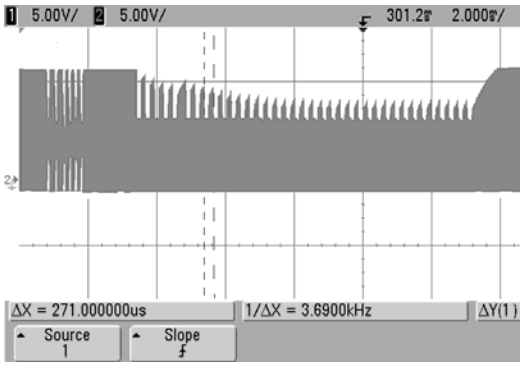

Figure 2. Leakage problem when modulation

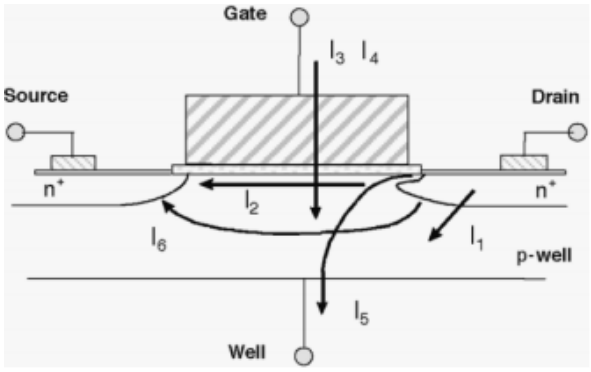

Figure 3. Summary of leakage current mechanisms of deep-submicrometer transistors

3. Theoretical Analysis

First the paper introduces the circuit modules of the chip analog front-end, including rectifier module, amplitude limiting module, band-gap module, clock generation module, modulator module, demodulator module, etc. Dividing the modules into two parts, one is called directly connected module, the other is called indirectly connected module, as shown in figure4. Directly connected modules mainly include the rectifier module and demodulator module which connected with the inductance directly, as shown in figure 5 and figure 6. The leakage mainly comes from the directly connected modules. After the transient simulation, testing antenna1 and antenna2, the waveform is shown in figure 7. Through the observation, we could find that the most negative potential of the antenna1 and antenna2 is 750mV. This is the key to resulting in the leakage. Usually the substrate of the NMOS connected to the ground is no problem in single power supply situation. But if the input signal is below zero volt, it is possible to cause problem. The large signal model [8],[9] of the MOS tube is shown in figure 8. From the figure 8 we can find equivalent diodes between the active area and the substrate. Generally, in single power supply situation, when the NMOS substrate is connected to the ground, the equivalent diodes are reverse-bias and the MOS tube works well. But when the potential of the antenna1 and antenna2 are negative, the equivalent diodes are forward-bias. Then there will be high leakage current on the substrate. The leakage current meets the equation (1) and equation (2). Diode volt-ampere characteristic curve is shown in figure 9. We can find that when the diode voltage reaches the threshold voltage, there will be a large current on the substrate. So when the potential of the antenna1 and antenna2 are negative, there will be leakage current on the

substrate. Measuring the substrate current of the tube which is directly connected to the instance, the waveform is shown in figure 10. We can find power consumption very big. The peak current of the substrate is 550uA. It proves the theory that there is high leakage current between source and substrate through forward-bias pn junction.

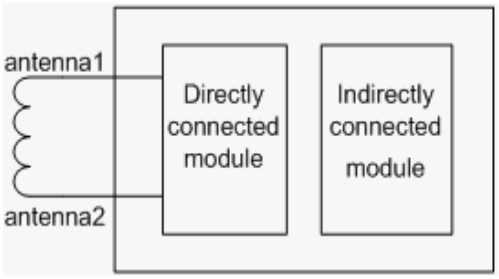

Figure 4. Modules of RFID chip

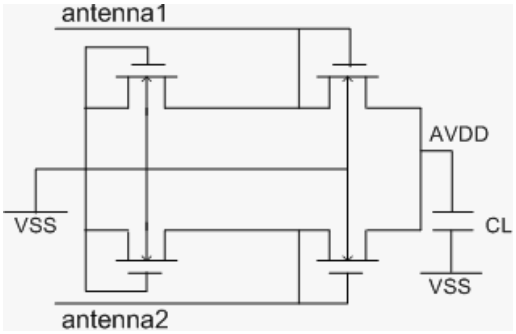

Figure 5. NMOS bridge rectifier circuit

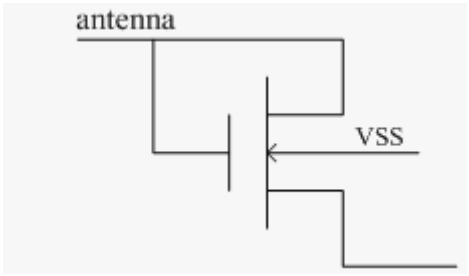

Figure 6. Simplified directly connected module

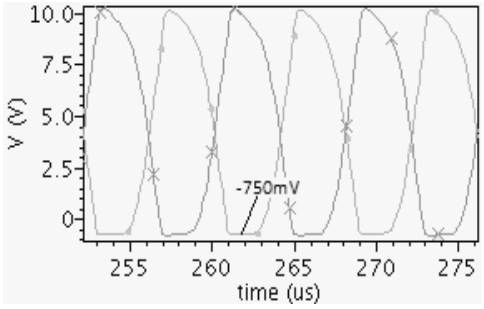

Figure 7. wave of antenna1 and antenna2

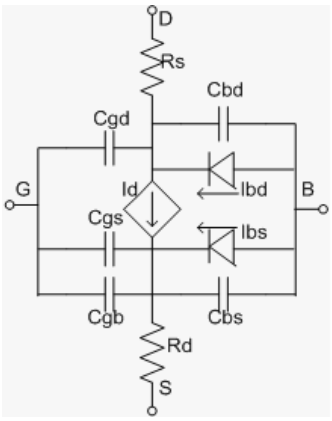

Figure 8. Large signal model

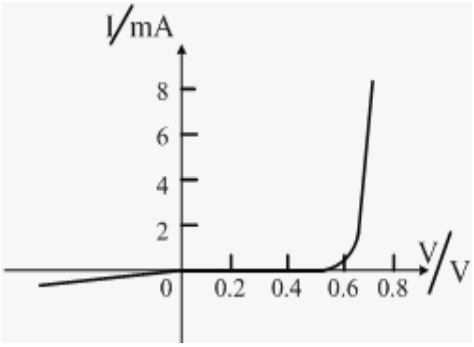

Figure 9. Diode V/A characteristic curve

$$i_{BS} = I_s\left[\exp\left(\frac{qv_{BS}}{kT}\right)-1\right] \quad (1)$$

$$i_{BD} = I_s\left[\exp\left(\frac{qv_{BD}}{kT}\right)-1\right] \quad (2)$$

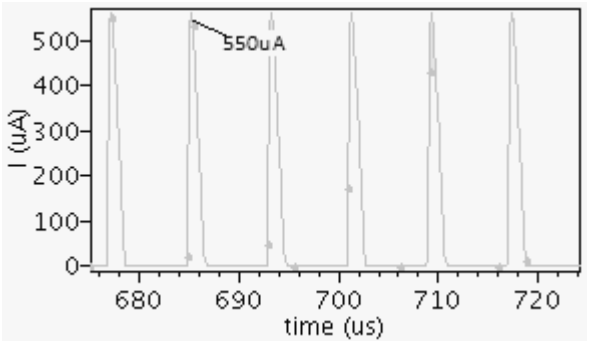

Figure 10. The substrate current

4. Optimized Rectifier Circuit

In view of the above analysis, we find that the most negative potential of the antenna1 and antenna2 can reach 750mV. Then there will be high leakage current on the substrate. What can we do to make the most negative potential of the antenna1 and antenna2 higher? In that case the leakage current will become small. After reading some papers, we find the NMOS gate cross-connected bridge rectifier circuit [10],[11] can make the most negative potential of the antenna higher. The circuit is shown in figure 11. For a single MOS tube, the volt-ampere characteristic curve is shown in figure 12. From the figure 12, we can find that when the gate source voltage is very high assuming the drain current is constant, the drain source voltage will be very small. The MOS tube meets the equation (3). Namely the MOS tube works in linear area. At this time the drain source voltage meets the equation (4). The drain current meets the equation (5) when the MOS tube works in the saturation. From the equation (5) we can get the equation (6). The drain source voltage in the saturation and the drain source voltage in the linear meet the equation (7). If the MOS tube works in the critical saturation, the drain source voltage will meet the equation (8). According to equation (7) and equation (8), we can get the equation (9). From the above analysis, we know when the gate voltage of the gate cross-connected bridge rectifier circuit is very high, two MOS tubes with their gates cross-connected work in the linear area. They meet the equation (9). Namely, the most negative potential of the antenna is very small, less than a driving voltage. However the MOS tubes of the NMOS bridge rectifier circuit are all diode connected form. They all work in the saturated zone. The gate source voltage of these tubes meets equation (6). At this time, the drain source voltage and the gate source voltage are equal. So the drain source voltage of the bridge rectifier circuit is very high. Combined with the theoretical analysis of the second section, we can draw a conclusion that the equivalent diodes between the active area and the substrate of the NMOS bridge rectifier circuit are conduction, but the equivalent diodes between the active area and the substrate of the NMOS gate cross-connected bridge rectifier circuit are not conduction. So the leakage current of the NMOS gate cross-connected bridge rectifier circuit is very small. The simulation result of the NMOS gate cross-connected bridge rectifier circuit is shown in figure 13. We can find that the most negative potential of the antenna is 215mV, far less than the threshold voltage. Measured the substrate current of the MOS tube which is connected with the inductance directly. The result is shown in figure 14. We find that the leakage current is very small, only 1uA. Then we optimized the rectifier circuit and made tape-out verification.

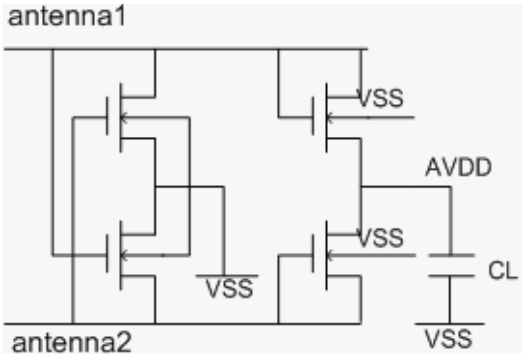

Figure 11. gate cross-connected rectifier

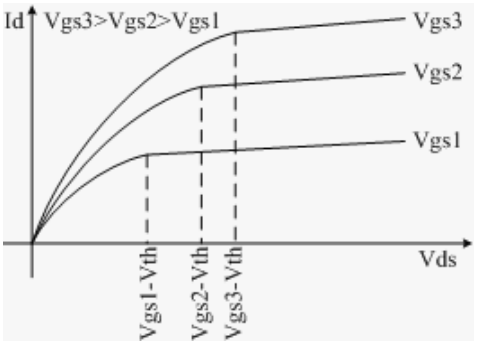

Figure 12. V/A characteristic of MOS tube

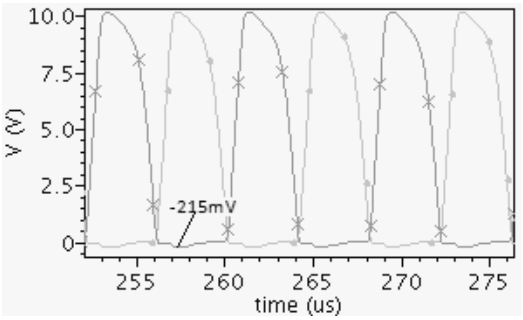

Figure 13. wave of the antenna

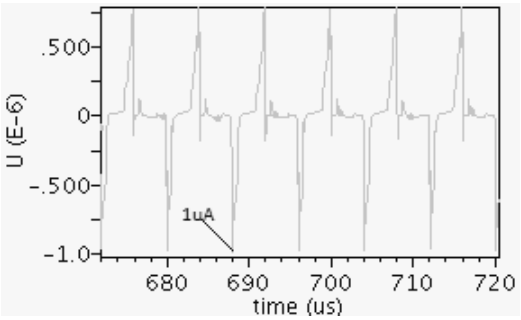

Figure14. substrate current

$$V_{GS} - V_{TH} > V_{DS} \tag{3}$$

$$V_{DS}\left(linear\right) < V_{DS}\left(critical - saturation\right) \tag{4}$$

$$I_D = \frac{1}{2}K'\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 \tag{5}$$

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{K'\frac{W}{L}}} \tag{6}$$

$$V_{DS}\left(linear\right) < V_{DS}\left(critical - saturation\right) < V_{DS}\left(saturation\right) \tag{7}$$

$$V_{DS}\left(critical - saturation\right) = V_{GS} - V_{TH} = \sqrt{\frac{2I_D}{K'\frac{W}{L}}} \tag{8}$$

$$V_{DS}\left(linear\right) < \sqrt{\frac{2I_D}{K'\frac{W}{L}}} \tag{9}$$

5. Comparison and Verification

Comparing the computer simulation results and the tape-out verification results, the first chip's (before optimized rectifier circuit) results are shown in figure 15 and figure 16, and the second chip's (after optimized rectifier circuit) results are shown in figure 17 and figure 18. Figure 15 and figure 17 are similar. But figure 16 and figure 18 are very different. The carrier of figure 16 has obvious attenuation. Comparing figure16 and figure 18, it proves the theory that there is high leakage current between source and substrate. From the four figures, we can conclude the degree of variation between tape-out verification results and computer simulation results for different circuits is different, and when the source potential is much lower than the substrate potential, tape-out verification results and computer simulation results have larger differences. But to what degree is the variation between tape-out verification results and computer simulation results when the source potential is much lower than the substrate potential? And how big the leakage current is? For the first chip, we give quantitative results. The simplified circuit of RFID chip is shown in figure 19. And the actual test results are shown in figure 20. Because the circuit is so complex that we cannot calculate the magnitude of leakage current using a series of formulas. But we have a better method. We can use computer simulating the actual test results to determine the leakage current. When the $I_{leakage}$ equals 425uA, we get figure 21 which is similar to figure 20. And at this time the total current is 518uA through simulation. So the actual leakage current accounts for 82% of total current. But our earlier (before tape-out) simulation results show that the leakage power only accounts for 3% of total power. So when the source potential is much lower than the substrate potential, the actual leakage current increases significantly. And the leakage power of tape-out verification results increases 26.3 times compares with the computer simulation results' when the source potential is -750mV.

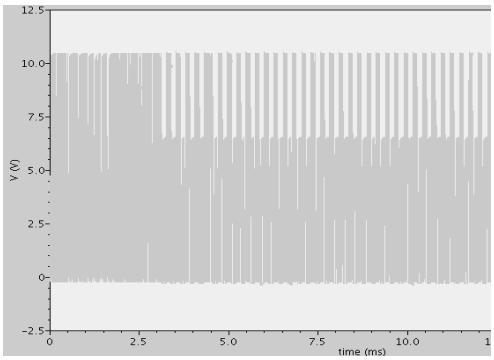

Figure 15. The first chip's simulation result

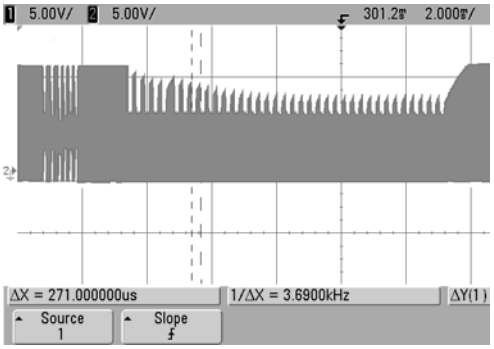

Figure 16. The first chip's actual result

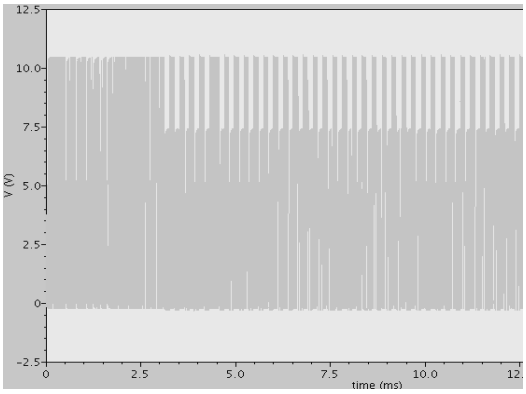

Figure 17. The second chip's simulation result

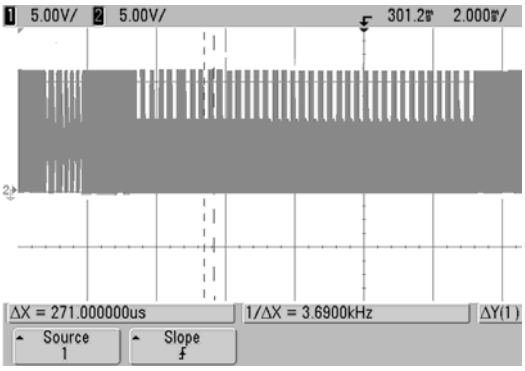

Figure 18. The second chip's actual result

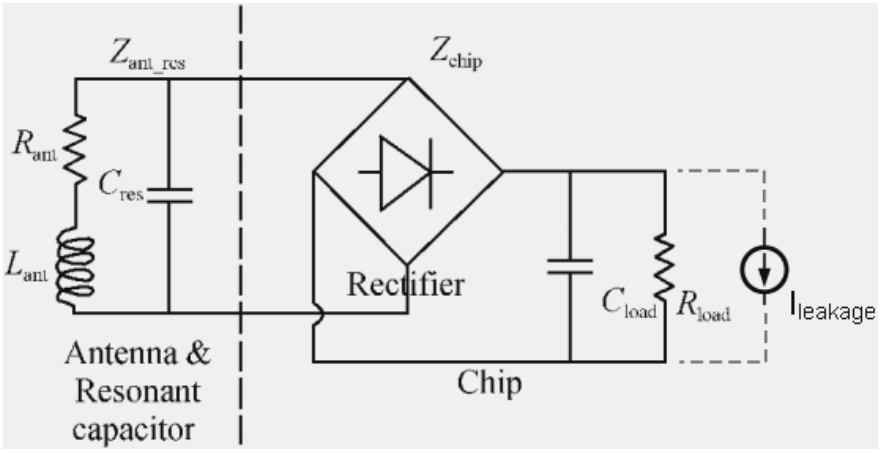

Figure 19. Power transmission in RFID transponder

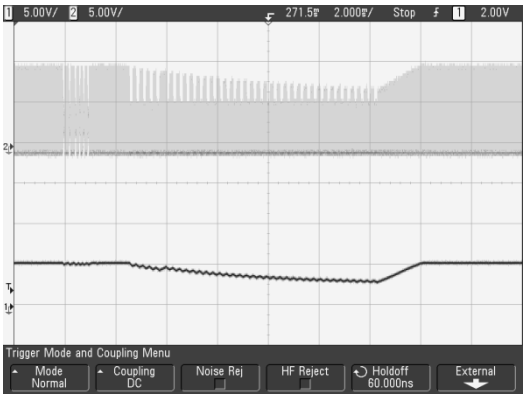

Figure 20. Actual test results

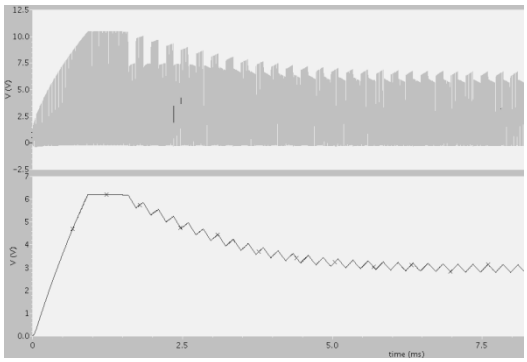

Figure 21. simulating results similar to figure19

6. Conclusion

For the leakage mechanism of RFID chip, the paper gives a theory that there must be high leakage current between source and substrate (namely the forward-bias pn junction leakage). In order to prove this theory, first this paper gives a detailed theoretical analysis. Then we optimized the circuit structure to prove the theory and to solve the leakage problem. At last we made tape-out verification. Through comparing the computer simulation results and the tape-out verification results, we successfully proved the leakage theory. We also drew a conclusion that the degree of variation between tape-out verification results and computer simulation results for different circuits is different. And when the source potential is much lower than the substrate potential, tape-out verification results and computer simulation results have larger differences. This leakage problem is really a hidden problem that we must pay attention to. When the potential of the active area is lower than the substrate, the simulation model is not very ideal. And all kinds of process corners have the deviation. So the actual performance has deviation to the computer simulation results. So we must pay attention to this hidden problem when we do RFID analog circuit design.

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