Buletin Teknik Elektro dan Informatika
(Bulletin of Electrical Engineering and Informatics)
Vol. 2, No. 3, September 2013, pp. 212~217
ISSN: 2089-3191

On the Investigation of a Novel Dual-Control-Gate Floating Gate Transistor for VCO Applications

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Abstract

A new MOS device called Dual-Control Gate Floating Gate Transistor (DCG-FGT) is used as a building block in analog design. This device offers new approaches in circuit design and allows developing new functionalities through two operating modes: Threshold Voltage Adjustable Mode, where the DCG-FGT behaves like a MOS transistor with an electrically adjustable threshold voltage. Mixer Signal Mode where the DCG-FGT can mix two independent signals on its floating gate. This device is developed to be fully compliant with CMOS Non Volatile Memory (NVM) process. An electrical model of the DCG-FGT has been implemented in an electrical simulator to be available for analog design. A DCG-FGT based ring oscillator is studied in this paper.

1. Introduction

All modern communication systems require a stable periodic signal to provide time base for synchronization, for alignment of clock sampling, for clock and data recovery and for frequency synthesis. Monolithically integrated CMOS voltage controlled oscillators (VCO) are for main interest in these domains. The key challenges in VCO development include: design of a high-*Q* tank on a substrate tailored for CMOS, multiband operation using a single VCO, enhanced manufacturability using digital frequency tuning, and optimization of the overall VCO topology for low power operation. According to the targeted operating frequency and field of applications, VCOs are implemented in Bipolar or in standards CMOS technology.

The solution presented here focuses on the integration of non-volatile memory cell (DCG-FGT), previously proposed by Regnier *et al.* in 2004 [1] which is diverted from their initial functionality into simple analog circuit. Indeed, these devices which are intended primarily to store information in the form of electric charges, can offer many advantages as well as simplest topology for analog and/or digital circuit functional blocks. Independent dual-gate transistor can provide interesting approach for basic solutions [2] as well as complex functions like Schmitt triggers [3] while reducing the size of the circuit.

Generally, the VCO can be built using the LC resonator structure [4] or ring oscillator [5] in the CMOS process. We will focus on the study of ring VCO. The ring oscillator VCO constructed from a chain of delay cells and can achieve a wider tuning range. Nevertheless, due to the required turn-on voltage to maintain the transistors of delay cells in proper operation region, the control voltage of delay cells can not exercise the full range of the power supply voltage. This will deteriorate the useful range of control voltage vastly as the power supply voltage keeps scaling down. For extend the control voltage range, a differential delay cell with complementary current control is proposed [6]. In this study we propose to increase the control voltage range with the DCG-FGT transistor used in the delay cell.

We present in this paper a new DCG-FGT based ring VCO operating at wide frequency range from few Hertz to 200MHz. The DCG-FGT transistor and the operating mode are introduced in section 2. Section 3 deals with DCG-FGT model and the related calibration. The new DCG-FGT-based ring VCO is presented in section 4, where the performances in terms of

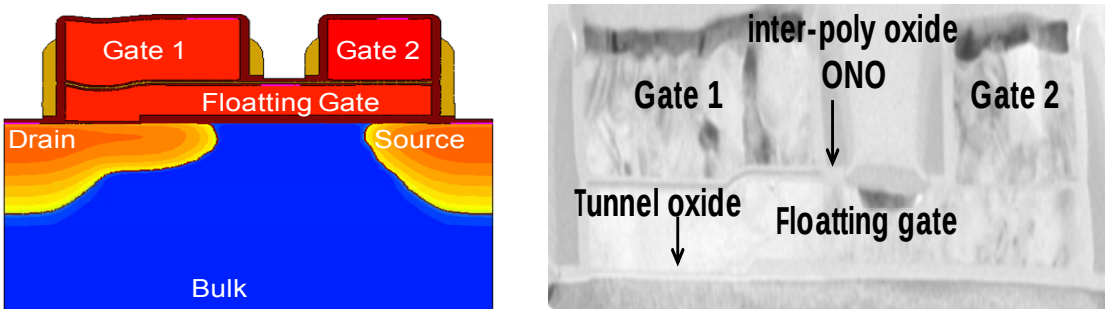
Received January 6, 2013; Revised June 13, 2013; Accepted June 30, 2013

conversion gain, power consumption and robustness of the VCO are dealt with. Section 5 concludes the paper.

2. The Dual-Control-Gate Floating Gate Transistor Concept

2.1. Architecture

Figure 1 presents DCG-FGT architecture used in a memory cell, as proposed by Regnier *et al.* in the previous work [1].



a) b)

Figure 1. a) DCG-FGT architecture, b) Cross section view of a DCG-FGT.

The first layer of polysilicon is used as a floating gate while the second one is used for the two control gates. The small gate, called gate 2 (V_{G2}), has a weak coupling effect and the large gate, called select gate (V_{G2}), has a stronger capacitive coupling with the floating gate. The two polysilicon layers are separated by a 15 nm ONO inter-poly isolation. The first oxide level is composed by thin tunnel oxide (< 10nm) upper the drain area and a thick oxide (20nm). These dual gates are isolated by lateral oxide.

2.2. Operating Principle

This device offers very useful scheme due to its two operating modes allowing very innovative approaches in circuit design [7]. This paper focuses on the threshold voltage adjustable mode where the DCG-FGT behaves like a MOS transistor with an electrically adjustable threshold voltage (**V_{TH}**). The DCG-FGT transistor threshold voltage V_{TH} can be controlled electrically by applying static bias into one of the control gate (G1 or G2). By applying Gauss's law on the floating gate, we demonstrated that V_{TH} is given by [7]:

$$V_{TH} = V_{TH\,0} - V_{G\,2} \cdot \frac{L_{G\,2}}{L_{G\,1}}$$

Where V_{TH0} is the threshold voltage of the DCG-FGT transistor for V_{G2}=0V, L_{G1} and L_{G2} are respectively the lengths of the gate G1 and gate G2. The threshold voltage variation clearly depends on the gate G2 bias voltage (V_{G2}) and on the gate length ratio. To obtain this expression, we assumed that the charge in the floating gate is constant. The transistor will be used in a bias ranging (V_{G2}) from -5V to 5V. In these conditions, it overcomes the phenomena of charge injection type Fowler Nordheim [8], which causes a change in the charge contained in the floating gate. To validate the threshold voltage adjustable mode, measurements were performed on various sizes of DGC-FGT transistor. DCG-FGT device has been successfully implemented on 0.13µm EEPROM CMOS technology from STMicroelectronics. Figure 2 shows a good correlation between simulated and measured values of the threshold voltage V_{TH} versus gate 2 voltage value V_{G2}, for various sizes of DGC-FGT transistor.

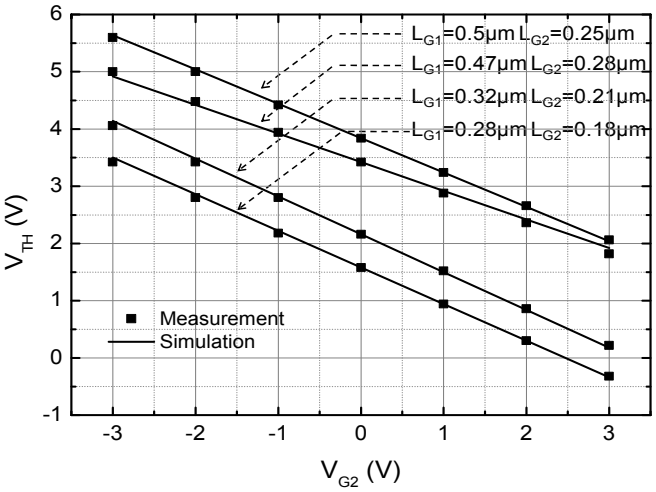


Figure 2. Measured and Calculated Threshold Voltage Values Versus V_{G2} for Different Length Ratio Configurations

3. DCG-FGT Electrical Modeling

Charge neutrality approach coupled with the PSP formulation [9] has been used for the DCG-FGT electrical modeling. In this approach, the charge neutrality, including the charge stored in the floating-gate, is applied to determine the floating gate potential from which all the variables can be computed in the PSP model formulation. The electrical equivalent circuit of DCG-FGT transistor is shown in Figure 4.

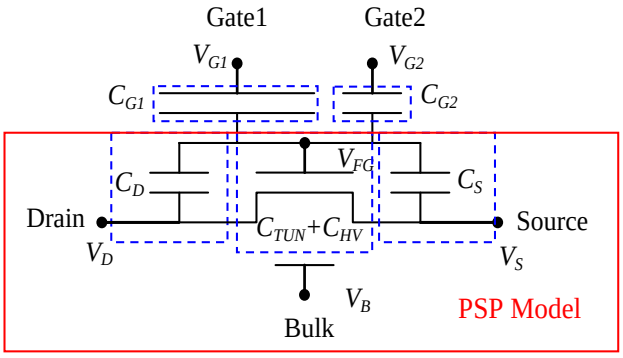


Figure 4. Electrical Equivalent Circuit of DCG-FGT Transistor

The model is running under electrical simulator (ELDO) and is characterized through ICCAP software. It has been validated on 90nm FLASH technology from STMicroelectronics. An accurate and scalable model is available in design framework [10]. The DCG-FGT transistor has been implemented on a FLASH technology to get a uniform tunnel oxide (removal of thick oxide).

4. DCG-FGT Used in Voltage Controlled Oscillator

4.1. Simulation Scheme

Figure 5 depicts an implementation of delay cell based ring oscillator with DCG-FGT transistors. The delay cell is an inverting amplifier composed by DCG-FGT transistor where gate 1 is connected to that of PMOS transistor and gate 2 allows VCO frequency control.

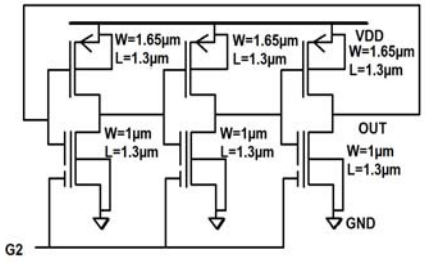


Figure 5. Scheme of Ring VCO Using DCG-FGT Transistor

The oscillation frequency is determined by the delay time introduced by each inverter and the inverter number. The ring VCO output frequency is usually controlled by the bias current that changes the inverters switching threshold voltage (see Figure 7.a). In our case this is done by gate 2 biasing which modify the DCG-FGT transistor threshold voltage and consequently the oscillation frequency.

4.2. VCO Gain Analysis

Figure 6 shows the oscillation frequency of the VCO supplied by V_{DD}=1.2V versus the tuning voltage V_{G2}, for different configurations of control gate lengths. The floating gate length is kept constant at 1.3µm while [a] space of 0.2µm is ensured between gate 1 and gate 2 in order to avoid short circuit between them.

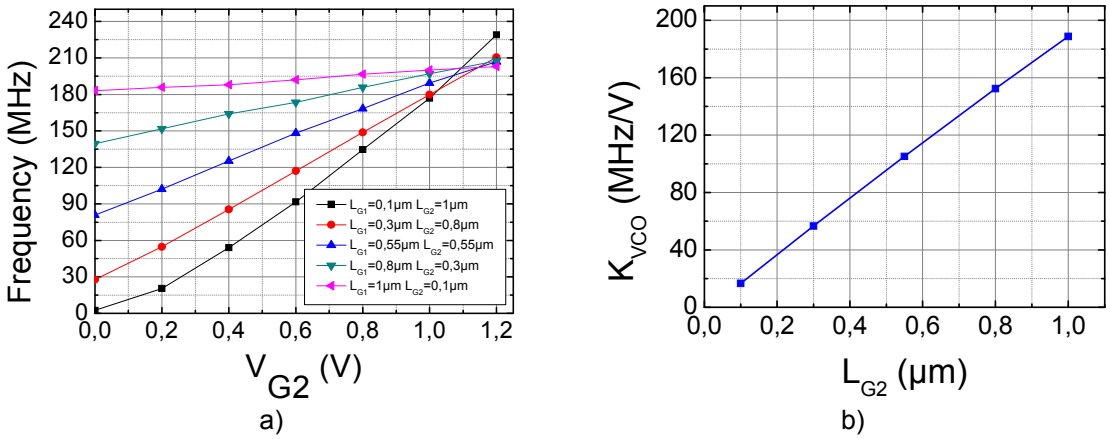


Figure 6. Simulated Characteristics of a) Frequency(V_{G2}) for different gate length b) K_{VCO}(L_{G2}), performed in DCG-FGT based ring VCO.

The set of transfer functions of the proposed VCO depicted in Figure 6a shows very interesting properties:

a. The transfer function Frequency(V_{G2}) is quasi-linear for the full range of control voltage. In fact, since the threshold voltage of the device is also controlled by the voltage applied to the gate 2 which is the same than that used to control the frequency, a non saturated transfer function is obtained. In order to underline this particular property, standard CMOS ring oscillator (illustrated in Figure 7a) has been simulated in the same conditions and shows clearly (Figure 7b) the saturation of the transfer function characteristic since there is no way to the threshold voltage control in this topology. That is, when Vctrl is less than 0.4V (turn-on voltage), control transistor is off and there is no current flowing in the inverter. The output frequency is zero. When Vctrl is greater than 0.8, the control transistor switches from linear mode to saturated mode and no more frequency control is achieved.

b. The gain of the VCO can be easily adjusted only by acting on L_{G2}. Figure 6b shows a linear control of the VCO conversion gain versus the control gate length.

The higher gain (K_{VCO}=189 MHz/V) is obtained for a gate2 length L_{G2}= 0.1µm where the largest threshold voltage variation can be achieved resulting to a wide frequency range varying from 2.5 MHz to 229 MHz under low power consumption of 12.8µA.

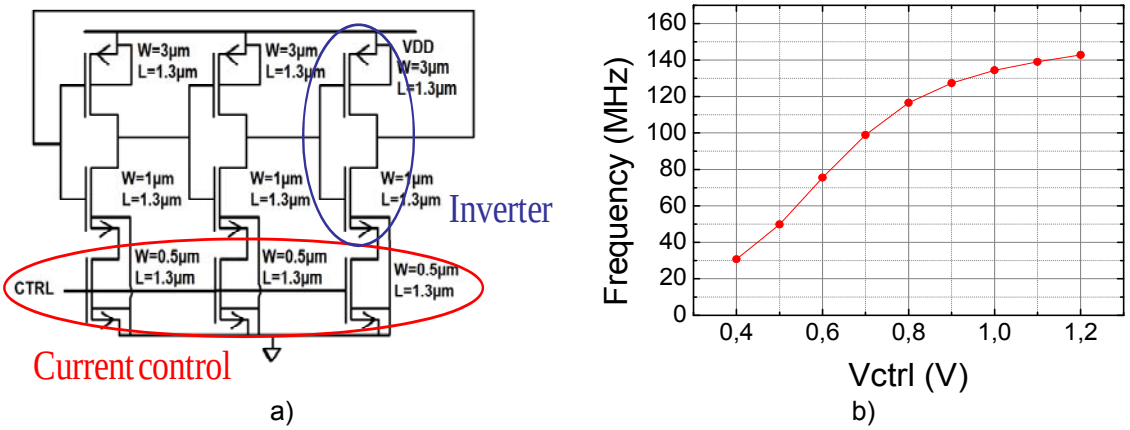


Figure 7. a) Schematic of standard CMOS ring VCO and b) simulated characteristic of Frequency(V_{ctrl})

4.3. Robustness Consideration

4.3.1. Supply Voltage Variation

As process, voltage and temperature (PVT) variations are critical for analog applications, the robustness of the oscillator over supply voltage as well as temperature changes has been investigated. In the first time a change of ±10% of V_{DD} has been taken into account. As stated in Figure 8, only a slight variation of the characteristic Frequency(V_{G2}) is showing the robustness of the design versus supply voltage change.

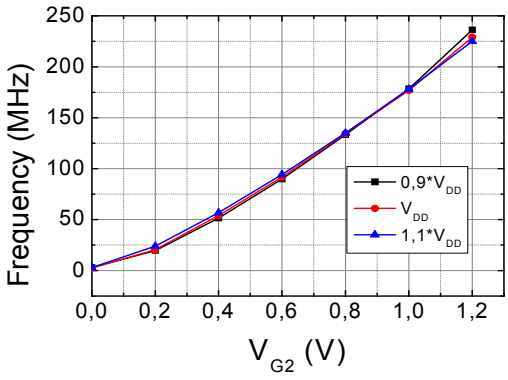


Figure 8. Simulation of Characteristic Frequency(V_{G2}) for Different Supply Voltage

4.3.2. Temperature Variation

The impact of temperature variation has been carried out on the proposed ring VCO as illustrated in Figure 9 where Frequency (V_{G2}) characteristics for different temperatures (-40 to 125 °C) are shown.

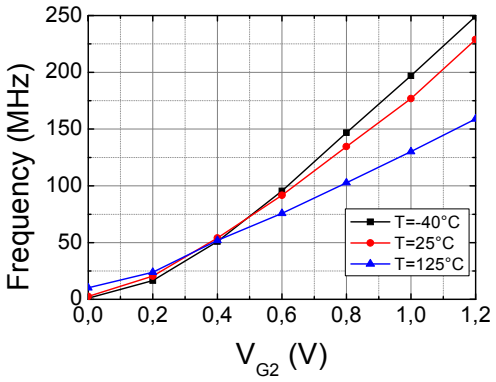


Figure 9. Simulation of Characteristic Frequency(V_{G2}) for Temperatures Ranging from -40 to 125 °C.

The VCO gain decreases significantly with temperature. When the temperature changes from -40 to 125°C, the gain fall down from 206 to 124 MHz/V. As expected, the current VCO has strong temperature dependence like standard CMOS based ring oscillator. However, as shown in section 4.2, the VCO gain can be adjusted by judiciously dimension the gate length ratio of DCG-FGT.

5. Conclusion

A new DCG-FGT transistor concept based on EEPROM structure cell devoid of select transistor has been presented in this paper. This device has been implemented on STMicroelectronics 0.13µm EEPROM technology. This transistor offers two operating modes leading to new approach in circuit design. The design flow has been completed by the extraction of compact model of DCG-FGT which is based on the PSP formulation [10]. This model has been calibrated with dummy cell implemented on STMicroelectronics 90nm FLASH technology. Ring VCO based on this new transistor concept exhibits good performance in terms of gain, frequency range, linearity and power consumption. Good robustness over PVT variation has been pointed out. Example of ring VCO has been developed in this paper, but many applications including comparators, amplifiers, frequency modulators and so on would be addressed by this new device.

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