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Development of an RF IV Waveform Based Stress Test Procedure for use on GaN HFETs

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Abstract

This paper reports on the development of an RF IV waveform based stress test procedure. DC and low-voltage RF characterisation was carried out before and after high power RF stress. RF waveform measurements showed that the exact change in the RF load line induced during RF degradation cannot be directly inferred from the DC or low power RF measurement. The RF degradation takes the form of a knee-walkout, a small pinch-off shift consistent with charge trapping and defect generation, and in addition gate leakage occurs once the RF voltage exceeds a critical voltage.

Keywords: GaN HFET, Reliability, RF Waveforms, Stress Test

1. Introduction

In modern communication systems, components are being pushed into ever more extreme operating environments in order to meet increasing demands. In order to ensure that component lifetimes are sufficient for the life of the product, they are subjected to rigorous reliability testing. This is no different for GaN HFETs, where most reliability testing is based around using DC techniques [1-2], however recently there is a greatly increased interest in the use of RF techniques [3-7].

Although there are concerns about how well DC techniques can accurately reflect the RF performance of the device, they are much simpler and cheaper than RF techniques. They also have the added benefit of being unaffected by reactive parasitic components within the device or packaging. On the other hand using RF techniques has the advantage of being able to place the device closer to, or even under, its actual operating conditions. However the reactive parasitic components of the device and the packaging will begin to have an effect on the measurements. There are two solutions to this, firstly use a fundamental frequency sufficiently low enough that the displacement currents caused by the parasitic reactances can be neglected [3-4]. Alternatively the second solution is to carry out the measurements at the intended operating frequency and then to use a de-embedding process to remove the displacement current caused by the drain-source capacitance (C_{DS}). This is the solution that we have used, along with several others [5-7], for the measurements presented in this paper and our previous work [8-9].

The simplest RF stress test involves measuring the RF power at the input and output of the device [6], from which parameters such as gain and efficiency can be calculated. This was extended to include DC and RF characterisation stages before and after the stress periods, as well as interrupting the stressing period in order to measure DC (voltage and current) and RF (power) figures of merit [7]. This provided a much greater understanding of the nature of the device degradation. However this approach can be improved by the use of an RF IV waveform measurement system, which measures the RF voltages and currents at

the input and output terminals of the device, allowing the exact state of the device to be known during the stress period [5,8]. Here we extend this approach to produce a more complex step stress test [9].

2. Measurement Procedure

The stress test procedure used to make the measurements shown in this paper was adapted from [7] and originally presented in [8]. This is shown in figure 1, and the different stages described below. The procedure was first used with a single stress period to assess how the DC and RF characterisation measurements relate to the RF waveform measurements made during the stress procedure, the results of which are shown in section 3. The procedure was then extended to include four stress periods with a DC and RF characterisation stage between each stress. This was used to perform a drain bias step-stress experiment, the results of which are shown in section 4.
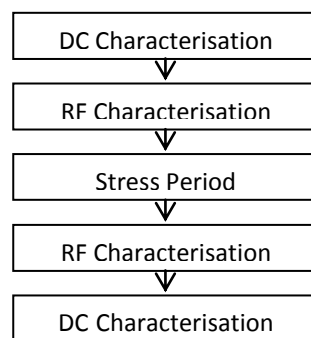
Figure 1 – Flow chart of the stress test procedure

The DC characterisation stage consisted of the DCIV measurement (V_{gs}=-6V to 1.5V in 0.5V steps and V_{ds}=0V to 10V in 0.5V steps) and a gate leakage current measurement (V_{gs}=-5V, V_{ds}=0V). The RF characterisation stage consisted of the single RF measurement of a load line that is directed at the knee of the DCIV from a V_{ds}=10V class A operating point, with the output power saturated. During the RF stress period the device was operated in class AB mode with the fundamental impedance set to the optimum and the second and third harmonics set to short circuits. RF IV waveform measurements were made every 30 minutes.

All of the measurements were performed on our time domain RF IV waveform measurement system [10] equipped with the Envelope Load Pull (ELP) system [11], using a fundamental frequency of 900MHz. The measurements were then de-embedded in order to remove the reactive current caused by the drain-source capacitance. All of the devices used were 2x100µm GaN HFETs from the same wafer with a gate length of 0.6µm, whose DC critical voltage for gate edge degradation was found to be ~30V [2, 12]. While these devices are not the immediate state of the art, the purpose of this paper is not to categorically define the operational constraints of GaN HFETs, in general. It is more to show the techniques that can be used to find such constraints and how RF IV waveform measurements can be used to support reliability measurements.

3. Comparison between Characterisation and Stress Measurements

The stress procedure described in section 2 was used to stress three nominally identical devices for 15 hours at a drain bias of 30V. Two of the three devices tested suffered very similar degradation (devices A and B), while the third (device C) showed very much less

degradation. The reason for this variation in susceptibility is unknown, but does reinforce the importance of a statistically significant sample size in any reliability study. The initial and final RF load lines measurements during the stress periods on device A are shown in figure 2a; along with the RF characterisation and DCIV measured before and after the stress period. It can be seen that for device A (figure 2a) and B (not shown) the results of the degradation suffered by the device are clearly evident in the RF load lines. From these load lines, and the waveforms shown in figure 4, it can be seen that the degradation is most evident in the knee region of the device, manifesting itself as knee walkout or current collapse. The fact that the RF drain current waveforms are still "squared up" after the stress period shows that the device is still being saturated, consistent with the current-limiting virtual-gate mechanism for current-collapse described in [13]. It can also be seen from the DCIV measurements that there is a small shift in the pinch off voltage of the device, suggesting a build-up of negative charge under the gate. Devices A and B also showed an increase of 2 orders of magnitude in the gate leakage current measured during the DC characterisation (not shown) whereas C showed essentially no change.

Figure 2b (devices A, B, and C to show the variation between devices) shows the comparison between the output powers measured during the stress period and with those of the low-voltage RF characterisation measurements made before and after the stress period. From this it can be seen that the change in RF output power measured at either high or low drain voltage agrees reasonably well. Figure 3 shows results which quantify change in RF waveform and demonstrate how the peak drain current and peak voltage varies during the stress period for devices A and B. These results show that the DC and low-voltage RF characterisation measurements only provide a rough approximation to those seen during the RF stress period. They do not show the full extent of the device degradation seen by the measurements made during the RF stress period. This occurs because only the high-voltage RF measurement accesses the regime where strong knee-walkout occurs, limiting the extent of the load line. These results are also consistent with those found in [7].
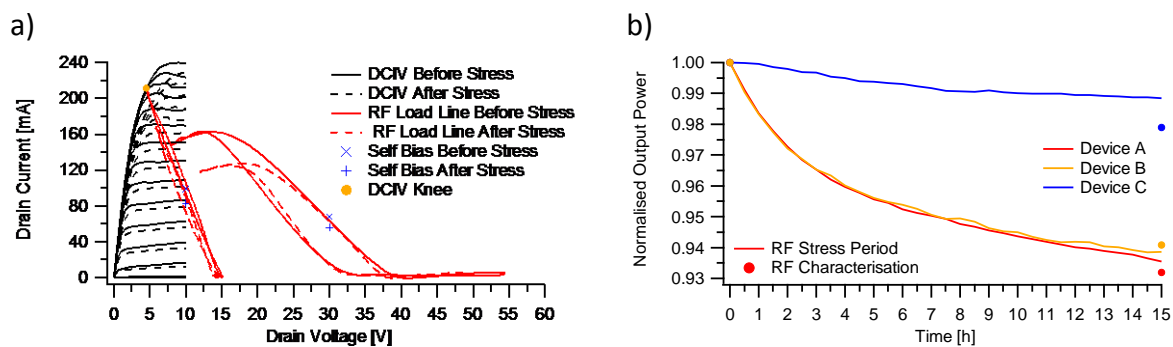
a)

b)

Figure 2 – a) The first and last RF load lines measured during the stress period along with the DCIV and RF characterisation measurements made before and after the stress period, on device A. b) The RF output power measured during the stress period and the before and after RF characterisation measurements, for all three devices.

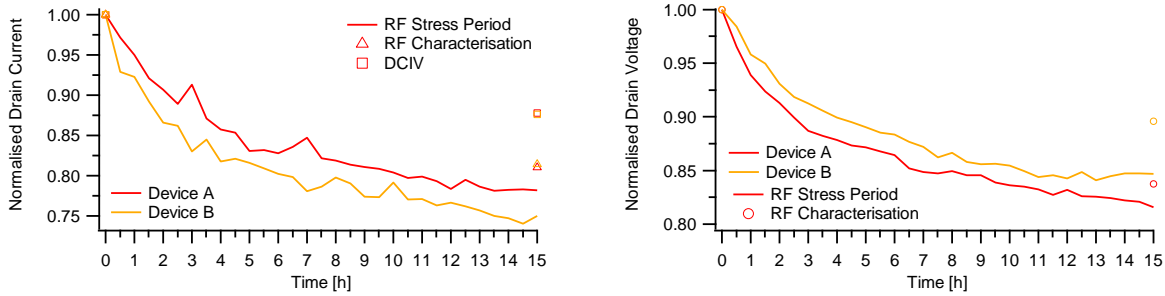a)   b)

Figure 3 – (a) The normalised peak drain current and (b) drain voltage swings measured during the stress period along with those from the RF characterisation measurements, for devices A and B
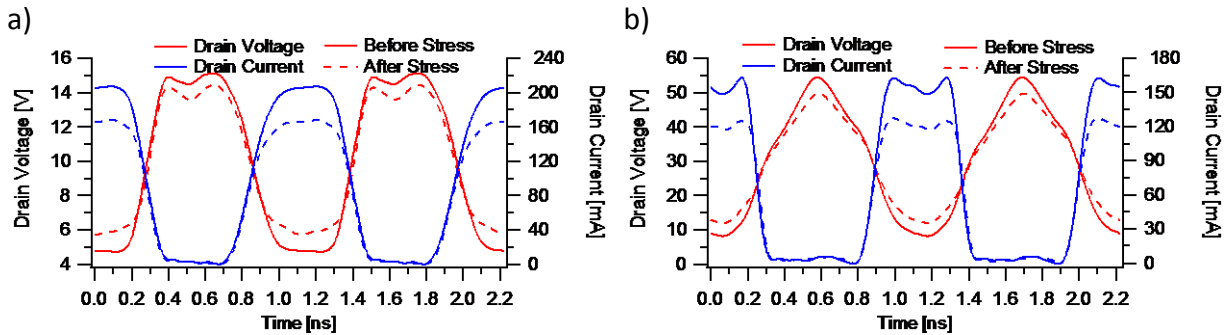

Figure 4 – (a) Drain RF voltage and current waveforms for the RF characterisation load lines, and (b) the initial and final load lines from the stress period shown in figure 2a

4. Drain Bias Step Stress Test

Once it had been established how the DC and RF characterisations related to the waveform measurements made during the stress period, the procedure was used to perform a drain bias step-stress test. The drain bias voltage was initially set to 15V for the first six hour stress period, and then increased in 5V steps for each subsequent six hour stress period, up to 30V for the final period. The initial and final RF load lines from each stressing period are shown in figure 5, below. It should be noted that the final stress period for this experiment will present the device with the same bias, input power and load impedance conditions used in the previous section.
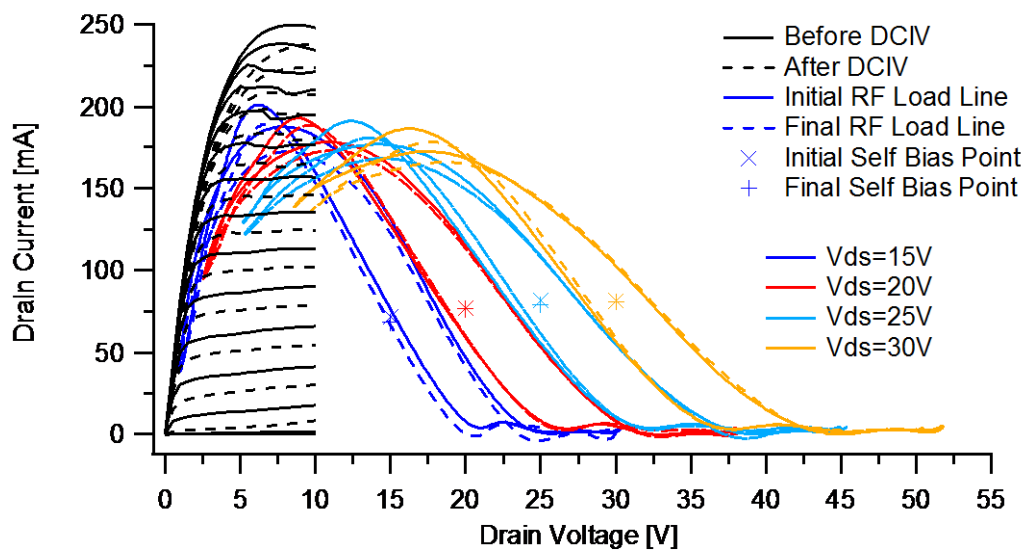

Figure 5 – Initial and final RF load lines of each of the stress periods for the drain bias stress test, along with the before and after DCIV measurements

The output power of the measurements made during the RF stress period is shown in figure 6a, along with the output power of the low-voltage RF characterisation measurements made between each stress period. There was an increase in output power in every period of the stress test due to the increase in drain bias. In order to show any degradation, the step-change in output power between stress periods was removed before normalisation to the first stress period as is shown in figure 6b. Also shown in figure 6a are the gate leakage current measurements, which show a dramatic increase after the stress period where the device was biased at 20V. The values of gate leakage current seen here were similar to those seen in the devices that suffered degradation in the experiments in section 3. It is during this period of the stress test that the RF drain voltage waveforms first extend beyond 30V, which as discussed earlier is the critical voltage for gate edge leakage for the devices used here. This result is consistent with the model that the gate edge breakdown process is field driven [2], but also suggest that the breakdown occurs on a timescale shorter than the RF period. The fact that the sudden increase in gate current is uncorrelated with the gradual RF degradation suggests, not surprisingly, that these are essentially independent processes. Gate leakage is a point failure whereas the degradation occurs across the entire gate width.

As with the experiments in the previous section the DC and low-voltage RF characterisation measurements show only a moderate degree of agreement with the high voltage RF measurements made during the stress period. Figure 7a shows the maximum RF drain currents, and figure 7b the RF drain voltage swings, from the waveform measurements made during the stress period, and also the low-voltage RF characterisation measurements. Additionally figure 7a shows the peak drain current of the DCIV. As with the normalised output power in figure 6b the natural increase in voltage swing caused by increasing the drain bias voltage is taken into account in figure 7b, so that only the changes caused by the device degradation are shown.

a)   b)
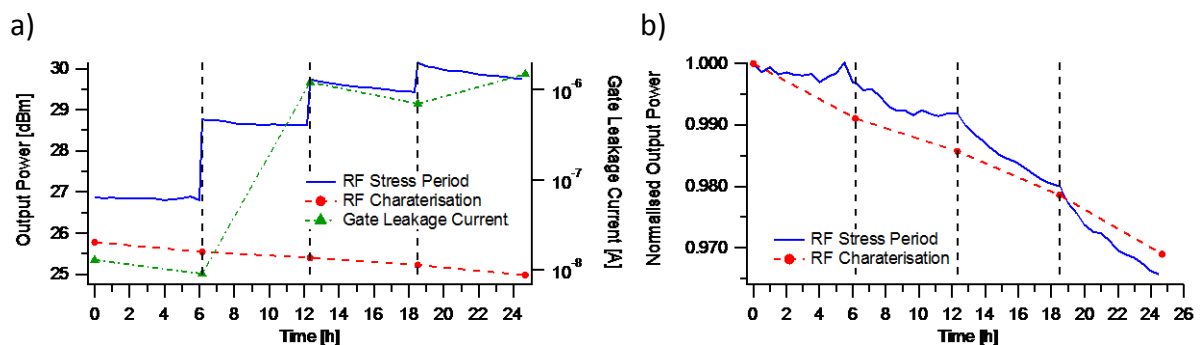

Figure 6 – a) Comparison of the RF output power measured during the stress period and the RF characterisation measurements in between the stress periods, together with the gate leakage current. b) The normalised output power with power steps removed.

a)   b)
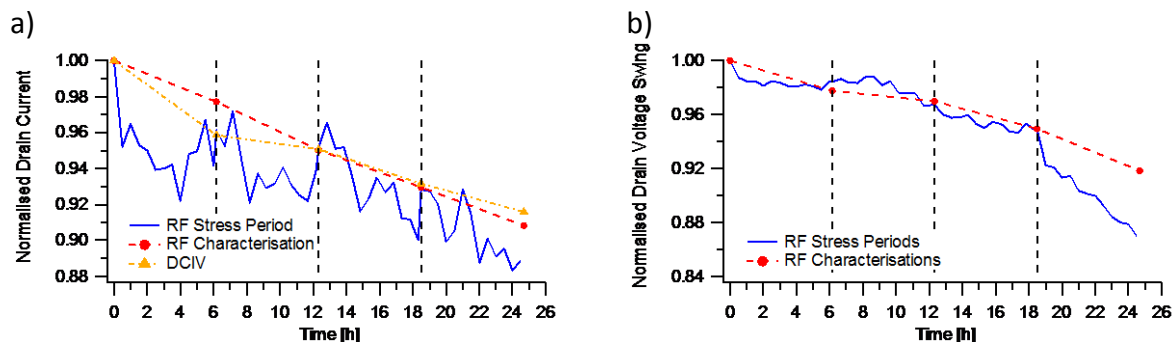
Figure 7 – (a) The normalised peak drain current and (b) drain voltage swings measured during the stress period along with those from the RF characterisation measurements. Step changes between stress periods have been removed in order to show degradation.

5. Conclusions

In this paper we have developed an RF IV based stress test procedure, primarily for use on GaN HFETs, where we have directly measured the RF stress IV waveforms. This procedure was first used to investigate how the measurements made during a high power RF stress period relate to those made during DC or low-voltage RF characterisation measurements made before and after the stress period. It was then shown how the stress testing procedure could be used with multiple stress periods to create a step stress test procedure, which was used to find the maximum safe drain bias.

It has been found that the percentage change in output power before and after RF stress was the same whether measured at either low or high drain voltage. However, when the actual RF waveforms were measured during the RF stress, it was found that the RF stress produced a larger percentage degradation in the peak RF drain currents and drain voltage swing of the high power RF measurements. Hence detailed RF measurements are required to see the full impact of RF stress induced degradation on the RF load line. From the drain bias step-stress test a safe bias point was found, with gate leakage degradation occurring as soon as the RF drain voltage swing exceeded a critical voltage.

Acknowledgement

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