View metadata, citation and similar papers at core.ac.uk

brought to you by CORE

provided by Explore Bristol Research

Silvestri, M., Uren, M. J., & Kuball, M. (2012). Dynamic Transconductance Dispersion Characterization of Channel Hot-Carrier Stressed 0.25um AlGaN/GaN HEMTs: Electron Device Letters, IEEE. IEEE Electron Device Letters, 33(11), 1550-1552. 10.1109/LED.2012.2214200

Link to published version (if available):
10.1109/LED.2012.2214200

Link to publication record in Explore Bristol Research
PDF-document

University of Bristol - Explore Bristol Research

General rights

This document is made available in accordance with publisher policies. Please cite only the published version using the reference above. Full terms of use are available: http://www.bristol.ac.uk/pure/about/ebr-terms.html

Take down policy

Explore Bristol Research is a digital archive and the intention is that deposited content should not be removed. However, if you believe that this version of the work breaches copyright law please contact open-access@bristol.ac.uk and include the following information in your message:

• Your contact details
• Bibliographic details for the item, including a URL
• An outline of the nature of the complaint

On receipt of your message the Open Access Team will immediately investigate your claim, make an initial judgement of the validity of the claim and, where appropriate, withdraw the item in question from public view.

Dynamic Transconductance Dispersion Characterization of Channel Hot Carrier Stressed 0.25-μm AlGaN/GaN HEMTs

Marco Silvestri, *Member, IEEE*, Michael J. Uren, *Member, IEEE*, and Martin Kuball

Abstract— **Using the dynamic transconductance frequency dispersion technique, we characterize unstressed and hot electron stressed short channel AlGaN/GaN High Electron Mobility Transistors (HEMT). The results reported in this letter demonstrate that the stress-induced degradation in DC and pulsed characteristics is unlikely to be ascribable to sizable trap generation at the AlGaN/GaN interface.**

Index Terms— **HEMT, hot carriers, interface traps, reliability**

I. Introduction

AlGaN/GaN High Electron Mobility Transistors (HEMT) are among the most promising candidates for future high power switching and microwave systems. However, the long-term reliability of such devices is still under investigation. In particular, the physical location and activation energy of hot electron induced traps is still debated [1], [2]. Impact ionization and the resulting defects in AlGaN/GaN HEMTs have been observed by different groups using optical and electro-optical techniques but providing different interpretations and models [2]-[4]. Conductance techniques are often used to electrically evaluate trap characteristics in large area MOS capacitors [5]-[7], however in HEMTs these become inaccurate in the case of short channel devices due to the weak capacitance signal offered by the small gate area. The use of transconductance (g_m) frequency dispersion to characterize traps has been proposed in several papers for both GaN and GaAs MESFETs [8], [9]. However, all the previous analyses focused on the real part of the measured g_m, not exploiting its imaginary part. In fact, it has been theoretically demonstrated that the imaginary part of the inverse of the g_m is conveniently related to the equivalent parallel trap admittance, and experimentally evaluated on silicon on insulator MOSFETs [10], [11]. As a consequence, any trap dynamic loss is reflected in the drain current via the device g_m without any need to measure the transistor capacitance. To date, this approach has not been taken advantage of for reliability studies of AlGaN/GaN HEMTs. In particular, the presence of channel hot carrier (CHC) induced traps can be assessed at or near the heterojunction interface which is often proposed as the location degraded by hot electrons [2], [12]. For the devices and stress conditions reported in this letter, we demonstrate that hot carrier stress does not result in a sizable density of traps at the heterointerface despite producing significant device degradation.

Manuscript received June 2012. This work was supported by the UK Engineering and Physical Science Research Council (EPSRC), EP/I033165/1.

M. Silvestri, M. J. Uren, and M. Kuball are with the Center for Device Thermography and Reliability (CDTR), H.H. Wills Physics Laboratory, University of Bristol, BS8 1TL, Bristol, UK; e-mail: marco.silvestri@bristol.ac.uk.

II. Experimental Setup and Devices

AlGaN/GaN HEMTs grown by metal-organic vapor phase epitaxy on SiC substrate and fabricated into silicon nitride passivated devices with 4μm source-drain gap, T-gates of 0.25μm length, and 26-nm AlGaN layer thickness were studied. Iron was incorporated into GaN during growth with a residual density of 10^{17} cm^{-3} in the channel region. The frequency response was evaluated with a Solartron 1255A Frequency Response Analyzer (FRA) in the range between 1 Hz and 100 kHz. The measurement system used in this work is sketched in the inset of Fig. 3a. The HEMT is biased in the sub-threshold region in order to minimise shorting effects of the inversion layer capacitance, and the gate voltage is modulated with a low AC signal (10 mV). The device is operated in the ohmic regime with a drain bias of 50 mV and the source current measured with a wideband, low-noise current to voltage (*I-V*) converter. The frequency dispersion was measured over the temperature range from 20°C to 80°C. Devices were CHC stressed at V_{gs}= -2V and V_{ds}= 20V in the semi-ON condition, which has been reported to be the conditions which maximise hot-electron damage [2]. Electrical DC characterisation and stress were performed with an Agilent 4156A parameter analyzer. Pulsed current-voltage characteristics have been measured with a Dynamic I-V Analyzer (DIVA) [13].

III. Results and Discussion

Fig. 1 shows the DC I_{ds}-V_{gs} characteristic as well as the transconductance before and after CHC stress. After stress, the maximum drain current (V_{gs}=0V) decreased by about 30% and the transconductance peak by 20%, with about +100 mV pinch-off voltage shift. Fig. 2 reports the DC and the pulsed I_{ds}-V_{ds} characteristics before and after CHC stress. Following stress, there was no obvious change in pinch-off voltage under pulse conditions but the transient increase in R_{on} was up to 40% and there was a corresponding transient reduction in the

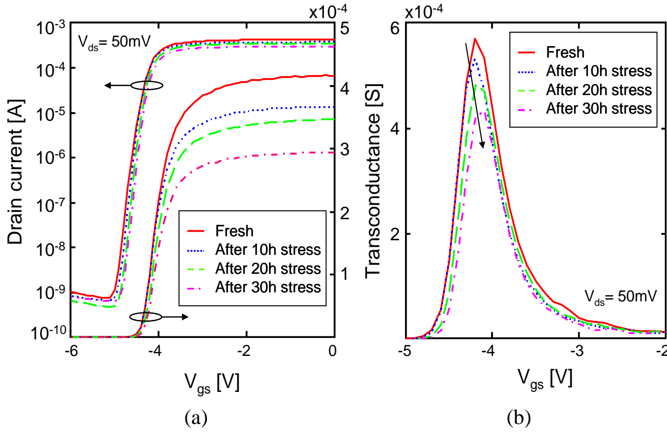

Fig. 1. DC drain current (a) and transconductance (b) vs. V_{gs} of AlGaN/GaN HEMTs before and during CHC stress; width 2x50 µm.

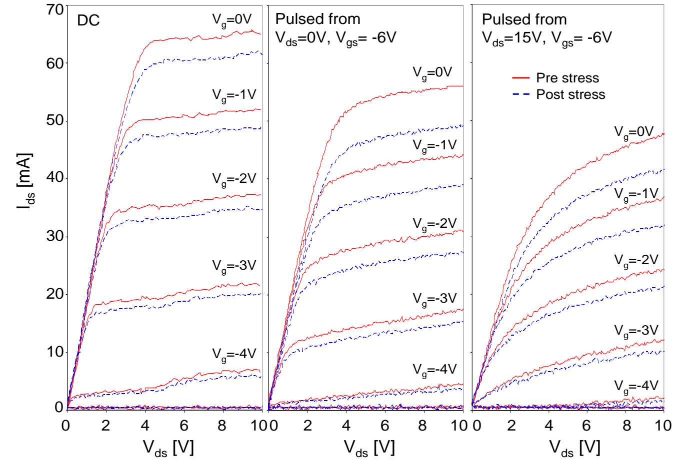

Fig. 2. DC and pulsed drain current vs. V_{ds} of AlGaN/GaN HEMTs before and after CHC stress; width 2x50 µm.

saturation current. This suggests that the location of these stress-induced traps was not under the gate, but located in the proximity of the drain either on the surface or close to the AlGaN/GaN interface.

In order to characterize the origin of the degradation, i.e., whether interface traps are generated by CHC, dynamic transconductance dispersion measurements were performed. Fig. 3a shows the g_m phase shift versus frequency measured at different temperatures in an unstressed device around the same value of g_m ~ 4x10^{-5} S to enable easy comparison. There is a distinct peak in the phase shift; a corresponding small increase of g_m with frequency was observed which reflects the same physical mechanism but is much less clearly apparent. This demonstrates the effectiveness of measuring the dispersion in phase rather than g_m. In fact, the trap conductance G_p/ω, assuming a constant mobility, is related to the phase shift through the imaginary part of the inverse of g_m through the equation $G_p/\omega=-qC_{barrier}I_{ds}(kT)^{-1}Im(1/g_m)$, [11], where q is the electronic charge, $C_{barrier}$ is the AlGaN barrier capacitance, I_{ds} is the drain current, k the Boltzmann's constant, T the temperature in Kelvin. Using the data shown in Fig. 3a, the trap conductance, G_p/ω, was determined and is illustrated in Fig. 3b as a function of frequency for the different temperatures for an unstressed device. This temperature dependent phase shift peak indicates the presence of slow traps in or close to the AlGaN/GaN channel in agreement with [14]. However the peak frequency did not vary with the DC gate bias at any temperature, and this necessarily means that these are not preferentially located at or close to the interface itself. This observation arises because the characteristic trap-time τ for interface states is inversely proportional to the density n_s of electrons in the channel through the relation $\tau=1/v_{th}\sigma_t n_s$, where v_{th} is the thermal velocity, and σ_t the trap capture cross-section. Consequently, any change in the DC gate voltage results in a change in n_s and hence would change the peak frequency.

Data reported in Fig. 3b was well fitted using the model $G_p/\omega=qD_t(2\omega\tau)^{-1}\{ln[1+(\omega\tau)^2]\}$, representing the conductance G_p/ω for a continuum of trap energy levels and for a given areal density D_t and characteristic time constant τ [5]. The areal density of traps extracted from the unstressed G_p/ω peak in Fig. 3b was ~ 7x10^{11} cm^{-2} eV^{-1}. Moreover, from the shift of the G_p/ω peak with temperature we determined an activation energy of 0.7 eV as reported in the inset of Fig. 3b.

Concerning the impact of hot carrier stress on trap generation, the conductance extracted before and after CHC stress is reported in Fig. 4a, showing little change with stress. The trap areal density as a function of the drain current was determined as shown in Fig. 4b, indicating perhaps a slight increase after stress up to ~ 1x10^{12} cm^{-2} eV^{-1}. As before, no DC-bias dependent conductance was observed.

In contrast to interface traps, bulk traps, either defects distributed within the AlGaN barrier or the GaN buffer would not show a distinct bias dependence as observed in our measurements (see the inset to Fig. 4a). Assuming these are GaN bulk traps 0.7 eV below the conduction band, gives a cross-section of 10^{-12} cm^2. This is reasonably consistent with published energy levels for Fe in GaN but the cross-section is much larger [15].

The dynamic g_m measurement does not show any indication of interface traps either before or after stress. We can conceive of three possibilities as to why we cannot see any such defects. Firstly the defects may have a cross-section such that they cannot respond in the accessible measurement time window. We estimate that we would have easily observed any interface traps with a density > 10^{10} cm^{-2}eV^{-1} and cross-section between 10^{-19} and 10^{-15} cm^2 not hidden by the bulk trap response. This spans the range for such defects seen in other systems. Secondly, the interface traps may not form a continuum in energy but exist at a discrete energy level outside the range of surface Fermi level accessed in this study of about 0.1 eV to 0.4 eV below the conduction band. Or thirdly, any stress induced interface traps are created in the ungated drain-gate access region well away from the gate corner so that their occupancy can not be modulated during measurements. All of these are possible, but it strongly constrains the location and properties of such AlGaN/GaN interface states. The CHC performance degradation reported in this work is similar in degree to that reported by other authors [2], [16]. CHC has previously been suggested to result in interface trap formation, but based on the results reported here, it is unlikely to be creating interface traps under the gate or in the vicinity of the

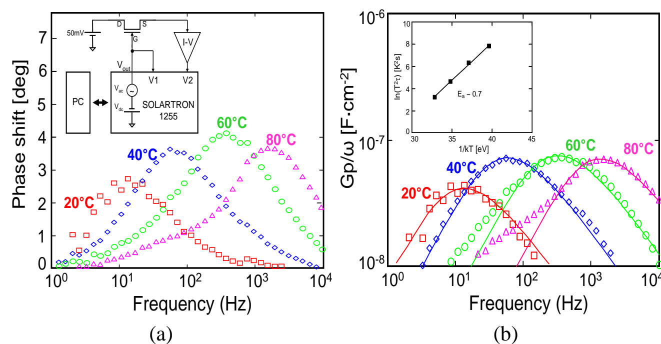

Fig. 3. (a) Measured phase shift dispersion and (b) Extracted conductance G_p/ω vs. frequency at different temperatures for unstressed device fitted with a continuum model. The extracted activation energy is about 0.7 eV as reported in the inset of (b).

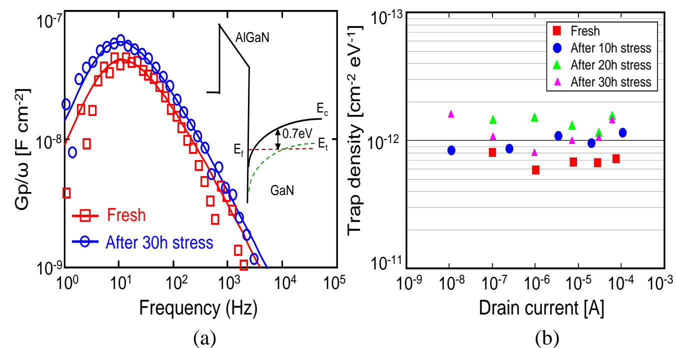

Fig. 4. (a) Bulk trap conductance vs. frequency before and after CHC stress; (b) Extracted trap densities vs. drain current before and during CHC stress.

gate corner. Based on this evidence and on the results of Fig. 1, we believe the traps are most likely to be located at the AlGaN surface.

In conclusion, electronic traps in AlGaN/GaN HEMTs have been measured by means of the dynamic transconductance frequency dispersion technique. This approach allows information to be gained on traps under quasi-equilibrium conditions in short-channel devices. The studied devices showed the signature of bulk trapping with activation energy of 0.7 eV consistent with the energy level for Fe-impurity in GaN. For the conditions reported in this work we found no evidence for interface traps either before or after CHC stress, whereas pulse measurements suggested that the damage is more likely to be surface related.

Acknowledgment

We would like to thank QinetiQ Ltd and the UK MOD for providing the devices.

References

[1] M. Kuball, M. Ťapajna, R. J. T. Simms, M. Faqir, and U. K. Mishra, "AlGaN/GaN HEMT device reliability and degradation evolution: Importnace of diffusion processes", *Microel. Reliab.*51 (2011) 195-200.

[2] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of GaN high-electron-mobility transistors: state of the art and perspectives", *IEEE Trans. Dev. Mat. Reliab.,* vol. 8, no. 2, pp. 332-343, June 2008.

[3] N. Killat, M. Ťapajna, M. Faqir, T. Palacios, and M. Kuball, "Evidence for impact ionization in AlGaN/GaN HEMTs with InGaN back-barrier", *Electronics Letters*, vol. 47, no. 6, 17th March 2011.

[4] M. Ťapajna, R. J. T. Simms, Y. Pei, U. K. Mishra, and M. Kuball, "Integrated optical and electrical analysis: identifying location and properties of traps in AlGaN/GaN HEMTs during electrical stress", *IEEE Electron Dev. Lett.,* vol. 31, no. 7, pp.662-664, July 2010.

[5] E. H. Nicollian and J. R. Brews, *MOS physics and technology*, Wiley, New York, 1982.

[6] R. Stoklas, D. Gregušová, J. Novák, A. Vescan, and P. Kordoš, "Investigation of trapping effects in AlGaN/GaN/Si field-effect transistors by frequency dependent capacitance and conductance analysis", *Appl. Phys. Lett.* 93, 124103 (2008).

[7] M. J. Uren, V. Nayar, K. M. Brunson, C. J. Anthony, J. H. Stathis, and E. Cartier, "Interface state capture cross-section measurements on vacuum annealed and radiation damaged Si:SiO_2 surfaces", *Journal of the Electrochemical Society* 145(2), 1998.

[8] S. S. Islam, A. F. M. Anwar, and R. T. Webster, "A physics-based frequency dispersion model of GaN MESFETs", *IEEE Trans. Electr. Dev.,* vol. 51, no. 6, pp. 846-853, June 2004.

[9] J. M. Golio, M. G. Miller, G. N. Maracas, and D. A. Johnson, "Frequency-dependent electrical characteristics of GaAs MESFETs", *IEEE Trans. Electr. Dev.,* vol. 37, no. 5, pp. 1217-1227, May 1990.

[10] H. Haddara, T. Elewa, and S. Cristoloveanu, "Static and dynamic transconductance model for depletion-mode transistors: a new characterization method for silicon-on-insulator materials", *IEEE Electr. Dev. Lett.,* vol. 9, no. 1, pp. 35-37, January 1988.

[11] H. Haddara and G. Ghibaudo, "Analytical modeling of transfer admittance in small MOSFETs and application to interface state characterization", *Solid-State Electronics,* vol. 31, no. 6, pp. 1077-1082, 1988.

[12] C-Y Hu and T. Hashizume, "Non-localized trapping effects in AlGaN/GaN heterojunction field-effect transistors subjected to on-state bias stress", *J. Appl. Phys,* 111, 084504 (2012).

[13] C. P. Baylis II, L. P. Dunleavy, "Performing and analyzing pulsed current-voltage measurements", *High Frequency Electronics*, pp. 64-69, 2004.

[14] W. Kruppa, S. C. Binari, and K. Doverspike, "Low-frequency dispersion characteristics of GaN HFETs", *Electronics Letters*, vol. 31, no. 22, pp. 1951-1952, 26th October 1995.

[15] T. Aggerstam, A. Pinos, S. Marcinkevicius, M. Linnarsson, and S. Lourdudoss, *J. Electronic Mater.* 36 (12), 1621 (2007).

[16] Y.S. Puzyrev, T. Roy, M. Beck, B. R. Tuttle, R. D. Schrimpf, D. M. Fleetwood, and S. T. "Dehydrogenation of defects and hot-electron degradation in GaN high-electron-mobility transistors", *J. Appl. Phys.* 109, 034501 (2011).