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On the link between electroluminescence, gate current leakage and surface defects in AlGaN/GaN high electron mobility transistors upon off-state stress

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Abstract. The degradation of AlGaN/GaN high electron mobility transistors after off-state stress is studied by means of electroluminescence (EL) analysis, gate leakage current (I_g) monitoring, and atomic force microscopy (AFM) mapping of the semiconductor surface. It is found that the degradation of I_g upon stress is due to the combined effect of the individual defects underlying each of the EL spots, which contribute a few µA each to the total I_g. After removal of contacts and passivation, a direct one-to-one correspondence between EL spots and pits on the semiconductor surface is found. Reverse bias, conducting-tip AFM imaging showed that these surface pits do indeed act as leakage paths. Thus, the direct relationship between EL hot spots, surface pits and gate current leakage is demonstrated. Discussion on the morphology of the surface pits and their possible origin is also provided.

AlGaN/GaN high electron mobility transistors (HEMTs) have shown excellent performance in high frequency and high power applications, mainly due to their high breakdown voltage and high electron mobility[1]. However, the long-term reliability of these devices is still a challenge that hinders their wide commercial deployment[2]. In order to increase the lifetime of AlGaN/GaN HEMTs, it is essential to have a detailed understanding of the mechanisms underlying the degradation of these devices. It has previously been reported that the gate leakage current, I_g, degrades when the devices are operated in pinched off conditions or when the gate Schottky contact is reverse biased [2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12]. Some reports have correlated the increase in I_g during off-state stress of the devices with the appearance of grooves and v-shaped pits on the surface of the semiconductor, located at the edges of the gate contact [6, 7, 9, 12]. In many cases, these surface defects appear when the gate-drain voltage exceeds a particular threshold value. Therefore, it was proposed the defects are related to the inverse piezoelectric effect due to the high electric field present, in particular near the drain edge of the gate[7]. However, the increase in I_g can also be induced on the devices at lower bias values if they are stressed for long enough time[4], suggesting an alternative time-dependent process such as diffusion or surface reactions, possibly related to the presence of oxygen [9, 13, 14].

It has also been reported that off-state stress of AlGaN/GaN HEMTs results in the progressive appearance of electroluminescence (EL) spots, predominantly on the drain side of the gate[3, 5, 8, 10, 11]. The total integrated intensity of the emitted EL correlates with the current leakage through the gate[3, 10, 11]. Actually, it is therefore usually assumed that the appearance of EL spots in AlGaN/GaN HEMTs during off-state stress is related to the progressive formation of pits on the surface of the semiconductor that would act as leakage paths for the gate current, so the phenomena

of v-shaped pit formation, increase in leakage current and EL spots would have a common origin. However, no direct experimental evidence of this one-to-one relationship between EL hot spots and surface defects has been provided so far, nor is there any detailed understanding of the physics of this degradation. In this letter, we provide direct evidence of the correspondence between EL spots, surface defects and leakage current, together with a detailed study of the pit morphology, focusing on the mechanisms responsible for off-state degradation.

The devices studied here were grown on semi-insulating SiC by metal-organic chemical vapor deposition and consist of an Fe doped GaN buffer layer with a 25 nm-thick AlGaN (28% Al) barrier on top. Ti/Al/Pt/Au ohmic contacts were used for the drain and source, whereas a Ni/Au Schottky contact was employed for the gate. The gate length in these devices was 0.6 µm, and the source-gate and gate-drain distances were 1 and 2.4 µm respectively. The devices were passivated with a multilayer of $Si_3N_4/SiO_2/Si_3N_4$, and were isolated by mesa etching. The devices were biased at V_{gs} = -15 V and at a V_{ds} value high enough to induce the appearance of EL spots (typically at 30-50 V). EL images from the devices were taken in dark conditions through a microscope lens (×50, numerical aperture = 0.5) by means of an astronomy-grade charge-coupled device (CCD) camera set at an exposure time of 1 s and a repetition rate of 2 - 3 s. During the stress experiment, I_g was also monitored at a repetition rate of 0.1 s. At the end of each experiment, an EL picture at V_{gs} = -15 V and a low V_{ds} value was taken to ensure the EL spots were still visible, i.e. that the damage due to off-state stress was permanent.

Figure 1(a) shows an EL image from a representative 50 µm-wide device after 760 s at V_{ds} = 30 V and V_{gs} = -15 V. The EL image is overlaid on a picture of the device taken under white light illumination. A set of EL spots can be seen along the

drain edge of the gate, associated with the higher electric field in that region. This phenomenon was consistently observed in all the devices tested, and, in general, the longer the accumulated stressing time, the higher the number of EL spots that could be seen on the EL pictures and also the higher the value of I_g, all in agreement with previous reports[3, 5, 8, 10, 11].

Figure 1(b) shows I_g as a function of stress time for the device of Figure 1(a). I_g becomes noisier and increases abruptly at the same time the first EL spot appears on the EL images. Then, I_g keeps increasing with time in a step-like manner. Figure 1(b) also shows the integrated EL intensity from each of the first seven EL spots to appear on the device (offset for clarity). There is a very good correlation between the appearance of each new EL spot and each of the steps in the increase of I_g, indicating the generation of defects underlying each EL spot that contribute a few μA each to I_g. Moreover, it is also shown in the figure that the sum of the EL integrated intensity from all the seven EL spots matches very closely not only the step increases of I_g, but also the evolution of I_g with time between the appearance of two successive EL spots. These results clearly illustrate that the EL intensity of each of the EL spots can be very well correlated to the contribution to I_g of the defect underlying it, and also that the total value of I_g is due to the combined contribution of the localised effect of each of these defects.

It is apparent from the above results that each EL spot must be linked to some sort of localised damage on the device that locally contributes to the total leakage current. In order to determine the nature of this damage, the passivation and metallic contacts were removed from the device, so the surface of the semiconductor becomes exposed and is then accessible with an atomic force microscope (AFM). The etching procedure employed for the removal of the metals and passivation was the same as indicated in

Ref. 6: $HF:H_2O$ (1:10) for the removal of SiN, aqua regia ($HCl:HNO_3$ 3:1) at 80 ºC for 20 minutes, for the removal of the metals, and piranha solution ($H_2SO_4:H_2O_2$) at 115 ºC for 5 minutes for a final cleansing of the chip surface. The regions of the semiconductor surface where the source and drain contacts used to be before their removal are easily identifiable in the AFM images (see Figure 2), and this aided locating the device fingers after the removal of the contacts. AFM scanning of these regions of the semiconductor surface reveals the presence of a series of small pits that forms an inhomogeneous and discontinuous line along where the drain edge of the gate contact used to be. In addition to this line of defects, larger pits have grown from the gate edge towards the drain at particular spots on the device surface (Figure 2), similar to those reported in Ref. 9. AFM scanning of reference, unstressed devices subjected to the same chemical treatment, did not show any of these surface pits, confirming that they are caused by the off-state stress of the devices. By comparison of the AFM and EL images from all the tested devices, it was apparent that EL hot spots correlate to these larger AFM pits. Moreover, when the AFM and EL images are carefully overlaid, an almost perfect one-to-one correspondence between EL spots and pits in the surface is found (see Figure 2), although such a correspondence becomes more difficult to verify when many EL spots appear together on the EL pictures due to the resolution of the EL capturing system, which implies that two adjacent EL spots have to be separated by at least ~1 μm in order to be well resolved. So, it can be concluded that EL spots do indeed originate at places where the surface defects appear during off-state stress.

To demonstrate that these large surface pits do indeed provide a leakage pathway in the devices, conducting-tip AFM (c-AFM) imaging of the surface of the semiconductor was employed. Figures 3(a) and (b) show a height map and a current

map obtained from one of these c-AFM scans, respectively. A reverse bias of -10 V was applied to the c-AFM tip to mimic the effect of a reverse bias on the device gate. The electric circuit was closed using focused ion beam-deposited Pt tracks to connect the device mesas to one corner of the chip that is subsequently grounded. Figure 3 shows results from a device that was stressed at forward and reverse V_{ds} biases, while keeping V_{gs} = -15 V, and thus EL spots, and correspondingly surface pits, appeared at both sides of the gate, confirming these defects are related to the high electric field at the drain-side edge of the gate. From the c-AFM images it is apparent that the current is higher through the pits than through the rest of the semiconductor surface thus confirming the role of the pits as current leakage paths. Therefore, these results directly demonstrate the common origin of EL spots, gate leakage and surface pits.

To study the physical nature of the stress induced large defects that produce the EL spots, detailed standard-tip AFM measurements were performed in order to investigate their morphology. These defects display an internal structure (Figures 4(a) and (b)) that seems to consist of smaller diameter pits which coalesce together as the larger defect structure is formed. This internal structure suggests that the large pits may be generated from the semiconductor surface into the semiconductor device during the off-state stress experiments. Typical sizes of the EL-emitting pits range from 2 to 3 nm in depth and from 30 to 110 nm in their lateral dimension. The EL integrated intensity and pit size were compared for selected pits which are far enough apart from other EL spots to extract a reliable value of the EL integrated intensity from the EL images. No clear correlation between the integrated EL intensity of the EL spots and the area, perimeter or depth of the corresponding pits was found. This suggests that the light emission is not evenly distributed across the whole area of the surface pits. Thus the EL may originate only from selected regions inside the pit such

as possible dislocations or point defect areas. Recalling the results of Figure 1(b), which correlate I_g and EL intensity, this would imply in turn that the leakage current is not evenly distributed across each of the surface pits. Indeed, c-AFM mapping of Figure 3 indicates the leakage current is higher towards the centre of the pit than towards the edges, consistently with the centre of the pits being deeper and thus closer to the two-dimensional electron gas (2DEG). Nevertheless, it must be noted that the typical pit depth (2 - 3 nm) is much smaller than the AlGaN barrier thickness of 25 nm. Therefore, in order to connect electrically the surface pit with the 2DEG, a conduction path for the electrons must be present. One possibility would be the presence of groups of trap states that would form a percolation path, consistently with what has been suggested in previous reports[8, 10]. The results shown in this letter would also be consistent with the preferential formation of pits on top of conducting threading dislocations, forming a current leakage path, similarly to that hypothesised in Refs. 13 and 14.

In conclusion, it was found that the degradation of I_g in AlGaN/GaN HEMTs upon off-state stress is the result of the combined action of each of the defects underlying the EL spots that appear on the drain side of the gate, which contribute a few μA each to the total value of I_g. Upon removal of the metallic contacts and the passivation layer, small defects were observed along the drain side edge of the gate. Also, larger pits 2 - 3 nm in depth and 30 - 110 nm in the lateral dimension, grown towards the drain during stress, were found to correlate in a one-to-one correspondence with the previously observed EL hot spots. Reverse-bias conducting-tip AFM confirmed these large pits act as current leakage paths. Therefore, the direct one-to-one correspondence between EL spots, surface defects and gate current leakage paths was demonstrated, confirming that the three phenomena have indeed the same origin.

Detailed AFM mapping was employed to conclude that the EL intensity of each EL spot does not depend on the size of the pit, but rather on its internal structure.

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Figures.

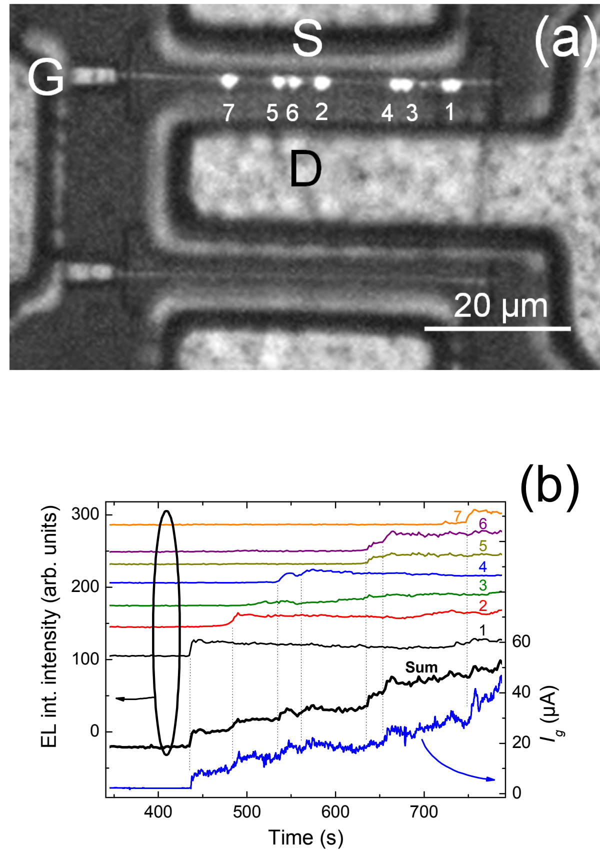

Figure 1. (a) Electroluminescence (EL) image from a representative 50 µm-wide device stressed at V_{gs} = -15 V and V_{ds} = 30 V for 760 seconds, where only the upper finger is biased. The EL image is overlaid on a white light image of the device. The numbers indicate the order of appearance of the EL spots. (b) EL integrated intensity as a function of stress time from each of the EL spots of (a) as indicated. The sum of the EL integrated intensities of all the seven spots is also shown. Curves are offset for clarity. The figure also shows I_g as a function of stress time. Vertical dotted lines are a guide to the eye.

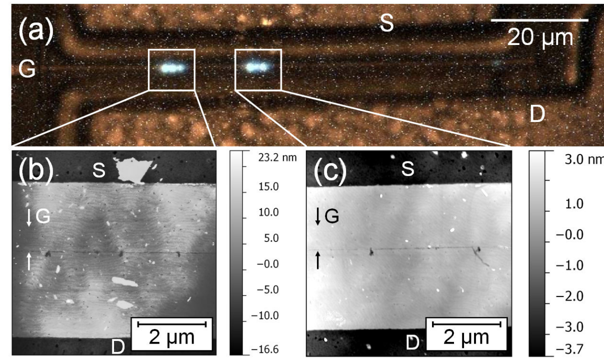

Figure 2. (a) Electroluminescence image of a 100 µm-wide HEMT stressed at V_{ds} = 40 V and V_{gs} = - 15V for 4 minutes. (b) and (c) AFM images of the areas inside the squares of (a) after removal of the passivation and contacts. The top and bottom dark bands in the images are the regions where the source and drain contact edges used to be before removal. The thickness and location of the gate contact before removal is indicated with arrows. The two light grey horizontal lines on both sides of the location of the gate contact in (b) are AFM artefacts.

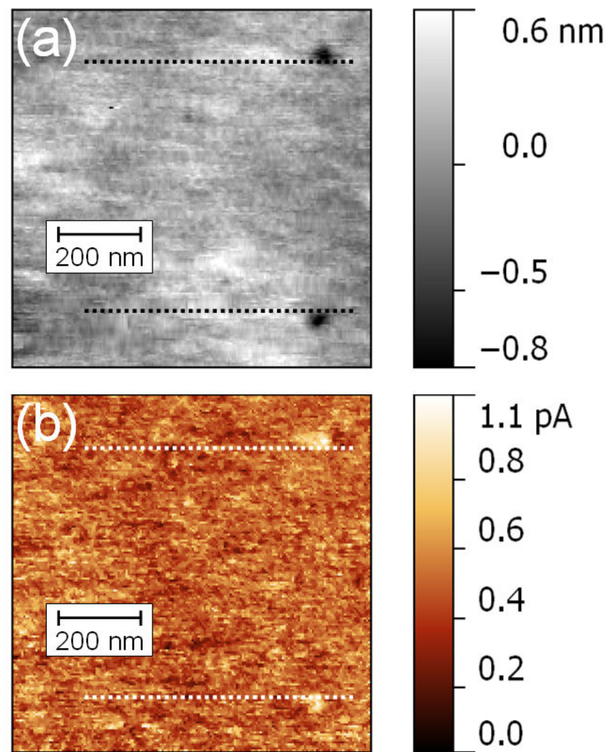

Figure 3. (a) Topography image and (b) current image from two large surface pits. Both images were acquired simultaneously by using a conducting AFM tip at -10 V. Dotted lines indicate the location of the gate contact before removal. This device was stressed at both forward and reverse values of V_{ds}, and thus shows surface pits on both sides of the gate.

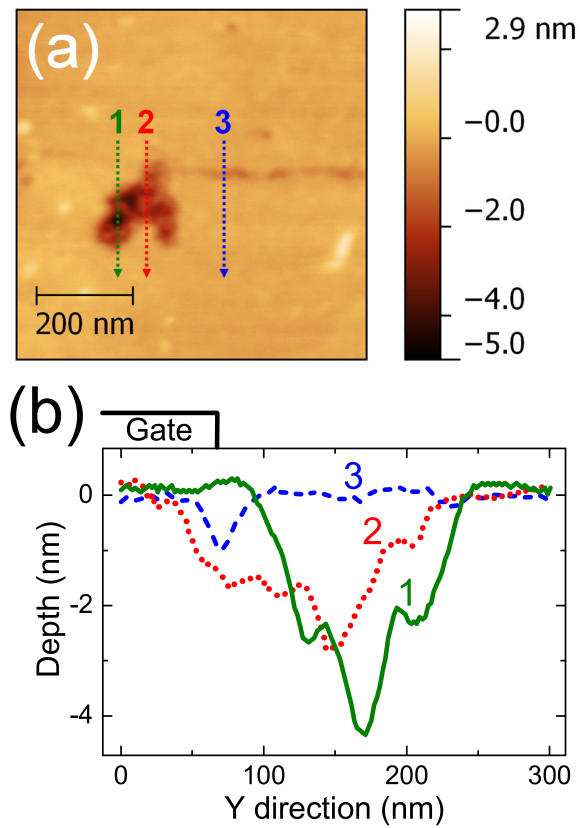

Figure 4. (a) Standard-tip AFM image of one of the surface defects of Figure 2(b). (b) Depth profiles of the surface pit of (a) along the indicated arrows.