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Analysis of dc-RF Dispersion in AlGaN/GaN HFETs using RF Waveform Engineering

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ABSTRACT

This paper describes how dc-RF dispersion manifests itself in AlGaN/GaN heterojunction FETs (HFET) when the devices are driven into different RF load impedances. The localised nature of the dispersion in the IV plane, which is confined to the "knee" region, is observed in both RF waveform and pulsed-IV measurements. The effect is fully reproduced using 2D physical modelling. The difference in dispersive behaviours has been attributed to the geometry of a trap induced virtual gate region and the resulting carrier velocity saturation being overcome by punch-through effects under high electric fields.

INDEX TERMS

Microwave FETs, microwave measurements, semiconductor device modeling, current collapse.

FIRST FOOTNOTE

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I. INTRODUCTION

GaN heterojunction field effect transistors (HFET) are widely recognised as an ideal technology for radio frequency power amplifier applications due to their good thermal performance and their capabilities for simultaneously delivering high frequency and high power operation [1][2]. However, GaN HFETs have been known to suffer from trapping problems resulting in dc-RF dispersion - a phenomenon also described as “current collapse” or “knee-walkout” - which limits the power capabilities of these devices [3].

The general belief is that the measured dispersion in GaN HFET structures is caused by electron trapping in the vicinity of the gate. Trapping has been proposed to occur by leakage from the gate into either the AlGaN barrier layer or onto the semiconductor surface [4], or by trapping of hot electrons into bulk traps [5,6]. The process is exacerbated by the high operational drain bias voltages in many GaN applications, which results in a large electric field at the drain side of the gate edge.

GaN devices have been shown to be highly sensitive to different surface preparation and passivation techniques, suggesting that trapped surface charge has a significant role in the dispersion [7]. Furthermore, the scanning Kelvin probe microscopy technique has been used to measure changes in surface potential as a function of distance away from the gate in stressed GaN HFETs [8]. The results of this study showed that electrons are able to migrate along the surface of the device up to 1.0μm away from the gate, depending on the electric field stress.

The accumulation of electrons into a region of trap states on the device surface is believed to lead to the “virtual gate” effect, whereby the trapped electrons generate an electrostatic charge which acts to partially deplete the conducting channel [9]. The consequence of the extended depletion region is an increase in the access region resistances resulting in lower current in the active channel and reduced RF output power. In general it is found that the effect is to increase the source, and especially the drain, resistance rather than to increase the channel resistance under the gate [10,11]. The behaviour of the current through these depleted regions has been described using a space-charge-limited current model [12]. This analysis has led to successful modelling of current collapse affected GaN HFET devices for use in circuit simulators using analytical equations derived for compact models [13]. The current

collapse phenomenon has also been linked to surface leakage, and it has been shown that this results in knee walkout and dc-RF dispersion [14].

It remains desirable to eliminate the dc-RF dispersion in GaN HFETs altogether. In order to reduce current collapse, refinements in layer structure as well as improved device processing techniques will likely be required. A number of device processing approaches, including various passivation, field-plate, gate recess and surface cap strategies, have already been employed in an effort to mitigate the detrimental effects of the trapped surface charge [7][15-17]. In many GaN processes these approaches have only led to partial success, and consequently measurement techniques that provide insight into the trap phenomena and can quantify device performance have been developed to help device designers produce better devices with less dispersion.

Gate and drain lag measurements have historically been a major technique for monitoring dispersion in microwave FETs [18,19]. More recently, dedicated pulsed-IV measurements have become possible where a device's gate and drain terminals are simultaneously pulsed in order to map out the IV-plane from a quiescent bias point, at speeds which are too fast for trap and thermal effects to alter significantly during the measurement. A pulsed-IV measurement can show an IV plot of the device in a trap and thermal state set by the quiescent bias point, and is thus capable of demonstrating bias related collapse problems in GaN HFETs [20].

The true RF behaviour of an FET can be measured and related to the IV plane using RF IV waveform measurement and engineering. This technique has previously been shown to be valuable for visualising and quantifying dc-RF dispersion phenomena in GaN HFETs [21]. Collecting dense plots of dynamic RF load-lines exciting different regions of the IV plane, but from the same quiescent bias point, can be used to map out the RF boundary of the device [22].

In this work the virtual gate explanation is extended, making its description more explicit. Measured RF waveform and pulsed-IV data have observed different dispersion behaviours occurring in different regions of the IV plane. The subtleties of the measured dispersion behaviours have been fully reproduced using physical modelling. The reason that the dispersion only impacts the knee region of

the device IV plane is explained for the first time in terms of the velocity saturation and punch-through behaviour of the electrons in the channel. The simulation only considers the effect of a static virtual gate charge, but a mechanism is proposed to explain the reversible trapping process from the gate contact.

II. MEASUREMENT SETUP

The measurements and simulations shown here are for 2x125µm wide AlGaN/GaN HFETs grown on a 4H SiC substrate, with a T gate of 0.25µm stalk length and an approximately 4µm source-drain gap. The process has been described elsewhere [23]. The layer structure consisted of a 25nm thick undoped $Al_{0.25}Ga_{0.75}N$ barrier layer, on a 1.9 µm GaN buffer which was Fe doped to control short-channel effects [24]. A 4H semi-insulating SiC substrate was used for optimum thermal performance. The devices had a pinch-off voltage of -5V, g_m of 270mS/mm, I_{DSS0} of 1.1A/mm and a cut-off frequency of 37GHz. The RF performance of the devices in a variety of RF load configurations have been investigated using the time domain RF waveform measurement systems developed at Cardiff University. The dispersion behaviour was also measured using an Accent DIVA pulsed-IV system.

The waveform measurement system (shown in Figure 1) operates using an Agilent 70820A Microwave Transition Analyser (MTA) with vector correction, which allows input and output voltage waveforms to be sampled. A sweeper at the source provides input power at the fundamental frequency (900MHz for all measurements in this paper). A multi-harmonic active load-pull system is used to present the device with a range of RF load impedances. RF probes are used to allow on-wafer measurements, and the whole system is computer controlled [25].

III. MEASUREMENT RESULTS

The dc-RF dispersion can be readily observed in both pulsed-IV and RF waveform measurements made at different static drain biases. It is believed that more electrons become trapped as the drain bias increases, resulting in more dispersion. This can be seen in Figure 2 where RF dynamic load-lines measured at 900MHz are shown for four different drain biases and a range of fundamental load impedances – a technique we have termed a ‘fan’-diagram [22]. When the device is driven into

compression by the RF stimulus the measured RF waveforms become harmonically rich and trace the RF boundary condition that they are interacting with. Using the compressed dynamic load-lines in Figure 2, the RF boundary condition for a range of drain biases can be visually compared to the dc boundary on the IV plane. The RF boundary can be seen to shift with the increasing drain bias, as the load-lines compress increasingly prematurely.

It is possible to observe in Figure 2 that different dispersion behaviours can exist at the same static bias point. Indeed, we can split the IV into three distinct regions where the dispersion is very different. To illustrate these regions the RF boundaries mapped by the fan diagrams have been traced out in Figure 3. Here region (a) describes the low current on-resistance boundary where very little dispersion is seen. Region (b) describes the knee region proper, where the dispersion is most pronounced. Finally, region (c) covers the saturation region which shows less dispersion as the drain voltage increases.

The same phenomenon can be observed in pulsed-IV measurements of the same device. Figure 4 shows pulsed-IV data measured on the same device but from two quiescent bias points: a control case with no applied bias (V_G = 0V, V_D = 0V) and a class A bias condition with a significant applied drain voltage (V_G = -3V, V_D = 30V). The pulsed-IV results show the distinct behaviour of all three identified regions, including region (c) at high drain voltages. The current recovery at these high voltages is likely to be masked to some degree by the increased self-heating occurring in these regions even for the 1 µs pulse length employed here [26]. The key feature is that dispersion only really occurs in the knee region, with little dispersion evident in the linear region (region (a)), in saturation (region (c)), or in the bulk of the IV plane including the pinch-off region.

The gate leakage under reverse bias was investigated using a dedicated surface leakage test structure [27] fabricated using an identical epitaxial specification and process to that employed for the device of figures 2 to 4. The test structure is shown as an inset to **Figure 5** and uses a guard ring to separate the leakage current from the gate across the AlGaN surface to the drain ($I_{surface}$), from the leakage current passing through the bulk of the AlGaN down to the channel (I_{bulk}). Experimentally it was found that there was no significant surface leakage (ie at the pA level) from the gate across the surface to source or drain, with all leakage (which was at the microamp level) passing through the AlGaN barrier down

to the channel. However, this result does not preclude local current flows taking place between traps on the surface and the gate, and it is such a charge transfer which is the subject of the simulations in the next section.

IV. SIMULATION RESULTS

To understand these measured results physical model simulations were run using the commercial ATLAS 2D finite element package. A similar approach was used to that employed previously [28], but with the addition of self-heating and a more complete inclusion of the effect of the surface charges. The saturation velocity was set to 1.9×10^7cm/sec.

The spontaneous and piezoelectric effects were included by adding sheet charges at the top and bottom of the AlGaN layer [29], and the fraction of Al in the AlGaN layer adjusted to give agreement with the measured pinch-off voltage. In the ungated access regions between the gate and the source and drain, the counter-balancing charge to the channel charge resides in interface traps at the top of the AlGaN layer [30]. It was found that reasonable agreement could only be obtained with the measured gate transfer characteristic if the interface trap level was close to the AlGaN conduction band edge (this key parameter varies widely in the literature from an energy level close to the valence band [31] through to the conduction band [32]). Transport across the surface of the AlGaN was suppressed by setting the mobility in the upper part of the AlGaN layer to zero, and the interface trap charge was included as a fixed charge extending over the entire ungated surface, whose numerical value was then adjusted to set the surface Fermi level to 0.5eV below the conduction band edge.

The virtual gate charge was modelled by assuming that traps exist on the surface of the AlGaN which can store a transient distribution of electrons. The route by which these traps are filled and emptied is not modelled here, but the path by which this occurs is assumed to be by local transport to and from the gate and a possible mechanism is now described. There is good evidence that the trapping/de-trapping process is highly non-linear in electric field proceeding in some circumstances by a Poole-Frenkel process [33, 27], further the peak electric field in the structure occurs at the gate corner with a high local value in the plane of the surface at high drain bias (eg see [34]), So we suppose that electron transport across the surface can only occur when the field exceeds a critical value. Hence during high

drain/gate biased operation electrons could transport across the surface from the gate into the traps by a process which might involve tunnelling and/or hopping until Coulomb screening by this newly trapped charge reduces the field suppressing further conduction. This is consistent with the observation that surface leakage current between the external contacts is insignificant since the in-plane electric field is relatively low over most of the ungated region. When the bias is removed, the Coulomb field associated with this newly trapped virtual gate charge will result in the local field between the traps and the gate corner reversing, tending to allow charge to transport back to the gate, and explaining the recovery of the knee walkout under dc or pulsed operation under zero quiescent bias. This mechanism is essentially independent of the channel and does not require hot electrons.

For the purposes of modelling, since the RF and pulsed-IV characteristics are measured under conditions where trapped charge is effectively static, the possible trapping dynamics described above were ignored, and it was assumed that the trapping could be modelled with a fixed charge distribution. It is unknown at present what the exact distribution of virtual gate charge is, but here it was simply modelled using a constant density and fixed length located on the surface of the AlGaN on the drain side of the gate. In this paper we are not seeking to determine the virtual gate dimensions, but simply to demonstrate that this simple model can explain the experimental observations.

Simulations were run to determine the effect of varying virtual gate length and charge density, resulting in a wide range of impacts varying from complete pinch-off of the channel to essentially no effect. Here we will concentrate on a single virtual gate charge distribution which generates behaviour comparable to the experimental results.

Figure 6 shows a cross-section through the device showing the electron density in the device with no voltages applied. To simulate the effect of a class A quiescent bias, a virtual gate fixed electron distribution of length 75nm and $-12 \times 10^{12} cm^{-2}$ charge density was placed on the AlGaN surface on the drain side of the T-gate to model the electrons transported from the gate and trapped in surface states. (This trapped charge distribution is in addition to the polarisation charges and the uniform interface state charge across the surface.) It can be seen that there is a local reduction in the electron density in the AlGaN region and also in the channel, but no change in the bulk of the GaN since the remaining

channel charge fully screens the virtual gate charge.

Figure 7 shows comparison IVs for the simulated device with and without the virtual gate charge. The IVs of the standard device can be considered as baseline performance with no trap effects. The case with the virtual gate charge included shows dispersion behaviour that is very similar to the measurement results. The same three distinct regions where different amounts of dispersion occur have been captured by the modelling approach. It is clear that the virtual gate charge only affects the transport in the knee region with almost no effect elsewhere on the IV plane.

To understand why there is an impact only in the knee region, we will examine in detail the transport along the channel for a gate voltage of 0V and at varying drain voltages. The simulated drain voltages span from region (a) at V_D=2V, through region (b) at V_D=4V to region (c) at V_D>10V. The electron concentration is shown in Figure 8 for each region with and without a virtual gate charge. The virtual gate charge results in a strong local reduction in the electron density, but never sufficient to fully pinch-off the channel. Under the gate itself it also produces a significant change, but only for region (b) at V_D=4V. Here, the virtual gate charge results in a smaller drop in carrier concentration and produces a much smaller gradient in carrier concentration compared to the control device.

The electron velocity in the channel under the gate is shown in Figure 9 which gives a clear demonstration of the impact of the virtual gate on the transport. Under the virtual gate, the electron concentration is reduced so far that carriers accelerate up to their saturation velocity of 1.9×10^7cm/sec for any drain voltage >2V. Effectively, the current carrying capability of the channel is limited due to current saturation under the virtual gate. At V_D=4V in region (b), the result is that a large part of the applied voltage is dropped under the virtual gate, and the electron velocity throughout the rest of the device is reduced resulting in a fall in the current through the device.

In region (c), the current handling capability of the device is effectively restored despite the fall in carrier concentration directly under the virtual gate that can be seen in Figure 9b. Figure 10 shows why this occurs. This figure shows the electron concentration under the gate for V_D=20V, and it can be seen that the electron concentration extends deep into the GaN buffer at the drain side of the gate. This

occurs almost equally in the control device. Effectively the virtual gate length of only 75nm is sufficiently short that it suffers from extreme short-channel effects and the electron current can punch-through under the virtual gate. Simulation of longer virtual gates (not shown here) indeed show that the knee walkout extends to higher drain voltages consistent with this model.

V. DISCUSSION

The virtual gate charge model has largely reproduced the observations seen in the measured waveform results, suggesting that it has also captured the impact of the trapped charge in the device. The main effect of the small area of excess surface electron charge beside the gate is to reduce the number of electrons available in the channel for a small area immediately beneath the virtual gate. This small area of reduced charge results in a limited saturation current in the knee region. However, because the area is geometrically small it has very little effect on the overall resistance of the channel in the linear regime. Furthermore, at high drain voltages punch-through effects (similar to short channel behaviour) occur which allow the current to recover with increasing drain voltage.

This virtual-gate model can now explain the three regions with different dispersive behaviour. Firstly, region (a) where there is very little dispersion with increasing drain bias can be explained because the IV characteristics are dominated by the parasitic access resistance (on-resistance) which is not greatly affected by the small depleted region introduced by the surface charge. Region (b) is where the surface charge has the most significant effect because the channel current saturates prematurely compared to the dc case. Region (c) also suffers from reduced current, but at higher drain voltages the current is able to punch through the small saturated region leading to a gradual recovery of current with increasing drain voltage.

Although a virtual gate surface charge distribution has been simulated here, all that is actually required for current collapse is that electron charge storage occurs near the gate edge. Storage in bulk traps located in this region of the device would have exactly the same impact on the IV characteristics provided it was similarly localised in extent.

This paper has concentrated on the situation such as would arise in a power amplifier where the gate

bias is relatively low, and there is a high drain bias applied. In this case, the peak electric field will arise on the drain side of the gate resulting in a virtual gate which will be largely located on the drain side of that gate. However, there are other circumstances where significant reverse gate bias can arise such as in switching or some LNA applications. Under those circumstances, there can be an almost equally large electric field on the source side of the gate, which will in turn lead to its own virtual gate. The impact of this source side virtual gate would be to exacerbate the already strongly bias dependent source resistance [35] resulting in increased knee walkout and reduction in drain current handling.

VI. CONCLUSION

This paper has presented a clarifying insight into dc-RF dispersion problems in GaN HFETs through RF waveform measurements performed across a range of RF load impedances and physical device modelling. It has been shown that the virtual-gate surface charge created when devices are biased with high drain voltages can explain the different dispersion effects seen when different regions of the device IV are probed by RF signals.

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FIGURE CAPTIONS

Figure 1. Schematic of the waveform measurement system.

Figure 2. Measured RF load-line fan diagrams for four class A bias points, V_D = 10V, 20V, 30V and 40V demonstrating increased dispersion with drain bias. Load-lines are overlaid on dc-IVs measured from V_G = -6 to 0V in 1V steps

Figure 3. RF boundary conditions mapped out by the dynamic load-lines of Figure 2 showing three regions with differing dispersion behaviour.

Figure 4. Pulsed-IV measurements showing current recovery at higher drain biases. IVs measured from V_G = -6V to +2V in 1V steps from two static bias points: V_G = 0V, V_D = 0V (full line) and V_G = -3V, V_D = 30V (dashed line). All measurements were made with a pulse length of 1μs and a pulse separation of 1ms.

Figure 5. Gate leakage measurements for devices from a wafer similar to those shown in figures 2 to 4. The surface leakage test structure is shown as an inset; pads are 80 μm square [26]. The leakage path from gate to the guard ring across the AlGaN surface is $I_{surface}$ and the leakage from gate to the ohmic contact is I_{bulk}.

Figure 6. Contour plot of electron concentration in the vicinity of the gate for V_G=0V, V_D=0V.

Figure 7. Simulated IV characteristics for the baseline case with no dispersion (full line) and the virtual gate model (dashed lines).

Figure 8. Channel electron concentration. V_G=0V, dashed line has virtual gate charge.

Figure 9. Electron velocity parallel to the surface. Vgs=0V. (a) control, (b) with virtual gate charge.

Figure 10. Contour plot of electron concentration for the gate region with virtual gate charge present. V_G=0V, V_D=20V.

FIGURES

Figure 1

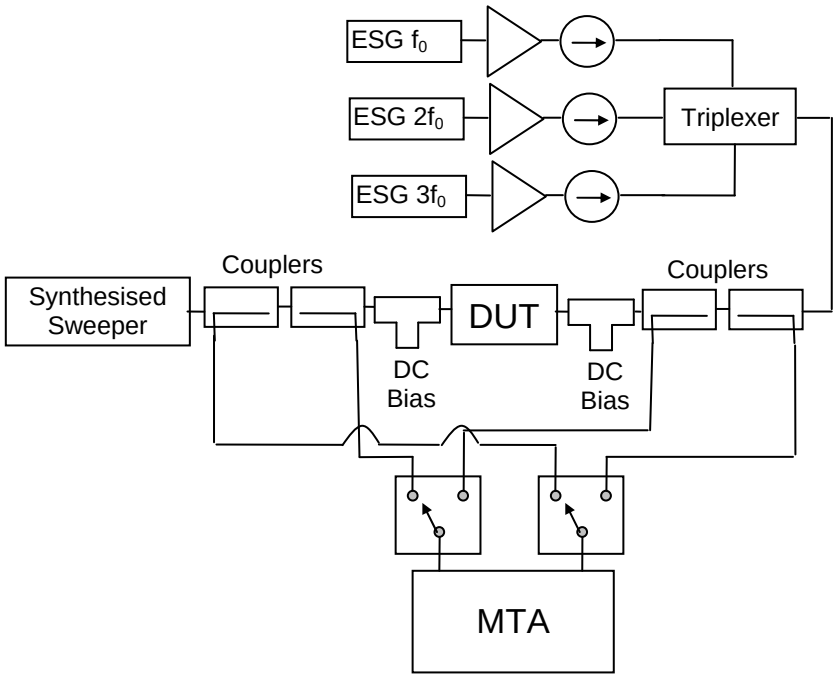


Figure 2

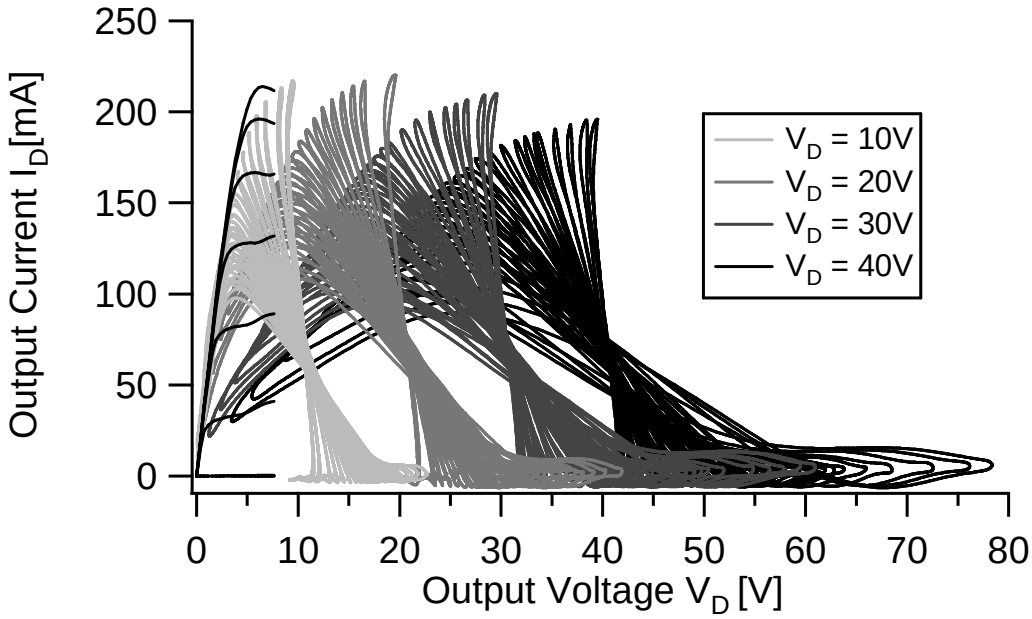

Output Current I_D[mA]
250
200
150
100
50
0
0
10
20
30
40
50
60
70
80
Output Voltage V_D [V]
V_D = 10V
V_D = 20V
V_D = 30V
V_D = 40V

Figure 3

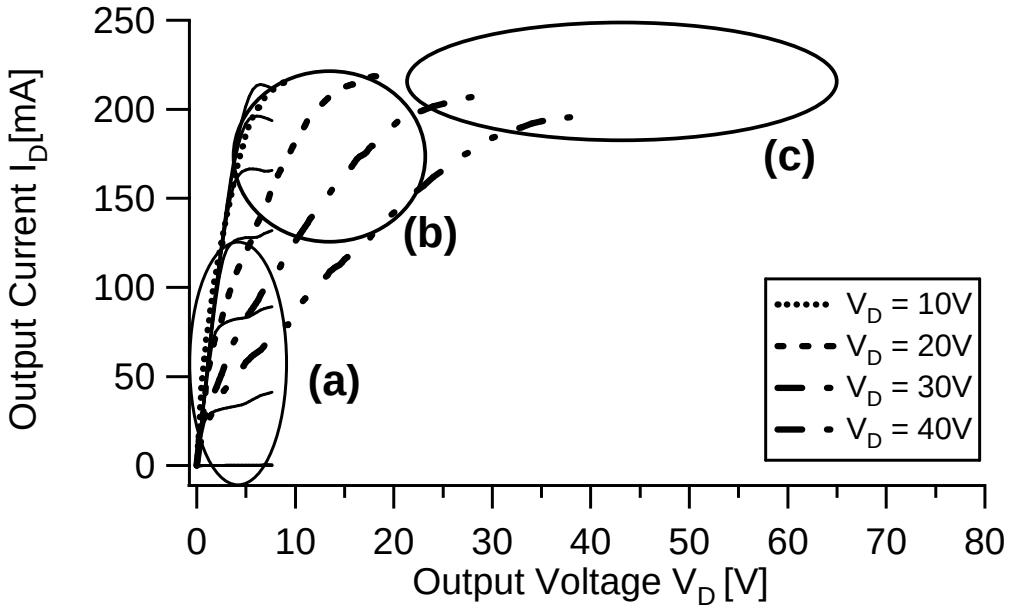

Output Current I_D[mA]
250
200
150
100
50
0
(a)
(b)
(c)
V_D = 10V
V_D = 20V
V_D = 30V
V_D = 40V
0
10
20
30
40
50
60
70
80
Output Voltage V_D [V]

Figure 4

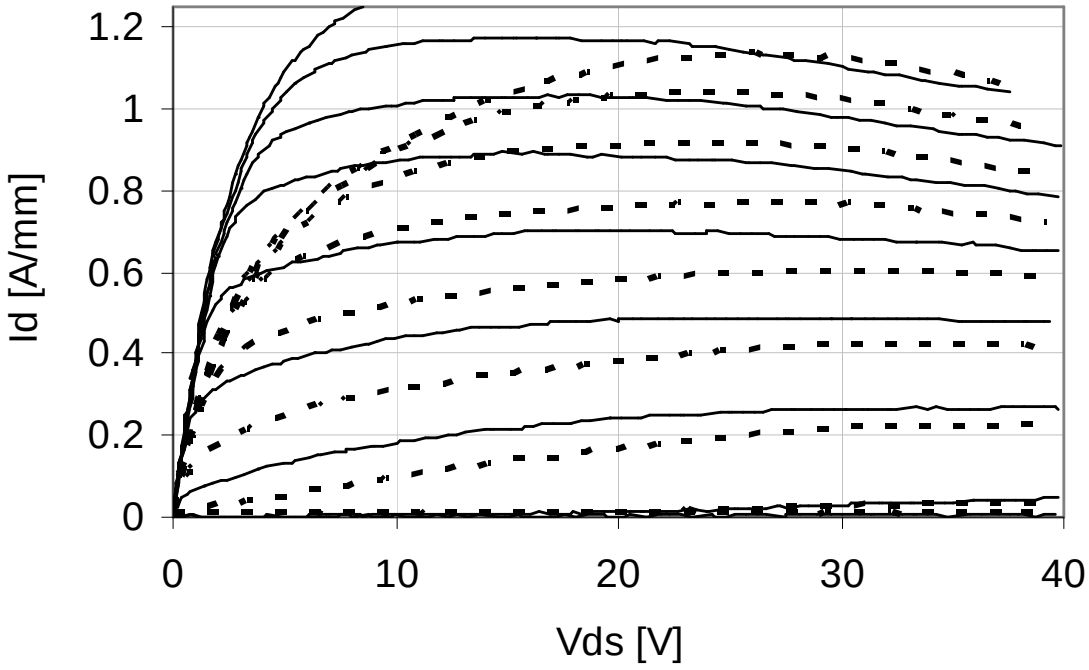


Figure 5

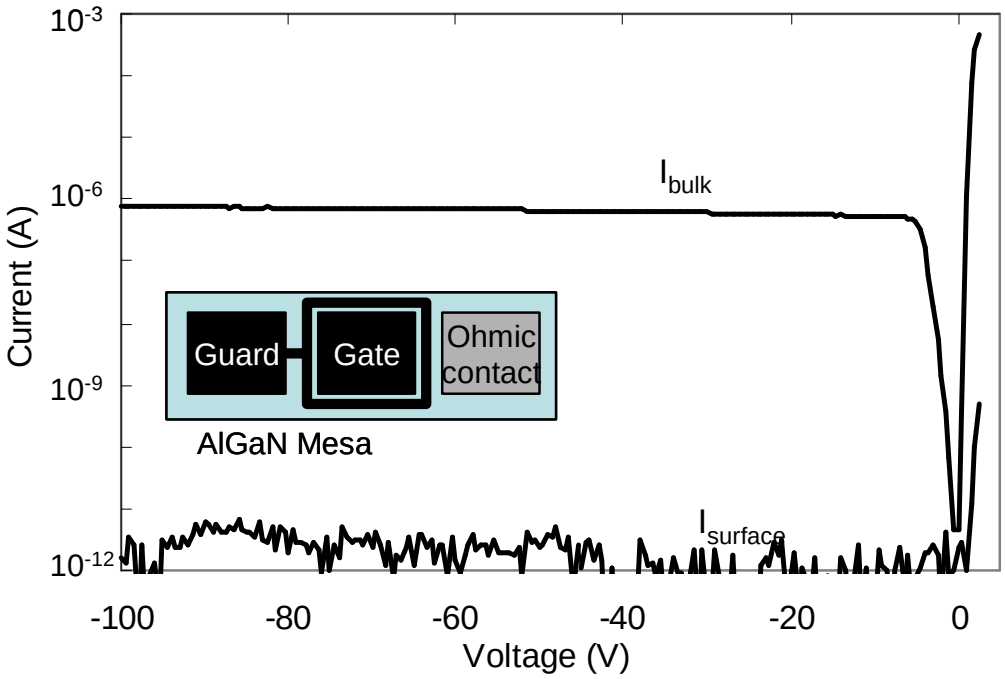

10-3
10-6
10-9
10-12
Current (A)
Ibulk
Guard
Gate
Ohmic contact
AlGaN Mesa
Isurface
-100
-80
-60
-40
-20
0
Voltage (V)

Figure 6

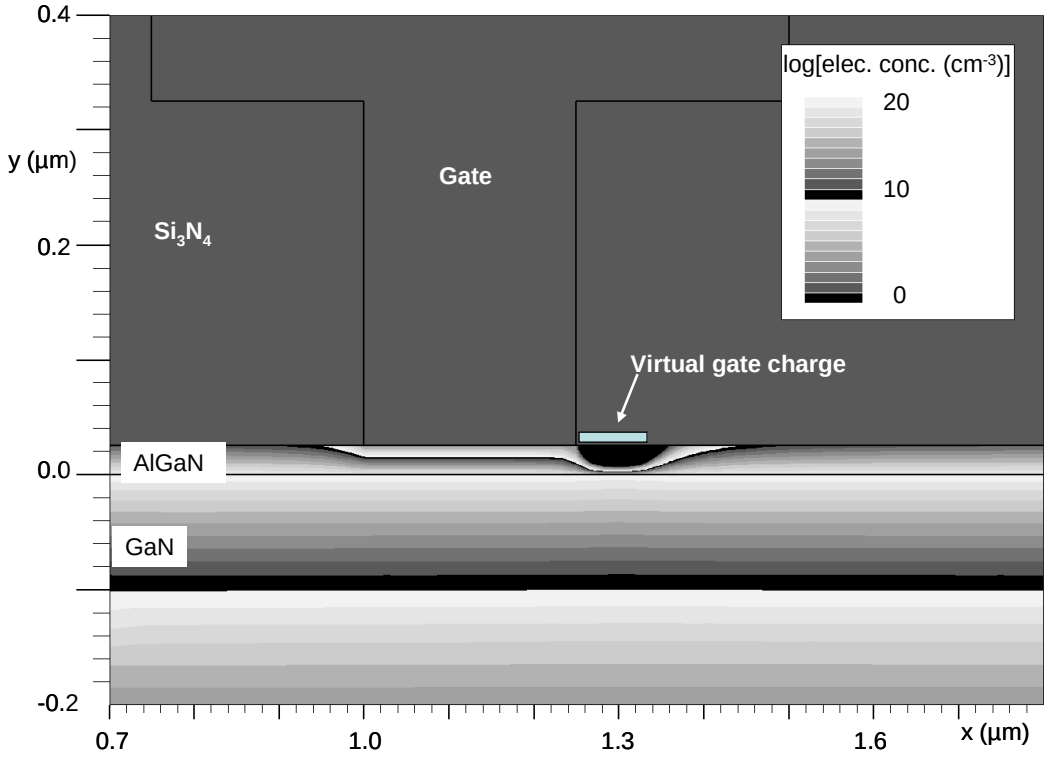

0.4
y (µm)
0.2
0.0
-0.2
0.7
1.0
1.3
1.6
x (µm)
log[elec. conc. (cm-3)]
20
10
0
Gate
Si3N4
Virtual gate charge
AlGaN
GaN

Figure 7

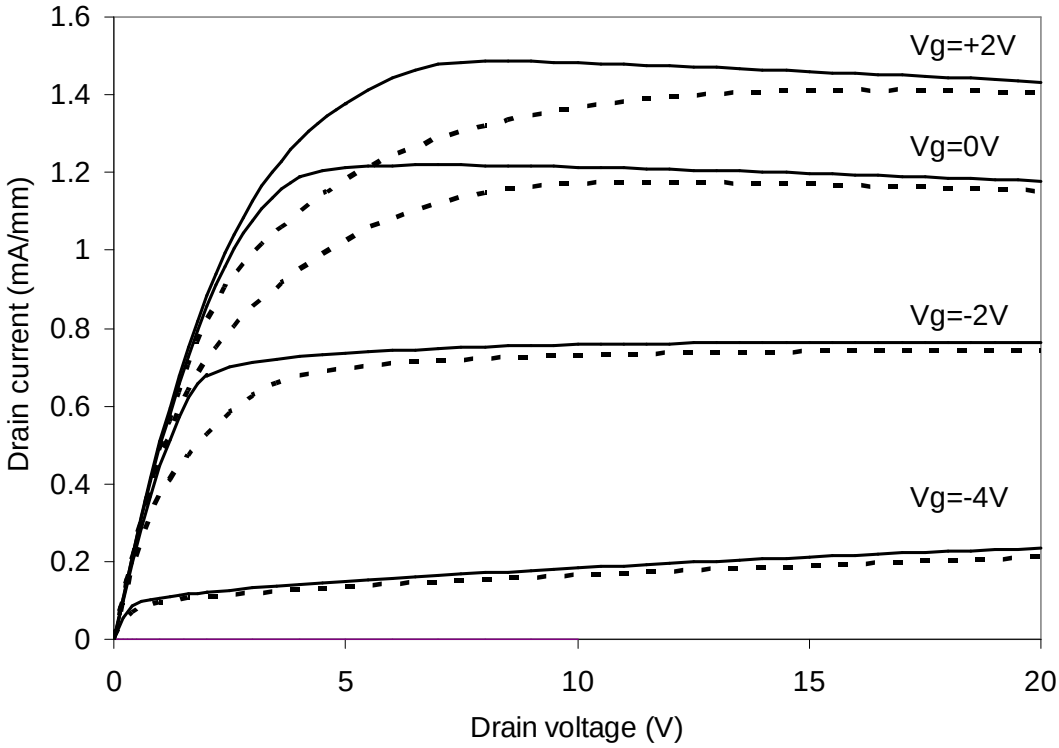

1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
Drain current (mA/mm)
0
5
10
15
20
Drain voltage (V)
Vg=+2V
Vg=0V
Vg=-2V
Vg=-4V

Figure 8

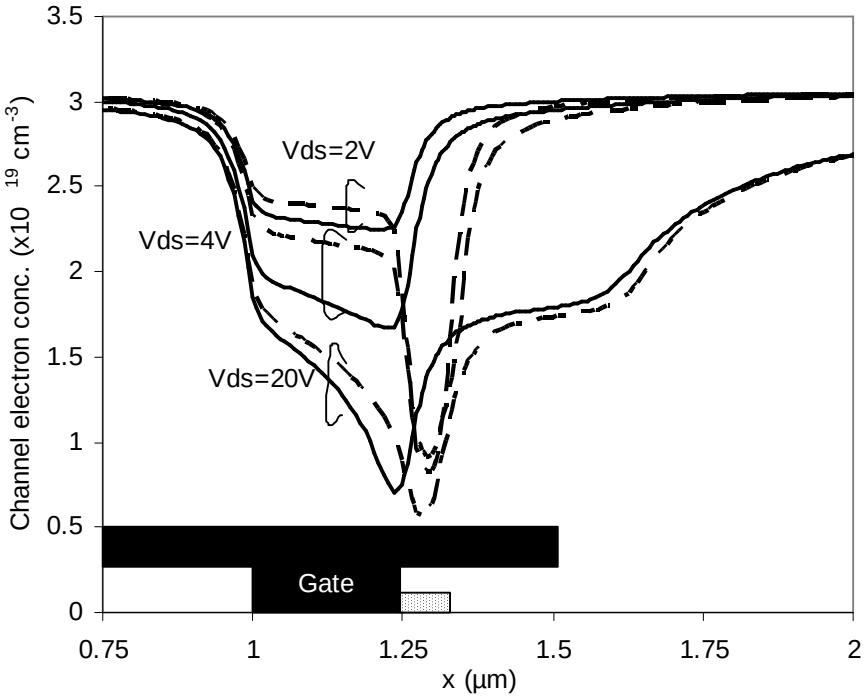
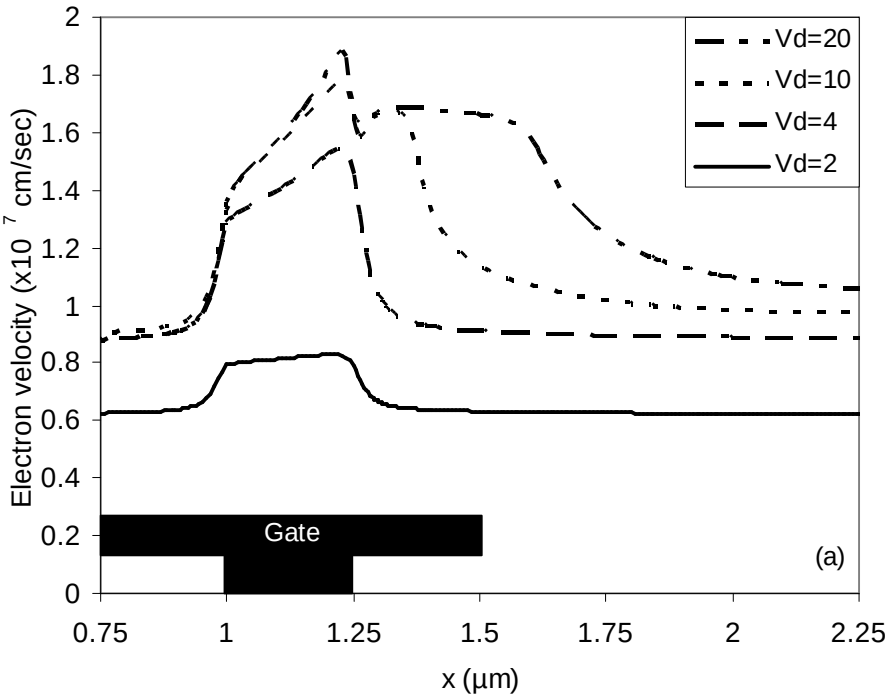

3.5
3
2.5
2
1.5
1
0.5
0
Channel electron conc. (x10 19 cm-3)
Vds=2V
Vds=4V
Vds=20V
Gate
0.75
1
1.25
1.5
1.75
2
x (µm)

Figure 9


Vd=20
Vd=10
Vd=4
Vd=2
Electron velocity (x10 7 cm/sec)
Gate
(a)
x (μm)

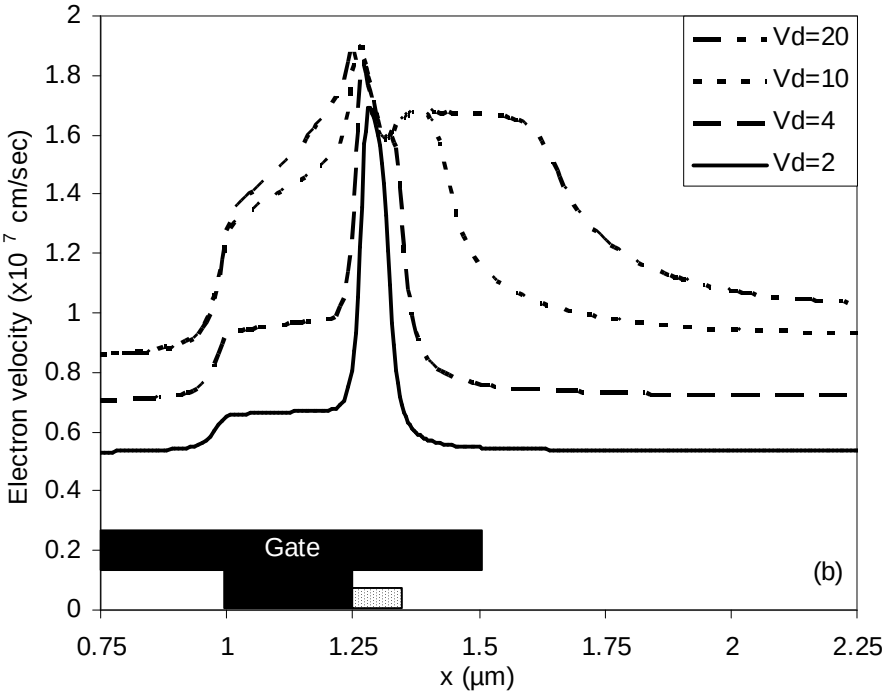
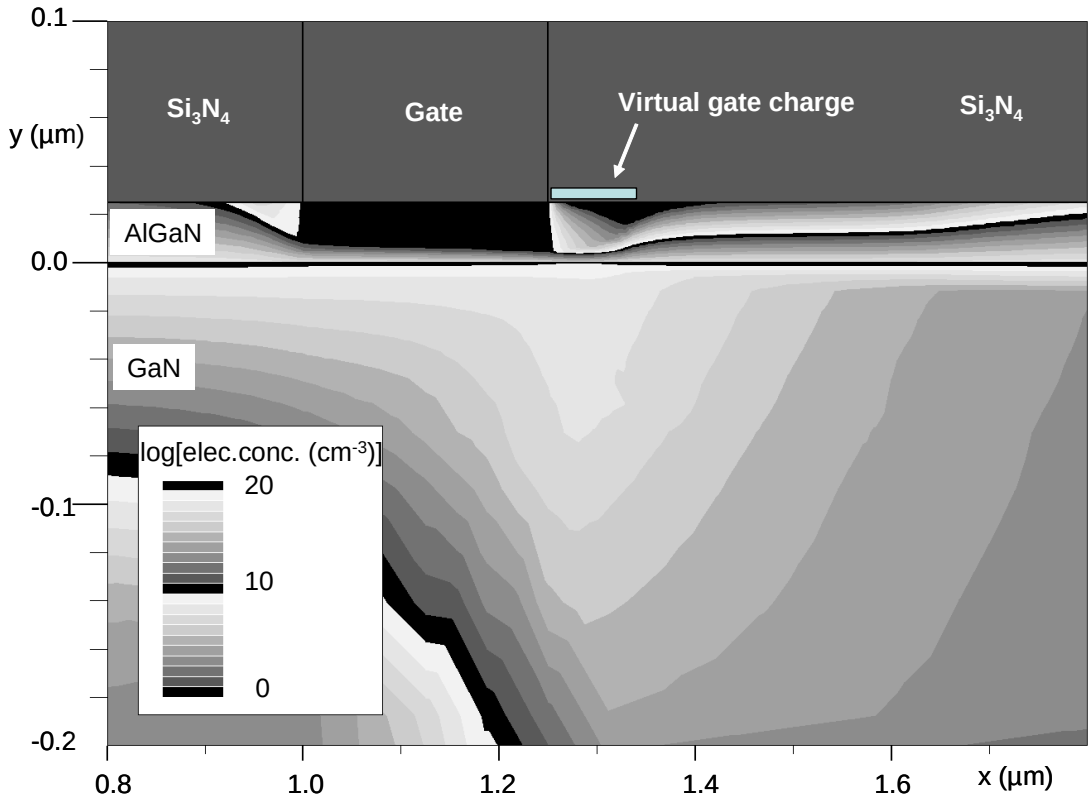

Vd=20
Vd=10
Vd=4
Vd=2
Electron velocity (x10 7 cm/sec)
Gate
(b)
x (μm)

Figure 10


0.1
y (µm)
0.0
-0.1
-0.2
0.8
1.0
1.2
1.4
1.6
x (µm)
Si3N4
Gate
Virtual gate charge
Si3N4
AlGaN
GaN
log[elec.conc. (cm-3)]
20
10
0